HT MICRON
semicondutores

iMCP HTNB32L-XXX – MEMORY LAYOUT

Memory layout for iMCP HTNB32L-XXX System-in-Package

Classification: PUBLIC

Doc. Type: USER MANUAL

Revision: v.02

Date: 28/09/2023

Code: HTNB32L-XXX-UM-0006

SUMMARY

DOCUMENT INFO

This document describes the flash and RAM memory layout for the iMCP HTNB32L-XXX.

1. FLASH MEMORY LAYOUT

The HTNB32L-XXX has a 1.6 MB partition for the system image and 0.9 MB is reserved for user and new features. Figure 1 shows the flash memory layout of the HTNB32L-XXX device:
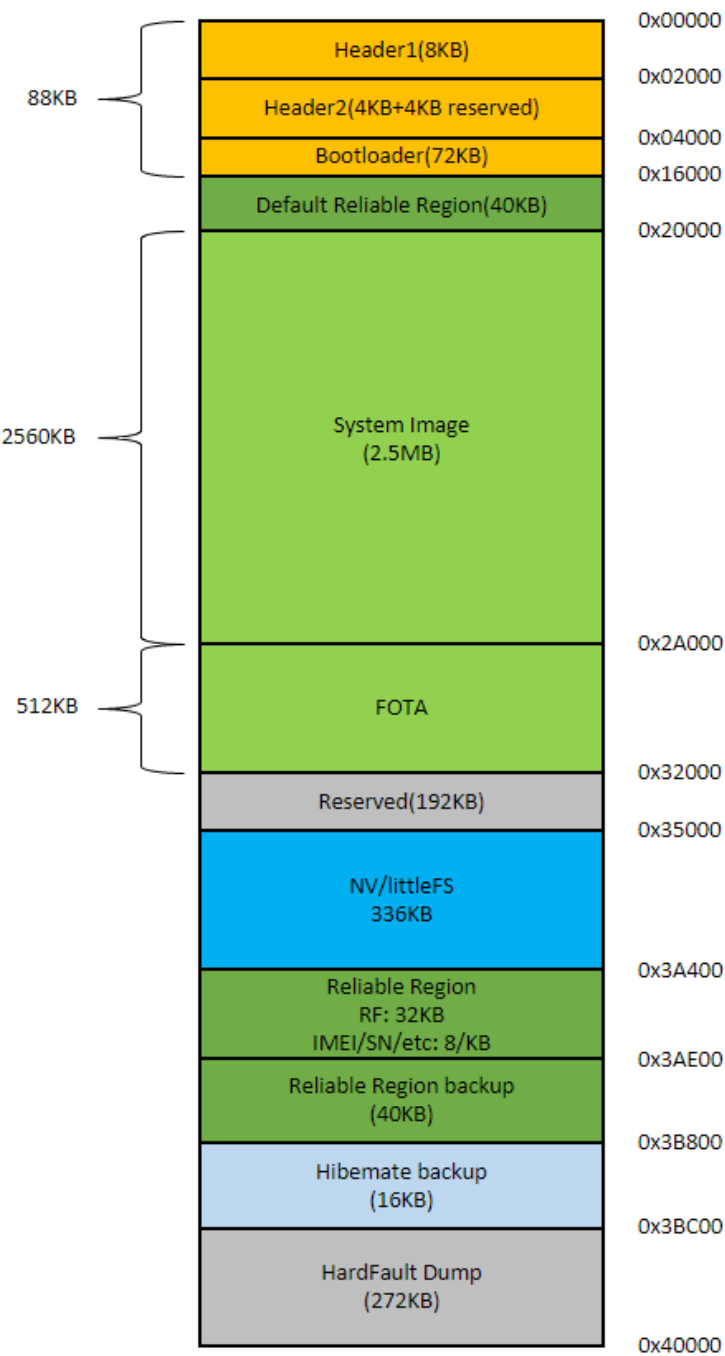

Figure 1: Flash memory layout

2. RAM MEMORY LAYOUT

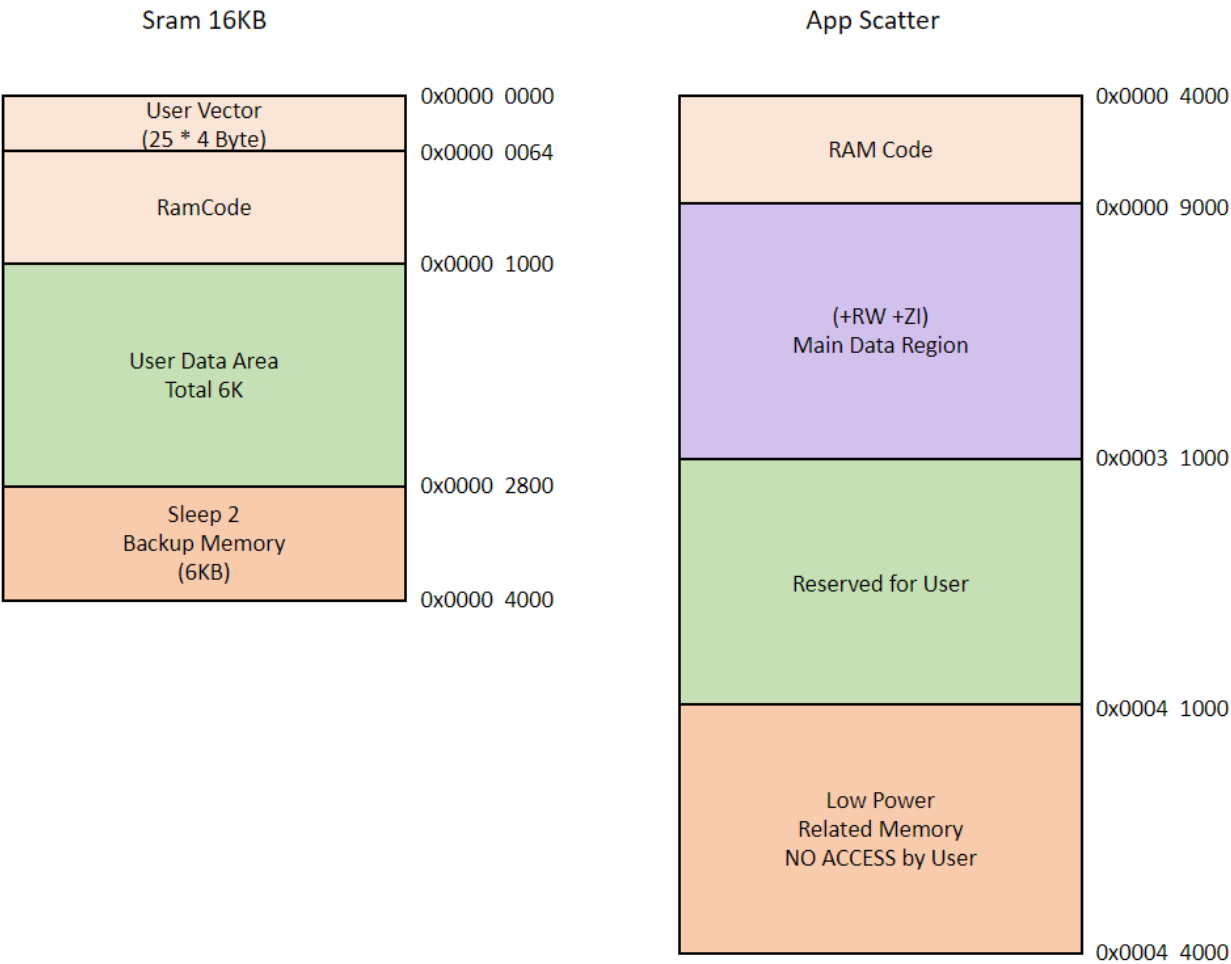The following figure shows the RAM layout of the iMCP HTNB32L-XXX:

Figure 2: RAM memory layout

ABBREVIATIONS

Table 1: Abbreviations

Acronym	Description
RAM	Random-access memory
FOTA	Firmware over-the-air
SRAM	Static random-access memory
SiP	System-in-Package

LIST OF FIGURES

LIST OF TABLES

REVISION HISTORY

Version	Date	Changes	Authors
00	28/09/2023	- Initial draft	MSZ
01	29/09/2023	Figure captions	HBG

CONTACT

HT MICRON SEMICONDUTORES S.A.
Av. Unisinos, 1550 | 93022-750 | São Leopoldo | RS | Brasil
www.htmicron.com.br

DOCUMENT INFORMATION

Document Title:	iMCP HTNB32L-XXX – Memory Layout
Document Subtitle:	Memory layout for iMCP HTNB32L-XXX System-in-Package
Classification:	PUBLIC
Doc. Type:	USER MANUAL
Revision:	v.02
Date:	28/09/2023
Code:	HTNB32L-XXX-UM-0006

DISCLAIMER

This document is a property of HT Micron.
HT Micron does not assume any responsibility for use what is described.
This document is subject to change without notice.