HT MICRON
semicondutores

iMCP HTNB32L-XXX DATASHEET

NB-IoT Wireless Communication System-in-Package

PRODUCT OVERVIEW

iMCP HTNBAT32L-XXX is a highly compact and low-power wireless communication device based on Qualcomm QCX-212 LTE IoT Modem, supporting single-mode 3GPP Release 14 Cat. NB2 IoT connectivity.

FEATURES

- CPU: ARM Cortex M3 @ 204MHz/102MHz/26MHz
- 4 MB NOR flash
- 272Kb SRAM: 256Kb + 16Kb instruction cache
- Digital Interfaces
  - 2x I^2C,
  - 3x UART,
  - 2x SPI,
  - 2-Channel 12-bit ADC,
  - 10x GPIOs:
    - 6x PWM,
    - 4x Timer
    - 1x WAKEUP
    - 1x AON (keeping output during deep sleep)
- Power Supply (range): 2.5 - 4.3V, typical 3.3V (3GPP min. 3.0V)
- Operating temperature: TBD
- Frequency range:
  - LTE low bands: 5, 8, 12, 13, 14, 17, 18, 19, 20, 26, 28, and 85 (698-960MHz)
  - LTE mid bands: 1, 2, 3, 4, 25, 66, and 70 (1710-2200MHz)
- Low-power mode (4 levels):
  - PSM: sub 1uA (M3 idle ~20mA)
  - DRX (2.56 s): 110 µA typically
  - Rx: 10 mA typically
  - Tx: 24 mA typically
- TX output power: up to 14, 20 and 23 dBm
- Antenna Pin Impedance: 50 ohms

PACKAGE

- Type: LGA
- Size: 13x13x1.5mm
- HW Integration:
  - 26 MHz crystal
  - 32.768KHz RTC crystal
  - RF filters and matching networks
  - SP6T Switch (SKY13416)
- eSIM
- Spray shielding (FCC requirement)

INTERFACES

- uSIM: external connection

CERTIFICATIONS

- ANATEL (on-going)
- FCC/ISED (on-going)
- CE (on-going)

SECURITY

- Hardware encryption and decryption module (AES and SHA)
- Flash encryption.
- True random number generator
- Non-Removable UICC
- Secure boot
- Secure Sockets Layer (SSL), Transport Layer Security (TLS), Datagram Transport Security (DTLS).

SOFTWARE FEATURES

- Location: ECID, OTDOA (LTE-based positioning) – network dependent
- FreeRTOS
- Control via AT Commands according to 3GPP TS27.005, 27.007 and customized AT commands.
- CMSIS
- OpenCPU
- IPv4, IPv6 and non-IP
- User Datagram Protocol (UDP), Transmission Control Protocol (TCP)
- MQTT, CoAP and HTTPS
- Lightweight M2M (LwM2M)

SUMMARY

DOCUMENT INFO

This document provides information about iMCP HTNB32L-XXX – NB-IoT System-in-package (SiP) family. If you need more information about the available features, or any other question, you can open your ticket support here. You can also access our github repository to stay updated with latest version of this document and find more information about our products.

1 OVERVIEW

The iMCP HTNBAT32L-XXX is a highly compact and low-power wireless communication device based on Qualcomm QCX-212 LTE IoT Modem, supporting single-mode 3GPP Release 14 Cat-NB2 IoT connectivity.

1.1. Internal system block diagram

The block diagram presents the elements integrated within the iMCP HTNB32L, embedded SIM is only available on the HTNB32L-XX1 devices.

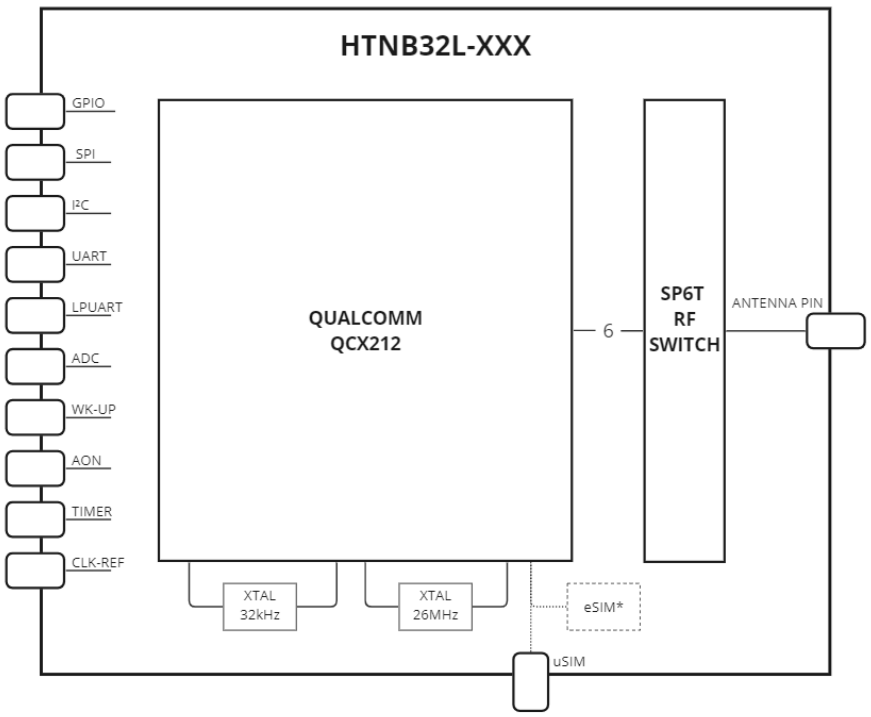


FIGURE 1: IMCP HTNB32L-XXX BLOCK DIAGRAM.

1.2. Application circuit

A common application diagram is presented to shows a simple application using the iMCP HTNB32L.

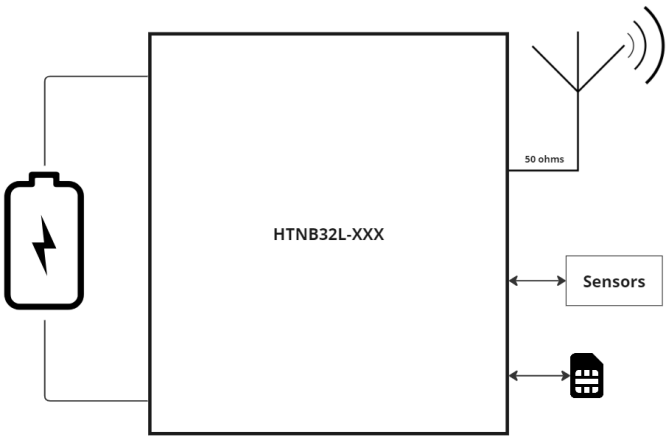


FIGURE 2. TYPICAL APPLICATION.

2 PINNING INFORMATION

This document section provides a detailed pin diagram, illustrating the configuration and connectivity of the pins on the System-in-Package.

2.1. Pin diagram

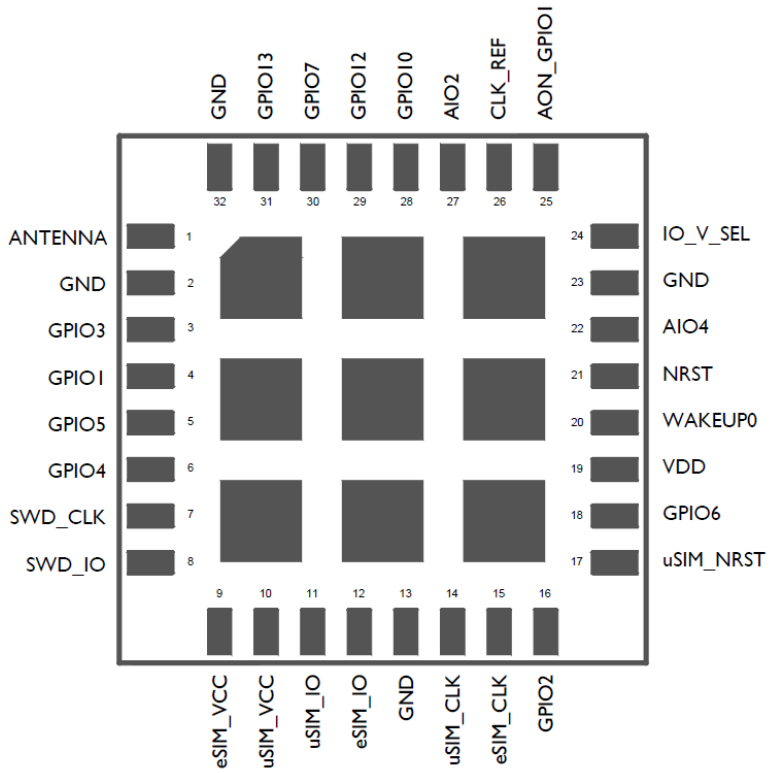


FIGURE 3: IMCP HTNB32L-XXX PINOUT.

2.2. Pin Diagram

TABLE 1: PINOUT ALTERNATIVE FUNCTION.

Pin Number	PAD name and/or function	Alt. Functions	Type	Functional Description
1	ANTENNA	–	RF	RF Input/Output
2	GND	–	Ground	–
3	GPIO3	UART0_CTSn UART2_TXD SPI1_MOSI PWM1	B-PU:nppd DI DO DO DO	Configurable I/O UART0 clear to send UART2 transmit data SPI1 master out/slave in Pulse-width modulation 1
4	GPIO1	UART2_TXD BOOT_CONFIG	B-PU:nppd DO DI	Configurable I/O UART2 transmit data Boot configuration control bit
5	GPIO5	UART0_TXD I2C1_SCL SPI1_SCLK PWM3	B-PU:nppd DO DO DO DO	Configurable I/O UART0 transmit data I2C1 serial clock SPI1 serial clock Pulse-width modulation 3
6	GPIO4	UART0_RXD I2C1_SDA SPI1_MISO	B-PU:nppd DI B DI	Configurable I/O UART0 receive data I2C1 serial data SPI1 master in/slave out

		PWM2	DO	Pulse-width modulation 2
7	SWD_CLK	UART2_RXD UART1_RTSn PWM4	DIO DI DO DO	Serial wire debug clock UART2 receive data UART 1 request to send Pulse-width modulation 4
8	SWD_IO	UART2_TXD UART1_CTSn PWM5	DIO DO DI DO	Serial wire debug data UART2 transmit data UART1 clear to send Pulse-width modulation 5
9	eSIM_VCC	-	VI	eSIM voltage input
10	uSIM_VCC	-	VO	SIM card voltage output
11	uSIM_IO	-	DIO	SIM card I/O
12	eSIM_IO	-	DIO	eSIM I/O
13	GND	–	Ground	–
14	uSIM_CLK	-	DIO	SIM card clock
15	eSIM_CLK	-	DIO	eSIM clock
16	GPIO2	TIMER [0] UART0_RTSn UART2_RXD SPI1_SSn0 PWM0	B-PU:nppd DIO DO DI DO DO	Configurable I/O Counter time [4] UART0 request to send UART2 receive data SPI 1 Slave Select 0 Pulse-width modulation 0
17	uSIM_NRST/ eSIM_NRST	-	DIO	SIM card reset
18	GPIO6	SPI0_SSn0 I2C0_SDA UART1_RTSn PWM4 TIMER [1]	B-PU:nppd DO B DO DO DIO	Configurable I/O SPIO 0 slave select 0 I2C 0 serial data UART 1 request to send Pulse-width modulation 4 Counter timer [1]
19	VDD	–	Power	Input Power (2.5 ~ 3.6V)
20	WAKEUP0	-	AI	External wakeup source
21	NRST	-	AI	System reset / Active-low
22	AIO4	-	AIO	ADC channel 4
23	GND	–	Ground	–
24	IO_V_SEL	-	AI	I/O voltage selection Floating - 1.8V Grounded (0V) - 3.3V
25	AON_GPIO1	AON_GPIO1 GPIO20 TIMER [5]	DIO-PD:nppu	Always on I/O Configurable I/O Counter time [5]
26	CLK_REF	-	-	–
27	AIO2	-	AIO	ADC channel 2
28	GPIO10	I2C0_SCL SPI1_SSn1 PWM0 TIMER [3]	B-PU:nppd DO DO DO DIO	Configurable I/O I2C 0 serial clock SPIO 1 slave select 1 Pulse-width modulation 0 Counter timer [3]
29	GPIO12	SPI0_SCLK I2C1_SCL UART1_TXD PWM1	B-PU:nppd DO DO DO DO	Configurable I/O SPI0 serial clock I2C1 serial clock UART1 transmit data Pulse-width modulation 1
30	GPIO7	SPI0_MOSI I2C0_SCL UART1_CTSn PWM5	B-PU:nppd DO DO DI DO	Configurable I/O SPI0 master out/slave in I2C0 serial clock UART1 clear to send Pulse-width modulation 5

31	GPIO13	SPI0_MISO I2C1_SDA UART1_RXD PWM0	B-PU:nppd DI B DI DO	Configurable I/O SPI0 master in/slave out I2C1 serial data UART1 receive data Pulse-width modulation 0
32	GND	–	Ground	–

2.3. Pin description and alternative functions

This document section provides a detailed pin diagram, illustrating the configuration and connectivity of the pins on the System-in-Package.

TABLE 2: PINOUT ALTERNATIVE FUNCTION.

Pad Number	Pad Name	Boot Configuration	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
1	ANTENNA	–	–	–	–	–	–	–	–	–
2	GND	–	–	–	–	–	–	–	–	–
3	GPIO3	–	GPIO3	UART0_CTSn	UART2_TXD	SPI1_MOSI	–	PWM1	–	–
4	GPIO1	BOOT_CONFIG	GPIO1	–	UART2_TXD	–	–	–	–	–
5	GPIO5	–	GPIO5	UART0_TXD	I2C1_SCL	SPI1_SCLK	–	PWM3	–	–
6	GPIO4	–	GPIO4	UART0_RXD	I2C1_SDA	SPI1_MISO	–	PWM2	–	–
7	SWD_CLK	–	–	–	UART2_RXD	UART1_RTSn	–	PWM4	–	GPIO18
8	SWD_IO	–	–	–	UART2_TXD	UART1_CTSn	–	PWM5	–	GPIO19
9	eSIM_VCC	–	–	–	–	–	–	–	–	–
10	uSIM_VCC	–	–	–	–	–	–	–	–	–
11	uSIM_IO	–	–	–	–	–	–	–	–	–
12	eSIM_IO	–	–	–	–	–	–	–	–	–
13	GND	–	–	–	–	–	–	–	–	–
14	uSIM_CLK	–	–	–	–	–	–	–	–	–
15	eSIM_CLK	–	–	–	–	–	–	–	–	–
16	GPIO2	–	GPIO2/Timer0	UART0_RTSn	UART2_RXD	SPI1_SSn0	–	PWM0	–	–
17	uSIM_RSTN / eSIM_RSTN	–	–	–	–	–	–	–	–	–
18	GPIO6	–	GPIO6/Timer1	SPI0_SSn0	I2C0_SDA	UART1_RTSn	–	PWM4	–	–
19	VDD	–	–	–	–	–	–	–	–	–
20	WAKEUP0	–	–	–	–	–	–	–	–	–
21	RESETN	–	–	–	–	–	–	–	–	–
22	AIO4	–	–	–	–	–	–	–	–	–
23	GND	–	–	–	–	–	–	–	–	–
24	IO_1833_SEL	–	–	–	–	–	–	–	–	–
25	AON_GPIO1	–	GPIO20/Timer5	–	–	–	–	–	–	–
26	CLK_REF	–	–	–	–	–	–	–	–	–
27	AIO2	–	–	–	–	–	–	–	–	–
28	GPIO10	–	GPIO10/Timer3	I2C0_SCL	–	SPI1_SSn1	–	PWM0	–	–
29	GPIO12	–	GPIO12	SPI0_SCLK	I2C1_SCL	UART1_TXD	–	PWM1	–	–
30	GPIO7	–	GPIO7	SPI0_MOSI	I2C0_SCL	UART1_CTSn	–	PWM5	–	–
31	GPIO13	–	GPIO13	SPI0_MISO	I2C1_SDA	UART1_RXD	–	PWM0	–	–
32	GND	–	–	–	–	–	–	–	–	–

Color code

TABLE 3: ALTERNATIVE FUNCTION COLOR CODE – BY INTERFACE.

Color	Interface
	UART0
	UART1
	UART2
	SPI0
	SPI1
	I2C0
	I2C1

3 STATIC CHARACTERISTICS

3.1 General operating range

Operating conditions include the iMCP HTNB32L parameters that meets all performance specifications, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

TABLE 4: GENERAL OPERATING RANGE.

Parameter	Min	Typ.	Max	Unit
Supply Voltage	2.7	3.3	3.6	V
Operating Temperature	-20	-	+75	°C

3.2 Absolute maximum ratings

The absolute maximum ratings reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications.

TABLE 5: ABSOLUTE MAXIMUM RATINGS.

Parameter	Min	Max	Unit
Supply Voltage	-0.3	4.5	V
Analog IO	-0.3	3.6	V
GPIO	-0.3	V_{DD} + 0.3	V
uSIM Interface	-0.3	V_{DD} + 0.3	V
Storage Temperature	-55	+150	°C

3.3 MCU I/O Port Characteristics

The MCU I/O ports characteristics depends on the configuration of the IO_1833_SEL pin, which configure the GPIO V_{DD} voltage value to 1.8V (floating) or 3.3V (connected to GND).

TABLE 6: 1.8 V DIGITAL I/O CHARACTERISTICS.

Symbol	Parameter	Min	Typ.	Max	Unit
$\mathbf{V_{IL}}$	I/O Input low level voltage	-	-	0.2 V_{DD}	V
$\mathbf{V_{IH}}$	I/O Input high level voltage	0.7 V_{DD}	-	-	
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	-	-	0.15 V_{DD}	
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin	0.8 V_{DD}	-	-	

$\mathbf{V_{HYS}}$	Schmitt hysteresis voltage	62	-	111	mV
$\mathbf{I_{IL}}$	Input low leakage current	-10	-	10	µA
$\mathbf{I_{IH}}$	Input high leakage current	-10	-	10	
$\mathbf{I_{OL}}$	Output low current	-	12.2	-	mA
$\mathbf{I_{OH}}$	Output high current	-	11.4	-	
$\mathbf{I_{OL-AON}}$	Output low current (AON_GPIO#)	-	12.2	-	
$\mathbf{I_{OH-AON}}$	Output high current (AON_GPIO#)	-	4	-	
$\mathbf{I_{OZL}}$	Low-level, tri-state leakage current	-10	-	10	µA
$\mathbf{I_{OZH}}$	High-level, tri-state leakage current	-10	-	10	
$\mathbf{R_{PU}}$	Pull-up resistor	117	-	331	kΩ
$\mathbf{R_{PD}}$	Pull-down resistor	91	-	291	
$\mathbf{C_{IO}}$	I/O capacitance	-	-	3.5	pF

TABLE 7: 3.3 V DIGITAL I/O CHARACTERISTICS.

Symbol	Parameter	Min	Typ.	Max	Unit
$\mathbf{V_{IL}}$	I/O Input low level voltage	-	-	0.2 V_{DD}	V
$\mathbf{V_{IH}}$	I/O Input high level voltage	0.7 V_{DD}	-	-	
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	-	-	0.15 V_{DD}	
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin	0.8 V_{DD}	-	-	
$\mathbf{V_{HYS}}$	Schmitt hysteresis voltage	121	-	181	mV
$\mathbf{I_{IL}}$	Input low leakage current	-10	-	10	µA
$\mathbf{I_{IH}}$	Input high leakage current	-10	-	10	
$\mathbf{I_{OL}}$	Output low current	-	19.3	-	mA
$\mathbf{I_{OH}}$	Output high current	-	37	-	
$\mathbf{I_{OL-AON}}$	Output low current (AON_GPIO#)	-	19.3	-	
$\mathbf{I_{OH-AON}}$	Output high current (AON_GPIO#)	-	4	-	
$\mathbf{I_{OZL}}$	Low-level, tri-state leakage current	-10	-	10	µA
$\mathbf{I_{OZH}}$	High-level, tri-state leakage current	-10	-	10	
$\mathbf{R_{PU}}$	Pull-up resistor	58	-	133	kΩ
$\mathbf{R_{PD}}$	Pull-down resistor	52	-	128	
$\mathbf{C_{IO}}$	I/O capacitance	-	-	3.5	pF

TABLE 8: DIGITAL I/O CHARACTERISTICS OF USIM INTERFACE.

Symbol	Parameter	Min	Typ.	Max	Unit
$\mathbf{V_{IL}}$	I/O Input low level voltage	-	-	0.2 V_{DD}	V
$\mathbf{V_{IH}}$	I/O Input high level voltage	0.7 V_{DD}	-	-	
$\mathbf{V_{OL}}$	Output low level voltage for an I/O pin	-	-	0.15 V_{DD}	
$\mathbf{V_{OH}}$	Output high level voltage for an I/O pin	0.8 V_{DD}	-	-	
$\mathbf{V_{HYS}}$	Schmitt hysteresis voltage	62	-	111	mV
$\mathbf{I_{IL}}$	Input low leakage current	-10	-	10	µA
$\mathbf{I_{IH}}$	Input high leakage current	-10	-	10	

$\mathbf{I_{OL}}$	Output low current	-	12.2	-	mA
$\mathbf{I_{OH}}$	Output high current	-	11.4	-	
$\mathbf{I_{OL-AON}}$	Output low current (AON_GPIO#)	-	12.2	-	
$\mathbf{I_{OH-AON}}$	Output high current (AON_GPIO#)	-	4	-	
$\mathbf{I_{OZL}}$	Low-level, tri-state leakage current	-10	-	10	µA
$\mathbf{I_{OZH}}$	High-level, tri-state leakage current	-10	-	10	
$\mathbf{R_{PU}}$	Pull-up resistor	117	-	331	kΩ
$\mathbf{R_{PD}}$	Pull-down resistor	91	-	291	
$\mathbf{C_{IO}}$	I/O capacitance	-	-	3.5	pF

TABLE 9: DIGITAL I/O CHARACTERISTICS OF RESET AND WAKE-UP PINS.

Symbol	Parameter	Min	Max	Unit
$\mathbf{V_{IL}}$	I/O Input low level voltage	-	0.2 V_{DD}	V
$\mathbf{V_{IH}}$	I/O Input high level voltage	0.7 V_{DD}	-	
$\mathbf{V_{HYS}}$	Schmitt hysteresis voltage	200	-	mV
$\mathbf{I_{IL}}$	Input low leakage current	-10	-	µA
$\mathbf{I_{IH}}$	Input high leakage current	-	0.3	
$\mathbf{R_{PU}}$	Pull-up resistor	200	300	kΩ
$\mathbf{C_{IO}}$	I/O capacitance	1.2	2	pF

4 RF CHARACTERISTICS

4.1. Supported RF bands/connectivity and Output Power

TABLE 10: IMCP HTNB32L SUPPORTED NB-IOT BANDS.

RF Band	Transmit (TX) Frequency [MHz]	Receive (RX) Frequency [MHz]	Max. Output Power [dBm]	Min. Output Power [dBm]
LTE B1	1920 – 1980	2110 – 2170	23dBm ± 2dB	< -39dBm
LTE B2	1850 – 1910	1930 – 1990		
LTE B3	1710 – 1785	1805 – 1880		
LTE B4	1710 – 1755	2110 – 2155		
LTE B5	824 – 849	869 – 894		
LTE B8	880 – 915	925 – 960		
LTE B12	699 – 716	729 – 746		
LTE B13	777 – 787	746 – 756		
LTE B14	788 – 798	758 – 768		
LTE B17	704 – 716	734 – 746		
LTE B18	815 – 830	860 – 875		
LTE B19	830 – 845	875 – 890		
LTE B20	832 – 862	791 – 821		
LTE B25	1850 – 1915	1930 – 1995		
LTE B26	814 – 849	859 – 894		
LTE B28	703 – 748	758 – 803		
LTE B66	1710 – 1780	2110 – 2200		
LTE B70	1695 – 1710	1995 – 2020		
LTE B85	698 – 716	728 – 746		

4.2. NB-IoT transmission current consumption

TABLE 11: IMCP HTNB32L NB-IOT TRANSMITTER CURRENT CONSUMPTION.

RF band	RF output power [dBm]	Current consumption [mA]
LTE B1	TBD	TBD
LTE B2	TBD	TBD
LTE B3	TBD	TBD
LTE B4	TBD	TBD
LTE B5	TBD	TBD
LTE B8	TBD	TBD
LTE B12	TBD	TBD
LTE B13	TBD	TBD
LTE B14	TBD	TBD
LTE B17	TBD	TBD
LTE B18	TBD	TBD
LTE B19	TBD	TBD
LTE B20	TBD	TBD
LTE B25	TBD	TBD
LTE B26	TBD	TBD
LTE B28	TBD	TBD

LTE B66	TBD	TBD
LTE B70	TBD	TBD
LTE B85	TBD	TBD

4.3. NB-IoT receiving sensitivity

The table X shows the conducted RF receiving sensitivity of iMCP HTNB32L.

TABLE 12: IMCP HTNB32L TYPICAL CONDUCTED RX SENSITIVITY.

RF band	Typical Conducted NB-IoT Sensitivity Level @ 95% of Maximum Throughput
LTE B1	TBD
LTE B2	TBD
LTE B3	TBD
LTE B4	TBD
LTE B5	TBD
LTE B8	TBD
LTE B12	TBD
LTE B13	TBD
LTE B14	TBD
LTE B17	TBD
LTE B18	TBD
LTE B19	TBD
LTE B20	TBD
LTE B25	TBD
LTE B26	TBD
LTE B28	TBD
LTE B66	TBD
LTE B70	TBD
LTE B85	TBD

4.4. Radio Frequency (RF) integration

A 50Ω RF track (with maximum VSWR 1.1:1, and 0.5 dB loss) is recommended to connect the module's antenna pin to standard RF antenna connectors (e.g. SMA, U.FL, etc.).

TABLE 13: RF TRACK REQUIREMENTS.

Pad #	RF Pin	Impedance	VSWR TX/RX (max.)
2	GND	-	-
1	Antenna	50Ω	1.8
32	GND	-	-

5 FUNCTIONAL OVERVIEW

5.1. Low power modes

The iMCP HTNB32L-XXX has two groups of low power modes. Each group is described in Subsection 5.1.1 and Subsection 5.1.2.

5.1.1. Sleep Manager

The Sleep Manager is implemented considering the state of each task running in the FreeRTOS environment. Thus, the Sleep Manager respects the deadline of every NB task, either waiting for its end or taking it into account to determine the most appropriate sleep mode level. More information can be found at HTNB32L-XXX-UM-0005 document.

TABLE 14: SLEEP MANAGER - LOW POWER MODES.

Power Mode	Current Consumption (µA)
Sleep1	0.8
Sleep2	6.33
Hibernate1	15.3
Hibernate2	4200

5.1.2. Sleep Mode Test Functions

The Sleep Mode Test Functions are low level routines that enables configuring the iMCP HTNB32L-XXX device to a specific low power mode. Unlike Sleep Manager, the test functions do not consider the state of any OS or NB-IoT (stack) task.

TABLE 15: SLEEP MODE TEST FUNCTIONS - LOW POWER MODES.

Power Mode	Current Consumption (µA)
Sleep1	0.8
Sleep2	2.99
Hibernate1	6.86
Hibernate2	14.97

5.2. USIM interface

The iMCP HTNB32L implements a USIM interface that can be used to control either:

- the module's internal embedded SIM (eSIM), HTNB32L-XX1devices, or
- an external USIM (plastic SIM card).

The iMCP HTNB32L-XX1 devices need an external connection, to ensure the internal eSIM connectivity to the module. The required connections are between pins eSIM_VCC (9) and uSIM_VCC (10), eSIM_IO (11) and uSIM_IO (12), eSIM_CLK (14) and eSIM_CLK (15).

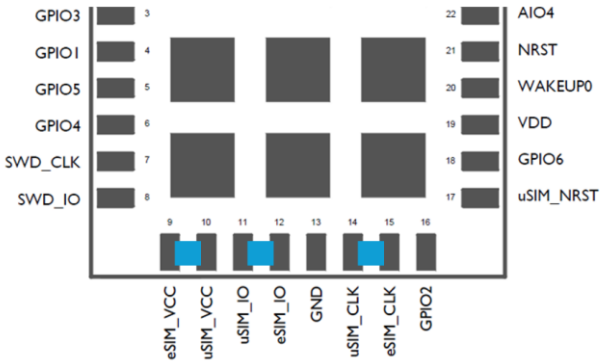


FIGURE 4: IMCP HTNB32L-XX1 CONNECTIONS FOR EMBEDDED SIM.

5.3. UART interface

iMCP HTNB32L supports up to three UART. The following are the UART specifications:

- Configurable band rate 4.9 Kbps, 9.6 Kbps, 115.2 Kbps, 921.6 Kbps, up to 3 Mbps
- Independent 32 bytes Tx/Rx FIFO
- Support transmit and receive 5-bit~8-bit characters
- Support odd, even, and no check
- Support 1 or 2 stop bit
- Support DMA operation
- Support flow control (UART0/1)
- Support NRZ coding

5.4. I^2C interface

iMCP HTNB32L supports up to two I2C. The following are the I2C specifications:

- Configurable clock up to 400 kHz
- Master or slave configurable
- Independent 16 bytes Tx/Rx FIFO
- Support 7/10-bit address
- Support DMA operation
- Support clock extension
- Configurable SCL waveform

5.5. SPI interface

iMCP HTNB32L supports up to two SPI. The following are the SPI specifications:

- Configurable clock up to 25.6 MHz
- Master or slave configurable
- Independent Tx/Rx FIFO
- Configurable CPOL/CPHA
- Support DMA operation

5.6. Analog to Digital Converter (ADC)

iMCP HTNB32L AUXADC includes the following functional modules:

- Analog channel module:

- Apply the channel to the divider circuit for voltage adjustment (m*R)
- Send this voltage signal to the input port of AUXADC

- Temperature sensor: The thermal sensor output voltage changes according to the change of the chip temperature.
- 12-bit AUXADC: Quantize the input voltage into 12-bit digital data

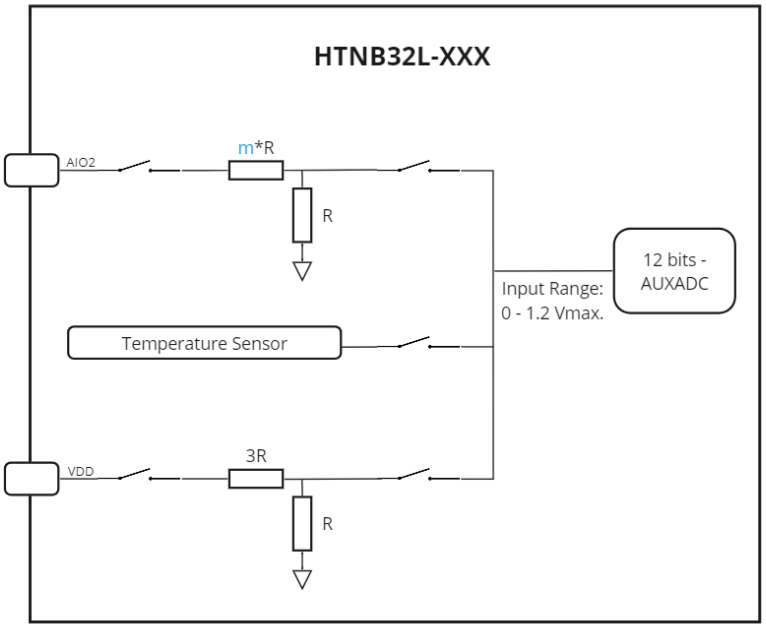


FIGURE 5: AUXADC DIAGRAM.

The internal AUXADC block have some requirements:

TABLE 16: AUXADC INPUT CHANNEL.

Input Chanel	Application	Input range
AIO2/4 pin	External signal acquisition	0 – 3.4 V
Temperature Sensor	Internal temperature sensor signal	- 40°C – 85°C
VDD pin	Voltage monitoring	2.7V – 4.3 V

5.7. Configurable GPIOs

There are 13 GPIOs in iMCP HTNB32L-XXX (including one AON GPIOs).

- Each GPIO supports:
  - Internal pull-up
  - Internal pull-down
  - No-pull options
- When powered up, default configuration of GPIOs are configured as input and pull-down

6 MEMORY MAPPING

8.1. Flash Memory Layout

The HTNB32L-XXX has a 1.6 MB partition for the system image and 0.9 MB is reserved for user and new features. The flash memory layout of the HTNB32L-XXX device is illustrated in Figure 6 :

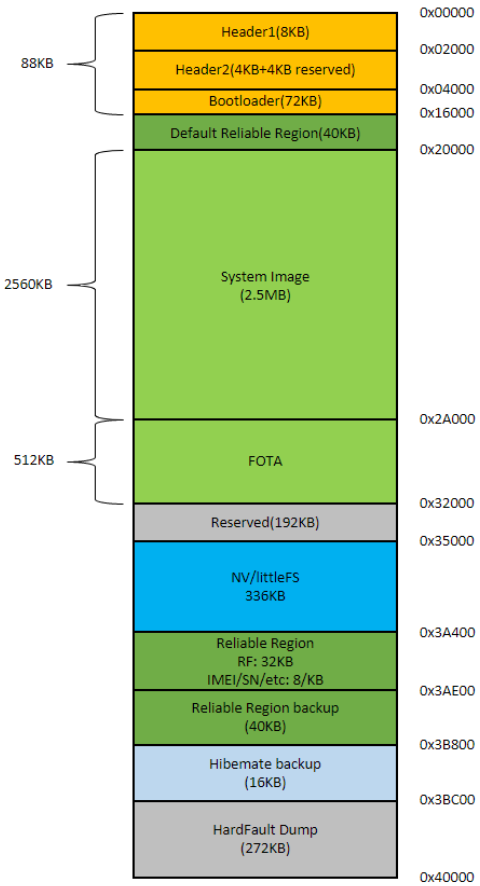


FIGURE 6: FLASH MEMORY LAYOUT.

8.2. RAM Memory Layout

The RAM memory layout of the iMCP HTNB32L-XXX device is illustrated in Figure 7:

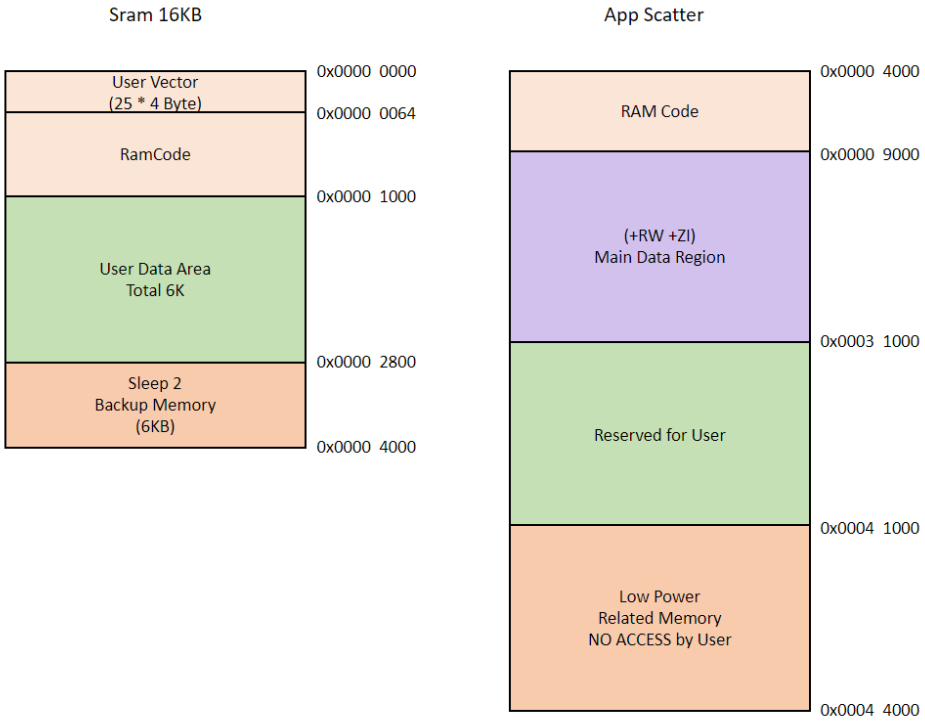


FIGURE 7: RAM MEMORY LAYOUT.

7 PACKAGING INFORMATION

7.1. Package Outline

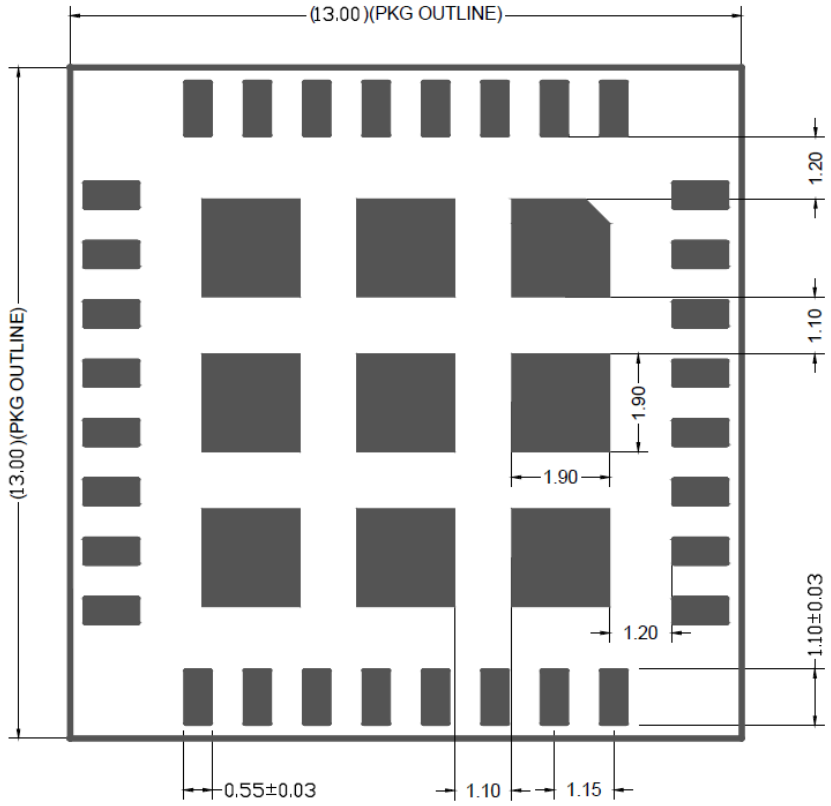


FIGURE 8: PACKAGE OUTLINE.

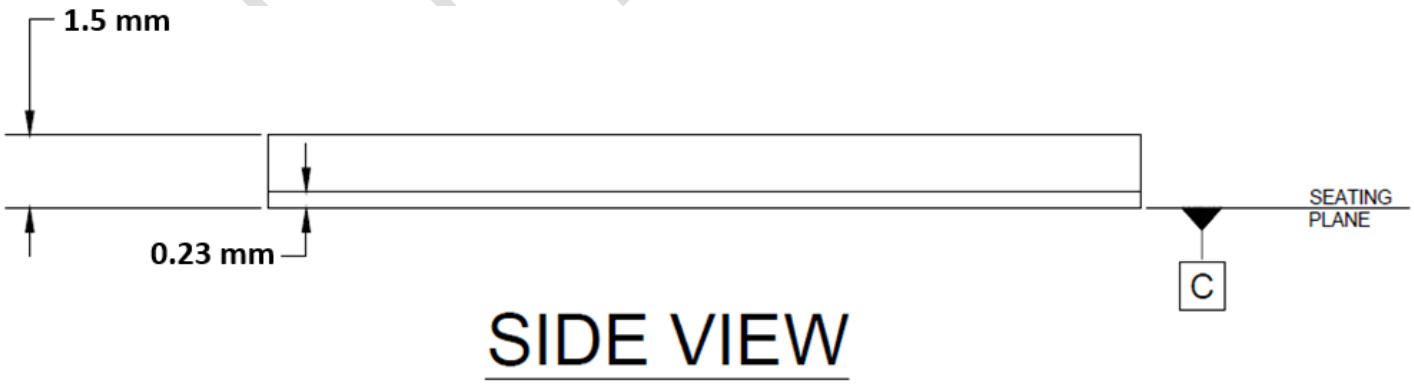


FIGURE 9: PACKAGE OUTLINE SIDE VIEW.

7.2. Recommended PCB Footprint

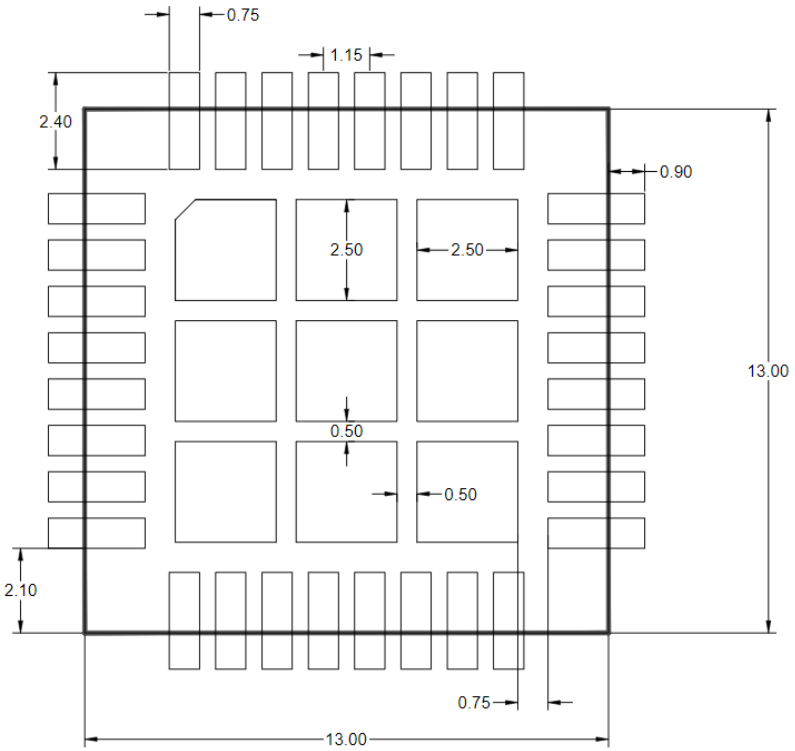


FIGURE 10: RECOMMENDED PCB FOOTPRINT.

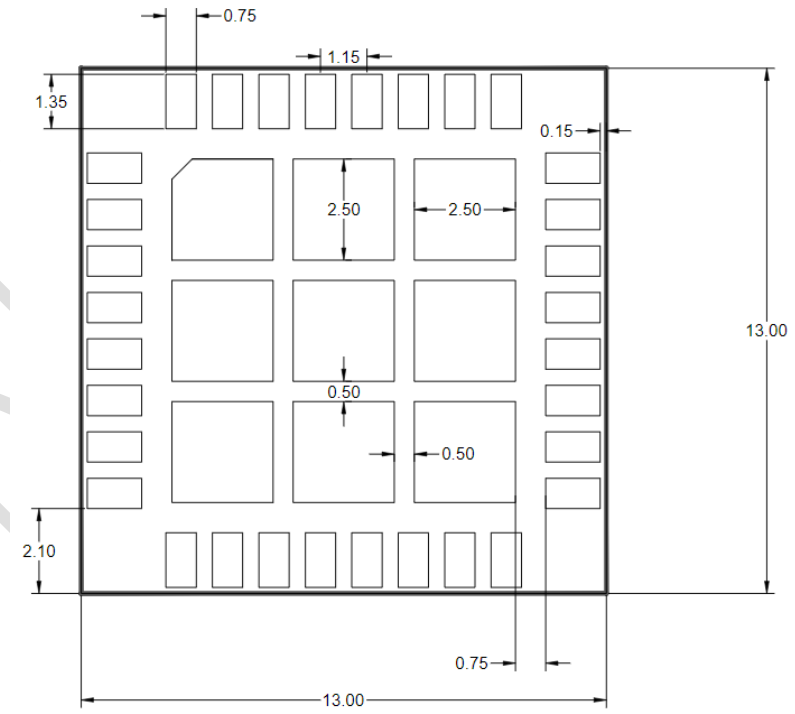


FIGURE 11: RECOMMENDED PCB FOOTPRINT FOR SHIELDED HTNB32L-XXX.

8 ORDERING INFORMATION

8.1. Marking

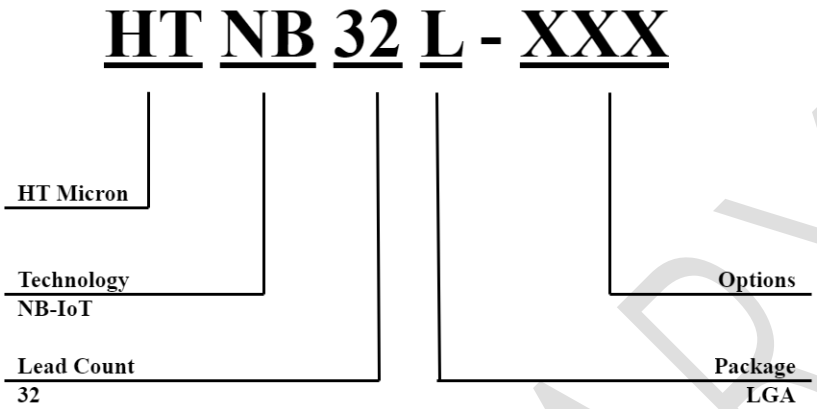


FIGURE 12: PART NUMBER DESCRIPTION.

TABLE 17: PART NUMBERS DESCRIPTION TABLE.

Option number	Region	Shielding	Integrated eSIM
000	BR	NO	NO
001	BR	NO	YES
010	BR	YES	NO
011	BR	YES	YES
Z00	GLOBAL	NO	NO
Z01	GLOBAL	NO	YES
Z10	GLOBAL	YES	NO
Z11	GLOBAL	YES	YES

8.2. Tray packaging

TABLE 18: ORDERING INFORMATION.

Part number	Package	
	Name	Description
HTNB32L-XXX	iMCP HTNB32L	SiP module in LGA package; body 13mm x 13mm

9 STORAGE AND HANDLING

CAUTION

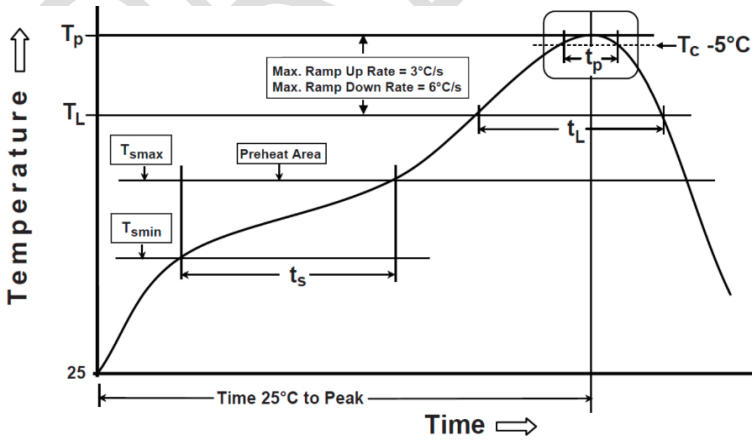
ELECTROSTATIC and MOISTURE SENSITIVE DEVICE

LEVEL 3

- Baking for 24 hours at 125 ±5°C is strongly recommended prior to mounting.
- Take proper precautions to avoid high-energy electrostatic discharge (ESD) as permanent damage may occur.
- For handling methods refer to the latest ESD Association standard ANSI/ESD S20.20.
- Do not expose the device to corrosive gases, extreme humidity, extensive direct sunlight.
- The device is susceptible to delamination or crack damage induced by absorbed moisture and high temperature.
- Shelf life in sealed bagged tray: 12 months at ≤40°C and ≤90% relative humidity (RH).
- This device is rated MSL 3.
- For bagged tray lots: after the bag is opened, the humidity card must read ≤20% (at 23 ±5°C), and the devices must be mounted within 168 hours at environmental conditions of ≤30°C, ≤60% RH.
- If the above condition is not met, baking for 24 hours at 125 ±5°C is mandatory prior to mounting.
- For moisture sensitivity devices precaution methods refer to the latest standard IPC/JEDEC-J-STD-033.
- For any other packing method: baking is required for 192 hours at 40°C prior to mounting.
- This device is composed of all RoHS-compliant materials. Refer to **Error! Reference source not found.** for typical Pb-Free reflow conditions.
- Hand soldering is not recommended for this device.
- For moisture sensitivity classification and soldering methods, refer to the latest standard IPC/JEDEC-J-STD-020.
- Do not drop, shock or apply mechanical stress.

9.1. Tray packaging

Soldering conditions depend greatly on the solder paste that is used and as such are application specific. The picture below depicts typical Pb-free soldering conditions as seen in IPC/JEDEC-J-STD-020 standard, which are commonly used in the industry. However, ultimately, we recommend that the instructions of the solder supplier are followed.



Min preheat temperature (T_{smin}): 150 °C
Max preheat temperature (T_{smax}): 200 °C
Preheat (soaking) time (T_s): 60 to 120 s
Liquidous temperature (T_L): 217 °C
Peak temperature (T_p): 260 °C
Max ramp-up rate (T_L to T_p): 3 °C/s
Time above T_L (t_L): 60 to 150 s
Classification temperature (T_c): 260 °C
Time above Tc -5 °C (t_p): 30 s
Max ramp-down rate (T_p to T_L): 6 °C/s
Max time 25°C to T_p: 8 minutes

FIGURE 13: TYPICAL PB-FREE REFLOW CONDITIONS (IPC/JEDEC-J-STD-020).

10 APPENDIX AND REFERENCES

A list of complementary documents (all available in the HTNB32L-XXX SDK) is presented in Table 19 and Table 20. To request access to these documents, please contact imcp@htmicron.com.

11.1. User Manuals

TABLE 19: IMCP HTNB32L-XXX USER MANUALS LIST.

Document	Status
HTNB32L-XXX-UM0001-Getting_Started	Confidential
HTNB32L-XXX-UM0002-AT_Commands	Confidential
HTNB32L-XXX-UM0003-HTTools	Confidential
HTNB32L-XXX-UM0004-SDK_User_Manual	Confidential
HTNB32L-XXX-UM0005-PMU_SleepModes	Confidential
HTNB32L-XXX-UM0006-Memory_Layout	Confidential

11.2. Application Notes

TABLE 20: IMCP HTNB32L-XXX APPLICATION NOTES LIST.

Document	Status
HTNB32L-XXX-AN0001-MQTT_Example	Confidential
HTNB32L-XXX-AN0002-Driver_Example	Confidential

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ABBREVIATIONS

LIST OF FIGURES

LIST OF TABLES

REVISION HISTORY

Revision	Date	Remarks
00	April, 2024	Initial draft

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