Evolving EDA Beyond its E-Roots: An Overview (invited paper)

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***Abstract*—Over the past decade, CMOS scaling has seen increasingly intrusive challenges from cost, variability, energy, reliability, and fundamental device-architectural and materials limitations. To maintain Moore's-Law scaling of integration value, the industry is urgently exploring beyond-silicon and beyond-CMOS device, interconnect and memory options, as well as heterogeneous, "More than Moore" integration and packaging technologies. This coincides with a turning point for the Electronic Design Automation (EDA) field, which has for 50+ years been a key enabler of the semiconductor industry's amazing growth. Maturation of the EDA industry and its related academic research efforts inevitably result in a spiral of declining valuations (multiples), venture capital investments, research funding, and student interest. To counter this trajectory, the EDA field's business models, research portfolios, and funding models have been going through various diversifications, but in a rather ad-hoc manner. This begs the question of how the paradigms and research methodologies of EDA can be leveraged for design automation (DA) in other, emerging domains. Arguably, more efficient evolution and growth as a community requires a more systematic, coherent effort – as well as forward-looking vision – to steer by. In this paper, we review initial efforts of a new IEEE CEDA technical activity group dedicated to this purpose. These efforts span the cataloguing of past and current research trends, development of new metrics of research impact, and visions for future applications of EDA paradigms in broader design automation contexts. It is hoped that these efforts will be useful to the EDA community as it continues to evolve beyond its "E-roots".**

I. Introduction: IEEE CEDA's Future of DA Initiative

Electronic Design Automation (EDA) is an engineering success story, one that has enabled the modern computing era. Over the past five decades, EDA innovations have increased designers' productivity by many orders of magnitude. Indeed, while the information and computing revolution is often credited to Moore's-Law scaling, the complexity challenge has been addressed by EDA, with today's tools and methodologies enabling design, verification and test of ICs across multiple levels of abstraction and complexity. Until recently, the vision and efforts of the EDA community have been primarily focused on supporting the cost scaling that is "More Moore". This is reflected in several key market criteria (capacity, turnaround time, license cost) for EDA tools. Yet, despite its dominant focus on electronics, EDA is one of the first fields in engineering that is truly interdisciplinary: its abstractions, computational models, algorithms, methodologies, and tools have drawn from the work of chemists, device physicists, electrical engineers, computer scientists, applied mathematicians, operations researchers, and optimization experts. EDA tools can automatically transform a complex system-on-chip design from high-level functional description to detailed geometric description, performing synthesis, optimization, simulation and verification across all of the intervening levels of abstraction. However, growth of the traditional EDA industry, as well as of underlying research and development activity, has slowed due to maturation of both the semiconductor industry and the EDA field itself.

As we approach a 2020 wall of silicon, patterning, device, interconnect and cost limits, and as EDA technologies and the industry itself remain in their present mature state, it is now urgent to revisit the question of how the field will evolve and grow. Healthy growth requires exciting new directions as well as a steady supply of new experts trained at the graduate level. Unfortunately, recent years have seen diminished interest in "VLSI CAD" among electrical engineering and computer science students, and many graduating students in the field take jobs in other areas with higher growth potential (finance, big-data, mobile, social, etc.) upon finishing their degrees. The standing question is: how can the paradigms and research methodologies of EDA be leveraged for design automation (DA) in other, emerging domains to solve important contemporary real-world problems? Many researchers in our community are actively contributing to DA for a variety of other fields such as emerging nanotechnologies, biomedical and security. But, timely evolution and growth as a community requires a more systematic, coherent effort – as well as forward-looking visions of new target application domains by which to steer.

This paper reports the status of a recent initiative of the IEEE Council on Electronic Design Automation (CEDA) to study how EDA can "move beyond its E-roots". We note two seeds of this initiative. First, a series of recent CCC workshops on Extreme Scale Design Automation resulted in a report that identifies EDA research and funding priorities through 2025 and beyond [3]. The report cites today's challenges and shortcomings, but also envisions EDA as a broader discipline that can extend its methods into new markets. Other efforts have also provided visions and roadmaps for the field [1] [2] [12] [13] [14]. Second, the CANDE (Computer-Aided Network DEsign) Committee has since 1972 been a technical activity of the IEEE Circuits and Systems Society and, more recently, of IEEE CEDA. Essentially a working group for electronic computer-aided design, with varying levels of prominence over the years, CANDE has played a key role in the overall history of EDA (e.g., ICCAD was conceived at CANDE). To respond to changes in the technology, industry, and research context, CANDE activities have been redirected under the CEDA president-elect, Dr. Shishpal Rawat, to focus on new initiatives and activities such as our present initiative.

In the following, we report on efforts of the new IEEE CEDA technical activity group to systematize past roadmaps, trends, metrics of impact, and visions for the EDA field. We discuss the group's initial methodologies and results, and how to participate going forward. Specifically, three study teams have achieved initial outcomes. The first study team investigates and synthesizes prior decades of organized efforts to set out visions, roadmaps, EDA research centers, etc. The aim is to systematically categorize previous efforts, so that the field can learn from and build on these past results and conclusions. The second study team focuses on analyses of existing research artifacts, as an initial step toward development of metrics and predictors of "research impact" that could help steer investment and effort within the field. The third study group has worked toward clarifying a vision and set of recommendations for moving forward as a DA community; the group calls out relevant state-of-the-art automation problems in a variety of emerging fields that will be fertile ground for DA methodologies. This effort also included a Design Automation (DA) Perspective Challenge, co-located with the DAC-2015 conference, which solicited community input of visions for DA [15]. The event attracted 30 submissions from across industry and academia.

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The remainder of this paper is organized as follows. Section II summarizes the first working group's review of previous efforts; Section III summarizes the second working group's analyses aimed at quantitative measures of (funding, publication) impacts. Section IV reviews activities of the forward-looking "vision" team; additional details of the first DA Perspective Challenge are given in the Appendix. For each of the working groups, we give brief further commentary and/or perspective. Moreover, in Section V we describe 2001-2003 "research gap" analyses performed by the Semiconductor Research Corporation (SRC), which provide calibration of the investment and effort required to "move the needle". We conclude and note several next steps in Section VII.

II. Systemization of Prior Efforts

The Systemization of Prior Efforts (SoPE) working group summarized and analyzed three types of previous efforts: (i) recent roadmaps; (ii) current SRC focused research centers; and (iii) NSF Expedition in Computing grants relevant to EDA. Here, we provide a snapshot of the SoPE studies, and refer readers to the more detailed report in [24].

A. Roadmaps

The SoPE report covers three major existing roadmaps.

(i) The NSF Workshop on EDA: Past, Present, and Future. This 2009 workshop had two major goals: (i) to reflect on EDA's past success and project the potential of applying EDA methodologies and tools to other computing fields and application domains; and (ii) to evaluate progress made under the National Design Initiative established in 2006, and suggest new topics to be added to it.

The first part of the workshop report estimates the average total funding for EDA to be about $20M annually; this is assessed as very low compared with other relevant disciplines, and compared with investments made by European and Taiwanese projects. The second part of the report outlines the major foundational areas for future EDA support, and highlights a few emerging areas relevant to EDA. Recommendations are also made for EDA-related education.

(ii) The CCC Workshop series on Extreme Scale Design Automation. This workshop series, held jointly by ACM SIGDA and CCC, evaluated challenges faced by the contemporary EDA industry in educating and funding the next generation of EDA professionals. The first workshop centered on education, e.g., how to increase undergraduate and graduate student interest in EDA, and how to connect classroom material to real-world impactful problems. Suggested strategies included use of using massively open online courses (MOOCs), emphasis on higher-level concepts over low-level design skills, and greater presence in social media.

The second and third workshops studied the EDA challenges and opportunities over the next decade. For new and emerging technologies, the conclusions emphasize the importance of design metrics, and practical benchmarks to guide research and develop good models for unreliable physical phenomena. The most critical markets that can be shaped by EDA are identified as the cyberphysical systems and cybersecurity issues; new efforts to expand EDA toward these markets were recommended.

(iii) The ITRS roadmap. The mission of the *International Technology Roadmap for Semiconductors* (ITRS) [13] is to assure the continued cost and performance scaling of IC technology by studying key challenges, and formulating a roadmap to guide future academic research and industry investments. The System Drivers and Design International Technology Working Groups (ITWGs) of the ITRS are most relevant to EDA. The ITRS has had a substantial impact on the semiconductor research and industry. For example, the 2005 edition set out a "More Than Moore" era where, in particular, innovations across design, design technology, device architecture, and packaging/integration supply "equivalent scaling" to complement the continued "More Moore" geometric scaling. The ITRS Design ITWG has since 2001 systematically (a) quantified the design technology roadmap with precise metrics, and predicted design requirements and challenges that have motivated new solutions such as design for manufacturability; and (b) introduced and roadmapped key system drivers that are aligned to key segments of semiconductor industry.

The ITRS has also called out a *design technology productivity gap*: the 2× per node increase in available transistors per Moore's-Law density scaling, versus the 1.6× per node of actually realized transistor density scaling in leading-edge product families (e.g., microprocessors and application processors) [21]. To mitigate this scaling crisis over the 15-year ITRS horizon, *design-based equivalent scaling* (DES) methodologies such as error correcting codes, clock gating and GALS, as well as adaptivity and resilience mechanisms have been integrated into the roadmap of DA-provided potential solutions.

B. Present SRC Focused Research Centers

The SRC consortium of semiconductor companies has for over three decades managed university research in support of CMOS scaling and the IC industry's needs. In recent years, the SRC horizon has expanded to novel research areas and identification of new technologies by investing in new centers. Recent major SRC initiatives/centers are summarized in Table I.

TABLE I: Recent Major SRC Initiatives.

Global Research Collaborations (GRC)
New initiatives: Trustworthy and Secure Semiconductors and Systems (T3S); Advanced Connectivity (EP3C); and Innovative and Intelligent Internet of Things (I3T).
Center for Low Energy System Technology (LEAST)
Low voltage and steep subthreshold swing components. Research on material, devices, transduction mechanisms, benchmarking, and applications.
Center for Spintronics Materials, Interfaces, and Novel Architectures (C-SPIN)
Research on spin-based memory and architecture, from magnetic material systems, 2D materials, interface engineering, as well as design, architecture and optimization of spin-based logic, models, and architecture.
Center for Future Architectures Research (C-FAR)
Research on non-conventional CMOS-based computational paradigms covering multiple layers of computing stack from circuit to architecture, compilers, and languages are covered.
Center for Systems On Nanoscale Information fabriCs (SONIC)
Research on nontraditional nanoscale post-CMOS fabrics emphasizing on information rather than data processing. The focus includes stochastic and error-tolerant models, mixed-signal systems from sensors to RF and ADC, cognitive information architectures, as well as nano-functions and nano-primitives.
Terraswarm Research Center
Research on pervasive integration of smart sensors and actuators into our connected world. The themes include smart cities, platform architecture and OS, services and cloud interactions, as well as methodologies, models, and tools.

C. Relevant NSF Expedition in Computing Projects

NSF's Expeditions in Computing grants target ambitious and transformative research within the purview of the Computer and Information Science and Engineering directorate. Since the program started, there have been two Expedition grants relevant to EDA.

(i) Customizable, Domain-Specific Computing (CDSC). This project looks beyond homogeneous multicores by focusing on domain-specific customization using hardware accelerators, reconfigurable interconnects, domain-specific languages, and automation of these approaches through development of compilers and runtime systems.

(ii) Variability-Aware Software for Efficient Computing (VE). The VE project suggests new classes of computing machines that are adaptive and highly energy efficient, and that constantly monitor, predict, and adapt to system and component variability through proactive, software-dominated mechanisms. Major technical challenges are addressed across five research thrusts: measurement and modeling; design tools and testing; microarchitecture and compilers; runtime support; and applications and testbed.

D. Commentary on SoPE Working Group Outputs

Additional historical perspective can be found in early roadmapping efforts that have also compiled design, productivity, test, research, etc. challenges of the EDA industry. For example, in the EDA 200X report [12], participants from industry and academia define approaches to design larger chips with fewer engineers while successfully dealing with new challenges introduced by the sub-100nm technology. The report identifies enhancements and modifications to semiconductor processing, design methodology, and electronic design automation necessary to reach this objective, and makes 13 specific recommendations in these areas. A number of these were timely: use of flip-chip packaging, use of multiple metal layers, development of interconnect-centric design tools, signal integrity-aware physical design, model-based verification, etc. The EDA200X report's "Further Research" recommendations include research on process changes for soft-error prevention, measures of design effectiveness, physical design for soft-error reduction and asynchronous design automation. These areas remain active and are arguably still very relevant for the late-CMOS and post-CMOS eras that lie ahead.

The ITRS Design Chapter has called out power, signal integrity and design productivity as "Grand Challenges" for the past 15+ years (cf. the chapter's Design Cost model from 2001-present, and the Low-Power Design Technology model from 2009-present); these remain overarching challenges for EDA today. The System Drivers Chapter's "system drivers" are the key IC products that align to major semiconductor industry segments and that spur process and device/interconnect technology innovation; these include the high-performance microprocessor (MPU-HP) and consumer portable system-on-chip (SOC-CP) product classes [10].

It is important to note that for the 15 years of its previous editions (1998-2013), the "ITRS1.0" roadmap has been IC-centric. However, industry consolidation, the foundry-fabless business structure, and the slowdown of Moore's-Law cost scaling have all led to a regime wherein the high-value system products and application markets ultimately determine the roadmap for underlying manufacturing, integration and design technologies. For example, enterprise utility applications might drive energy harvesting, cloud storage and nano-power units. Hence, beginning with the 2015 edition, an "ITRS2.0" structure of the roadmap will highlight System Integration [9] (e.g., roadmaps for mobility/smartphone, cloud/datacenter/microserver, and IoT systems), Heterogeneous Integration, Outside System Connectivity, etc. in addition to More Moore. The new "top-down" organization of ITRS2.0 will likely identify important directions for DA evolution, such as autonomous vehicle, IoT, embedded health, etc.

III. Toward Metrics of DA Research Impact

For 50+ years, DA research has been performed in academia, semiconductor and system companies, and EDA companies worldwide. The DA Metrics group has performed analyses of DA research artifacts (research project abstracts, research needs statements, conference and journal papers, and patents) as a first step toward measurements of DA research impacts. Outcomes of DA research are just part of a much larger picture (Figure 1), and causal relationships between research activities (publications, student training) and ultimate impacts (company valuations, commercial tool availability, design productivity improvement) are not yet addressed by this working group.

The DA Metrics group's analyses of DA research *outputs* (papers, patents, EDA companies), upon which future metrics of DA research *impact* might be based, have leveraged industry and publication data along with modern text mining approaches [23]. Specific analyses include (i) evolution over time of latent Dirichlet analysis (LDA)-based topic models, (ii) temporal offsets of topic models between various corpora (e.g., research funding vs. patents vs. papers), and (iii) topological studies of the patent citation graph. Correlations with commercial tool availability are also made.

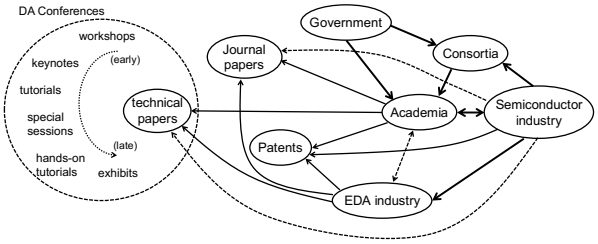

Fig. 1: Antecedents, creators, consumers and artifacts of DA research. The "life cycle" of ideas at DA conferences is also shown.

A. Methodology

Figure 2 summarizes the flow of data collection, processing and analyses used by the group to conduct their studies.

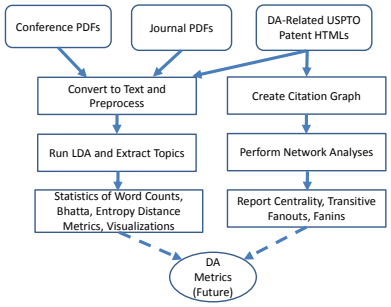

Fig. 2: Data collection and analysis flows.

Three basic types of documents are analyzed by the working group. **(i) DA-related papers.** The group analyzed papers from DA conferences and journals, chiefly those sponsored by the IEEE CEDA and ACM SIGDA professional societies. PDF files, OCR'd as needed, are converted to text; a total of 47000+ conference and journal papers is in this corpus. **(ii) DA-related patents.** DA-related U.S. patents are obtained as full-text HTML from the www.uspto.gov website, using three levels of "forward" search in the directed graph of patent citations starting from a level-0 core of approximately 4000 DA-related patents; this is followed by one level of "backward" search from the patents at levels 0 and 1. A total of 759000+ patents is in this corpus. **(iii) NSF project abstracts and SRC research needs.** Abstracts of 1190 NSF projects from 1984 to 2015 were identified by search under "CISE/CCF" with either of two well-known program managers for DA research. A set of 36 SRC Research Needs documents spanning 2000-2013, in the long-standing areas of circuit design, integrated system design, logic and physical design, verification and test, were obtained from SRC [28].

A basic framework for analysis is provided by **LDA analysis of papers and patents.** The group has performed latent Dirichlet analysis (LDA) on preprocessed text files, comparing K (K a user-specified parameter) topic vectors from two corpora to understand similarities and evolutions of topic models across different years or sources. For example, given two corpora of words, LDA analysis is used to obtain topic vectors for each corpus. Then, dissimilarity of the two sets of topic vectors can be assessed with either the Bhatta [16] or the entropy [27] distance metric.

B. Example Analyses

LDA Topic Models. An example topic model analysis result is given in Figure 3, which shows the first ten words (i.e., words with the highest weight in the given vector's distribution) in each of the

top-10 topic vectors returned by LDA for the 1983 and 2014 ICCAD conferences.

1983 ICCAD	2014 ICCAD
Topic 1: partit graph array termin densiti channel gate modul heurist optim	Topic 1: power voltag current resist block standard pin wire reduc layer
Topic 2: instruct memori control execut microcod microcomput address bus decod sequenc	Topic 2: model propos process perform estim probabl techniqu appli order optim
Topic 3: fault detect concurr faulti storag gate evalu express subcircuit effect	Topic 3: variabl boolean encod gate assign fault synthesi execut domain formula
Topic 4: block analog abstract build variabl resourc declar behavior methodolog queri	Topic 4: power energi electr batteri price consumpt channel charg control action
Topic 5: speech weinberg sensor optic vista opusi fabric planner pitch inhibit	Topic 5: memori write energi context pipelin overhead checkpoint thread architectur segment
Topic 6: devic model process paramet voltag statist current extract calcul defect	Topic 6: error approxim vertic adder pariti array detect tsafe network protect
Topic 7: implement model perform process techniqu order control requir block reduc	Topic 7: clock delay asynchron network frequenc optim topolog common synchron capacit
Topic 8: layout connect symbol specif technolog compon languag gate automat physic	Topic 8: devic interfac temperatur emiss oscil inductor reson coupl tsv phase
Topic 9: color testabl token complet construct incomplet approxim assign pin measur	Topic 9: placement pattern layout boundari optim block graph segment space instanc
Topic 10: connect wire compact optim grid symbol plane segment split block	Topic 10: detect secur power attack hardwar sensor devic random physic entropi

Fig. 3: 10-topic LDA models (top 10 words shown) of ICCAD 1983 and 2014.

Alignment (Lead-Lag) Analyses. Figure 4 shows an example *alignment* analysis between the NSF project abstract and DAC conference text corpora. Parts (a) and (b) of the figure respectively show normalized Bhatta distances of DAC conference papers within three-year windows surrounding the 2001-2002 and 2011-2012 NSF project abstracts. Decreasing distance after project initiation is expected if the NSF projects are a precursor of DAC's publication trajectory. This correlation (with a three-year lag) is particularly apparent in the years following 2011-2012.

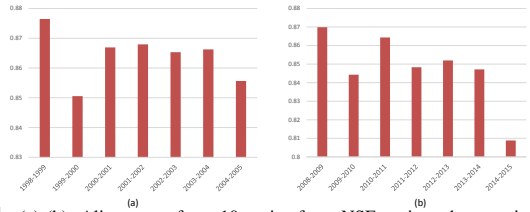

Fig. 4: (a)-(b): Alignment of top-10 topics from NSF project abstracts in the two-year intervals 2001-2002 and 2011-2012, respectively, with displacements of up to three years in the DAC conference paper corpus. Bhatta distance is used, with smaller distance suggesting stronger correlation or alignment.

C. Commentary on DA Metrics Working Group Outputs

The DA Metrics group's studies suggest that intervals of rapid evolution as well as periods of stagnation can be identified in the research literature. Moreover, lead/lag relationships among various types of research outcomes (e.g., papers and commercial tools) have chicken-egg or other complex dynamics. A key initial conclusion from their studies is that papers and patents by themselves are not "impact". Moreover, their initial report does not yet define any metrics of DA research impact. Making the connection from DA research funding to DA research outputs (which include software, benchmarks, student training, books, courseware, etc. – none of which have yet been studied by the working group) to "ultimate measures" of DA research impact (design productivity, M&A valuations, and commercial tool deployment) remain a crucial open task for this effort. Toward this end, near-term efforts proposed by the group include (i) analyses of additional citation graphs (papers, papers+patents, etc.), (ii) assessment of assumed indicators of impact (e.g., "best paper" vs. "test of time"), (iii) development of statistical and machine-learning models for real- world impacts of both individuals, individual research results and the value of graduate training, and (iv) development of predictors of future high-impact DA research on other fields.

IV. Visions for the DA Field

The Vision working group report [25] evaluates the status of design automation from several points of view and outlines strategic objectives and technical challenges and opportunities. The group's strategic goal is to propose systematized changes that aim not just to revive DA research but also to profoundly change its focus, scope, and internal organization. Technical opportunities and challenges are traced along three directions. (i) The first direction is the consideration of, and retargeting to, new technological advances. (ii) The second direction is related to emerging applications. (iii) The third direction is for the DA field to enrich itself by leveraging machine learning and statistical techniques along with modern optimization algorithms, and by exploring improved ways to organize DA flows for given specific application and technology contexts.

A. Technical Opportunities and Challenges

Opportunities and Challenges Driven by New Implementation Technologies. A number of highly influential papers in leading DA conferences and journals are dedicated to synthesis techniques that target emerging or pending technologies. There is a close relationship between new technologies and new architectures, in particular, microarchitectures. Historically, the emergence of FPGA, several new types of nonvolatile storage elements such as flash memory, and in particular the impact of process variation and device aging has attracted a great deal of attention. The current new technology frontier for synthesis of next generations of integrated circuits and systems includes finFET, a wide variety of nanotechnologies, optical nanophotonics, topological insulators [30], superconductors, and a variety of smart materials.

The working group notes that it is both important and often unavoidable that DA introduces and addresses new technologies. Yet, it is also crucial to realize that there is a relatively low chance for any new technology to find industrial application, and that false starts are historically much more common than actual new economically-viable technologies.

New Application Domains. The working group observes that important problems that can benefit from EDA are no longer found on the surface of a silicon chip, but rather come from fundamental long-term problems for society as a whole. Important global problems are cited by the group for potential direct impact by DA researchers, from a variety of sources. These include:

- Ensure that everyone has access to safe and clean water
- Ensure that everyone has nutritious, sustainable food
- Prevent the rise of resistance to antibiotics
- Advance health informatics and engineer better medicines
- Restore movement to people with paralysis
- Provide energy from fusion and make solar energy affordable
- Develop wireless transmission of electricity
- Restore and improve urban infrastructure
- Enable air travel without environmental damage
- Develop carbon sequestration methods and manage the nitrogen cycle
- Reverse-engineer the brain and provide brain-computer interfaces
- Enhance virtual reality and personalized learning
- Engineer the tools for scientific discovery

The challenge for the EDA community is to make a serious, long-term, financial and intellectual commitment to solving one, some, or all of these problems.

Conceptual DA Advances. DA has its roots in tools that have supported IC designers by allowing them to focus on creative and conceptual problems, and by automating computationally complex and tedious tasks. However, the Vision working group observes that DA has not developed sufficiently as a scientific and engineering field unto itself. There remains huge potential for many constructive actions in this direction. For example, uncertainty is intrinsic in both modern DA applications as well as in implementation. Therefore, there is a strong and natural need for integration of statistics and machine learning into DA flows. We also require systems that allow rapid customization. Further, a new generation of iterative improvement optimization algorithms are essentially mandatory to address ever larger designs. Finally, the working group argues for

(i) generalization of existing synthesis and optimization techniques, and (ii) logical as well as statistical understanding of which types of objective functions, constraints and instances are best solved using which particular classes of algorithms.

B. Commentary on DA Vision Working Group Outputs

The Vision working group believes that DA is at a "singularity" point where it has a chance to redefine its scope, greatly enrich its algorithmic and modeling arsenal, and enable evolution of new tools and methods that are required for synthesis and analysis of electronic devices and systems. DA has the potential to address many strategically and economically important problems well beyond its current scope. At the same time, several limitations in the current DA research and industry are observed. According to their report [25], major constraints are set by the (relatively) small size of the industry; by the maturity of the technology; by the low level of research funding in the United States compared with some other countries and in comparison with other electrical engineering and computer science fields; and by the structure of the DA conferences and journals which fragments the citations and visibility of published papers in this field.

Members of the Vision group are currently working to address some of the major challenges in this field, while suggesting conceptual DA advances such as generalizing the DA methodologies by disentangling them from electronics, adding uncertainty and stochastic models in the current abstractions, considering security and privacy, and evolving new incremental synthesis techniques. The team is also working to facilitate an educational reform by suggesting reorganization, recompilation, enrichment, and transformation of traditional CAD course material to be more conceptual, appealing and general. The Vision report emphasizes that funding is a major enabler for research and development in DA. Certainly, more funding opportunities may be available from expanding the scope of DA to address society's fundamental problems. Yet, without proper and timely investment in reformations and retargeting of the field to address contemporary and oncoming problems, the many opportunities awaiting the field of DA may be missed. To this subject, we next provide a review of SRC's 2001-2003 "Research Gap" analyses, which quantified the research investments needed for DA research to address known technology roadmap challenges of that era.

V. More Context: "Research Gap" Analyses

From 1994, coincident with the first Semiconductor Industry Association *National Technology Roadmap for Semiconductors*, the SRC has periodically conducted studies to determine the magnitude of the U.S. and worldwide "Research Gap" – the difference between the research funding needed to deliver the semiconductor industry's identified technology requirements, and the funding actually being expended for that purpose.[1] In the 2001 and 2003 SRC analyses, "research needs" were derived directly – literally, per each row in the tables of technology requirements – from the ITRS roadmap. A key finding of the Research Gap studies was the existence of *massive* funding gaps. For example, the effective research gap to support the semiconductor industry in 2003 was ∼$1600M for the U.S. alone, and was still on the order of $800M when funding across three geographic regions (U.S., Asia, Europe) was considered. Here, we review the Research Gap methodology from the 2001 and 2003 analyses. The key takeaways are that (i) research needs have in the past been directly derived from the semiconductor industry's roadmap for its supplier industries (of which EDA is one), and (ii) even nearly 15 years ago, it was recognized that *billions* of dollars – not tens of millions – were needed to solve critical technical challenges.

Tables II and III respectively summarize circuit design needs and system architecture needs from the 2003 study by Integrated Circuit and Systems Sciences. Table IV details the Computer-Aided Design and Test Sciences needs according to the 2003 study. Rows in green color denote tasks that are new in 2003 relative to 2001; rows in yellow color denote tasks that can be mapped to tasks in 2001 but with a changed number of "quanta"; and the rows with no color fill indicate that the task scope remained the same between 2001 and 2003. Comparing the two studies performed in 2001 and 2003 shows that the extent of the major challenges in the 2001 ITRS have not been noticeably reduced in 2003, and that after a more comprehensive (In other SRC science areas, stalled research progress in aspects of front-end processes/devices and patterning between 2001 and 2003 are seen to have caused slippage in the 2003 ITRS itself, relative to the 2001 ITRS.)

TABLE II: Circuit Design (2003).

Year 2003		
Task #	Task Description	Quanta
1	Circuits that comprehend, manage and possibly leverage the effects of large sub-threshold source-drain leakage currents and large gate leakage currents	2
2	Exploit RF potential for aggressively scaled digital CMOS	2
3	Low-cost circuit and process techniques for improving soft-error immunity in sub-100 nm Leff technology generation	2
4	Novel device structures that permit complex circuit operations at the device level	3
5	Circuits that handle the increasing statistical variability of smaller numbers of dopant atoms and patterning at the diffraction limits of light	4
6	Innovative methods of reshaping state-of-the-art front-end analog processing for improving the robustness of subsequent digital processing	3
7	Circuit techniques that comprehend upgradability and reconfigurability	4
8	Novel signaling for low cost, low power, high bandwidth chip-to-chip communication	2
9	CMOS RF (1-10GHz) building blocks	1
10	Methods to include the package and PCB in the intrinsic design (5-20GHz)	2
11	Advanced power distribution and noise abatement techniques	2
12	Alternatives to aggressive voltage scaling to minimize power (e.g., noise-tolerant, ultra-low-swing logic schemes, adiabatic circuit styles, and on-chip magnetics)	2
13	Electrostatic Discharge (ESD) protection, device modeling and design	1
14	Circuit research that is closely coupled to architectural innovations for developing low power scalable digital systems	1.5
15	Circuits on non-silicon based technologies	2
16	Analog/mixed signal/RF built-in self test	2
17	High performance, low power data converters	2
	Total Research Needs	37.5

TABLE III: System Architecture (2003).

Year 2003		
Task #	Task Description	Quanta
1	Application analysis for architectural requirements	3.6
2	Application mapping for nuclear spin state and/or Tunneling Phase Logic (TPL) devices	2.4
3	Efficient space-time processing communication algorithms and radio architectures	1.2
4	Energy efficient communications with MIMO	0.6
5	Energy efficient computing in leakage dominated regimes	0.9
6	On-chip multiprocessing architectures	2.4
7	Memory-based computing architectures; support for molecular computing	3
8	Defect tolerant architectures; support for CNT, nano-wires; dependability, availability and fault tolerance to unreliable devices	6
9	Architectural support for 3D integration	1.2
10	Biologically inspired computing architectures	1.2
11	Architectural advances to incorporate intelligence in silicon systems	3.6
12	Semantic preservation and architectural interface in compilation tools	1.2
13	Novel OS/RT architectures that enable incremental composition	4.5
14	Validation in compilation (proof-carrying compilation and assume guarantee frameworks)	1.2
15	Novel OS services for energy, precision/fidelity, and distribution	1.5
16	Application specific OS services	1.5
17	Heterogeneity: hybrid systems model and analysis	1.2
18	Quality of service models and optimizations	1.2
19	Correctness guarantees: composability, compositionality in SIP	2.4
20	Miniaturization of novel sensing techniques	3.6
21	Miniaturization of biological/chemical processing	3.6
22	Microfluidic processing integration (simulation, verification)	3
23	Bio/chemical processing in microelectronic systems: handling of biological samples and processing	1.2
	Total Research Needs	52.2

The "research needs" in the tables are estimated by bottom-up analysis of individual tasks in the roadmap. Essentially, the numbers of "quanta" indicate relative degree of difficulty and effort needed for different tasks within the ITRS. Each quantum can ultimately be mapped to an *annual* research funding cost, e.g., (i) progress requires at least one faculty (partial effort throughout the year) to work with at least two graduate students (full effort throughout the year); (ii) redundancy is needed (out of five projects launched, the expectation is that one will succeed); and (iii) due to imperfect communication as well as competition across geographic regions, three regional efforts to solve a given problem may be simultaneously ongoing. The analyses in 2001 and 2003

[1] One of us (ABK) worked with Chuck Nuese, Bill Joyner, David Yeh, Dale Edwards and Justin Harlow during the 2001-2004 timeframe to develop these gap analyses for the DA-related science areas. We are grateful for the opportunity to describe the "Research Gap" analysis here.

TABLE IV: Computer-Aided Design and Test Sciences (2003).

Year 2003		
Task #	Task Description	Quanta
1	Electronic system-level design methodology	2
2	Language-level modeling advances and composition interfaces	3
3	Architectural and microarchitectural design exploration	3
4	Design methods for embedded software	6
5	CAD infrastructure for rapid prototyping and evaluation of design tools (like MOSIS)	1
6	Interoperability standards for design technology	3
7	Collaborative, geographically distributed design methodologies	2
8	Assess/solve quality and yield impact due to test equipment limits (e.g., utility of at-speed test)	1.5
9	Fault modeling for defects/noise in nanometer technologies	2
10	Diagnosis and failure analysis for analog/mixed-signal parts	3
11	Self-test solutions and test methods for (heterogeneous) core-based SOC (including RF, analog, MEMs, etc.)	4
12	Intelligent testbench	1.5
13	Energy/power management at system, architecture, and microarchitecure levels	5
14	Power reduction/management at logic/physical/timing level	5
15	Power management addressing circuit-level issues and manufacturing variability	5
16	Unification of design-mask and design-silicon flows (RET, mask data prep/write/inspect, prep for future advanced patterning solutions)	4
17	Design under high manufacturing variability and parameter uncertainty	5
18	Cost-driven design that is aware of manufacturability/yield	4
19	Core-based design verification	2
20	Verification of heterogeneous systems	4
21	Verification for novel devices and high-frequency novel interconnects	2
22	Equivalence checking between design levels	2
23	Convergent, predictable physical implementation methodologies (e.g., one-pass design with incremental/partial specification)	5
24	Design with partial or probabilistic information	3
25	Core optimization algorithms and techniques	3
26	Reliability with permanent faults (reconfigurability, graceful degradation)	4
27	Design techniques to address SEU (soft errors)	1
28	Design with novel (future) devices	4
29	Analysis/optimization for system-in-package and 3D integration	3
30	Global (multi-disciplinary) solution of ITRS red bricks (Design-LITHO, Design-PIDS, Design-A&P, etc.)	2
31	Modeling and simulation tools for new devices	2.5
	Total Research Needs	99.5

further assumed that each person-year of effort costs \$200K, after various deratings (overhead expenses applied to research grants, averaging of salary scales across geographic regions, etc.). Then, each "quantum" in the tables corresponds to 20 person-years, or \$4M. For example, required annual research investment in the "electronic system-level design methodology" CADTS need was 2 quanta = 40 man-years = \$8000K in the 2003 Research Gap analysis.

Table V summarizes the total of research needs estimated by the SRC across all of its science areas in 2001 and 2003. The increase in front-end processing arises due to difficulties related to new gate and interconnect-level dielectric materials. Estimated support for patterning research was viewed as conservative even 14 years ago, in light of the already apparent difficulties associated with beyond-ArF lithography. Viewed retrospectively from today's delayed EUV deployment, this under-investment concern was correct. Overall, 123 of the 152 tasks in 2003 continue from tasks already in place in 2001. 29 tasks are new in the 2003 analysis, of which 13 are packaging-related tasks that were overlooked in 2001.[2]

In that "gap" is equal to "needs" minus "investments", we now mention the top-down methodology used to estimate "investments". Compiled annual totals of semiconductor industry sales (as well as sales for the equipment, material and EDA suppliers that support the industry) were derated by analyzing the fraction of total R&D budgets earmarked for long-term ITRS-type research. This fraction in turn was estimated by examining the amount spent by U.S. companies on SRC and MARCO Focus Center fees. The 2001 and 2003 analyses determined that U.S. companies typically spend between 1.0 and 1.5% of their R&D budgets on such activities. Therefore, a total of 2.0% of sales was used in the analysis to include research support to universities by individual semiconductor companies (beyond what is provided by SRC and MARCO fees). Government funding in support of the ITRS was estimated by examining the individual programs of the major federal agencies within the U.S. and the major research consortia abroad (that are supported in part by the government). Such numbers are typically quite large (e.g., governmental investments in "nanotechnology" alone at the time spanned China, Japan, South Korea, the EU (EC 6th Framework) and the U.S. (National Nanotechnology Initiative), and added up to approximately \$4.2B per year). However, huge redundancies and lack of direct application to ITRS needs resulted in an estimate of only 5% to 10% of such funding being related to the ITRS over the following 7-15 years.

Finally, after taking "needs" minus "investments", the Research Gap itself is still a function of the assumed level of access to research products that exists between world regions. For example, in the 2001 analysis, if all regions' research investments were applied with zero redundancy or waste, and 100% access, then the effective worldwide funding toward the ITRS needs was estimated to be close to \$1000M, resulting in a research gap of approximately \$400M ($\approx \$1406 - \$1000$). However, the combined impact of redundant effort and lack of access to research products limits the value of foreign research substantially. Specifically, the 2001 study separated all funding geographically, and assumed that foreign research funding was 30% redundant (i.e., 30% was duplicative of U.S. efforts), with accessibility to U.S. semiconductor companies being 70% for Europe and 40% for Asia. These assumptions reduced to \$672M the effective worldwide research funding accessible to the U.S., and hence increased the research gap for the U.S. semiconductor community to \$733M. For Japan and Europe, the analysis assumed accessibility factors of 70% for U.S. or European research to Asia, and 80% and 50% for U.S. and Asian research to Europe; this implied research gaps of \$800M and \$784M for Europe and Japan, respectively. Hence, for every geographic region, the 2001 Research Gap analysis pointed to a roughly \$800M investment gap, or roughly half of the amount needed.

TABLE V: Estimated Worldwide Annual Research Investment to Support 2008-2014 ITRS Needs.

Science Area	Number of Tasks		Needs (\$M)	
	2001	2003	2001	2003
Front-End Processing	22	19	150	513
Proc Integr, Dev & Struct	15	14	280	410
Patterning	25	22	245	338
Interconnects	13	13	153	244
Design CAD	26	31	280	398
Circuit Des & Sys Arch	20	40	168	359
ES&H	5	5	30	30
Assembly & Packaging	–	13	–	224
Factory Integration	5	5	100	155
Total	131	152	**1406**	**2671**

To address the "Research Gap", recommendations made in 2001 included: (i) the U.S. semiconductor industry should consider increasing the amount of long-term horizon ITRS research in light of the "red brick walls" that had surfaced in several areas of the roadmap; (ii) the SRC and MARCO programs should explore options to attract foreign semiconductor companies as full members, thus expanding the value of these consortia to member companies without impact to the fee structure; (iii) SRC and MARCO should also explore approaches to collaborate with foreign consortia; and (iv) the SRC should coordinate better with the U.S. Government's semiconductor-related funding programs, and pursue improved assimilation of relevant results from other Government-funded programs. Again with the benefit of 20-20 hindsight, many of these recommendations, along with the basic conclusions of the Research Gap analyses, seem to have been well-taken at the time that they were developed. We hope that lessons regarding "critical mass" of research investment can be applied when initiating research in the future growth and evolution of the DA field.

VI. The 2015 DA Perspective Challenge

The first Design Automation (DA) Perspective Challenge, held at DAC-2015, sought long-term research problems in emerging

[2]In 2001, assembly and packaging research was not included in the back-end/factory estimate.

domains that could benefit from, and further evolve, the EDA practices and methodologies that have been developed over the past decades. Submitters of these "perspectives" were asked to describe challenges inherent in the suggested long-term problems, as well as the potential scientific or industrial impacts of solutions. Specifically, submissions required a brief document that addressed the following questions:

- What is the long-term problem?
- Why is the problem important and challenging?
- What is the state-of-the-art?
- What is the problem's relevance to existing DA tools and methods? Or, how could DA help in addressing the challenge(s)?
- What knowledge, skills, and/or tools are needed to address the challenge(s)?
- Is the problem interdisciplinary, i.e., requiring expertise in DA and in another domain?
- What are the broader impacts?

Initial screening of the 30 submissions resulted in a shortlist of 13, whose topics may be grouped as shown in Table VI. The 13 submitters were invited to give short, three-minute pitches to a panel of six judges (four from industry, two from academia). First prize went to T. Huang and K.-T. Cheng from UC Santa Barbara, on the topic of design automation for flexible electronics. Second prize went to Y. Chen and H. Li from Penn State University, on the topic of DA for neuromorphic computing. Third prize went to N. Chang from KAIST, on the topic of energy optimization of EV systems. A team of U. of Calgary researchers (N. K. Darav, L. Behjat, A. Farshidi, A. F. Tabrizi and I. Gates) was the audience favorite with a proposal for automation of energy systems. Two additional proposals received honorable mention recognition: DA for networks of autonomous vehicles (R. Topaloglu from IBM Research) and trusted hardware automation (V. Costan, I. Lebedev and S. Devadas from MIT).

TABLE VI: Relative interest of selected proposals. Summary of proposals (e.g., P1, P2, etc) are in Appendix.

Category	Proposals
New application	P3, P5, P7, P9, P10
Social engineering	P1, P2, P11, P12
New computing models	P8, P13
More DA	P4, P6

DA Perspective Challenge submissions with long-term prospects will be maintained in a DA Challenge Archive at the IEEE CEDA web-portal. Several judges and winners of the DA Perspective Challenge at DAC-2015 will participate in a panel at ICCAD-2015 to discuss the outcomes and their vision going forward.

VII. Looking Forward

For more than a half century, the design automation field has focused on and enabled the growth of the semiconductor industry. With maturation of both the semiconductor and EDA industries, the design automation research community should more vigorously and systematically explore new vistas, particularly those wherein great potential and need for automation have been clearly identified. A new IEEE CEDA technical activity group, born of the over 40 year-old CANDE technical committee, is working to support more efficient and coherent evolution of the field as a whole. Three initial study teams have compiled (i) a catalog of past and current roadmaps and research initiatives; (ii) views of DA literature as a precursor to metrics of DA research impact; and (iii) visions for future applications of EDA in broader DA contexts. Our activities have also included the first DA Perspective Challenge, co-located with DAC-2015, which solicited proposals from the broader DA community for key long-term research problems and applications of DA in emerging domains. We have also described SRC's 2001-2003 "Research Gap" process and conclusions; this was an early quantification of research funding needed to meet the ITRS roadmap's stated technology requirements in the design technology field. The Research Gap analysis is notable for the magnitude of worldwide DA research funding that it viewed as necessary to support the semiconductor industry roadmap. In retrospect, actual funding has been far less. The SRC's analysis also pointed to increased partnership with foreign countries and consortia; this has been realized over the past decade. We are hopeful that our new IEEE CEDA technical activity group and its initiatives will help stimulate successful evolutions of the EDA field beyond its traditional "E-roots".

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APPENDIX

P1: *Design Automation without Borders: From EDA Tools to DA Toolboxes* (Z. Zhang) suggests to decouple models and algorithms from their IC-specific applications, and then design and distribute DA techniques as toolboxes that can be efficiently leveraged by domain experts without deep DA knowledge. This recalls, e.g., the "CAD-IP reuse" goals and contents of the MARCO GSRC Bookshelf for Fundamental CAD Algorithms [4].

P2: *Thinking Outside the Silicon Box* (S. Levitan) notes that fundamental long-term problems for society as a whole can benefit from EDA. City traffic control, carbon sequestration and water purification are three example grand challenges. This proposal suggests that the DA community must pick a subset of grand engineering challenges and commit to working together to apply expertise developed for EDA toward solutions.

P3: *Design Automation and Test Challenge for Flexible Hybrid Electronics* (T. Huang and K. Cheng) calls out flexible hybrid electronics (FHE) technology – low-power VLSI chips and printed electronics on flexible substrates – for wearable devices and the Internet of Things (IoT). This proposal discusses key design automation problems, challenges and potential solutions for FHE.

P4: *Simulation and Design Challenges of Integrated Silicon Photonics for High-Speed Optical Data Communication* (M. A. Seyedi, J. Chen, M. Fiorentino and R. Beausoleil) discusses process design kit (PDK) development to help streamline Silicon Photonic (SiP) component integration into future IC designs to meet projected future bandwidth needs.

P5: *Design Automation of Things The Future of EDA: Electric Vehicle Power and Energy Optimization* (N. Chang) explores the potential application of minimizing energy consumption of electric vehicles for deadline-constrained driving missions.

P6: *Integrated System-Package-Chip CoDesign Environment* (R. Radojcic, P. Gupta and A. Keval) proposes a design environment to enable system-package-chip codesign. The proposed system is targeted at the "pathfinding" phase of design, enabling rapid prototyping and assessment of the tradeoffs inherent in system-level global optimization of multi-die architecture, technology selection, and integration.

P7: *Design Automation for Networks of Autonomous Vehicles: A Visionary Perspective* (R. O. Topaloglu) notes that the area of DA for Networks of Autonomous Vehicles (NAV) has a tremendous potential. The proposal suggests that extending design automation to such an application can lead to a new industrial revolution, beyond improving the human quality of life.

P8: *Embrace the BRAIN Century: EDA Challenges in Neuromorphic Computing* (Y. Chen and H. Li) notes that despite many significant advances in understanding the brain function, a lack of consensus and agreed frameworks persists in almost every facet of research, including abstraction level, implementation, and realization details. The proposal frames three important challenges and open questions in neuromorphic computing (NC) research from the EDA perspective.

P9: *Design Automation in Energy Systems* (N. K. Darav, L. Behjat, A. Farshidi, A. F. Tabrizi and I. Gates) suggests that the energy industry can greatly benefit from EDA tools which have had success in dealing with complex problems using computational techniques.

P10: *Finding structure from chaos: automation of clinical genomics pipeline* (F. Liu) notes that clinical genomics presents emerging big data problems where billions of sequencing reads are meticulously reconstructed and genetic variations are determined. The proposal suggests that EDA paradigms can be applied to improve solver performance for various big data problems such as clinical genomics.

P11: *Bourbaki Design Automation* (M. Potkonjak) suggests a conceptual refocusing for the DA via axiomatization and abstraction. For instance, synthesis and analysis techniques that are universal across all subdomains can be invoked for creation; modeling and design automation optimization techniques that are not overtuned to particular contexts or benchmarks are also needed.

P12: *Leveraging EDA Research for Design of Things* (G.-J. Nam) calls out smart grid network analysis and optimization as a potential area to which CAD techniques can be easily ported and find immediate application.

P13: *A Call for Trustworthy Trusted Hardware* (V. Costan, I. Lebedev, and S. Devadas) notes that consideration of security aspects of computer systems is a must. The proposal suggests that only an open hardware platform with strong guarantees of software isolation would enable compelling security protocols.