A 196µW, Reconfigurable Light-to-Digital Converter with 119dB Dynamic Range, for Wearable PPG/NIRS Sensors

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Abstract

This paper presents a low power, reconfigurable, high dynamic range (DR), light-to-digital converter (LDC) for wearable PPG/NIRS recording. The LDC converts light into the time domain with a dual-slope mode integrator, followed by a counter-based time-to-digital converter. This architecture merges the functionalities of a conventional transimpedance amplifier and ADC, while quantization in time domain significantly improves the DR. The inherent low pulse repetition frequency (PRF) of LDC also reduces the LED power. Furthermore, the DR of the LDC can be easily reconfigured by re-programming the counting step size or the PRF of the LEDs, allowing optimal power consumption for different DR scenarios. The IC achieves a maximum DR of 119dB while only consuming 196µW (including 2X LEDs). The IC is validated with PPG and NIRS tests, using photodiodes (PDs) and silicon photomultipliers (SiPMs) respectively.

Keywords — PPG, NIRS, LDC, reconfigurable, DR.

Introduction

Measuring the volume and oxygenation changes in blood with light can provide timely health information with improved user comfort. Photoplethysmography (PPG) and Near Infrared Spectroscopy (NIRS) are well-established techniques enabling measurement of heart rate variability (HRV), blood oxygen saturation (SpO_2) and brain monitoring. One of the key challenges of optical sensor readouts is a high dynamic range (DR), which is due to the small AC/DC perfusion index, the background ambient light and large motion artifact [1][2]. For light-sensitive detectors like Silicon Photomultipliers (SiPMs), their output current can be 100X large than photodiodes (PDs). Optical readouts with limited DR will suffer from severe signal distortion and saturation. Therefore, a high DR (>100dB) readout circuitry is usually needed for wearable PPG/NIRS recording [1]. Furthermore, the required DR depends on the measurement location, skin tone and contact pressure [2]. A reconfigurable optical readout with user-defined DR and power consumption provides flexibility for various scenarios.

Existing PPG readouts [3] can achieve more than 100dB DR, but require high power (5.87mW), because the readout contains a high-resolution ADC with a high oversampling ratio (OSR) and hence a high pulse repetition frequency (PRF) of the LEDs. On the other hand, the low power solution in [4] consumes 0.39mW by reducing the PRF, which results in increased noise and reduced DR of 95dB. Besides, these readouts are not sufficient for NIRS recording. This paper presents a time-based light-to-digital converter (LDC) for large DR, low power and reconfigurability. The LDC uses a dual-slope mode integrator to realize the functionalities of signal amplification, anti-aliasing filter, sample & hold, and part of the quantization, achieving an effective 119dB DR with 196µW including 2X LEDs.

Proposed LDC topology

Fig.1 (a) shows a conventional optical readout circuit including a transimpedance amplifier (or integrator) and a high-resolution ADC. These often require a high PRF to support the oversampling [3], increasing the average current of LEDs. The core idea of the LDC is a dual-slope ADC, which provides a high resolution with a low OSR by leveraging a longer conversion time. This still suits PPG/NIRS applications well because of the small bandwidth of interest (<20Hz) [3], while at the same time reducing LED power.

Fig. 1 (b) shows the detailed architecture of the LDC. The input stage consists of a periodically reset integrator and a reference current source (I_{ref}), which generate the dual-slope output voltage. It is followed by a dynamic comparator and a counter, converting integrator output directly into a digital code. To support the dual-wavelength recording for SpO_2 estimation, the readout channel is time-interleaved between 2 LEDs. The proposed LDC results in a simpler and compact architecture by integrating amplification, filtering and sample & hold into a single active block reducing noise and power contributors.

Fig. 2 shows the timing diagram of the LDC. Each sampling period starts with the integrator reset. In the integration phase, the LDC integrates the ambient light signal onto C_f during t_1 by closing the switch I_{IN_SW}. Then the LED is activated (pulsed), and both signal current and ambient light current are integrated on the capacitor C_f. Keeping the LED pulse width exactly the same as t_1, the polarity of C_f is swapped just before the LED pulse. This effectively cancels the ambient light in each sampling period [3]. The transimpedance gain of the integrator depends on the integration time and the value of C_f. After the LED pulse, the integrated signal is automatically sampled on C_f. Furthermore, the integration also inherently acts as a low-pass, sinc anti-aliasing filter. In the conversion phase, I_{IN_SW} is disabled and I_{REF_SW} is enabled. Then, the voltage stored on the C_f is converted to a digital code by counting the number of time intervals (determined by the comparator clock) to discharge C_f to initial reference V_{REF} by I_{ref}. To remove the large baseline component from the PPG/NIRS signal before integration, two 7-bit current DACs synchronized with the LED pulses provide compensation current, further increasing the effective DR. The LED driver can provide up to 100mA peak current for two LEDs.

The DR of the LDC can be easily reconfigured digitally by changing the comparator clock frequency and PRF. The clock frequency of dynamic comparator determines the quantization step size and hence higher resolution can be achieved at the expense of higher comparator dynamic power and vice versa. Moreover, the OSR can be increased by using a higher PRF at the expense of the LED power. Therefore, the LDC power (including LEDs) can be optimized for different DR requirements.

Measurement results and conclusion

Fig. 4(a)(b) show the power spectrum of the LDC AC signal path with a (up to 1µA) sinusoid input current (baseline I-DACs disabled). The PRF of 512Hz and a 12-bit counter are used here. An SFDR of 90.6dB and an SNDR of 79.2dB are

achieved after filtering to the bandwidth of the interest (<20Hz), equivalent to an ENOB of 12.9b for the AC part. Fig. 4(c) shows the effective DR of the complete LDC (AC+DC path) after enabling the I-DACs. Fig. 3(b) shows the trade-off between the achieved DR and the power consumption at different LED PRFs and the associated comparator frequencies. For a fixed PRF, the DR increases monotonically with comparator frequency, before reaching a limit dominant by the front-end integrator noise. A higher DR can be achieved with a higher PRF which provides a higher OSR and reduced noise folding. When baseline compensation is active, a 119 dB effective DR is achieved with 196µW system power, while a effective DR of 95dB is achieved only consuming 87µW.

Fig. 5(a) shows dual wavelength PPG signals recorded on the finger from regular PDs. Heart rates are well recognized. Fig. 5(c) shows the SpO_2 measurement during a breath-holding test. Finally, the LDC is also connected to SiPMs. Fig. 5(b) show a NIRS recording obtained on the forehead. The IC was manufactured in 0.18µm CMOS (Fig. 3(a)). The performance is compared to the state-of-the-art work in Table I. The proposed LDC achieves the highest DR and the lowest system power including LEDs. It also provides the maximum input current range of 200µA that complies to SiPMs, and an ambient cancellation running in the background with maximum 50µA tolerance.

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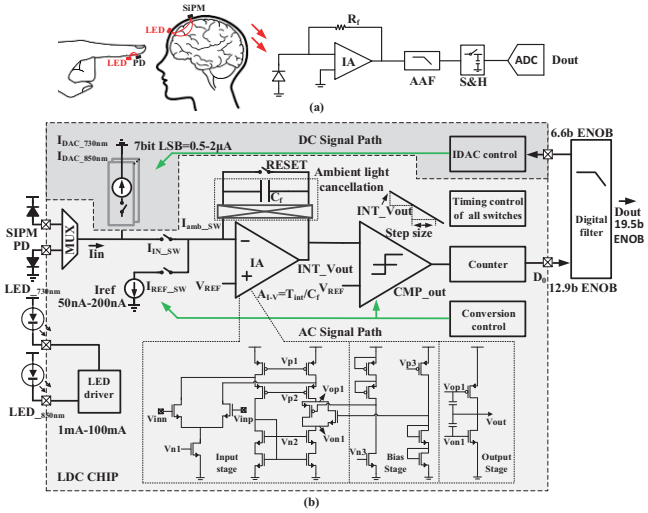

Fig. 1. (a) Conventional PPG/NIRS readout (b) Proposed dual-slope LDC

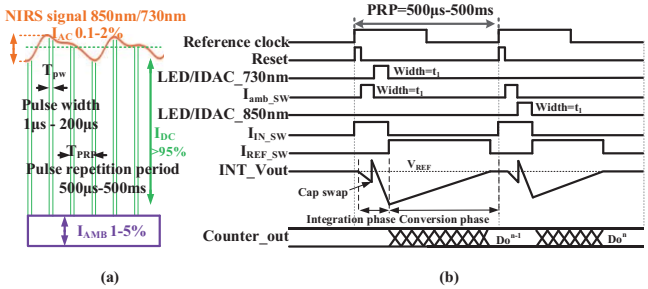

Fig. 2. (a) Typical PPG/NIRS signal (b) The LDC timing diagram

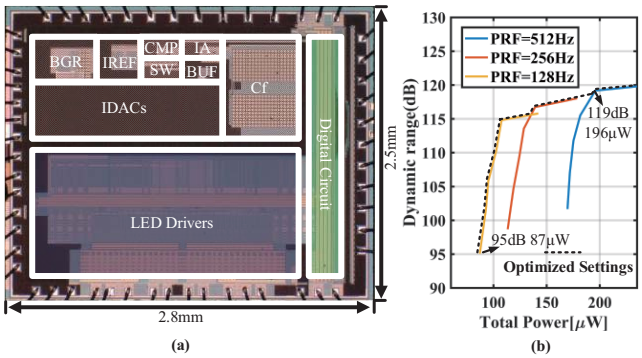

Figure 3 (a) Chip photograph (b) LDC power versus dynamic range, indicating the optimized DR settings

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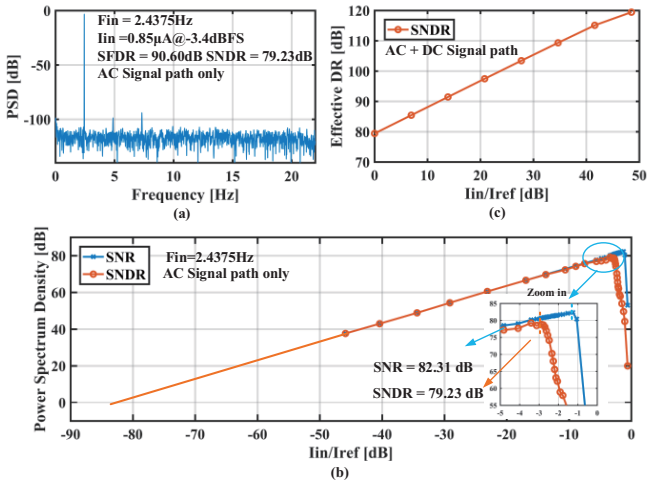

Figure 4 (a) AC signal path PSD vs frequency (b) AC signal path SNDR/SNR vs Iin (c)Effective DR vs Iin with AC&DC path enabled

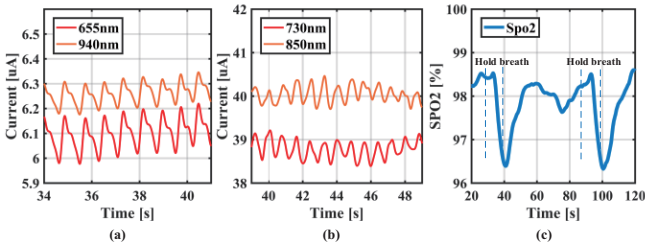

Figure 5(a) PPG recording from PDs on the index finger (b) NIRS recording from SiPMs on the forehead (c) SpO_2 recording when hold the breath

Parameters	JSSC'18[3]	VLSI'16[4]	ISSCC'18[5]	JSSC'18[6]	This Work
Technology	0.13µm	0.13µm	0.18µm	65nm	0.18µm
Supply	1.2/3.3	1.5/2.7	1.2/3.3	1.2/3.3	1.2/3.3
NIRS Detector	PD	PD	PD, SIPM	PD	PD, SIPM
# of LEDS	8	2	2	2	2
Max input	63µA	35µA	200µA	10nA	200µA
Ambient light compensation	10µA	6µA	40µA	--	**50µA**
DC compensation	7.6bit	6bit	7bit	--	7bit
Gain	19k-90M	--	1k-100k	56M-560G	5k-4M
Sample Freq	100-2000 Hz	30-670Hz	2-512 Hz	20-80Hz	**2-2000 Hz**
Max DR	112dB	95dB	87dB	60dB	**95dB** / **119dB**
LED Power	5.5mW	0.32mW*	0.15mW	--	**26µW** / **107µW**
IC Power	370µW	69 µW	132µW	--	**61µW** / **89µW**
Power	5.87mW	0.39mW	0.28mW	25.2mW	**87µW** / **196µW**
Achitecture	TIA+ADC	TIA+ADC	TIA+ADC	TIA+ADC	**LDC**

* One LED power

Table I Benchmark table compared with the state-of-the-art work