A 50μW Fully Differential Interface Amplifier With a Current Steering Class AB Output Stage for PPG and NIRS Recordings

Shuang Song, *Member, IEEE*, Qiuyang Lin, *Graduate Student Member, IEEE*, Chris van Hoof, *Member, IEEE*, and Nick van Helleputte, *Member, IEEE*

***Abstract*—This brief presents a low-power fully differential optical sensor interface amplifier for photoplethysmography (PPG) and near infrared spectroscopy (NIRS) recordings. The proposed amplifier employs a stacked current reuse input stage that provides a DC biasing voltage for the photodiode, reducing the parasitic capacitance. The output stage exploits a fully differential current steering class AB topology with a self-regulated common mode voltage, providing a 70μA input current range with minimized quiescent current. Moreover, the interface amplifier can be reconfigured as either single-ended mode suitable for photo detectors biased at a high voltage or fully differential mode for those biased at a low voltage. This amplifier is implemented in a standard 0.18μm CMOS process and characterized experimentally. Measurement results show that, with a 1.5V supply, the amplifier can provide up to 1V biasing voltage for the photodiode and consumes a static power of around 50μW. It achieves a dynamic range of 97dB in fully differential mode with an input referred noise of 67pArms in 32Hz band and 102dB in single -ended mode with an input referred noise of 582pArms.**

***Index Terms*—Interface amplifier, near infrared spectroscopy (NIRS), photoplethysmography (PPG), low-power.**

I. Introduction

WEARABLE photoplethysmography (PPG) recordings can provide heart rate (HR), blood oxygenation level (SpO_2) and blood pressure together with electrocardiography (ECG) and all of them are useful for detection and prevention of cardiovascular diseases-the leading cause of death globally [1], [2]. Besides, another optical sensing technique, i.e., near infrared spectroscopy (NIRS) that enables functional brain imaging is appearing in wearable devices [3], [4]. Both PPG and NIRS can be obtained by shining a light, usually by a LED and detecting the transmitted or reflected light by a photodetector together with the readout amplifier [5], as shown in Fig. 1.

The power consumption of wearable devices is usually dominating by the radio and the PPG/NIRS recording channels [7], [8], because of the high LED peak current (10 to 100mA) needed for enough signal to noise ratio (SNR). Reflective mode PPG recording can be used instead of transmissive mode, reducing the peak current to less than 10mA. More efficient optical sensing devices, e.g., avalanche photodiodes and silicon photomultipliers (SiPM) can further reduce the peak LED current to sub mA level [9]. Therefore, the interface amplifier that usually consumes 100μA level current can become an important part of the total power consumption and thus needs to be investigated and improved [9], [10], [11], [12].

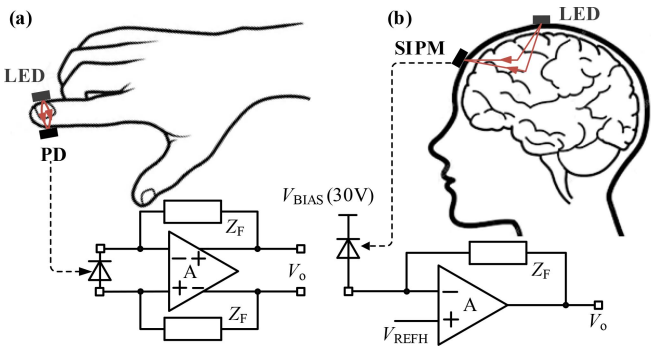

Fig. 1. (a) Transmissive mode detection with fully differential readout and (b) Reflective mode detection with single-ended readout.

Besides low power consumption, a high dynamic range is also of paramount importance to resolve the small PPG/NIRS signal in the presence of a large DC component and possible motion artifact. Comparing to single-ended solutions, fully differential output architecture can provide a higher dynamic range and better compatibility with differential input ADC [8], [13]. Most currently available fully differential readout architectures cannot provide a DC bias voltage to the photodiode [13], [14] as single-ended solutions. This can reduce the performance of the photodiode and increase the parasitic capacitance, which is not desirable because it increases the required pulse width of LED current for longer settling time of the interface amplifier. Therefore, an interface amplifier with low power and high dynamic is required, while providing a DC biasing voltage for the photodiode.

In this brief, a fully differential optical sensor interface amplifier is proposed. The power consumption is minimized by reusing current in the input stage and steering current in the class AB output stage without the need for a common-mode feedback circuit. The interface amplifier can be (re)configured as a differential input mode for photodiode or single-end

Manuscript received April 1, 2020; revised June 1, 2020; accepted June 12, 2020. Date of publication June 16, 2020; date of current version September 3, 2020. This brief was recommended by Associate Editor Y. H. E. Bonizzoni. *(Corresponding author: Qiuyang Lin.)*

Shuang Song and Nick Van Helleputte are with BECHS, imec, 3001 Heverlee, Belgium (e-mail: shuang.song@imec.be; nick.vanhelleputte@imec.be).

Qiuyang Lin and Chris Van Hoof are with BECHS, imec, 3001 Heverlee, Belgium, and also with the Department ESAT-MICAS, KU Leuven, 3000 Leuven, Belgium (e-mail: qiuyang.lin@imec.be; chris.vanhoof@imec.be).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2020.3002952

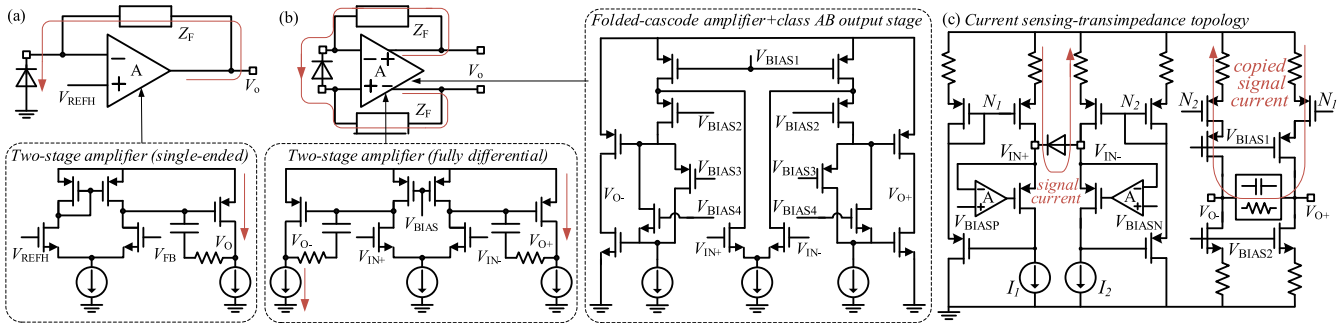

Fig. 2. (a) Single-ended readout topology with miller-compensated two-stage amplifier, (b) fully differential readout topology with miller-compensated two-stage amplifier and folded-cascode/class-AB output stage amplifier, (c) fully differential readout topology with current sensing-transimpedance amplifier.

input mode for SiPM where a high DC biasing voltage is required. Working in transimpedance mode, the dynamic range of the amplifier is maximized by a current DAC. Measurement results shows that an input current range of 70μA is achieved with a power consumption of 48.7μW. In differential mode (gain = 150kΩ), an input noise of 67pArms with a DR of 97dB is achieved and in single-ended mode (gain = 10kΩ), an input noise of 582pArms with a DR of 102dB is achieved.

The rest of this brief is organized as follows. In Section II, existing circuit topologies for optical readout are discussed, In Section III, the proposed fully differential amplifier is described in detail. In Section IV, the operation modalities of the proposed amplifier including the TIA/INT mode, the single-ended/differential input mode are explained. Implementation results are presented in Section V, and conclusions are drawn in Section VI.

II. Optical Readout Amplifier Topologies

Optical sensor interface amplifiers are less intensively studied comparing to amplifiers for biopotential signals, e.g., ECG. Three existing amplifier topologies used for PPG/NIRS readout are discussed [8], [10], [14], [15], where two of them are based on shunt-shunt feedback. Each topology has certain limitations, which motivate this brief.

A. Shunt-Shunt Feedback-Based Amplifier Topology

A transimpedance amplifier is usually implemented with shunt-shunt feedback and both single-ended and differential topologies are reported [10], [12], [14] as shown in Fig. 2 (a) and (b), respectively. As the focus of this brief, the core amplifier is investigated. Miller compensated two-stage amplifiers are commonly used, shown in the dashed box of Fig. 1(a) [10], [12], [15]. Its output stage works in a semi-class AB way, namely, it can source more current (flows to the photodiode shown by arrow) than the quiescent bias, while the sinking ability is limited. But the fully differential version of this topology (dashed box of Fig. 2(b)) loses this feature since the signal current in the two output branches are counter phase, requiring a class A output stage. A well-designed miller compensated fully differential amplifier consumes a current of around 120μA (modified version from [10]) including the common-mode feedback, achieving a closed-loop bandwidth of ∼500kHz and a maximum output current of 50μA.

In order to reduce the current consumption of the readout, a single-stage (folded-cascode) fully differential amplifier with a class AB buffer can be used, shown in the dashed box of Fig. 2(b) [11], [13], [14]. This amplifier is also miller-compensated, which is not shown in the figure for simplicity This topology can provide a large output current at low quiescent bias. A well designed fully differential amplifier with such an output stage consumes a current of around 60μA (modified version from [11]) to achieve the similar performance, i.e., bandwidth and noise. However, both the two-stage and folded-cascode topology cannot provide the photodiode a differential DC biasing voltage for the photodiode and they require a common mode feedback circuitry that increases the current consumption and complicates that design.

B. Current-Sensing Transimpedance Amplifier Topology

A current-sensing transimpedance topology is reported in [8], which senses the signal current in a fully differential manner and provides a DC bias for the photodiode by the two auxiliary amplifiers as shown in Fig. 2(c). The signal current is then copied to the transimpedance stage and converted to an output voltage. The current consumption of this topology is high due to the class-A mode operation of the current-sensing stage, namely, if a 50μA input current range is required, the current in sink I_1 and I_2 needs to be larger than 50μA. In addition, this topology is not compatible with SiPM where a high bias voltage is required, and the DC bias provided by the topology is limited to 0.6V from 1.2V supply.

III. Proposed Topology

A two-stage fully differential interface amplifier is proposed to achieve low power consumption, high current output range and good compatibility with different sensors at the same time. The amplifier with its feedback components is shown in Fig. 3 (a). The photodiode biasing voltage is set by the positive nodes of equitant amplifies, which are implemented by the input stage of the proposed amplifier as shown in Fig. 3 (c).

A. Core Amplifier Description

The input stage of the proposed amplifier exploits a middle-rail current sink/source (MCS, Fig. 3 (b)) proposed by the first author in [16] to reuse the current of the input stage, which occupies around 1/3 of the total current consumption. This MCS enables building two sub-amplifiers by the input stage as shown in Fig. 3 (c). Namely, two fully differential cross-coupled gain boosting stages are used on both sides of the MCS to allow setting the biasing voltage for the PD by V_{REFH} and V_{REFL}. The output stage is controlled by the cross-coupled transistors, sourcing and sinking the signal current in a differential class AB manner.

As the most important feature of this topology, the gain boosting ratios at node N_1 and N_2 (N_3 and N_4) are intentionally designed to be unbalanced to allow the current steering class AB operation of the output stage. Namely, the

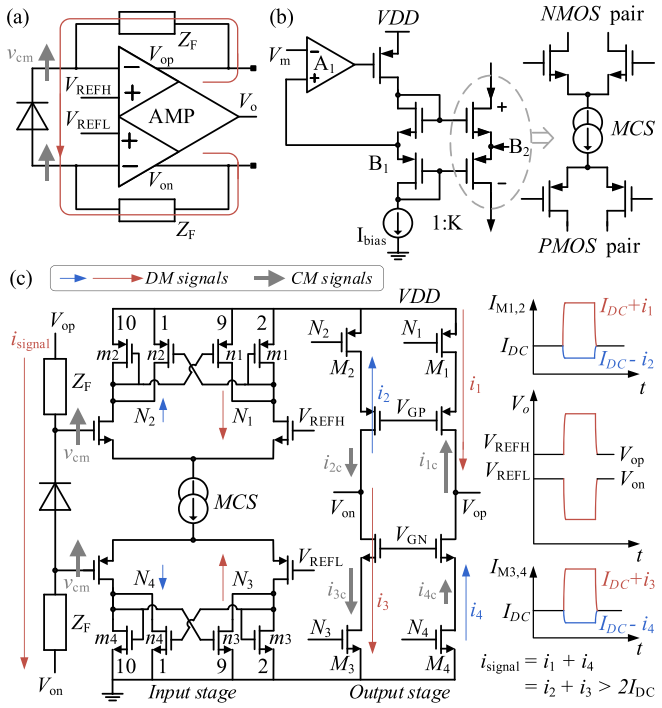

Fig. 3. (a) The proposed amplifier with feedback components (b) the middle-rail current sink/source (MCS) (c) The topology of amplifier core.

gain at $N_1(N_3)$ is designed higher than the one at $N_2(N_4)$ for steering more current along with the signal current direction as shown in Fig. 3(c). This unbalanced gain boosting ratios (both on P side and N side) are determined by the current ratios of branches. Namely, the impedances at N_1 and N_2 can be calculated by Eq. (1) and Eq. (2), respectively, where the transconductance of the four transistors are $m1{\cdot}g_m$, $n1{\cdot}g_m$, $n2{\cdot}g_m$ and $m2{\cdot}g_m$ as shown in Fig. 3(c). The ratio is chosen to be 10: 1: 9: 2, resulting in an impedance of $19/11{\cdot}(1/g_m)$ and $3/11{\cdot}(1/g_m)$ at N_1 and N_2, respectively. These values are determined by a trade-off between the current efficiency, the complexity of the layout, and the local stability of the cross-coupled stages. The same equations can be used for calculating the gain from the bottom side of the *MCS*.

$$Z_1 = \frac{m_2 + n_1}{m_1 m_2 - n_1 n_2} \cdot \frac{1}{g_m} \tag{1}$$

$$Z_2 = \frac{m_1 + n_2}{m_1 m_2 - n_1 n_2} \cdot \frac{1}{g_m} \tag{2}$$

The current steering output stage is driven from both the PMOS and NMOS side. Since the gain at $N_1(N_3)$ is around 6 times of the one at $N_2(N_4)$, an output current up to $7 \cdot I_{DC}$ ($6.5 \cdot I_{DC}$ achieved to keep certain biasing current in each branch) can be provided while consuming only $2 \cdot I_{DC}$ quiescent current. This compact class AB output stage suits with the optical sensor since the signal current flows in the known direction. Furthermore, no common-mode feedback (CMFB) circuit is needed because the DC output voltage at both V_{op} and V_{on} are fixed also by V_{REFH} and V_{REFL} through the gain components, saving power. The CMFB loop stability is discussed in Section III-B.

B. Stability Analysis

There are three feedback loops within this amplifier, where the loop stability needs to be analyzed. Firstly, the local feedback in the input stage (the P side is used in the following discussion), the boosted impedance at node N_1 and N_2 can be expressed in Eq. (1) and (2). Considering cutting of the loop at the drain of transistor n_1, the current gain from the drain of transistor m_1 to the n_2/m_2 side and back to the drain of n_1 is $(n_1{\cdot}n_2)/(m_1 \cdot m_2)$ and its value should be <1. Thus, $m_1 \cdot m_2 > n_1{\cdot}n_2$ must be fulfilled to avoid negative impedance that causes positive feedback. The ratio of the gains at N_1 and N_2 is chosen to be around 6 (19:3) to have high output current swing at low I_{DC} with good stability.

Secondly, the CMFB loop in the amplifier is discussed. Assuming there is a positive common-mode voltage signal at both input nodes (connected to the PD) of the core amplifier, the small signal current generated from the N side (through transistor $M3$ and $M4$) is shown as i_{3c} and i_{4c} in Fig. 3 (c), which has the same direction as differential current i_3 and i_4. However, the small signal current generated from the P side (i_{1c} and i_{2c} in Fig. 3(c)) has the opposite direction to the differential current i_1 and i_2. Because of the unbalanced gain discussed in Section III-A, these currents have the following relationship: $i_{1c} > i_{4c}$, $i_{2c} < i_{3c}$. As a result, the total small signal current at node V_{on} and V_{op} are drawing from these nodes, making both nodes negative. Therefore, the circuit has an intrinsic negative gain of CMFB loop transfer function, which stabilizes the common mode voltage to $(V_{REFH} + V_{REFL})/2$ without using any additional circuit. This feature simplifies the amplifier architecture and reduces the total power consumption. The frequency behavior of the CMFB loop is similar to the following discussion.

Finally, the main feedback back loop including the core amplifier, the gain components R_F (Z_F in Fig. 3) and the photodetector parasitic has three poles, as shown in Eq. (3). The pole at the input stage (node $N_1/N_2/N_3/N_4$) $1/R_I C_I$ is pushed to high frequency range with relatively low impedance at these nodes. The pole at the output at the class AB stage $1/(R_F||R_{II})C_{II}$ is compensated by the phantom zero $1/R_{ph}C_P$ by inserting a resistor between the PD and the core amplifier input [17]. The pole originated from the bipolar capacitance PD $1/(R_F + R_{II}) \cdot C_P$ dominates.

$$T(s) = \frac{A}{1 + sR_I C_I} \cdot \frac{1 + sR + phC_P}{(1 + s(R_F||R_{II})C_{II})(1 + s(R_F||R_{II})C_P)}. \tag{3}$$

IV. Reconfigurabilities

The proposed amplifier can be (re)configured to differential and single-ended input mode to be compatible with common photodiodes and SiPMs that need high biasing voltage. It also can be (re)configured to TIA/INT mode to have more exploration possibilities.

A. Single-Ended and Differential Mode

As discussed in Section III, the proposed amplifier can work well with photodiode by providing a bias voltage up to 1.1V(V_{DD} = 1.5V). In recent years, more efficient optical sensing devices, e.g., avalanche photodiode and silicon photomultiplier (SiPM) are being developed. These devices have a much higher optical responsivity, which can reduce the peak LED current to sub mA level. However, they need a very high reverse bias voltage that ranges from several volts to 30V. Therefore, in order to be compatible with these devices, the interface amplifier can be configured as single-ended input (Fig. 4[a][b]) by turning off the PMOS part of

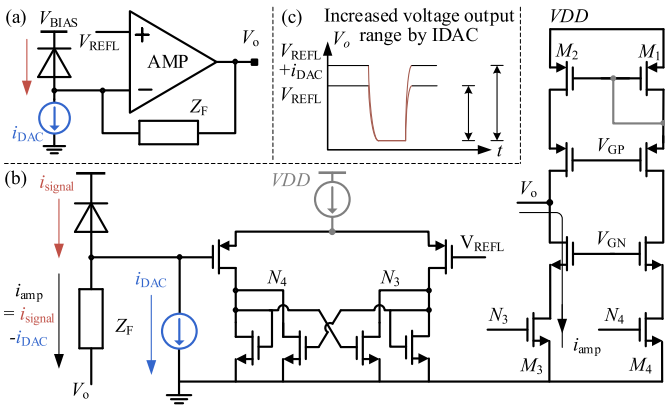

Fig. 4. (a) The proposed amplifier in single-ended configuration (b) detailed schematic of the proposed amplifier (c) increased voltage range by IDAC.

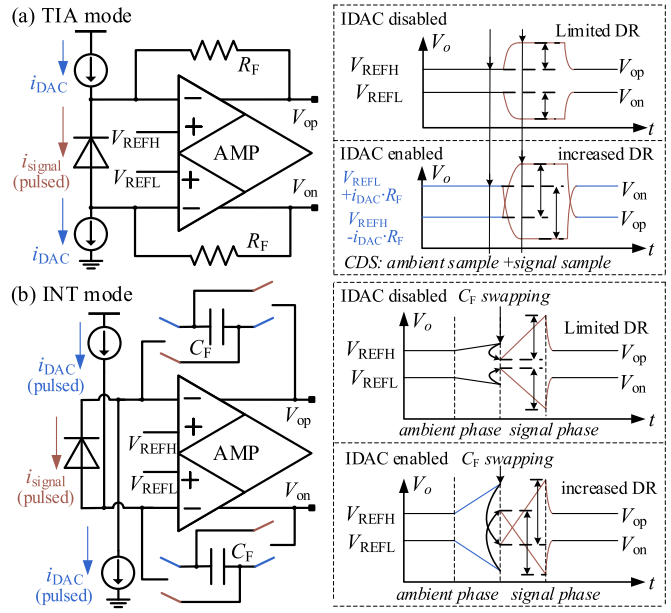

Fig. 5. TIA mode (a) and INT (b) mode operation with DR enhancement.

the *MCS* (connecting the current source transistor directly to V_{DD}) and connecting the gate and source of transistor M_2.

It is worth noting that, in the single-ended mode, the amplifier draws even less current from V_{DD} when there is a large current flowing through the photodetector. Namely, the current in transistor M_4, M_1 and M_2 are reduced due to the current steering operation controlled by the unbalanced gain. The signal current is drawn from the device bias V_{BIAS} through transistor M_3. In addition, the output voltage range can be increased by using a current DAC (IDAC) as shown in Fig. 4.

B. TIA and INT Mode

The amplifier can be (re)configured as TIA/INT by switching the feedback component Z_F. In TIA mode, the ambient component can be canceled by correlated double sampling (CDS) as shown in Fig. 5 (a), The PD biasing voltage is also copied to the output voltage, limiting the output voltage range. This can be solved by using a complementary IDAC as shown in Fig. 5 (b). In INT mode, the ambient component can be canceled by swapping the C_F capacitor in the same way as [10] and the issue on the limited output voltage range can be solved by a pulsed IDAC current [18].

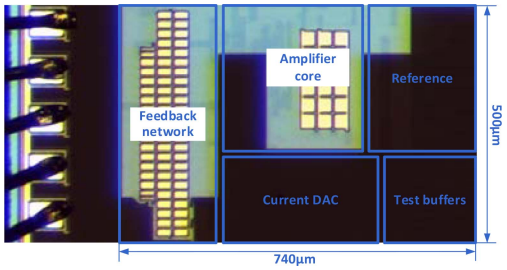

Fig. 6. Die-photo of the interface amplifier testchip (the shade is metal fillings).

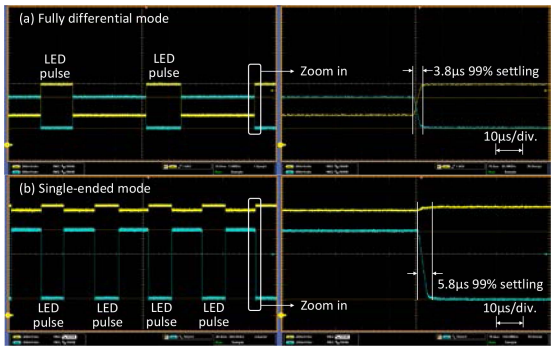

Fig. 7. The output voltage waveform of the amplifier measured by oscilloscope (a) Fully differential mode with photodiode (b) Single-ended mode with SiPM.

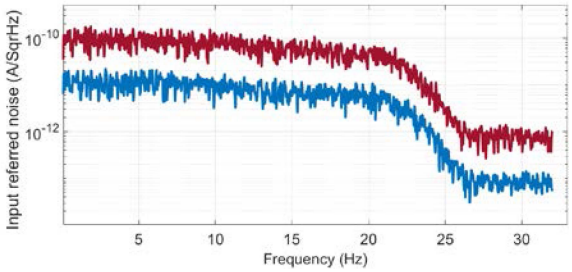

Fig. 8. The input referred current noise spectrum at gain of 10kΩ and 150kΩ.

V. Implementation Results

The proposed optical interface amplifier is implemented in a standard 180nm CMOS process. The test chip is shown in the die-photo (Fig. 6), including the amplifier core, the feedback components, the biasing generation block and two test buffers with unit gain feedback configuration for measurement. The whole system occupies a total area of 0.37 mm^2. The design is verified by suitable measurements. Fig. 7 (a) shows the pulse response of the amplifier in differential mode with a TIA gain of 150kΩ, connecting to a SFH7050 PPG sensor [19]. Fig. 7 (b) show the pulse response of the amplifier in single-ended mode with a TIA gain of 20kΩ, connecting to a SiPM. In both cases, the transient response shows good stability and the settling time is <10μS, which allows to used narrow LED pulses, saving power. Fig. 8 shows the noise spectrum of the PPG interface amplifier, measured by connecting the output of the proposed amplifier (with additional X10 gain by an external amplifier) to the SAR ADC and digital filter chain that are included in the SoC test board in [8]. The noise spectrum is obtained by after the ADC and digital signal conditioning chain. With a pulse repetition frequency of 4kHz and correlated double sampling scheme cancelling 1/*f* noise [10], the amplifier achieves an input noise of 67pArms

TABLE I
PERFORMANCE BENCHMARKING OF PPG/NIRS INTERFACE AMPLIFIERS

	[8]	[10]	[13]	[14]	[20]	[21]	This Work	
Technology	55nm	180nm	0.13μm	0.18μm	0.18μm	0.18μm	0.18μm	
VDD	1.2V	1.2V	1.2V	1.5V	1.0V	N.A.	1.5V	
Readout topology	Differential Current-Sensing	Single-ended Two-stage	Differential FC* w/o output stage	Differential Two-stage	Single-ended Two-stage.	Integration on PD capacitor	Proposed Differential	
Photodetector Bias	0~0.6V	0.5V	0V	0V	0.5	No	1V	
Transimpedance	10k-1MΩ	10k-1MΩ	19k-90MΩ	10k-3.2MΩ	N.A.	N.A.	5k-500kΩ	
Max. input range	25μA*	50μA	63μA	N. A.	56.3μA	N.A.	70μA	
Input noise	151pA$_{rms}$*	956pA$_{rms}$*	157pA$_{rms}$	10pA$_{rms}$	N.A.	20.4pA$_{rms}$	67pA$_{rms}$	582pA$_{rms}$
Dynamic range	104dB	94dB	112dB	97dB	93dB	N.A.	97dB$^{\#}$	102dB$^{\#\#}$
AFE Power	54μW*	120μW*	340μW	4.5μW**	8.1μW	13~25μW	48.7μW	

* only the AFE is considered; FC: Folded-cascode; **450μW continuous power with 1% duty cycling; $^{\#}$Differential mode; $^{\#\#}$Single-ended mode

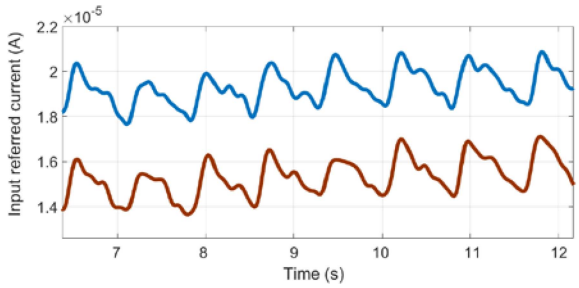

Fig. 9. The input referred current signal of red/IR PPG measured with SFH 7050.

in 32Hz bandwidth in differential mode with a gain of 150kΩ and a noise of 582pArms in 32Hz bandwidth in single-ended mode with a gain of 10kΩ. An on-body finger measured with SFH 7050 PPG sensor is shown in Fig. 9, where clear PPG pulses can be observed. The amplifier core consumes a total power of 48.7μW.

VI. BENCHMARK AND CONCLUSION

The performance of the proposed interface amplifier is compared to the state-of-the-art in Table I. The proposed amplifier with its fully differential unbalanced current steering operation provides the photodiode a DC bias voltage, while achieving a good power vs. noise, current range and DR trade off. With 32μA quiescent current, the amplifier can sink/source up to 70μA signal current, which is the highest among fully differential readouts. The achieved <100pArms in-band noise and >100dB DR are among the best in class. It is worth noting that, this brief focused on the design of the interface amplifier itself, duty cycling the amplifier according to the LED pulse can further reduce the average power consumption. Moreover, the reconfigurabilities allow this interface amplifier to operate with common photodiodes and SiPMs.

REFERENCES

[1] J. Allen, "Photoplethysmography and its application in clinical physiological measurement," *Physiol. Meas.*, vol. 28, no. 3, p. R1-39, 2007.
[2] A. A. Alian and K. H. Shelley, "Photoplethysmography," *Best Pract. Res. Clin. Anaesthesiol.*, vol. 28, no. 4, pp. 395–406, 2014.
[3] M. Wolf, M. Ferrari, and V. Quaresima, "Progress of near-infrared spectroscopy and topography for brain and muscle clinical applications," *J. Biomed. Opt.*, vol. 12, no. 6, 2007, Art. no. 062104.
[4] A. H. Hielscher *et al.*, "Near-infrared diffuse optical tomography," *Dis. Markers*, vo. 18, nos. 5–6, pp. 313–337, 2002.
[5] G. Wang, M. Atef, and Y. Lian, "Towards a continuous non-invasive cuffless blood pressure monitoring system using PPG: Systems and circuits review," *IEEE Circuits Syst. Mag.*, vol. 18, no. 3, pp. 6–26, 3rd Quart., 2018.
[6] K. N. Glaros and E. M. Drakakis, "A sub-mW fully-integrated pulse oximeter front-end," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 363–375, Jun. 2013.
[7] S. Vadrevu and M. S. Manikandan, "Real-time PPG signal quality assessment system for improving battery life and false alarms," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 11, pp. 1910–1914, Nov. 2019.
[8] S. Song *et al.*, "A 769 μW battery-powered single-chip SoC with BLE for multi-modal vital sign monitoring health patches," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1506–1517, Dec. 2019.
[9] J. Xu *et al.*, "A 665 μW silicon photomultiplier-based NIRS/EEG/EIT monitoring ASIC for wearable functional brain imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1267–1277, Dec. 2018.
[10] M. Konijnenburg *et al.*, "A multi(bio)sensor acquisition system with integrated processor, power management, 8×8 LED drivers, and simultaneously synchronized ECG, BIO-Z, GSR, and two PPG readouts," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2584–2595, Nov. 2016.
[11] Q. Lin *et al.*, "A 196μW, reconfigurable light-to-digital converter with 119dB dynamic range, for wearable PPG/NIRS sensors," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 2019, pp. C58–C59.
[12] A. K. Y. Wong, K. N. Leung, K.-P. Pun, and Y.-T. Zhang, "A 0.5-Hz high-pass cutoff dual-loop transimpedance amplifier for wearable NIR sensing device," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 7, pp. 531–535, Jul. 2010.
[13] P. Schönle, F. Glaser T. Burger, G. Rovere, L. Benini, and Q. Huang, "A multi-sensor and parallel processing SoC for miniaturized medical instrumentation," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2076–2087, Jul. 2018.
[14] A. Sharma *et al.*, "A sub-60 μA multimodal smart biosensing SoC with >80-dB SNR, 35μA photoplethysmography signal chain," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1021–1033, Apr. 2017.
[15] E. S. Winokur, T. O'Dwyer, and C. G. Sodini, "A low-power, dual-wavelength photoplethysmogram (PPG) SoC with static and time-varying interferer removal," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 4, pp. 581–589, Aug. 2015.
[16] S. Song *et al.*, "A low-voltage chopper-stabilized amplifier for fetal ECG monitoring with a 1.41 power efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 237–247, Apr. 2015.
[17] K. van Hartingsveldt, C. J. M. Verthoeven, and J. Willms, "Influence of frequency compensation on the linearity of negative feedback amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2. Kobe, Japan, 2005, pp. 1610–1613.
[18] M. Atef, M. Wang, and G. Wang, "A fully integrated high-sensitivity wide dynamic range PPG sensor with an integrated photodiode and an automatic dimming control LED driver," *IEEE Sensors J.*, vol. 18, no. 2, pp. 652–659, Jan. 2018.
[19] (2014). *OSRAM-SFH 7050, Application Note*. [Online]. Available: https://www.osram.com/ Home/Opto Semiconductors/tech
[20] F. Marefat, R. Erfani, and P. Mohseni, "A 1-V 8.1μW PPG-recording front-end with > 92-dB DR using light-to-digital conversion with signal-aware DC subtraction and ambient light removal," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 17–20, 2020.
[21] H. Kim and D. Jee, "A <25 μW CMOS monolithic photoplethysmographic sensor with distributed 1b delta-sigma light-to-digital convertor," in *Proc. 43rd IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Leuven, Belgium, 2017, pp. 55–58.