Review:

Out-of-order Execution

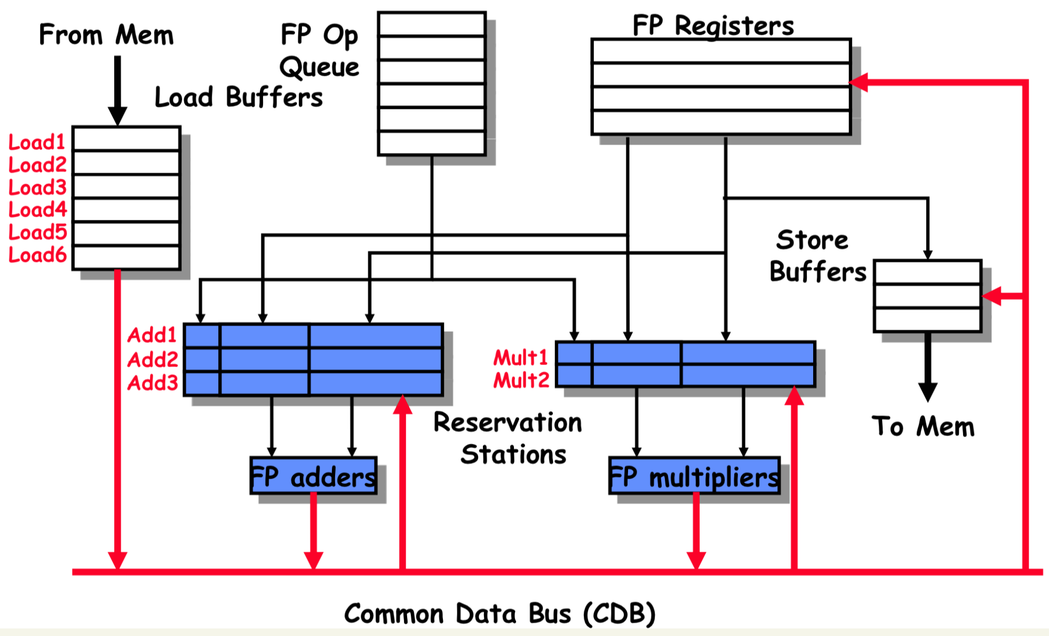
- History (of parallelism)
  - 1960s Vector (or Array) vs. Superscalar CDC6600
  - Scoreboarding vs. Tomasulo vs. Pipeline + OoO
    Thorton 1964
- Q: How to WAR, WAW?
  A: Renaming: Scoreboarding ×
  Tomasulo ✓
  Pentinum (1993): Renaming Register

Preview:

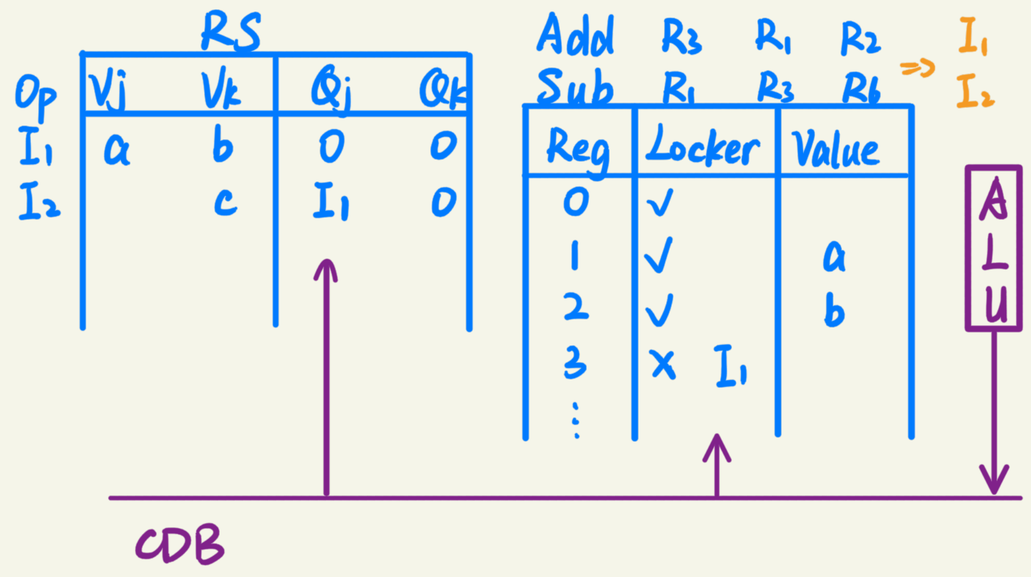
- Challenges → ROB 顺序提交
  - branch (inside Basic Block)
  - Exception 中断
  - Context Switching (multiprocess @ OS)
    进程切换 (向 Issue 中塞 NOP)

(H/w) forwarding ← distance ← RAW (True-dep)
(S/w) code movement
WAR
renaming ← WAW } pseudo

Tomasulo Organization



example1:



example2:

MUL R1
RAW
ADD R3 R1 R2
WAR
SUB ~~R1~~ R5 R6
R8
RAW
MUL ~~R1~~
R8

高端处理器 reg 较大
分离无关指令

Reservation Station Components

Op: Operation to perform in the unit (e.g., + or –)

Vj, Vk: **Value** of Source operands
- Store buffers has V field, result to be stored

Qj, Qk: Reservation stations producing source registers (value to be written)
- Note: Qj,Qk=0 => ready
- Store buffers only have Qi for RS producing result

Busy: Indicates reservation station or FU is busy

Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

What about Precise Interrupts?

- Tomasulo had:

  In-order issue, out-of-order execution, and out-of-order completion

- Need to "fix" the out-of-order completion aspect so that we can find precise breakpoint in instruction stream.

Precise Interrupts

Unprecise:
x:
y: page-fault x需要重做 → handler
z:

Win: 即时修改
linux: GG.

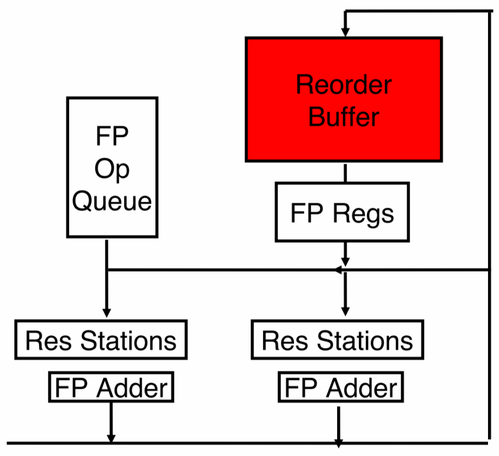
精确中断(precise interrupt)：精确中断是一种能够使机器处于良好状态下的中断，它具有如下特征

- PC （程序计数器）保存在一个已知的地方
- PC 所指向的指令之前所有的指令已经完全执行
- PC 所指向的指令之后所有的指令都没有执行
- PC 所指向的指令的执行状态是已知的

非精确中断(imprecise interrupt)：不满足以上要求的中断，指令的执行时序和完成度具有不确定性，而且恢复起来也非常麻烦。

HW support for precise interrupts

- Need HW buffer for results of uncommitted instructions: *reorder buffer*
  - 3 fields: instr, destination, value
  - Use reorder buffer number instead of reservation station when execution completes
  - Supplies operands between execution complete & commit
  - (Reorder buffer can be operand source => more registers like RS)
  - Instructions commit
  - Once instruction commits, result is put into register
  - As a result, easy to undo speculated instructions on mispredicted branches or exceptions



Challenges to ROB:

某条指令极其缓慢导致ROB满.

Sol: To be continued...