9.28 notes

1. Review

- pip line
- three hazard: data hazard, load hazard, control hazard

2. Performance

Boeing 747 VS Sud Concodre

Speed

depends on:

- **Time to run the task Execution time, response time, latency** (Execution Time)
- **Tasks per day, hour, week, sec, ns ...** (Performance)

CPU Performance

Aspects of CPU Performance (CPU Law)

$$\text{CPU time} = \frac{\text{Seconds}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}$$

	Inst Count	CPI	Clock Rate
Program	X		
Compiler	X	(X)	
Inst. Set.	X	X	
Organization		X	X
Technology			X

1/17/01 CS252/Patterson Lec 1.37

How Compiler promotes CPI: reordering the instruction

1965，IBM360，

Brook's "Man Month Myth"

Amdahl "Arch of IBM 360"

$S_p = \frac{1-\eta+\eta}{1-\eta+\frac{\eta}{S}}$ and η means the most common part, S means the number of parallel operating units.

Parallelism :

- ILP (Arch)
- TLP (OS)
- LLP (Compiler)

Cache

Cache vs Buffer

Cache: to temporarily store the frequently used data

Buffer: to merge the gap of the data input speed and the data consuming speed

Memory visiting

Maurice Wilkes, EDSAC(英), Subroutine,micro-programming

1. 最经被访问，则最近被访问的概率更大:

   the recently visited data are more likely to be visit in a short time span

2. 相邻数据访问概率大:

   the nearby data are more likely to be visit in a short time span

AMAT: Average Mem Access Time

AMAT = Hit Time + Miss Rate $\times$ Miss Penalty

Cache Mapping

1. **DM:** direct mapping
2. **FA:** Full Associative
3. **SA:** Set Associative