

# Note W14D1

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## Functions

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## Performance

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### Parallelism

Pipeline

#### Basic Principle

- Balance (stage-stage)
- Speed up = N-stages

#### Hazard

stalls

#### Structural

Duplicating

eg. memory conflict → I-Cache/D-Cache

#### Data

- RAW → Distance Prod/Cons
- WAR, WAW → renaming

#### Control

a control list (JMP B CALL/RET)

- do nothing
- kill branch
- delay-slot

## Locality

Cache

$$AMAT_{Cache} = T_{hit} + \eta_{miss} \times T_{penalty}$$

- $T_{hit}$  : small, DM is fast and FA is slow
- $\eta_{miss}$  : high associative, small miss-rate
- $T_{penalty}$  : Mem (L2-Cache) → wider bus, multi-bank

## Reducing Latency

- freq
- CLA

## Principles

- Small: fast
- Simple: RISC
- Tradeoff/compromise
- Amdahl's law:  $S_P = \frac{1}{(1-\eta) + \eta/s}$