# **Cache Optimization Summary**

	Technique	MR	MP	HT	Compl	exity	
miss rate	Larger Block Size Higher Associativity	+ 1	of Seating	() 31 () M	的。 UX H	0 1	
	Victim Caches Pseudo-Associative Caches HW Prefetching of Instr/Data (Street Compiler Controlled Prefetching Compiler Reduce Misses	· · · /	bindi non bi	ng din	υ / A	2 2 2 3	4
enalty	Priority to Read Misses red & write Early Restart & Critical Word 1st Non-Blocking Caches Second Level Caches	满忧羌. À Write Bu		, our g		1 2 3 2	<u>1</u>
Ω.							

- MR: miss rate
- MP: miss penalty
- HT: hit time

RW: non-blocking Cache? (in P83)

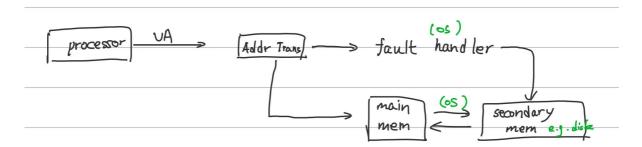
reduce  $T_{hit}$ : prefetch, outstanding...

需要寄存器: Miss Status Holding Registers

## **Virtual Memory**

disk 内划分一块作为 mem

### virtual address



#### **Translation**

- section
- segment
- page

碎片分类: external fragment, internal fragment

### **Page**

- VA: (vp # , offset)
- PA: (physical page #, offset)
- translate : page table in mem

### 与 Cache 的关系

1. virtual addressing cache: 歧义 (ambiguity) & 别名 (alias)
2. physical addressing cache: 每次访问 Cache 都要翻译,开销大

hint: 当 page 字段够左边,此时不会出问题