1. Tx Memory. (考述:一个Tx一个核15)

ataline Cache 被监控、看题在总域有发 invalid 信号

不考虑一个 core上跑多个Tx 情况

(双发射了不够国时发一个 branch 725 \$27 dual issue Tomasulo tother (?) 待着的病认 d. Store Buffer 一个 FIFO/非 FIFO BUSI Snoopy MESI 状态机光档清楚 会参 CPU - Cache / 2. Write buffer: 李彻大行世的那个 SB? 与 Cache B国相关 commit 后慢慢的 3. 17 addm. xbegin xend Jim L1 Cache XN? idea: 加时间差 / addm. at内在物质加 这一: 2 逐次逼近 / 由于借了 Cache一致性协议 2k+1个操作后, 有一个 Cache line 序并 (aborted) 江伽家观

4. MESI 状态转换 P1. p2 伐指

Snoop Cache Extensions

CPU Read hit Remote Write or Miss due to address conflict Write back block Write back block Write back block Write back block Write back when shared state (no memory access) Illinois Protocol

Snoop Cache Extensions

Extensions:

Fourth State: Ownership

Shared-> Modified, need invalidate only (upgrade request), don't read memory Berkeley Protocol

Remote Write or Miss due to address conflict Write back block Write back block Write back block Write back block Pu Write back block Write back when shared state (no memory access) Illinois Protocol

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Write back block Write back when shared state (no memory access) Illinois Protocol

Scales very read white Write back when shared state (no memory access) Illinois Protocol

CPU Write Miss on Bus?

CPU Write

Miss on Bus?

CPU Write

Miss on Bus?

CPU Write

Miss on Bus?

CPU Write

Miss on Bus?

CPU Write

Miss on Bus?

CPU Read hit

CPU Write

Miss on Bus?

