Formative Assessment 3: Multi-stage Amplifier Design

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***Abstract*—This paper presents a design of a Multi-stage Amplifier circuit utilizing a current mirror and a current sink configuration to achieve high precision in replicating current across the circuit's branches. The design is centered around the provided specifications, thus all decisions made in this paper were in pursuit of attaining the required currents and percent error. In line with that, a 1:1 Current Transfer Ratio was utilized for the computations due to the lack of a GCF between the specified currents, this ratio also results in a very accurate current replication across the branches. The findings demonstrate that CTR chosen proved effective in reducing both the component count, while simulatenously increasing the accuracy of the current mirror circuit. This design also demonstrates the effectiveness of a load resistor in place of an load transistor.**

Keywords – Multi-stage Amplifier, Current Mirror Circuit, Biasing Network, Current Transfer Ratio

I. INTRODUCTION

A current mirror, as the name implies is a circuit used to copy a current from one branch, to another branch [3]. It is a fundamental component in analog circuits and are frequently utilized in amplification and biasing of circuits [1]. An important trademark of the current mirror is its low input and high output impedances, these properties enable the current mirror to deliver a constant current regardless of load conditions [2]. The accuracy of a current mirror is based on the matching of the devices used to construct it, the higher the matching the better the accuracy of the resulting current mirror [3]. A multi-stage amplifier consists of multiple stages cascaded that each require a biasing voltage to function, this paper will be using current mirrors as biasing devices to develop a highly optimized and well-performing amplifier circuit that meets the specified requirements.

II. DESIGN METHODOLOGY

The task is to design a multi-stage amplifier that precisely replicates the current to the different branches and biases the amplifier, the specifications were provided by the instructor and are shown in Table I.

TABLE I. DESIGN SPECIFICATIONS

I_1	I_2	V_{CC}
4µ	7µ	15V

The design will be centered around the provided specifications, with the goal to achieve high-precision current mirroring in the biasing and load resistors of the circuit, with less than a 5% error.

A. Computations

1) Reference Current I_{REF1}: Due to the lack of a common factor between the provided currents I_1 and I_2, a ratio of 1:1 to the reference current(I_{REF}) ratio is set. This ratio is known as the Current Transfer Ratio(CTR) and will be important in determining the total component count of the circuit. For the first stage of the amplifier I_{REF} is as follows:

$$I_{REF1} = 4\ \mu A \tag{1}$$

2) Biasing Resistor: With the value of I_{REF} established, we can then solve for the biasing resistor, R_1 using equation (2), via manipulation we get equation (3) and are able to solve for R_1 given the values of V_{CC} which is included in the provided specificaitons, a voltage drop of 0.7, and I_{REF}.

$$IREF = \frac{15V-0.7V}{R_1} \tag{2}$$

$$4\mu A = \frac{15V-0.7V}{R_1}$$

$$R_1 = \frac{15V-0.7V}{4\mu A} = 3.575M\Omega \tag{3}$$

3) Current Source: With the values of R_1 and I_{REF}, we can now proceed in configuring the biasing branch for our circuit. A PNP transistor was utilized as it regulates current flow from the supply voltage to the load, and proves to be a more flexible option for current sourcing.

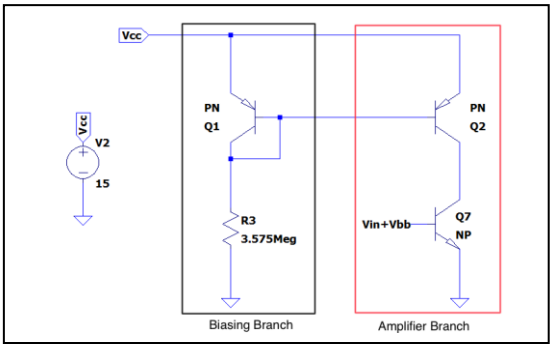

Fig. 1. Biasing Branch & Initial Topology for I_1

4) Current Transfer Ratio: With the completion of the biasing branch, we will utilize the topology shown in Fig. 1 and solve for the number of components needed in both the

biasing and amplifier branch. The CTR, set to a ratio of 1:1 is utilized in the computation for the number of components and can be seen in equations (4-5).

$$\text{CTR} = \frac{I_1}{I_{REF2}} = \frac{4\mu A}{4\mu A} = 1 \quad (4)$$

$$n = 1 \times m$$

$$\text{let } m = 2$$

$$n = 1 \times m = 2 \quad (5)$$

5) Load Resistor: A load resistor is capable of scaling its output with reference to a current, thus more suitable to be in this multi-stage amplifier instead of a NPN transistor. A transitor can be used, but this design opted for a resistor due to providing a lower percent error overall. The value of load resistor R_{L1} is shown in equation (6), and the final biasing topology for I_1 with the load resistor is shown in Fig. 2

$$R_{L1} = \frac{Vcc}{I_1} = \frac{15}{4\mu A} = 3.75M\Omega \quad (6)$$

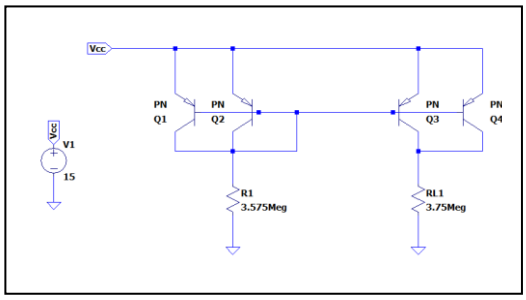

Fig. 2. Final Topology for I_1

6) Current Sink: For the second stage, a current sink configuration is utilized to achieve accurate control as it drains current to the ground. Enabling a much lower percent error in the reference currents for the second stage of the amplifier design.

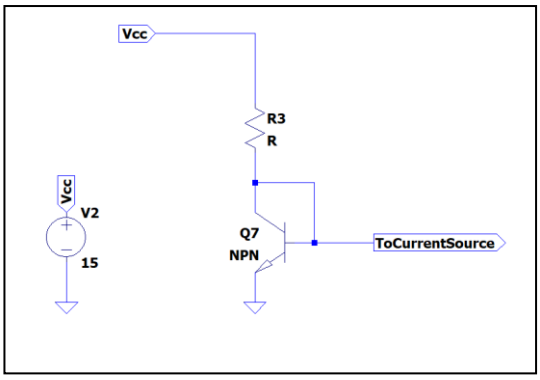

Fig. 3. Current Sink Topology

7) Reference Current I_2: The CTR of 1 also applies to the second stage of the circuit, therefore:

$$I_{REF2} = 7\ \mu A \quad (7)$$

8) Biasing and Load Resistor: With the value of I_{REF2} established, solving for biasing resistor R_2 and load resistor R_{L2} is shown in equations (8-9)

$$R_2 = \frac{15V - 0.7V}{7\mu A} = 2.0428M\Omega \quad (8)$$

$$R_{L2} = \frac{15V}{7\mu A} = 2.21428M\Omega \quad (9)$$

9) Biasing Topology for I_2: Similar to the first stage the CTR is set at 1:1. An NPN transistor has good current regulation, therefore no additional amplifier branches are needed, and thus m is set to 1.

$$\text{CTR} = \frac{I_2}{I_{REF2}} = \frac{4\mu A}{4\mu A} = 1 \quad (10)$$

$$n = 1 \times m$$

$$\text{let } m = 1$$

$$n = 1 \times m = 1 \quad (11)$$

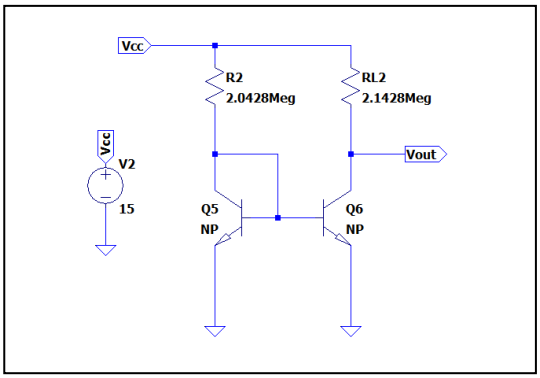

Fig. 4. Initial Biasing Topology for I_2

10) Completed Circuit: After completing the components for the first stage and second stage, cascading them results in Fig. 5. and thus results in our final circuit. The model for the PNP and NPN transistors are as follows:

.model NP NPN(BF=125 Cje=.5p Cjc=.5p Rb=500)

.model PN LPNP(BF=50 Cje=.3p Cjc=1.5p Rb=250)

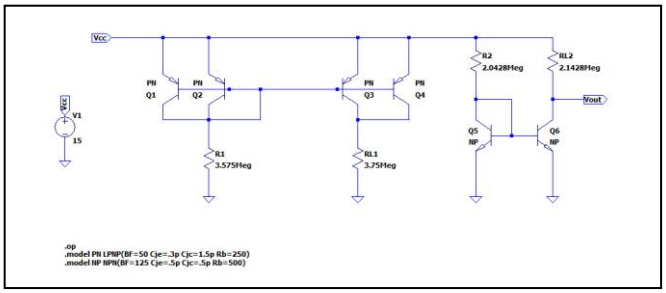

Fig. 5. Current Sink Topology

III. DESIGN VERIFICATION

The design can be verified through SPICE simulations using the ".op" command, which displays the operating point of our circuit. The measured values from the software are then compared to the initial specifications given. The percent error is calculated using the formula in equation (12), and the results are summarized in Table II.

$$\%ERROR = \left|\frac{Measured - Ideal}{Ideal}\right| x\ 100\% \qquad (12)$$

TABLE II. RESULTS

	Ideal Value	Measured	%Error
I_{REF1}	4 µA	4.0244 µA	0.0061%
I_1		3.8696 µA	0.0326%
I_{REF2}	7 µA	7.0268 µA	0.0038%
I2		6.9068 µA	0.0133%

As seen in Table II. The design meets the given specifications with a percent error significantly less than the stated maximum of 5%. It can be concluded that the amplifier works efficiently and as expected.

IV. COMPONENT COUNT

The total component count can be seen in Table III. This includes all transistors and biasing resistors utilized in the design of the circuit, but do note that it does not include the load resistors in place of the transistor loads.

TABLE III. COMPONENT COUNT

Component	Count
PNP	4
NPN	2
RESISTOR	2

A major contributing factor to the component count is the CTR, changing this ratio can result in a much higher component count than what is needed. Carefully considering the specifications and setting the CTR ensures optimum amplifier performance with minimal component usage.

V. CONCLUSION

Designing a multi-stage amplifier requires a fundamental understanding of the workings of a current mirror circuit, its downfalls and techniques as to how to increase its precision without increasing the cost and/or component count of the design. This is necessary due to the fact that a current mirror works well as a biasing source, removing the need for multiple voltage sources in a multi-stage amplifier. The strengths of PNP and NPN transistors were observed in this design, a PNP transistor is effective at acting as a current source, while an NPN transistor is effective for current sinking. Although it should be noted that due to the nature of using simulations, the current mirror may not work as effectively due to real world variances and mismatch in the components, which greatly affect the performance of a current mirroring circuit. Another possible issue that may arise is the use of resistors in this design. While the resistors scale the current through it and led to the low percent error, there could be issues in acquiring the necessary resistor values to make this design plausible in the real world. Nonetheless, the design utilized a minimal number of components, and successfully achieved the desired parameters and percentage errors.

VI. REFERENCES

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