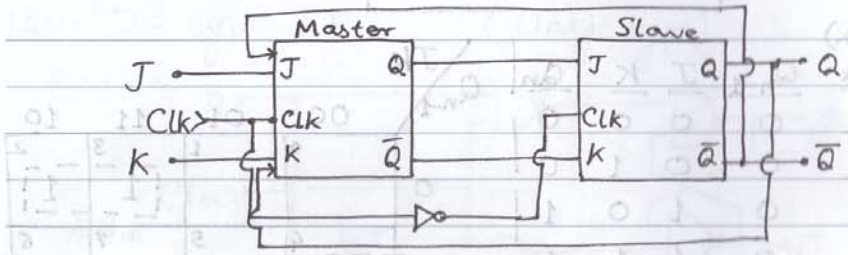
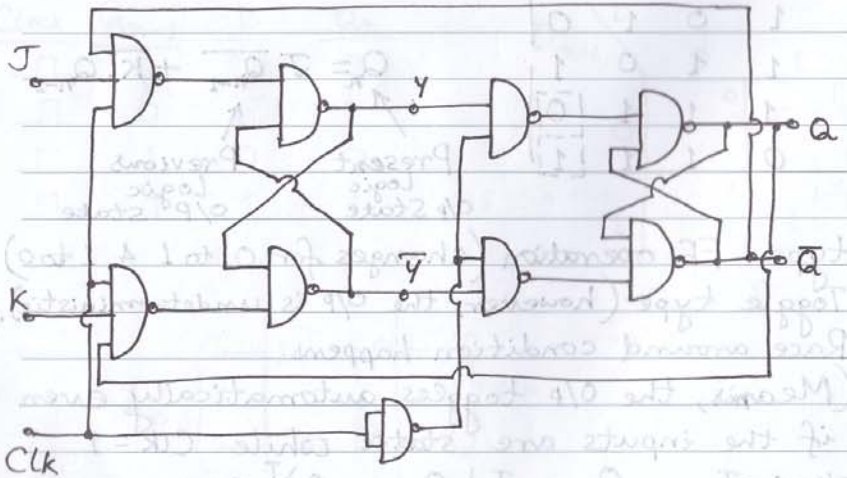
16. J-K Master-Slave flip-flop:

Clock pulse width is larger than the propagation delay, which causes problem while J=K=1 (toggle mode), as at the end of a clock pulse, O/Ps may/may not toggle to a correct value/logic. Such a problem is solved by using a master-slave FF (Solves the problem of race around)





Clk	Q_{n-1}	J	K	Q_n
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0
0	0	1	1	1

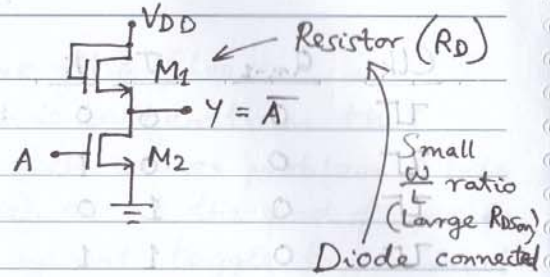
} Toggle mode is correctly implemented by using J-K M-S FF.

17. Logic families: Ckt. & Voltage selection in digital systems. (Components)

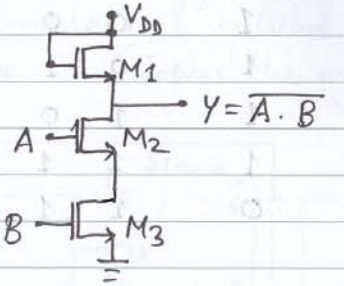
RTL : Resistor Transistor Logic
DTL : Diode Transistor Logic
TTL : Transistor Transistor Logic
ECL : Emitter Coupled Logic
nMOS & pMOS : n- or p-channel MOS
CMOS : Complementary Metal Oxide Semiconductor

a) n-MOS logic: Uses only n-ch MOSFETs.
Basic gates:
1) Inverter (NOT)
2) NAND
3) NOR

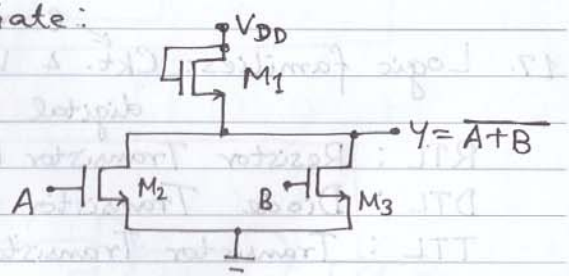
nMOS NOT Gate:



nMOS NAND Gate:



nMOS NOR Gate:

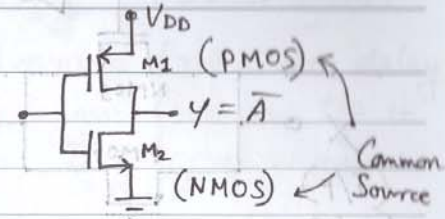


b) CMOS Logic: Both n-channel & p-channel MOSFETs are used (typically same in number)
- → Avoids R_D or Diode connected MOSFETs.
- → Offers Low power, as current (static) in between V_{DD} & Gnd is always zero. However (dynamic) current is present during logic transitions only.
- → Smaller area on a semiconductor integrated circuit (IC).

CMOS NOT Gate

A=0, M_1 (ON), M_2 (OFF), $Y = V_{DD}$

A=1, M_1 (OFF), M_2 (ON), $Y = 0V$

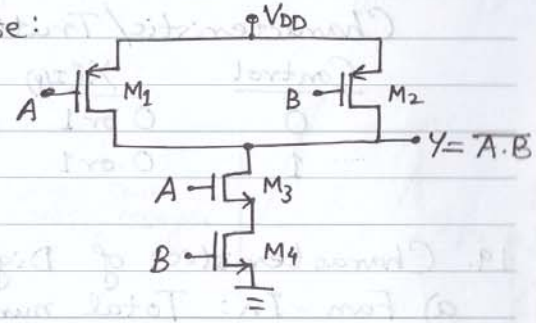


CMOS NAND Gate:

M_1, M_2 : PMOS

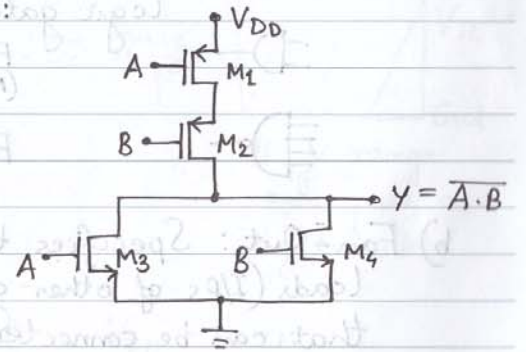
M_3, M_4 : NMOS

A	B	Y
0V	0V	V_{DD}
0V	Vdd	V_{DD}
Vdd	0V	V_{DD}
Vdd	Vdd	0V



CMOS NOR Gate:

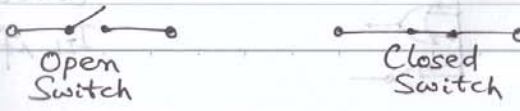
A	B	Y
0V	0V	Vdd
0V	Vdd	0V
Vdd	0V	0V
Vdd	Vdd	0V

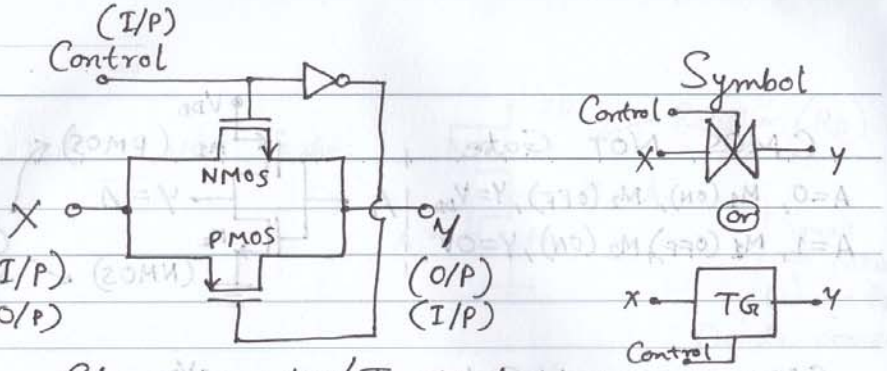


18. CMOS Transmission Gate:

Digitally controlled switch: For Analog or Digital Signal propagation.

(Solid-state ← Semiconductor or no moving parts)



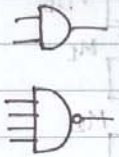


Characteristic/Truth table:

Control	X(I/P)	Y(O/P)
0	0 or 1	Tri-state (or don't care) / Open-ckt
1	0 or 1	$X_{(I/P)}$

19. Characteristics of Digital ckts:

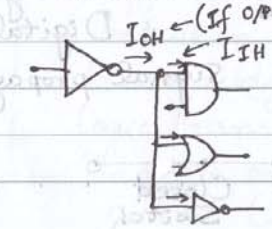
a) Fan-In: Total number of I/Ps in a logic gate. (may be odd or even)



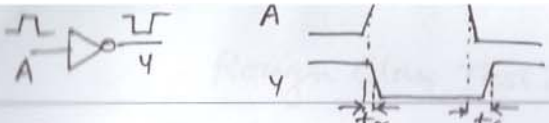
Fan-in = 2
(No. of I/Ps)

Fan-in = 4

b) Fan-Out: Specifies the number of standard loads (I/Ps of other gates/digital logic I/Ps) that can be connected safely to the O/P of a gate without degrading its normal operation (change in O/P logic state due to excessive loading does not occur)



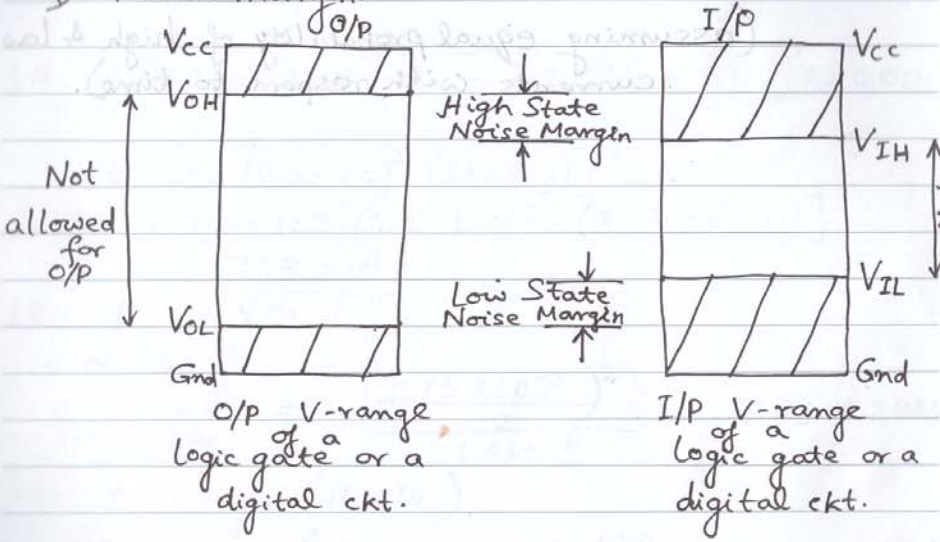
(Same with opp. direction of I_{OL}, & I_{IL} if O/P is 0)



$$PD = \frac{t_r + t_f}{2}$$

c) Propagation delay: Average transition delay time for signal to propagate from an I/P to its O/P when a binary I/P signal changes a value/logic.
(Time delay of a gate or any digital ckt)

d) Noise margin:



O/P V-range of a logic gate or a digital ckt.

I/P V-range of a logic gate or a digital ckt.

Noise margin (high) = $V_{OH} - V_{IH}$
Noise margin (low) = $V_{IL} - V_{OL}$

where,

V_{OH} : Voltage O/P high ('1' state)
V_{OL} : " " low ('0' state)
V_{IH} : " I/P high ('1' state)
V_{IL} : " " low ('0' state)