Experiment-5

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I ran the experiment-4 codes in Intel Quartus Prime Lite software then the following reports are generated for FIR filter:

Before pipelining:

Direct method:

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Oct 8 18:29:23 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CEBA9F31C8
Timing Models	Final
Logic utilization (in ALMs)	821 / 113,560 (< 1 %)
Total registers	1639
Total pins	68 / 480 (14 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	1 / 342 (< 1 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

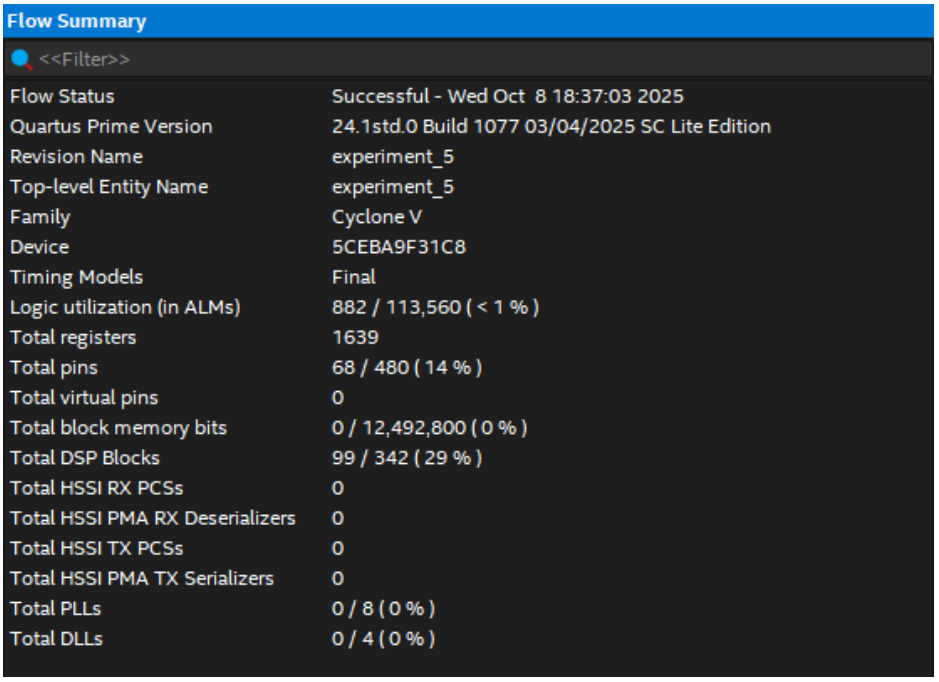
Optimized method:

Flow Summary

<<Filter>>

Flow Status	Successful - Wed Oct 8 18:33:00 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CEBA9F31C8
Timing Models	Final
Logic utilization (in ALMs)	1,756 / 113,560 (2 %)
Total registers	1639
Total pins	68 / 480 (14 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

Genvar method:



Flow Summary

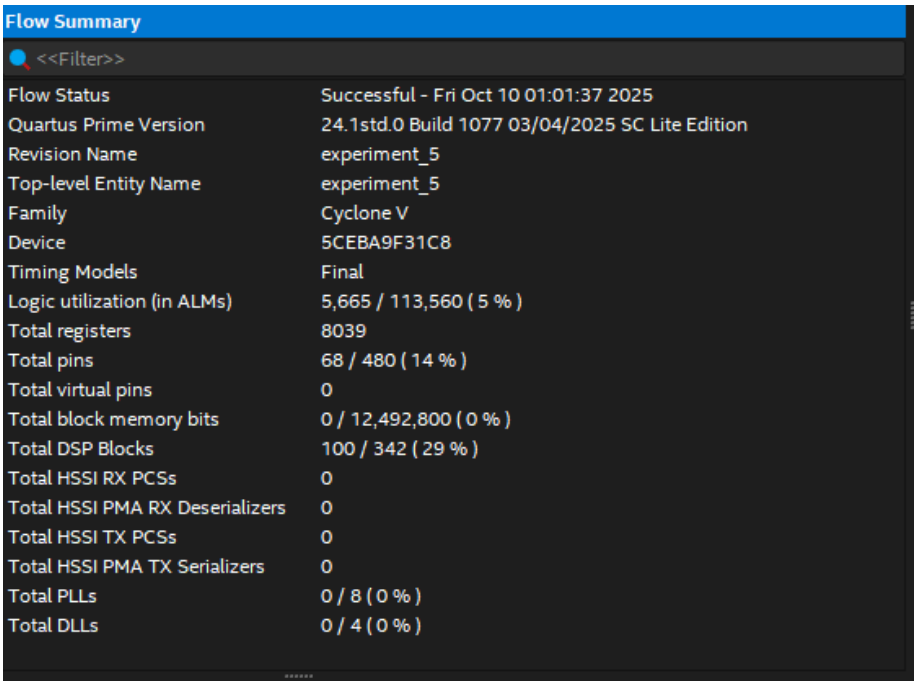
<<Filter>>

Flow Status	Successful - Wed Oct 8 18:37:03 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CEBA9F31C8
Timing Models	Final
Logic utilization (in ALMs)	882 / 113,560 (< 1 %)
Total registers	1639
Total pins	68 / 480 (14 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	99 / 342 (29 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

As we can see from the above reports the number of registers are same in all of the above methods as I am not using any new registers in any of the codes, the change is only in the logic or the way we are implementing the FIR filter.
So the logic utilization and DSP blocks are changing for the three methods. The DSP blocks and logic utilization are more in optimized method as here we are grouping the terms with same coefficients so it is taking more DSP blocks.

After pipelining:

Direct method:

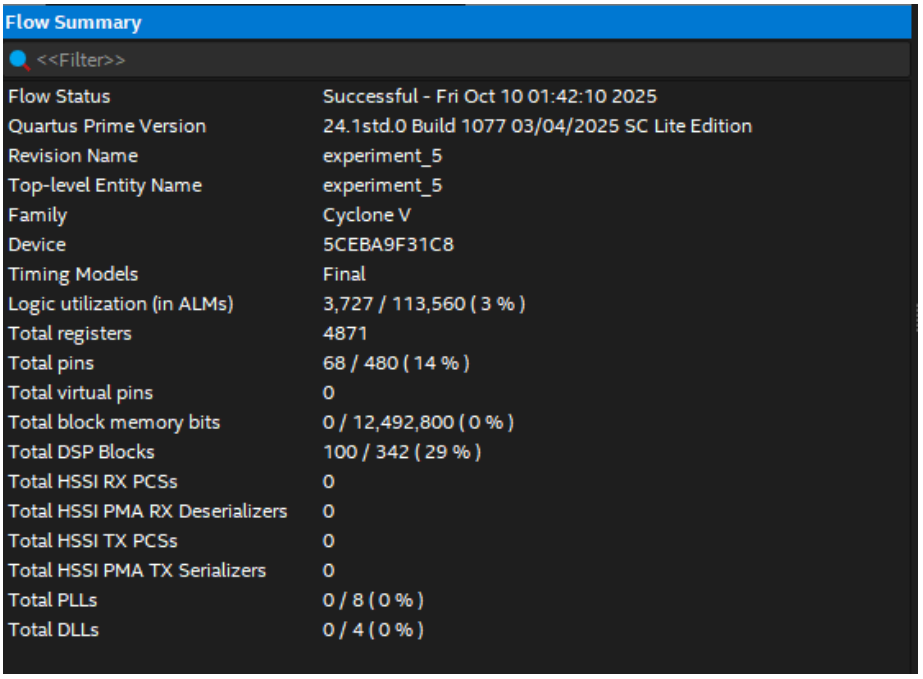


Flow Summary

<<Filter>>

Flow Status	Successful - Fri Oct 10 01:01:37 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CEBA9F31C8
Timing Models	Final
Logic utilization (in ALMs)	5,665 / 113,560 (5 %)
Total registers	8039
Total pins	68 / 480 (14 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

Optimized method:



Flow Summary

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Flow Status	Successful - Fri Oct 10 01:42:10 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CEBA9F31C8
Timing Models	Final
Logic utilization (in ALMs)	3,727 / 113,560 (3 %)
Total registers	4871
Total pins	68 / 480 (14 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

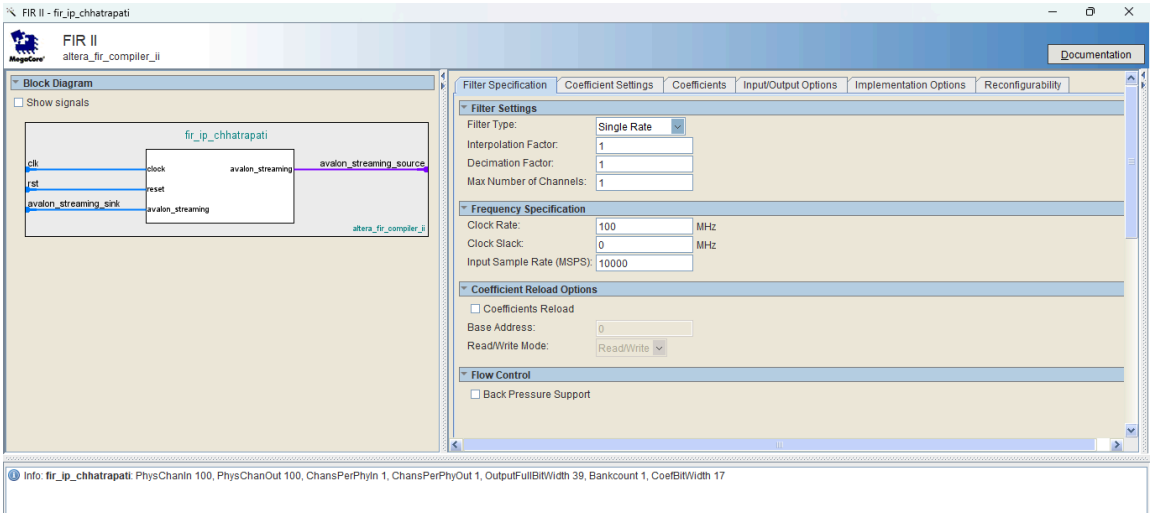
Genvar method:

Flow Summary

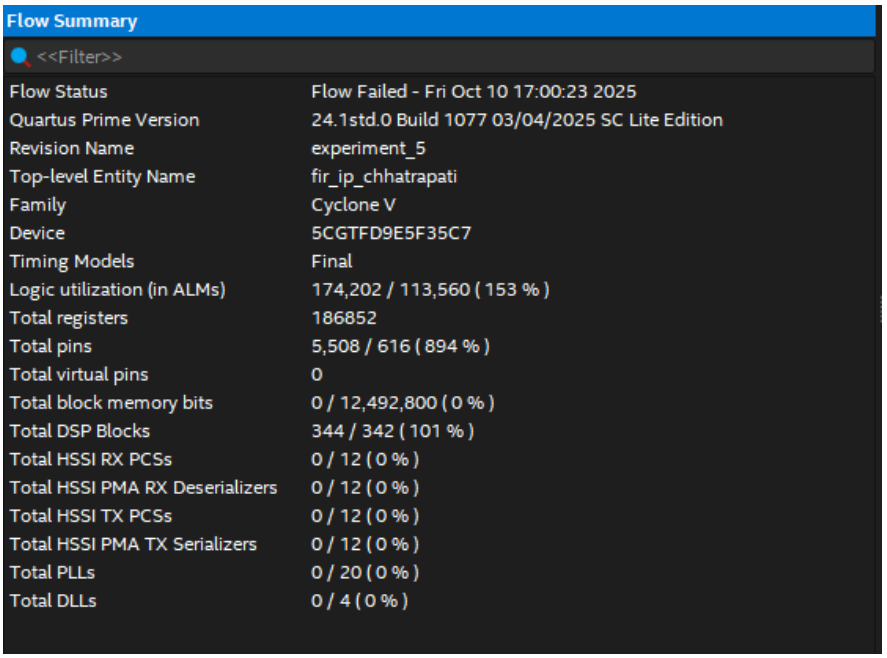
<<Filter>>

Flow Status	Successful - Fri Oct 10 19:58:39 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	63 / 113,560 (< 1 %)
Total registers	199
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	10 / 342 (3 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)

Here after pipelining also Optimized method has more logic utilization then the other methods.
But the logic utilization and registers used are significantly increased after pipelining as in pipelining we introduced registers to store data before performing the FIR filter.
Using FIR IP:
Here I am using a FIR || which is already present in intel quartus prime lite for running the FIR filter. Here a MegaWizard named GUI is opening and I have to give the specification for the FIR filter to run.
The GUI and the circuit block of FIR ||.



Flow summary:



Flow Summary

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Flow Status	Flow Failed - Fri Oct 10 17:00:23 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	fir_ip_chhatrapati
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	174,202 / 113,560 (153 %)
Total registers	186852
Total pins	5,508 / 616 (894 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	344 / 342 (101 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

Here in flow summary we can see it is using a significant amount registers and resources.

Flow status	Without pipelining			With pipelining			FIR IP
	Direct	Optimized	Genvar	Direct	Optimized	Genvar	
Logic utilization	821	1756	882	5665	3727	63	174202
Registers	1639	1639	1639	8039	4871	199	186852
DSP blocks	1	100	99	100	100	10	344