Experiment_7

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Here for the implementation of 8-point FFT I wrote the verilog code as follows:

I calculated the values of twiddle-factor before by hand and directly defined these values as local parameters. Then I assigned the input values to the input. Then I defined three stages for pipelining where I manually wrote code for each stage formulawise. Where each stage inputs for the formula are given parallelly using parallel processing. Then finally from the last stage the output is stored in the real and imaginary part of output.

Utilization report:

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Oct 31 17:55:57 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_7
Top-level Entity Name	experiment_7
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	108 / 56,480 (< 1 %)
Total registers	234
Total pins	44 / 268 (16 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	8 / 156 (5 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

Throughput:

	Fmax	Restricted Fmax	Clock Name	Note
1	94.89 MHz	94.89 MHz	clk	