Experiment-6

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In this experiment I am comparing the FIR filter with and without pipelining and parallel processing using three methods that are direct method, optimized method and using genvar method.

Direct method:

Normal FIR filter without any pipelining and parallel processing.

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Oct 21 00:30:13 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_direct
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	880 / 113,560 (< 1 %)
Total registers	1639
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	99 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	2.53 MHz	2.53 MHz	clk	

Using pipelining in direct method:

Flow Summary

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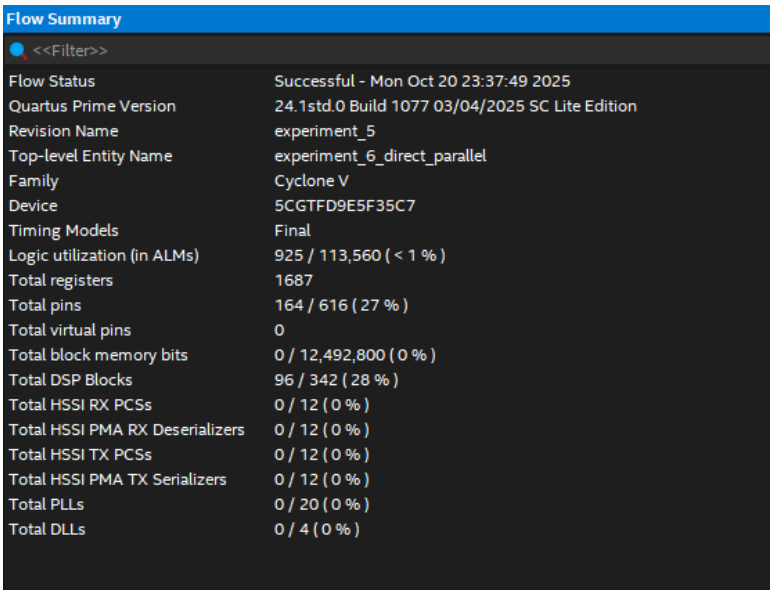
Flow Status	Successful - Tue Oct 21 00:22:56 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_direct_pipelining
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	2,454 / 113,560 (2 %)
Total registers	4839
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	172.89 MHz	172.89 MHz	clk	

Using parallel processing in direct method:



	Fmax	Restricted Fmax	Clock Name	Note
1	7.77 MHz	7.77 MHz	clk	

Comparison:

Throughput & resource utilization	Direct method	Direct method using pipelining	Direct method using parallel processing
Throughput/ Fmax(in MHz)	2.53	172.89	7.77
Logic utilization	880	2454	925
Total registers	1639	4839	1687
Total pins	68	68	164
Total DSP blocks	99	100	96

Throughput_pipelining = 68.33*Throughput_nonpipelining

Throughput_parallel_processing = 3.07*Throughput_nonpipelining

Optimized method:

Normal FIR filter without any pipelining and parallel processing.

Flow Summary

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Flow Status	Successful - Mon Oct 20 23:47:55 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_opt
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	1,757 / 113,560 (2 %)
Total registers	1639
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

0 / 12,492,800 (

	Fmax	Restricted Fmax	Clock Name	Note
1	44.52 MHz	44.52 MHz	clk	

Using pipelining in optimized method:

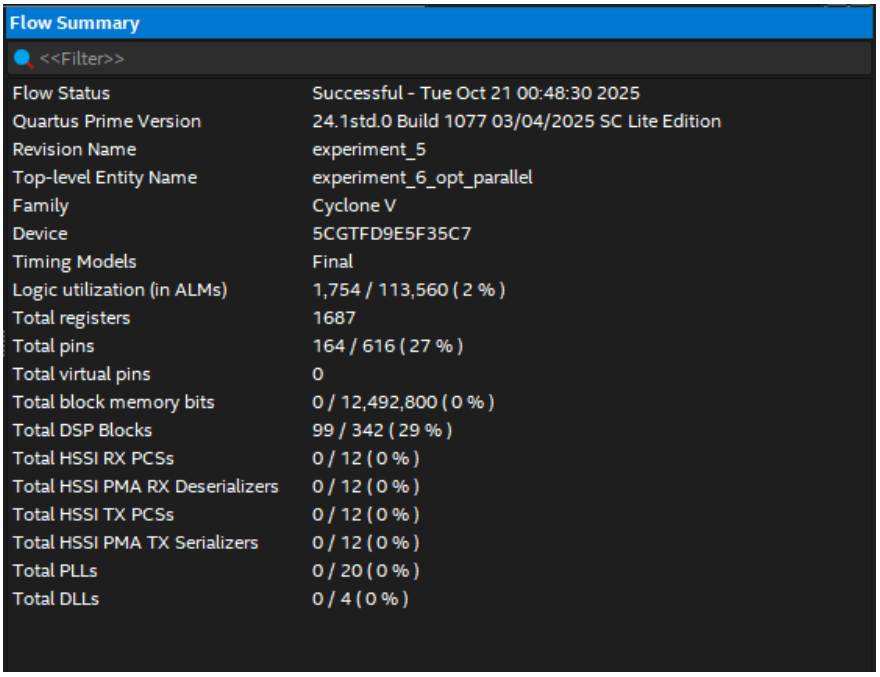
Flow Summary

<<Filter>>

Flow Status	Successful - Tue Oct 21 00:13:47 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_opt_pipelining
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	2,074 / 113,560 (2 %)
Total registers	3285
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	100 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	135.04 MHz	135.04 MHz	clk	

Using parallel processing in optimized method:



Flow Summary

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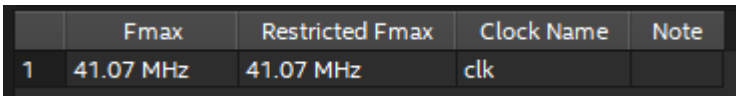
Flow Status	Successful - Tue Oct 21 00:48:30 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_6_opt_parallel
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	1,754 / 113,560 (2 %)
Total registers	1687
Total pins	164 / 616 (27 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	99 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)



	Fmax	Restricted Fmax	Clock Name	Note
1	41.07 MHz	41.07 MHz	clk	

Comparison:

Throughput & resource utilization	Optimized method	Optimized method using pipelining	Optimized method using parallel processing
Fmax(in MHz)	44.52	135.04	41.07
Logic utilization	1757	2074	1754
Total registers	1639	3285	1687
Total pins	68	68	164
Total DSP blocks	100	100	99

Throughput_pipelining = 3.033*Throughput_nonpipelining

Throughput_parallel_processing = 1.084*Throughput_nonpipelining

Genvar method:

Normal FIR filter without any pipelining and parallel processing.

Flow Summary

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Flow Status	Successful - Tue Oct 21 00:57:41 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_genvar
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	880 / 113,560 (< 1 %)
Total registers	1639
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	99 / 342 (29 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	2.54 MHz	2.54 MHz	clk	

Using pipelining in Genvar method:

Flow Summary

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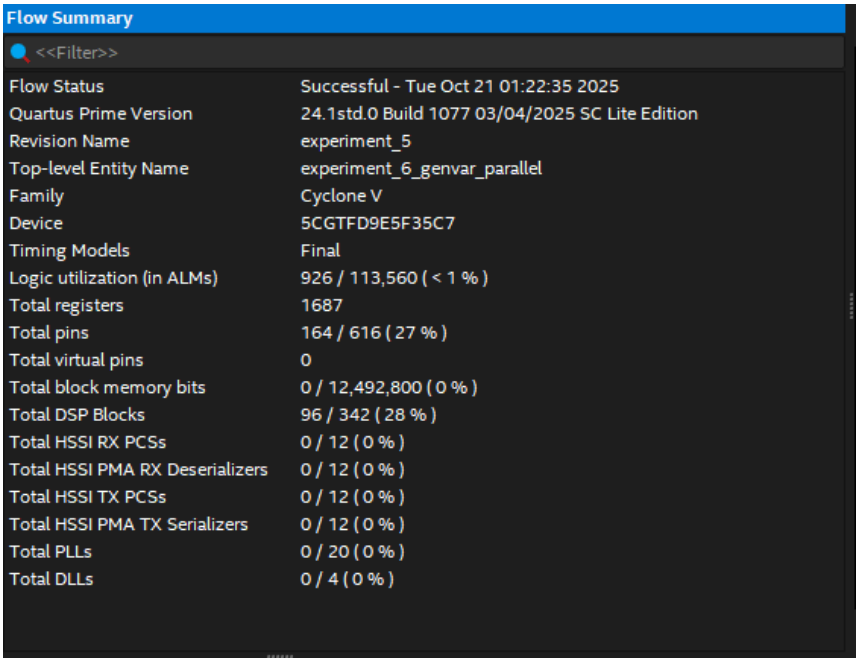
Flow Status	Successful - Tue Oct 21 01:05:19 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_5_genvar_pipelining
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	63 / 113,560 (< 1 %)
Total registers	199
Total pins	68 / 616 (11 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	10 / 342 (3 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	246.55 MHz	246.55 MHz	clk	

Using parallel processing in Genvar method:



Flow Summary

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Flow Status	Successful - Tue Oct 21 01:22:35 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	experiment_5
Top-level Entity Name	experiment_6_genvar_parallel
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	926 / 113,560 (< 1 %)
Total registers	1687
Total pins	164 / 616 (27 %)
Total virtual pins	0
Total block memory bits	0 / 12,492,800 (0 %)
Total DSP Blocks	96 / 342 (28 %)
Total HSSI RX PCSs	0 / 12 (0 %)
Total HSSI PMA RX Deserializers	0 / 12 (0 %)
Total HSSI TX PCSs	0 / 12 (0 %)
Total HSSI PMA TX Serializers	0 / 12 (0 %)
Total PLLs	0 / 20 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name	Note
1	7.86 MHz	7.86 MHz	clk	

Comparison:

Throughput & resource utilization	Genvar method	Genvar method using pipelining	Genvar method using parallel processing
Fmax(in MHz)	2.54	246.55	7.86
Logic utilization	880	63	926
Total registers	1639	199	1687
Total pins	68	68	164
Total DSP blocks	99	10	96

Throughput_pipelining = 97.06*Thoughput_nonpipelining

Throughput_parallel_processing = 3.094*Throughput_nonpipelining