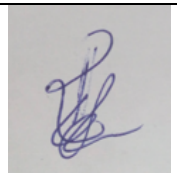
MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL
(A constituent unit of MAHE, Manipal)

Master of Engineering - ME (Big Data Analytics)

Course File

Course Name	:	Advanced Computer Architecture Lab
Course Code	:	ESD 5151
Academic Year	:	2023 - 24
Semester	:	I
Name of the Course Coordinator	:	Ravikala Kamath
Name of the Program Coordinator	:	Dr. Dinesh Rao

	
Signature of Program Coordinator with Date	**Signature of Course Coordinator with Date**

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Program Education Objectives (PEOs)

The overall objectives of the Learning Outcomes-based Curriculum Framework (LOCF) for **ME (Embedded Systems)**, program are as follows.

PEO No.	Education Objective
PEO 1	Enable to draw upon fundamental and advanced knowledge to apply analytical and computational approaches to solve technological problems in embedded systems.
PEO 2	Introduce state of art technologies in the area of embedded systems and inculcate ethical practices to make industry-ready professionals.
PEO 3	Promote scientific and societal advancement through research and entrepreneurship.

Program Outcomes (POs)

By the end of the postgraduate program in **ME (Embedded Systems)**, graduates will be able to:

PO1	Independently carry out research /investigation and development work to solve practical problems.
PO2	Write and present a substantial technical report/document.
PO3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO4	Develop and implement embedded systems requirements based on theoretical principles and practical knowledge.
PO5	Demonstrate knowledge of the underlying principles and evaluation methods for analyzing data for decision-making.

1. Course Plan

1.1 Primary Information

Course Name	**:**	Advanced Computer Architecture Lab [ESD 5151]
L-T-P-C	**:**	0-0-3-1
Contact Hours	**:**	36 Hours
Pre-requisite	**:**	Basic Programming with C
Core/ PE/OE	**:**	Core

1.2 Course Outcomes (COs)

CO	At the end of this course, the student should be able to:	No. of Contact Hours	Program Outcomes (PO's)	BL
CO1	**Implement** the basic gates by understanding the software tools of processors	6	PO3	3
CO2	**Apply** the knowledge for implementing the combinational circuits	6	PO3	3
CO3	**Analyze** the performance of sequential circuits for given problem statements.	6	PO4	4
CO4	**Analyze** the performance of ARM processors architecture by various set of programs	9	PO4	4
CO5	**Evaluate** the performance of different control unit and processors	9	PO5	5

1.3 Assessment Plan

Components	**Lab Test**	**Flexible Assessments (2 – 3 in number)**	**End semester/ Makeup examination**
Duration	90 minutes	To be decided by the faculty.	180 minutes
Weightage	0.3	0.2	0.5
Typology of questions	Applying; Analyzing.	Applying; Analyzing. Evaluating.	Applying; Analyzing; Evaluating.
Pattern	Answer all the questions. Maximum marks 30.	**Assignment : Implentation of combinational and sequential circuits. Implementation and analysing the programs output of processors**. Maximum 20 marks. [To be decided by the faculty members. May be Assignments, Problem solving, etc.]	Answer all the questions. Maximum marks 50.

Schedule	As per academic calendar.	**Assignment submission:** November 2023	As per academic calendar.
Topics covered	Combinational , sequential, assembly and embedded C programs		Comprehensive examination covering the full syllabus.

1.4 Lesson Plan

L. No.	TOPICS	Course Outcome Addressed
L0	Course delivery plan, Course assessment plan, Course outcomes, Program outcomes, CO-PO mapping, reference books	---
Lab1	Basic gates using verilog	CO1

Lab2	Implementing SOP and POS form equations	CO1
Lab3	Analysis of combinational circuits	CO2
Lab4	Implantation of Adder circuit	CO3
Lab5	Analyze the performance of Multiplier circuits	CO4
Lab6	Analyze the performance of divisor circuits	CO4
IT1	Internal lab test	CO1, CO2, CO3,CO4
Lab7	Analyze the performance sequential circuits	CO4
Lab8	Analyze the performance of instructions programs using aasembly languages	CO4
Lab9	Analyze the thumb instructions	CO4
Lab10	Evaluate the performance of processing units of systems	CO5
Lab11	Evaluate the performance of sequential systems	CO5
Lab12	Evaluate the performance of arm processing units with embed c and assembly programs	CO5

1.5 References

1. CV Hamacher, Vranseic and Zaky , “Computer Organization”, Fifth Edition, Tata-MacgrawHill
2. Rafiquzzamann ,“Modern Computer Architecture”,Chandra,Galgotia Publications
3. John L Hennessy and David A Patterson ,“Computer Architecture: A Quantitative approach”, 2nd Edition
4. John L Hennessy and David A Patterson ,“Principles of Computer Architecture”, Prentice Hall
5. Shivarama Danadamudi, “Guide to RISC Processors for Programmers & Engineers”, Springer Publications.
6. “ARM Architecture Reference Manual”, David Seal ,Addison-Wesley,2nd Edition
7. “AMBA Specification”, ARM7TDMI Datasheet.
8. “Computer Organisation and Design”, David A Patterson, John L Hennessy
9. David Seal, "ARM Architecture Reference Manual", 2nd Edition, Addison-Wesley Professional.
10. Steve Furber,"ARM System-on-Chip Architecture",2nd Edition, Addison-Wesley Professional, ISBN-13: 078-5342675191,ISBN-10: 0201675196
11. William Hohl, Christopher Hinds,"ARM Assembly Language: Fundamentals and Techniques",2nd Edition, ISBN-13: 978-1482229851, ISBN-10: 1482229854

1.6 Other Resources (Online, Text, Multimedia, etc.)

1. Web Resources: Blog, Online tools and cloud resources.
2. Journal Articles.

1.7 Course Timetable

1st Semester Embedded Systems				Lab: Embedded System Lab				
	9-10	10-11	11 -12	12-1	1-2	2-3	3-4	4-5
MON								
TUE								
WED								
THU						ACA LAB		
FRI								
SAT								

1.8 Assessment Plan

COs		**Marks & weightage**			
CO No.	CO Name	Lab Test (Max. 30)	Assignment (Max. 20)	End Semester (Max. 50)	CO wise Weightage
CO1	Implement the basic gates by understanding the software tools of processors	0	0	0	**0**
CO2	Apply the knowledge for implementing the combinational circuits	0	5	0	**0.05**
CO3	Analyze the performance of sequential circuits for given problem statements.	20	5	20	**0.45**
CO4	Analyze the performance of ARM processors architecture by various set of programs	20	5	10	**0.35**
CO5	Evaluate the performance of different control unit and processors and programs.	-	5	20	**0.25**
	Marks (weightage)	**0.40**	**0.20**	**0.5**	**1.0**

Note:

- In-semester Assessment is considered as the Internal Assessment (IA) in this course for 50 marks, which includes the performances in lab participation, assignment work, lab work, lab tests, quizzes etc.
- End-semester examination (ESE) for this course is conducted for a maximum of 50.
- End-semester marks for a maximum of 50 and IA marks for a maximum of 50 are added for a maximum of 100 marks to decide upon the grade in this course.

Weightage for CO1 = (Lab Test marks for CO1 + Assignment marks for CO1 + ESE marks for CO1) /100
= (5 + 2 +5)/100 = 0.12

1.9 Assessment Details

The assessment tools to be used for the Current Academic Year (CAY) are as follows:

SI. No.	Tools	Weightage	Frequency	Details of Measurement (Weightage/Rubrics/Duration, etc.)
1	Lab Test	0.3	1	• Performance is measured using lab internal test attainment level. • Reference: question paper and answer scheme. • Lab internal test is assessed for a maximum of 30 marks.
2	Assignments	0.2	1	• Performance is measured using assignments attainment level. • Assignment is evaluated for a maximum of 20 marks.
3	ESE	0.5	1	• Performance is measured using ESE attainment level. • Reference: question paper and answer scheme. • ESE is assessed for a maximum of 50 marks.

1.10 Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5
CO1					
CO2			**Y**		
CO3			**Y**	**Y**	
CO4				**Y**	
CO5					**Y**
Average Articulation Level			*	*	*