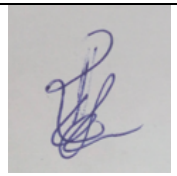
MANIPAL SCHOOL OF INFORMATION SCIENCES
MANIPAL
(A constituent unit of MAHE, Manipal)

Master of Engineering - ME (Embedded Systems)

Course File

Course Name	:	Advanced Computer Architecture
Course Code	:	ESD 5101
Academic Year	:	2023 - 24
Semester	:	I
Name of the Course Coordinator	:	Ravikala Kamath
Name of the Program Coordinator	:	Dr. Dinesh Rao

	
Signature of Program Coordinator with Date	**Signature of Course Coordinator with Date 5.8.23**

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Program Education Objectives (PEOs)

The overall objectives of the Learning Outcomes-based Curriculum Framework (LOCF) for **ME (Embedded Systems)**, program are as follows.

PEO No.	Education Objective
PEO 1	Enable to draw upon fundamental and advanced knowledge to apply analytical and computational approaches to solve technological problems in embedded systems.
PEO 2	Introduce state of art technologies in the area of embedded systems and inculcate ethical practices to make industry-ready professionals.
PEO 3	Promote scientific and societal advancement through research and entrepreneurship.

Program Outcomes (POs)

By the end of the postgraduate program in **ME (Embedded Systems)**, graduates will be able to:

PO1	Independently carry out research /investigation and development work to solve practical problems.
PO2	Write and present a substantial technical report/document.
PO3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO4	Develop and implement embedded systems requirements based on theoretical principles and practical knowledge.
PO5	Demonstrate knowledge of the underlying principles and evaluation methods for analyzing data for decision-making.

1. Course Plan

1.1 Primary Information

Course Name	**:**	Advanced Computer Architecture [ESD 5101]
L-T-P-C	**:**	3-0-0-3
Contact Hours	**:**	36 Hours
Pre-requisite	**:**	Basic Programming with C
Core/ PE/OE	**:**	Core

1.2 Course Outcomes (COs), Program outcomes (POs) and Bloom's Taxonomy Mapping

CO	At the end of this course, the student should be able to:	No. of Contact Hours	Program Outcomes (PO's)	BL
CO1	**Apply** and use the various type of architectures and its classes	5	PO3	3
CO2	**Analyze** and design the various components of processors and developing applications on ARM	9	PO5	4
CO3	**Evaluate and justify the processing section of** control units	9	PO4	5
CO4	**Apply** and understand the pipeline stages of instruction sets	7	PO3	3
CO5	**Analyze** the performance of different parallel computer structures Ensemble methods.	6	PO4	4

1.3 Assessment Plan

Components	Internal Test 1	Internal Test 2	Flexible Assessments (2 – 3 in number)	End semester/ Makeup examination
Duration	90 minutes	90 minutes	To be decided by the faculty.	180 minutes
Weightage	0.2	0.2	0.1	0.5
Typology of questions	Applying; Analyzing.	Applying; Evaluating.	Applying; Analyzing. Evaluating.	Applying; Analyzing; Evaluating.
Pattern	Answer all 5 questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks.	Answer all 5 questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks.	**Assignment:** [To be decided by the faculty. May be Assignments, Problem solving, etc.]	Answer all 10 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks.
Schedule	As per academic calendar.	As per academic calendar.	**Assignment submission:** Decided by faculty	As per academic calendar.

Topics covered	Introduction - ECODING TECHNIUES, INSTRUCTION SET, BUS STRUCTURES ADDERS MULTIPLIERS DIVISORS	TYPES OF REGISTERS DESIGN OF CONTROL UNITS APPLICATIONS OF ARM PROGRAMS	MEMORY CONCEPTS PARALLEL ARCHITECTURES HAZARDS VECTOR PROCESSORS	Comprehensive examination covering the full syllabus. Students are expected to answer all questions.

1.4 Lesson Plan

L. No.	TOPICS	Course Outcome Addressed
L0	Course delivery plan, Course assessment plan, Course outcomes, Program outcomes, CO-PO mapping, reference books	---
L1	Introduction of types of architectures, bus structures and classifications	CO1
L2	Bus structures, classification	CO1
L3	Introduction of ARM processors architectures	CO1
L4	Instruction level register ,general purpose register designs	CO4
L5	Instruction sets, types	CO3
L6	Adders, types of adders logical designs	CO3
L7	Multipliers, designs	CO5
L8	Barrel shifters	CO2
L9	Barrel shift registers	CO2
L10	Sequential multipliers	CO2
L11	Sequential multipliers and design	CO5

L12	ROM based multipliers	CO5
L13	ALU design	CO2
L14	Addressing modes	CO2
IT1	Internal test 1	CO1,CO2,CO3,CO5
L15	Addressing modes	CO3
L16	ARM and THUMB instructions, endianness assembly programming	CO2
L17	Booths algorithms	CO4
L18	Division algorithms	CO3
L19	Control unit	CO5
L20	Hardware approach	CO5
L21	Microprogrammed approach	CO4
L22	Firmware coprocesoor float point numbers	CO3
L23	Memory , types	CO2
L24	Memory hierarchy	CO2
L25	Static and dynamic RAM, ROM, types	CO2
L26	Cache memory perfomaces	CO3
L27	Virtual memoryies	CO2
L28	Introduction to pipeling	CO3
L29	hazards	CO3
L30	Datapath and control considerations	CO3

IT2	Internal test 2	CO3 & CO4
L31	Parallel processing	CO2
L32	Uni and multi processor	CO2
L33	Parallel computer structures, architectures	CO3
L34	Classification schemes of parallel computer structures	CO2
L35	Principle and vector processing	CO2
L36	Structures and algorithms for array processors	CO3

1.5 References

1. CV Hamacher, Vranseic and Zaky , “Computer Organization”, Fifth Edition, Tata-MacgrawHill
2. Rafiquzzamann ,“Modern Computer Architecture”,Chandra,Galgotia Publications
3. John L Hennessy and David A Patterson ,“Computer Architecture: A Quantitative approach”, 2nd Edition
4. John L Hennessy and David A Patterson ,“Principles of Computer Architecture”, Prentice Hall
5. Shivarama Danadamudi, “Guide to RISC Processors for Programmers & Engineers”, Springer Publications.
6. “ARM Architecture Reference Manual”, David Seal ,Addison-Wesley,2nd Edition
7. “AMBA Specification”, ARM7TDMI Datasheet.
8. “Computer Organisation and Design”, David A Patterson, John L Hennessy
9. David Seal, "ARM Architecture Reference Manual", 2nd Edition, Addison-Wesley Professional.
10. Steve Furber,"ARM System-on-Chip Architecture",2nd Edition, Addison-Wesley Professional, ISBN-13: 078-5342675191,ISBN-10: 0201675196
11. William Hohl, Christopher Hinds,"ARM Assembly Language: Fundamentals and Techniques",2nd Edition, ISBN-13: 978-1482229851, ISBN-10: 1482229854
12. Andrew Sloss, Dominic Symes, Chris Wright,"ARM System Developer's Guide: Designing and Optimizing System Software",1st Edition,The Morgan Kaufmann Series in Computer Architecture and Design, ISBN13: 978-1558608740, ISBN-10: 1558608745
13. Websites & Transaction Papers 14.
14. MOOC: https://www.mooc-list.com/course/computer-architecture-coursera

1.6 Other Resources (Online, Text, Multimedia, etc.)

1. Web Resources: Blog, Online tools and cloud resources.
2. Journal Articles.

1.7 Course Timetable

1st Semester Embedded Systems				Room: LG1 LH				
	9-10	10-11	11-12	12-1	1-2	2-3	3-4	4-5
MON							ACA	
TUE								
WED							ACA	
THU						ACA LAB		
FRI							ACA	
SAT								

1.8 Assessment Plan

COs		**Marks & Weightage**				
CO No.	CO Name	IT-1 (Max. 50)	IT-2 (Max. 50)	Assignment (Max. 10)	End Semester (Max. 100)	CO wise Weightage
CO1	**Apply** and use the various type of architectures and its classes	25	-	-	20	**0.2**
CO2	**Analyze** and design the various components of processors and developing applications on ARM	25	-	-	35	**0.275**
CO3	**Evaluate and justify the processing section of** control units	-	25	-	25	**0.225**
CO4	**Apply** and understand the pipeline stages of instruction sets	-	25	-	10	**0.115**
CO5	**Analyze** the performance of different parallel computer structures Ensemble methods.	-	-	10	10	**0.15**
	Marks (weightage)	**0.2**	**0.2**	**0.1**	**0.5**	**1.0**

Note:

- In-semester Assessment is considered as the Internal Assessment (IA) in this course for 50 marks, which includes the performances in class participation, assignment work, class tests, mid-term tests, quizzes etc.
- End-semester examination (ESE) for this course is conducted for a maximum of 100 and the same will be scaled down to 50.
- End-semester marks for a maximum of 50 and IA marks for a maximum of 50 are added for a maximum of 100 marks to decide upon the grade in this course.

Weightage for CO1 = (IT1 marks for CO1 / 2.5 + IT2 marks for CO1 / 2.5 + Assignment marks for CO1 + ESE marks for CO1 / 2)/100
= (25/2.5 + 0 + 0 + 20/ 2)/100 = 0.2

1.9 Assessment Details

The assessment tools to be used for the Current Academic Year (CAY) are as follows:

SI. No.	Tools	Weightage	Frequency	Details of Measurement (Weightage/Rubrics/Duration, etc.)
1	Internal Test	0.4	2	• Performance is measured using internal test attainment level. • Reference: question paper and answer scheme. • Each internal test is assessed for a maximum of 50 marks and scaled down to 40 marks.
2	Assignments	0.1	1	• Performance is measured using assignments/quiz attainment level. • Assignments/quiz are evaluated for a maximum of 10 marks.
3	ESE	0.5	1	• Performance is measured using ESE attainment level. • Reference: question paper and answer scheme. • ESE is assessed for a maximum of 100 marks and scaled down to 50 marks.

1.10 Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5
CO1			**Y**		
CO2				**Y**	
CO3				**Y**	
CO4			**Y**		
CO5					**Y**
Average Articulation Level			*	*	*