Ameba-Z

SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2016/09/01	Change chapter organization Change features Add timer & RTC datasheet Add all peripherals features Update table list Update package and pin description
1.1	2016/09/01	Add exception table

Revision	Release Date	Summary
1.2	2016/09/02	Add package， pin number and dimension information
1.3	2016/10/21	Fix some errors
1.4	2016/11/03	Advanced time just have 2 groups
1.5	2016/11/29	Fix some errors
1.6	2016/12/09	Add ADC pin definations

Table of Contents

List of Tables

List of Figures

1. Product Overview

1.1. General Description

Ameba-Z is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-CM4 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

Ameba-Z integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

1.2. Features

Table 1 Ameba-Z Features

Feature list			*QFN68 RTL8711BG*	*QFN48 RTL8711BN*	*QFN32 RTL8710BN*
Integrated core	Core type		ARM CM4F		
	Core clock maximum freq.		125MHz		
Memory	Internal ROM		512KB		
	Internal SRAM		256KB		
	External FLASH		128MB		
FPU	Float process unit		Yes		
SWD/JTAG			SWD		
Backup register	Backup register for power save		16B		
Boot Reason			Yes		
F/W protection			Yes		
Read protection	RAM read protection		4KB		
WIFI	802.11 B/G/N		Yes		
BOR	BOR Detection		Yes		
peripherals	UART	Normal-UART	2	2	1
		Log-UART	1	1	1
	SPI Master	Max. 31.25Mbps	1	1	1
	SPI Slave	Max. 31.25Mbps	1	1	1
	I2C	Max. 400Kbps	2	2	2
	ADC	VBAT	1	0	1
		Thermal	1	1	1

		Normal	2	2	0
	GDMA	2*6 channels	2	2	2
	GPIO	IN/OUT/INT	39	26	17
	I2S		1	1	0
	RTC	D/H/M/S	1	1	1
		OUTPUT	1	1	1
	Timer	Basic timer use 32K	4	4	4
		Advanced timer use XTAL	2	2	2
	PWM	OUTPUT	6	6	6
		INPUT Capture	2	2	2
	WDG		1	1	1
	USB device		1	0	0
	SDIO 2.0 Device		1	1	1
External 32K	External 32K		1	1	1
Dsleep Wakepin	Deep sleep wake pin		4	4	4
Package	trays and tape-in-reel		(8x8mm^2)	(6x6mm^2)	(5x5mm^2)
Part Number			RTL8711BG	RTL8711BN	RTL8710BN

1.3. Package Types and Pin Descriptions

1.3.1. QFN32

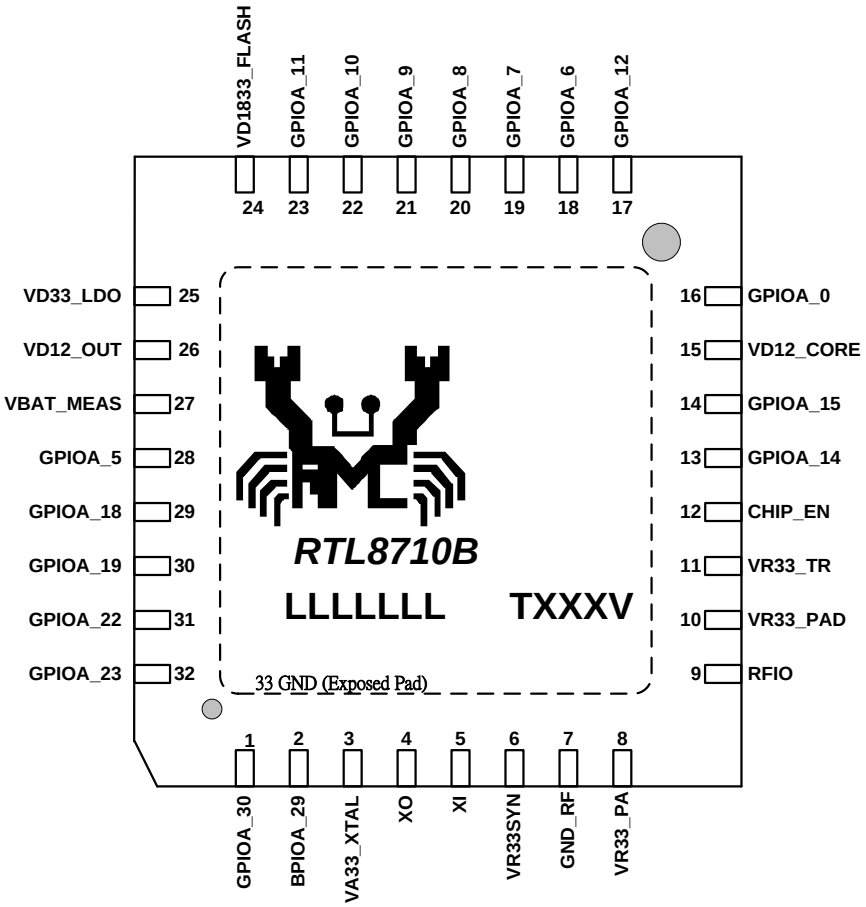

Figure 1 QFN32 Pin Assignments

1.3.2. QFN48

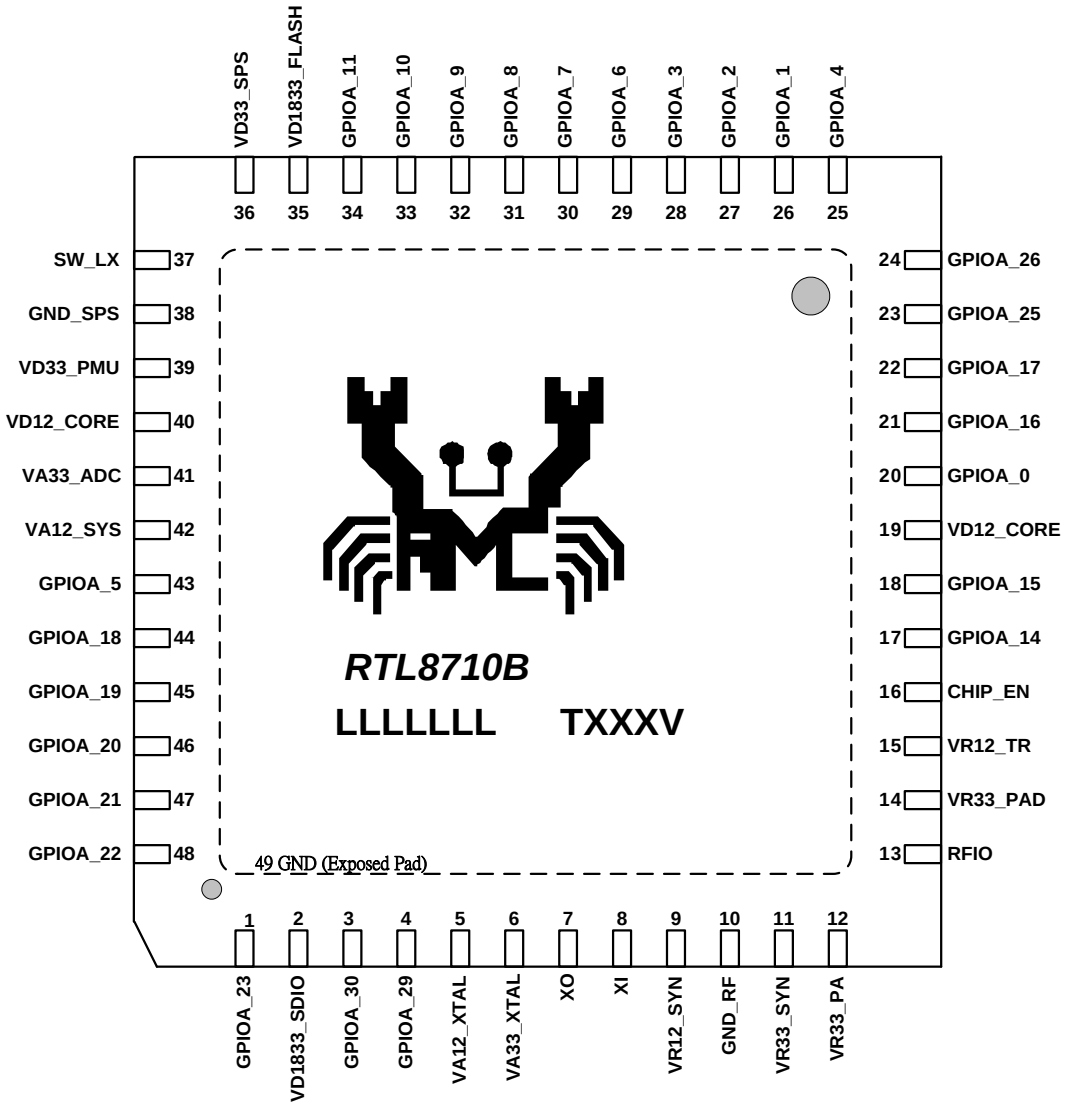

Figure 2 QFN48 Pin Assignments

1.3.3. QFN68

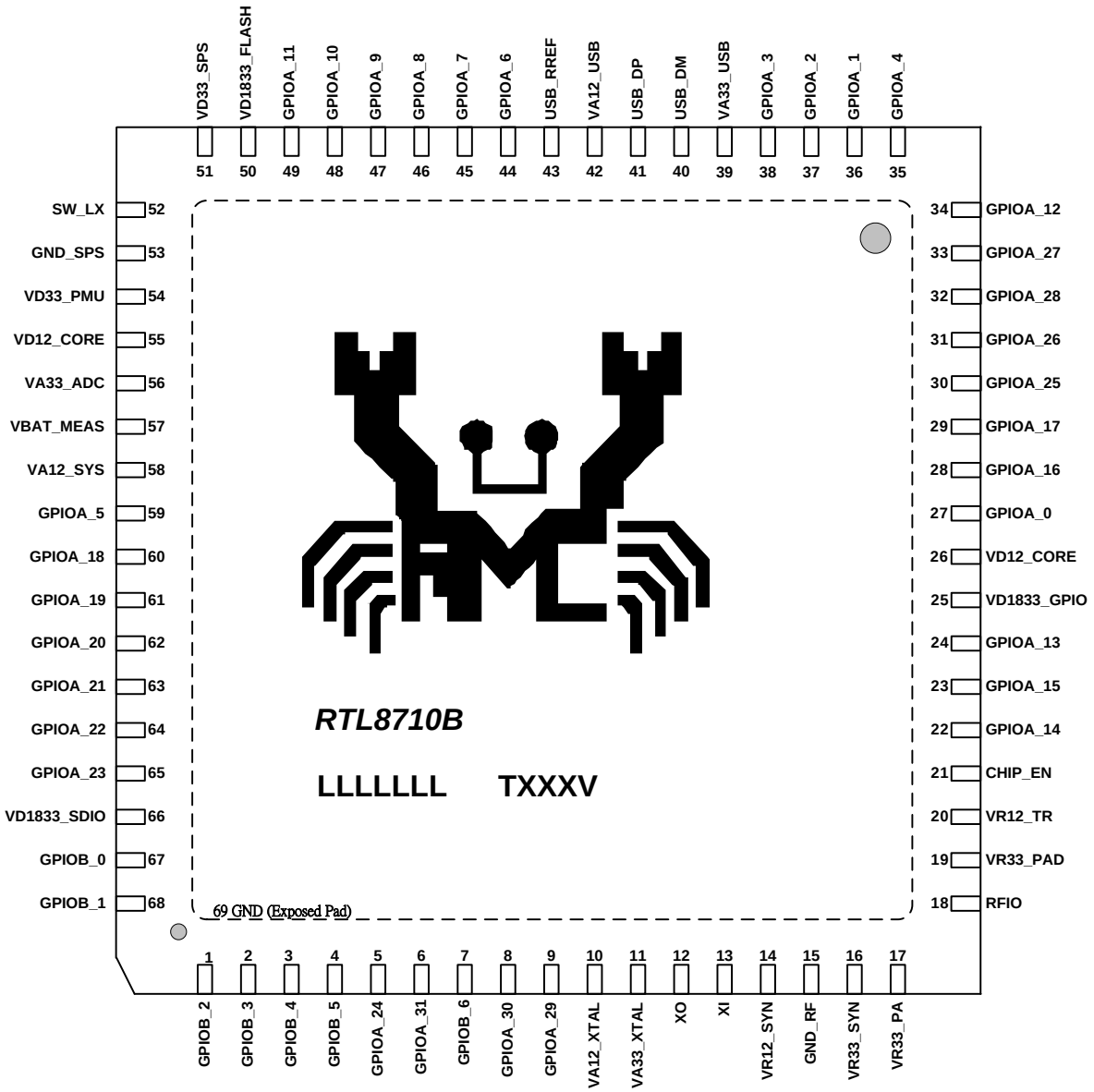

Figure 3 QFN68 Pin Assignments

1.3.4. Pin Descriptions

The following signal type codes are used in the tables:

Table 2 Pin Description

I:	*Input*	*O:*	*Output*
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

1.3.4.1 Power On Trap Pin

Table 3 Power On Trap Pins

Symbol	*Type*	*QFN68*	*QFN48*	*QFN32*	*Description*
TEST_MODE_SEL	I	27	20	16	Shared with GPIOA_0 1: Enter into test/debug mode 0: Normal operation mode
UART_DOWNLOAD	I	8	3	1	Shared with GPIOA_30 1: Boot from flash 0: Download image from UART
SPS_LDO_SEL	I	38	28	NA	Shared with GPIOA_3 1: Boot from flash 0: Download image from UART

1.3.4.2 RF pin

Table 4 RF pin

Symbol	Type	QFN68	QFN48	QFN32	Description
RF_IO	IO	18	13	9	WL RF signal

1.3.4.3 CHIP EN

Table 5 CHIP EN

Symbol	Type	QFN68	QFN48	QFN32	Description
CHIP_EN	I	21	16	12	Enable chip. 1: enable chip; 0: shutdown chip

1.3.4.4 Power Pins

Table 6 Power Pins

Symbol	Type	QFN68	QFN48	QFN32	Description
VA33_XTAL	P	11	6	3	3.3V for Crystal Oscillator
VA12_XTAL	P	10	5	NA	1.2V for Crystal Oscillator
VR33_SYN	P	16	11	6	3.3V for RF Synthesizer
VR12_SYN	P	14	9	NA	1.2V for RF Synthesizer
VR33_PA	P	17	12	8	3.3V for RF Power amplifier
VR33_PAD	P	19	14	10	3.3V for RF
VR33_TR	P	NA	NA	11	3.3V for RF
VR12_TR	P	20	15	NA	1.2V for RF
VD12_CORE	P	26	19	15	1.2V for digital core power
VD1833_FLASH	P	50	35	24	3.3V/1.8V for Flash IO power
VD33_LDO	P	NA	NA	25	Linear Regulator input from 3.3V to 1.2V
VD33_SPS	P	51	36	NA	Switching/Linear Regulator input from 3.3V to

					1.2V
VD12_OUT	P	NA	NA	26	1.2V output from Linear Regulator
SW_LX	P	52	37	NA	1.2V output from Switching/Linear Regulator
GND_SPS	P	53	38	NA	Ground for Switching/Linear Regulator
VA33_USB	P	39	NA	NA	3.3V power for USB Analog
VA12_USB	P	42	NA	NA	1.2V power for USB Analog

1.3.4.5 XTAL Pins

Table 7 XTAL Pins

Symbol	*Type*	*QFN68*	*QFN48*	*QFN32*	*Description*
XI	I	13	8	5	40MHz OSC Input Input of 40MHz Crystal Clock Reference
XO	O	12	7	4	Output of 40MHz Crystal Clock Reference

1.3.4.6 ADC Pins

Table 8 ADC Pins

Symbol	*Type*	*QFN68*	*QFN48*	*QFN32*	*Description*
ADC_1	I	61	45	NA	ADC input pin, 3.3V tolerance
VBAT_MEAS	I	57	NA	27	ADC input pin, 5V tolerance
ADC_3	I	62	46	NA	ADC input pin, 3.3V tolerance

1.3.4.7 USB Pins

Table 9 USB Pins

Symbol	*Type*	*QFN68*	*QFN48*	*QFN32*	*Description*

USB_DP	I/O	41	NA	NA	USB differential bus
USB_DM	I/O	40	NA	NA	USB differential bus
USB_RREF	I	43	NA	NA	External reference resistor for USB Analog, 1% accuracy

1.3.4.8 GPIO Pins

Table 10 Ameba-Z GPIO

Symbol	Type	QFN68	QFN48	QFN32	Description
GPIOA_14	I/O	22	17	13	PWM0
					SWD_CLK
GPIOA_15	I/O	23	18	14	PWM1
					SWD_DATA
GPIOA_13	I/O	24	NA	NA	PWM4
GPIOA_0	I/O	27	20	16	PWM2
					EXT_32K
					WL_LED
GPIOA_16	I/O	28	21	NA	UART2_Log_RXD
					PWM1
					RTC_OUT
GPIOA_17	I/O	29	22	NA	UART2_Log_TXD
					PWM2
GPIOA_25	I/O	30	23	NA	UART1_RXD
GPIOA_26	I/O	31	24	NA	UART1_TXD
GPIOA_28	I/O	32	NA	NA	I2C1_ SCL
GPIOA_27	I/O	33	NA	NA	I2C1_ SDA
GPIOA_12	I/O	34	NA	17	PWM3
GPIOA_4	I/O	35	25	NA	UART0_TXD
					SPI1_MOSI
					SPI0_MOSI

					I2C0_SDA
GPIOA_1	I/O	36	26	NA	UART0_RXD
					SPI1_CLK
					SPI0_SCK
					I2C0_SCL
GPIOA_2	I/O	37	27	NA	UART0_CTS
					SPI1_CS
					SPI0_CS
					I2C1_SDA
GPIOA_3	I/O	38	28	NA	UART0_RTS
					SPI1_MISO SPS_LDO_SEL
					SPI0_MISO
					I2C1_SCL
GPIOA_6	I/O	44	29	18	SPIC_CS
					SD_D2
GPIOA_7	I/O	45	30	19	SPIC_DATA1
					SD_D3
GPIOA_8	I/O	46	31	20	SPIC_DATA2
					SD_CMD
GPIOA_9	I/O	47	32	21	SPIC_DATA0
					SD_CLK
GPIOA_10	I/O	48	33	22	SPIC_CLK
					SD_D0
GPIOA_11	I/O	49	34	23	SPIC_DATA3
					SD_D1

GPIOA_5	I/O	59	43	28	SDIO_SIDEBAND_INT
					PWM4
GPIOA_18	I/O	60	44	29	UART0_RXD
					SPI1_CLK
					SPI0_SCK
					I2C1_SCL
					SD_D2
					TIMER4_TRIG
					I2S_MCK
GPIOA_19	I/O	61	45	30	UART0_CTS
					SPI1_CS
					SPI0_CS
					I2C0_SDA
					SD_D3
					TIMER5_TRIG
					I2S_SD_TX
GPIOA_20	I/O	62	46	NA	SD_CMD
					I2S_SD_RX
GPIOA_21	I/O	63	47	NA	SD_CLK
					PWM3
					I2S_CLK
GPIOA_22	I/O	64	48	31	UART0_RTS
					SPI1_MISO
					SPI0_MISO
					I2C0_SCL

					SD_D0
					PWM5
					I2S_WS
GPIOA_23	I/O	64	1	32	UART0_TXD
					SPI1_MOSI
					SPI0_MOSI
					I2C1_SDA
					SD_D1
					PWM0
GPIOB_1	I/O	68	NA	NA	SPI1_CLK
					SPI0_SCK
GPIOB_0	I/O	67	NA	NA	SPI1_CS
					SPI0_CS
GPIOB_2	I/O	1	NA	NA	SPI1_MISO
					SPI0_MISO
GPIOB_3	I/O	2	NA	NA	SPI1_MOSI
					SPI0_MOSI
GPIOB_4	I/O	3	NA	NA	SWD_CLK
					I2S_MCK
GPIOB_5	I/O	4	NA	NA	SWD_DATA
					I2S_SD_TX
GPIOA_24	I/O	5	NA	NA	I2S_SD_RX
GPIOA_31	I/O	6	NA	NA	I2S_CLK
GPIOB_6	I/O	7	NA	NA	I2S_WS
GPIOA_30	I/O	8	3	1	UART2_Log_TXD

					I2C0_SDA
					PWM3
					RTC_OUT
GPIOA_29	I/O	9	4	2	UART2_Log_RXD
					I2C0_SCL
					PWM4

2. Block Diagram

2.1. Functional Block Diagram

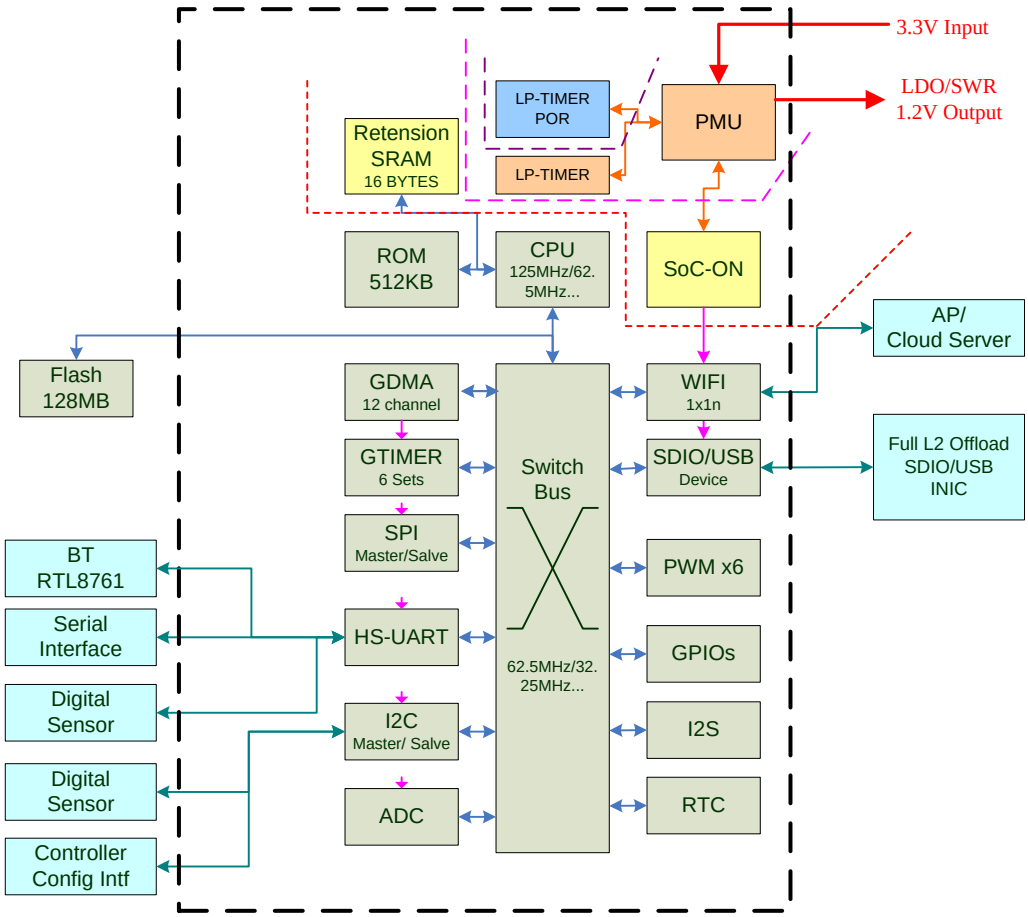

Figure 4 Block Diagram

2.2. WIFI Application Diagram

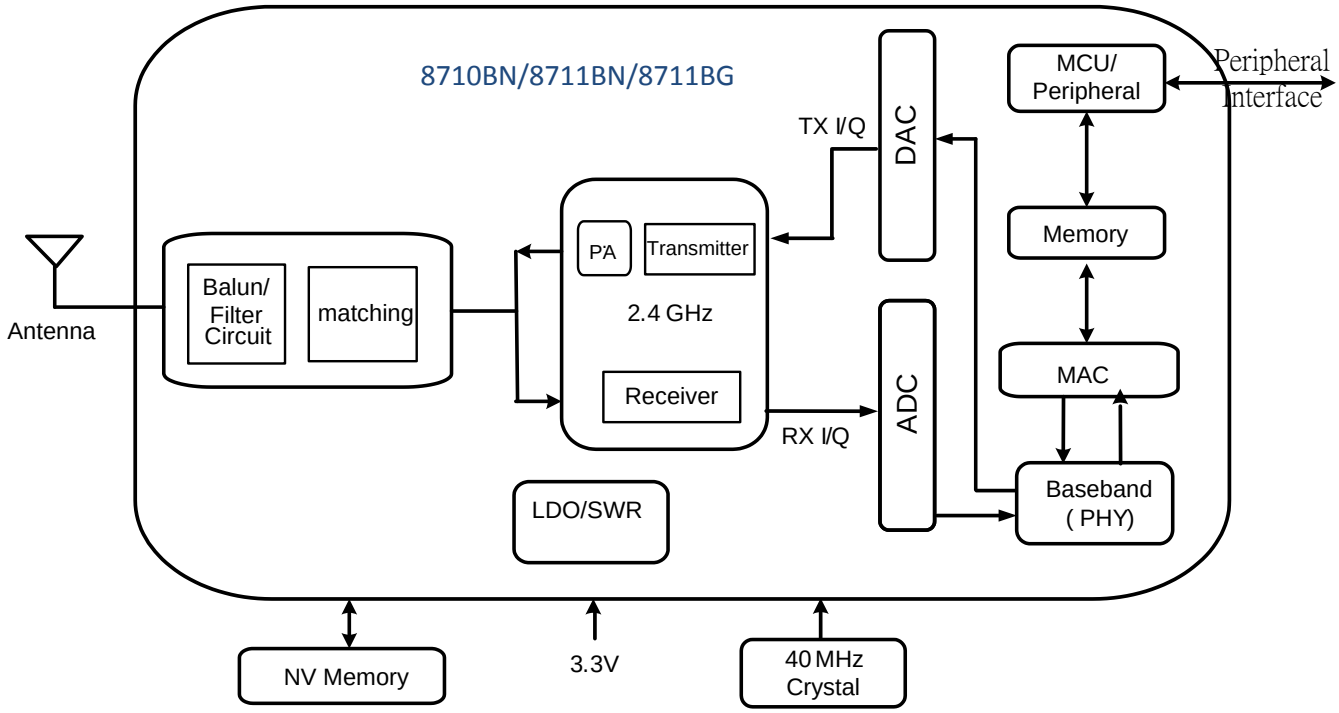

Figure 5 Single-Band 11n (1x1) Solution

2.3. Power Supply Application Diagram

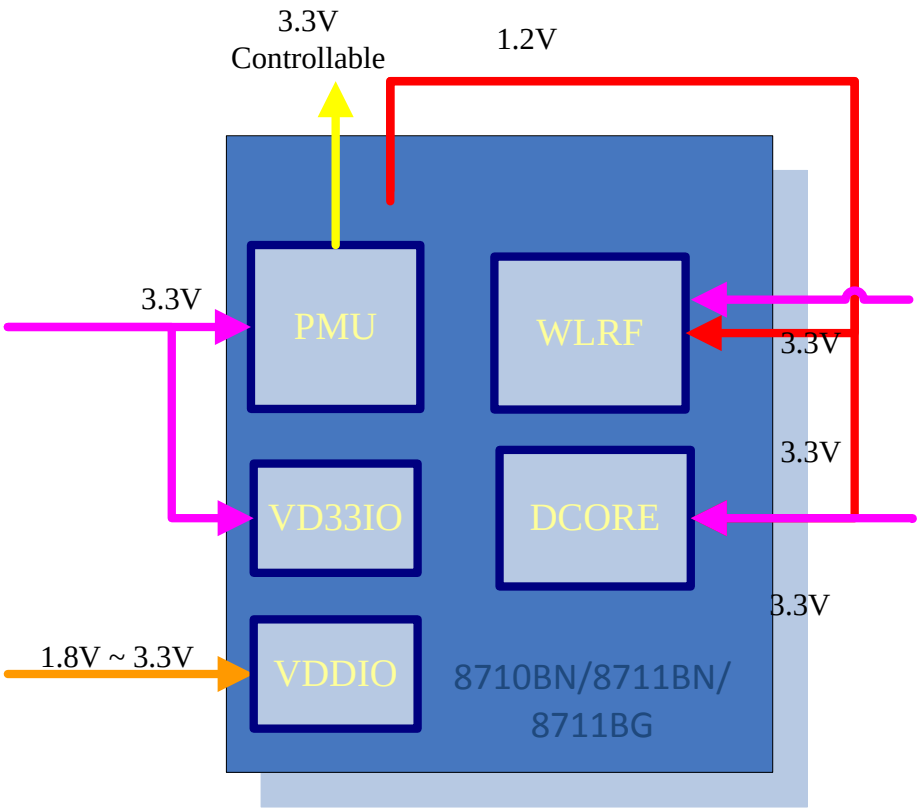

Figure 6 Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V LDO/SWR(Switching Regulator)
- 3.3V power source integrated power cut controlled by FW.

3. Memory organization

3.1. Introduction

Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

Ameba-Z integrates ROM, internal SRAM, NOR flash controller to provide applications with a variety of memory requirements.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

All the memory areas that are not allocated to on-chip memories and peripherals are considered "Reserved". For the detailed mapping of available memory and register areas, please refer to the Memory map and register boundary addresses chapter and peripheral chapters.

3.2. Memory map and register boundary addresses

Table 11 Ameba-Z memory map

Name	*Physical address*	*size*	*IP function*
ROM	0x0000_0000~0x0007_FFFF	512KB	Internal ROM memory
SRAM	0x1000_0000~0x1001_FFFF	256KB	Internal SRAM memory
FLASH	0x0800_0000~0x0FFF_FFFF	128MB	External Flash memory
SYSON	0x4000_0000~0x4000_0FFF	4KB	SYS Control
GPIO	0x4000_1000~0x4000_17FF	2KB	GPIO Control
Timer	0x4000_2000~0x4000_2FFF	4KB	Timer Control
LOGUART	0x4000_3000~0x4000_33FF	1KB	UART for Log
RTC	0x4000_3400~0x4000_37FF	1KB	RTC control
Cache	0x4000_3C00~0x4000_4FFF	1KB	Flash cache control
ADC	0x4001_0000~0x4001_0FFF	4KB	ADC control
SPIC	0x4002_0000~0x4002_0FFF	4KB	SPI flash controller

UART0	0x4004_0000~0x4004_03FF	1KB	UART0 control
UART1	0x4004_0400~0x4004_07FF	1KB	UART1 control
SPI0	0x4004_2000~0x4004_23FF	1KB	SPI0 control
SPI1	0x4004_2400~0x4004_27FF	1KB	SPI1 control
I2C0	0x4004_4000~0x4004_43FF	1KB	I2C0 control
I2C1	0x4004_4400~0x4004_47FF	1KB	I2C1 control
SDIO	0x4005_0000~0x4005_3FFF	16KB	SDIO device control
GDMA0	0x4006_0000~0x4006_07FF	2KB	GDMA0 control
GDMA1	0x4006_1000~0x4006_17FF	2KB	GDMA1 control
I2S	0x4006_2000~0x4006_23FF	1KB	I2S control
IPSEC	0x4007_0000~0x4007_3FFF	16KB	Security control
WIFI	0x4008_0000~0x400B_FFFF	256KB	WIFI register
USB SIE	0x400C_0000~0x400C_0FFF	4KB	USB SIE control
USOC	0x400C_2000~0x400C_2FFF	4KB	USB device register

3.3. Internal ROM

512KB ROM is integrated to provide high access speed, low leakage memory. The ROM memory clock speed is up to 125MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

3.4. Internal SRAM

256KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 125MHz.

3.5. External SPI NOR Flash

3.5.1. Features

- SPI baud rate:
  - 100/83/71/62/50MHz …
- Execute in place (XIP):
  - we supports a memory-mapped I/O interface for read operation
  - Support 32K I/D read cache, 2-way associative
  - Support decryption on the fly
- SPI mode:
  - SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI
- Flash size
  - Support up to 128MB flash size

3.5.2. Supported NOR Flash List

Table 12 Flash supported

Vendor	*Part Number*	*Density*	*Voltage*	*IO*
MXIC	MX25L1633E	2MB	3.3V	4IO
MXIC	MX25L3236F	4MB	3.3V	4IO
MXIC	MX25L6433F	8MB	3.3V	4IO
MXIC	MX25L12845G	16MB	3.3V	4IO
Winbond	W25Q80DV	1MB	3.3V	4IO
Winbond	W25Q16DV	2MB	3.3V	4IO
Winbond	W25Q32FV	4MB	3.3V	4IO
Winbond	W25R64FV	8MB	3.3V	4IO
Winbond	W25R128FV	16MB	3.3V	4IO
Micron	N25Q032A13ESE40E	4MB	3.3V	4IO
Micron	N25Q064A13ESED0E	8MB	3.3V	4IO

Micron	N25Q128A	16MB	3.3V	4IO
Micron	N25Q00AA13GSF40F	128MB	3.3V	4IO
Gigadevice	GD25Q80C	1MB	3.3V	4IO
Gigadevice	GD25Q16C	2MB	3.3V	4IO
Gigadevice	GD25Q32C	4MB	3.3V	4IO
Gigadevice	GD25Q64C	8MB	3.3V	4IO
Gigadevice	GD25Q128C	16MB	3.3V	4IO

3.5.3. Electrical Specifications

Table 13 Flash Bus DC Parameters

Symbol	*Parameter*	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*	*Notes*
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: VIH (MAX)=VDDH + 2V for a pulse width ≤3ns.

Note 2: V_{IL} undershoot: $V_{IL\,(MIN)}$=-2V for a pulse width ≤3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

4. Exception table

Table 14 Exception table

Exception Number	Exception Type	Description
	Reset	Reset
	NMI	Nonmaskable interrupt (external NMI input). The WDG is linked to the NMI vector
	Hard Fault	All fault conditions if the corresponding fault handler is not enabled
	MemManager Fault	Memory management fault; Memory Protection Unit (MPU) violation or access to illegal locations
	Bus Fault	Bus error; occurs when Advanced High-Performance Bus (AHB) interface receives an error response from a bus slave (also called prefetch abort if it is an instruction fetch or data abort if it is a data access)
	Usage Fault	Exceptions resulting from program error or trying to access coprocessor (the Cortex-M3 does not support a coprocessor)
	RSVD	-
	SVC	Supervisor Call
	Debug Monitor	Debug monitor (breakpoints, watchpoints, or external debug requests)
	RSVD	-
	PendSV	Pendable Service Call
	SYSTICK	System Tick Timer
[0]	System_ISR	
[1]	WDG	Watch dog global insterrupt
[2]	Timer0	Timer0 global interrupt
[3]	Timer1	Timer1 global interrupt
[4]	Timer2	Timer2 global interrupt

[5]	Timer3	Timer3 global interrupt
[6]	SPI0	SPI0 global interrupt for communication spi
[7]	GPIO	GPIO portA global interrupt
[8]	UART0	UART0 global interrupt
[9]	SPI_FLASH	SPI Flash global interrupt
[10]	UART1	UART1 global interrupt
[11]	Timer4	Timer4 global interrupt
[12]	SDIO_Dev	SDIO device global interrupt
[13]	I2S0	I2S0 global interrupt
[14]	Timer5	Timer5 global interrupt
[15]	WL_DMA	Wlan Host global interrupt
[16]	WL_PROTOCOL	Wlan Firmware Wlan global interrupt
[17]	CRYPTO	IPsec global interrupt
[18]	SPI1	SPI1 global interrupt for communication spi
[19]	Peripheral_ISR	See Below Table
[20]	GDMA0_Channel0	GDMA0 channel 0 global interrupt
[21]	GDMA0_Channel1	GDMA0 channel 1 global interrupt
[22]	GDMA0_Channel2	GDMA0 channel 2 global interrupt
[23]	GDMA0_Channel3	GDMA0 channel 3 global interrupt
[24]	GDMA0_Channel4	GDMA0 channel 4 global interrupt
[25]	GDMA0_Channel5	GDMA0 channel 5 global interrupt
[26]	I2C0	I2C0 global interrupt
[27]	I2C1	I2C1 global interrupt
[28]	uart log	log uart intr
[29]	adc	adc intr
[30]	rdp_int	cpu rdp protection int
[31]	rtc_int	rtc timer int
[32]	GDMA1_CHANNEL0_IRQ	GDMA1 channel 0 global interrupt
[33]	GDMA1_CHANNEL1_IRQ	GDMA1 channel 1 global interrupt

[34]	GDMA1_CHANNEL2_IRQ	GDMA1 channel 2 global interrupt
[35]	GDMA1_CHANNEL3_IRQ	GDMA1 channel 3 global interrupt
[36]	GDMA1_CHANNEL4_IRQ	GDMA1 channel 4 global interrupt
[37]	GDMA1_CHANNEL5_IRQ	GDMA1 channel 5 global interrupt
[38]	USB_IRQ	USOC interrupt
[39]	RXI300_IRQ	
[40]	USB_SIE	USB SIE interrupt

5. Pinmux Alternate Functions

Table 15 Pinmux Alternate Function mapping

QFN68	QFN48	QFN32	GPIO	UART	SPI Master	SPI Slave	SPI Flash	I2C	SDIO	PWM/TIMER	EXT32K	I2S	Others
✔	✔	✔	PA_14							PWM0	SWD_CLK		
✔	✔	✔	PA_15							PWM1	SWD_DATA		
✔			PA_13							PWM4			
✔	✔	✔	PA_0							PWM2	ext_32K		
✔	✔		PA_16	UART2_log_RXD						PWM1	RTC_OUT		
✔	✔		PA_17	UART2_log_TXD						PWM2			
✔	✔		PA_25	UART1_RXD									
✔	✔		PA_26	UART1_TXD									
✔			PA_28					I2C1_SCL					
✔			PA_27					I2C1_SDA					
✔		✔	PA_12							PWM3			
✔	✔		PA_4	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C0_SDA					
✔	✔		PA_1	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C0_SCL					
✔	✔		PA_2	UART0_CTS	SPI1_CS	SPI0_CS		I2C1_SDA					
✔	✔		PA_3	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C1_SCL					
✔	✔	✔	PA_6				SPIC_CS		SD_D2				
✔	✔	✔	PA_7				SPIC_DATA1		SD_D3				
✔	✔	✔	PA_8				SPIC_DATA2		SD_CMD				
✔	✔	✔	PA_9				SPIC_DATA0		SD_CLK				
✔	✔	✔	PA_10				SPIC_CLK		SD_D0				
✔	✔	✔	PA_11				SPIC_DATA3		SD_D1				
✔	✔	✔	PA_5						SDIO_SIDEBAND_INT	PWM4			WAKEUP_1
✔	✔	✔	PA_18	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C1_SCL	SD_D2	TIMER4_TRIG		I2S_MCK	WAKEUP_0
✔	✔	✔	PA_19	UART0_CTS	SPI1_CS	SPI0_CS		I2C0_SDA	SD_D3	TIMER5_TRIG		I2S_SD_TX	ADC1
✔	✔		PA_20						SD_CMD			I2S_SD_RX	ADC3

✔	✔		PA_21						SD_CLK	PWM3		I2S_CLK	
✔	✔	✔	PA_22	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C0_SCL	SD_D0	PWM5		I2S_WS	WAKEUP_2
✔	✔	✔	PA_23	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C1_SDA	SD_D1	PWM0			WAKEUP_3
✔			PB_1		SPI1_CLK	SPI0_SCK							
✔			PB_0		SPI1_CS	SPI0_CS							
✔			PB_2		SPI1_MISO	SPI0_MISO							
✔			PB_3		SPI1_MOSI	SPI0_MOSI							
✔			PB_4								SWD_CLK	I2S_MCK	
✔			PB_5								SWD_DATA	I2S_SD_TX	
✔			PA_24									I2S_SD_RX	
✔			PA_31									I2S_CLK	
✔			PB_6									I2S_WS	
✔	✔	✔	PA_30	UART2_log_TXD				I2C0_SDA		PWM3	RTC_OUT		
✔	✔	✔	PA_29	UART2_log_RXD				I2C0_SCL		PWM4			

6. PMU

6.1. Features

The PMU provides the following functions:

- LDO to output 1.2V
- 2 very Low power clock source with less accuracy: 8M and 4M
- Wakeup system detector to resume from low power state

6.2. Power Mode and Power Consumption

Table 16 Power Mode Brief Summary and Typical Power Consumption and Resume Time

Power Mode	*Power Consumption*		
	Typical	**Maximum**	**Units**
Deep Sleep Mode	7	7	uA
Deep Standby Mode	70	70	uA
Sleep Power Gate	120	120	uA
Sleep Clock Gate	350	350	uA

6.3. Shutdown Mode

- CHIP_EN deasserts to shutdown whole chip without external power cut components required.

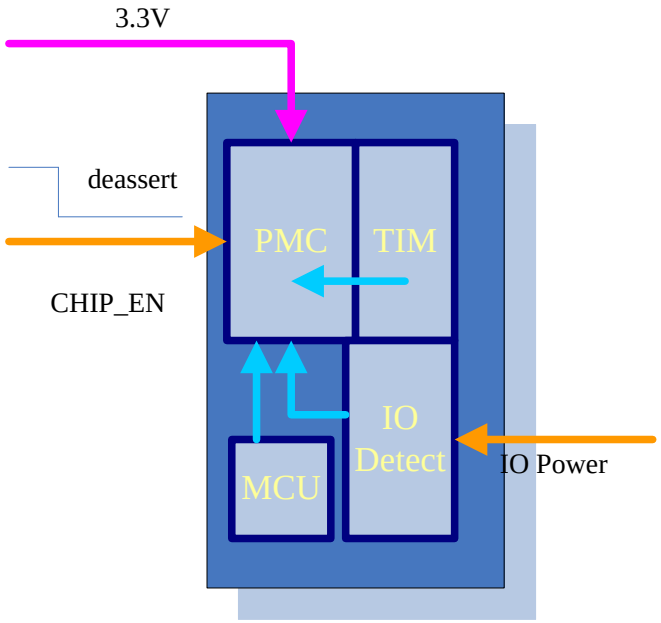

Figure 7 Shutdown Mode

6.4. Deep Sleep Mode

- CHIP_EN keeps high. Enter into Deep Sleep mode by API.

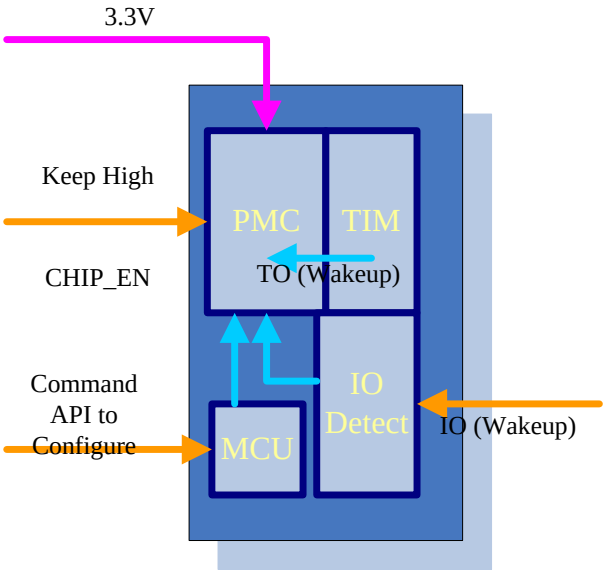

Figure 8 Deep Sleep Mode

6.4.1. Power Domain

Table 17 Deep Sleep Mode Power Domain

Functions	*Power State*	*Comment*
cortex-M4 core	OFF	
system clock	OFF	
SRAM	OFF	
Regulator	OFF	
Peripherals	OFF	
Backup register	OFF	
RTC	OFF	
low precision timer	ON	1
Dsleep wake pin	ON	4

6.4.2. Wakeup Source

Table 18 Deep Sleep Wakeup Source

Wakeup source	*Wakeup*	*Comment*
low precision timer	YES	
Dsleep Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23

6.5. Deep Standby Mode

- CHIP_EN keeps high. Entering into Deep Sleep mode by API.

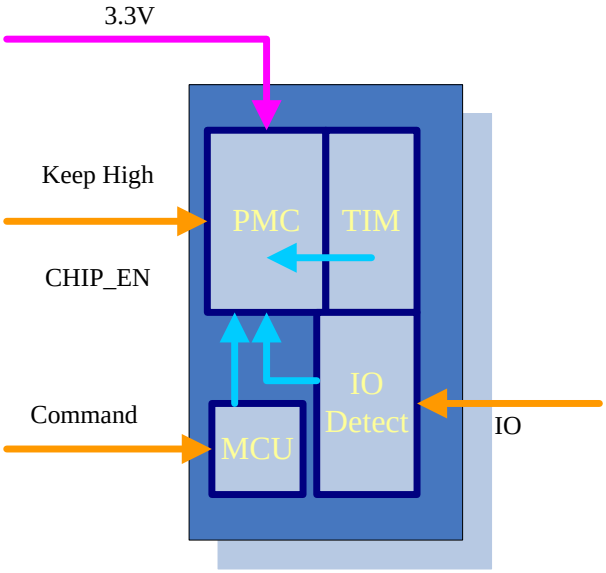

Figure 9 Deep Standby Mode

6.5.1. Power Domain

Table 19 Deep Standby Power Domain

functions	*Power State*	*comment*
cortex-M4 core	OFF	
system clock	OFF	
SRAM	OFF	
Regulator	OFF	
Peripherals	OFF	
Backup register	ON	16B
RTC	ON	
System timer	ON	1
low precision timer	ON	1
wake pin	ON	4

6.5.2. Wakeup Source

Table 20 Deep Standby Wakeup Source

Wakeup source	*Wakeup*	*Comment*
Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
RTC	YES	
System timer	YES	
low precision timer	YES	

6.6. Sleep Power Gate

6.6.1. Power Domain

Sleep mode turn off power domain including cortex-M4 core, and system clock. System is not required to restart after wakeup.

6.6.2. Wakeup source

Table 21 Sleep Power Gate Wakeup Source

Wakeup source	*Wakeup*	*comment*
GPIO interrupt	YES	High/Low active
general purpose timer	YES	
wlan	YES	
ADC	YES	
UART	YES	

I2C	YES	
SDIO/GSPI	YES	
USB	YES	
Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
RTC	YES	
System timer	YES	
low precision timer	YES	

6.7. Sleep Clock Gate

6.7.1. Power Domain

Sleep mode turn off system clock. System is not required to restart after wakeup.

6.7.2. Wakeup source

Table 22 Sleep Clock Gate Wakeup Source

Wakeup source	*Wakeup*	*comment*
GPIO interrupt	YES	High/Low active
general purpose timer	YES	
wlan	YES	
ADC	YES	
UART	YES	
I2C	YES	

SDIO/GSPI	YES	
USB	YES	
Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
RTC	YES	
System timer	YES	
low precision timer	YES	

7. Firmware Protection

7.1. RAM Read Protection

- Top 4k RAM cannot be read.
- RDP Interrupt will happen when invalid access happen.
- RDP image should be encrypted use RDP KEY,
- RDP image can only be decrypted and load to RDP RAM use IPSEC.
- KEY
  - 16B RDP key should be written to EFUSE RDP key area
  - Hidden EFUSE 0xB0~0xBF
  - Cannot read back again. (HW protect)
  - Auto-load to IPSEC when boot.
- Enable
  - Hidden EFUSE 0xC0[0].
  - Cannot be closed after open.

8. WIFI

8.1. General

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

8.2. Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol

8.3. WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility

- Power saving mechanism

8.4. WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 640QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)

9. Basic timer

9.1. Introduction

The basic timers TIM0/TIM1/TIM2/TIM3 consist of a 32-bit auto-reload counter without prescaler.

They may be used as generic timers for time-base generation.

9.2. Features

Table 23 Basic timer features

Name	*TIM0/1/2/3*
channels	1
clock source	32k
resolution	32bit
prescaler	8bit
counter mode	Up
one pulse mode	-
PWM mode with polarity selection	-
statistic pulse width	-
statistic pulse number	-
interrupt generation	●
DMA generation	-
input pin	-
output pin	-

10. Capture timer

10.1. Introduction

The Capture timer (TIM4) consists of a 16-bit auto-reload counter driven by a 8-bit programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths or numbers of input signals.

10.2. Features

Table 24 Capture timer features

Name	*TIM4*
channels	1
clock source	XTAL
resolution	16bit
prescaler	8bit
counter mode	Up
one pulse mode	-
PWM mode with polarity selection	-
statistic pulse width	●
statistic pulse number	●
interrupt generation	●
DMA generation	●
input pin	1 input capture
output pin	-

11. PWM timer

11.1. Introduction

The PWM timer (TIM5) consists of a 16-bit auto-reload counter driven by a 8-bit programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler.

11.2. Features

Table 25 PWM timer features

Name	*TIM5*
channels	6
clock source	XTAL
resolution	16bit
prescaler	8bit
counter mode	Up
one pulse mode	●
PWM mode with polarity selection	●
statistic pulse width	-
statistic pulse number	-
interrupt generation	●
DMA generation	●
input pin	1 input capture
output pin	6 PWM out

11.3. Function description

11.3.1. PWM mode

Pulse Width Modulation mode allows you to generate a signal with a frequency determined by the value of the TIMx_ARR register and a duty cycle determined by the value of the CCRx field of TIMx_CCRx register.

Period: $= (\mathrm{ARR} + 1) * T_{CNT}$

Duty cycle: $D_{PWM} = \frac{(\mathrm{CCRx}+1) * T_{CNT}}{T_{PWM}}$

Where $T_{CNT} = T_{\mathrm{XTAL}} * (\mathrm{PSC} + 1)$

The PWM mode can be selected independently on each channel (one PWM per OCx output) by setting '0' in the OCxM bits in the TIMx_CCRx register. You must enable the corresponding preload register by setting the OCxPE bit in the TIMx_CCRx register, and eventually the auto-reload preload register by setting the ARPE bit in the TIMx_CR register.

As the preload registers are transferred to the shadow registers only when an update event occurs, before starting the counter, you have to initialize all the registers by setting the UG bit in the TIMx_EGR register.

OCx polarity is software programmable using the CCxP bit in the TIMx_CCRx register. It can be programmed as active high or active low.

In PWM mode, TIMx_CNT and CCRx (in TIMx_CCRx) are always compared to determine whether TIMx_CNT $\leqslant$ CCRx (in TIMx_CCRx). The PWM signal OCx is active as long as TIMx_CNT $\leqslant$CCRx (in TIMx_CCRx), otherwise it becomes inactive.

The timer is only able to generate PWM in edge-aligned mode.

12. RTC

12.1. Introduction

The real-time clock (RTC) is an independent BCD timer/counter.

One 32-bit registers contain the seconds, minutes, hours (12 or 24-hour format) expressed in binary coded decimal format (BCD).

One 32-bit registers contain the days expressed in binary format.

Daylight saving time compensation can also be performed.

Additional two 32-bit registers contain the programmable alarm seconds, minutes, hours and days.

A digital calibration feature is available to compensate for some deviation.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low power mode or under reset).

12.2. Features

- Time with seconds, minutes, hours, days (12 or 24-hour format).
- Daylight saving compensation programmable by software.
- One programmable alarm with interrupt function. The alarms can be triggered by any combination of the time fields.
- Maskable interrupts/events:
  - Alarm
- Digital calibration circuit
- Register write protection

12.3. Clock and Prescalers

A programmable prescaler stage generates a 1 Hz clock which is used to update the calendar. To minimize power consumption, the prescaler is split into 2 programmable prescalers.

A 9-bit asynchronous prescaler configured through the PREDIV_A bits of the RTC_PRER register.

A 9-bit synchronous prescaler configured through the PREDIV_S bits of the RTC_PRER register.

Note: It is recommended to configure the asynchronous prescaler to a high value to minimize consumption.

Default, the asynchronous prescaler division factor is set to 128, and the synchronous division factor to 256, to obtain an internal clock frequency of 1 Hz (ck_spre) with 32.768 kHz as RTCLCK

f_{clk_apre} is given by the following formula:

$$f_{clk\_apre} = \frac{f_{RTCCLK}}{\text{PREDIV\_A} + 1}$$

f_{clk_spre} is given by the following formula:

$$f_{clk\_spre} = \frac{f_{clk\_apre}}{\text{PREDIV\_S} + 1}$$

13. UART

13.1. Introduction

The Universal Asynchronous Receiver Transmitter (UART) module offers a flexible means of full duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

It offers a very wide range of baud rates using a fractional baud rate generator.

Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

This chip integrates three UART modules:

- 2 normal UART with low power or high speed.
- 1 LOGUART with high speed.

13.2. Features

- Support UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bit
- Support a very wide range of baud rate, 110~6Mbps.
- APB3 bus interface
- Support DMA mode
- Support auto flow control
- Support interrupt control
- Support IrDA
- Support loopback mode for test
- Differentiate clk for Tx path and Rx path
- Fractional baud rate generator for Tx path and Rx path
- Support low power Rx path without XTAL & PLL, Baud rate 110~500000.
- Monitor and eliminate Rx baud rate error and own frequency drift automatically for new Rx path
- Transmit and Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level

13.3. Baud Rate

Table 26 UART Baud Rate

	High Rate	*Low Power*
clock select	40MHz XTAL	8MHz
supported baud rate(bps)	1200, 9600, 14400, 19200, 28800, 38400, 57600, 76800, 115200, 128000, 153600, 230400, 406800, 500000, 921600, 1000000, 1382400, 1444400, 1500000, 1843200, 2000000, 2100000, 2764800, 3000000, 3250000, 3692300, 3750000, 4000000, 6000000	1200, 9600, 14400, 19200, 28800, 38400, 57600, 76800, 115200, 128000, 153600, 230400, 406800, 500000

13.4. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the Ameba-Z UART interface via the IO power.

14. SPI

14.1. Introduction

Ameba-Z support Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol from Motorola.

There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of the slave select signal or the first edge of the serial clock.

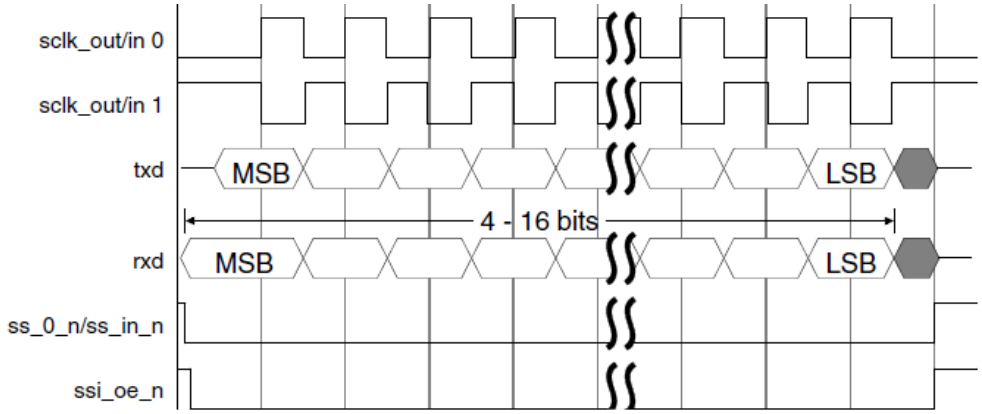

Figure 10 SPI Serial Format (SCPH = 0)

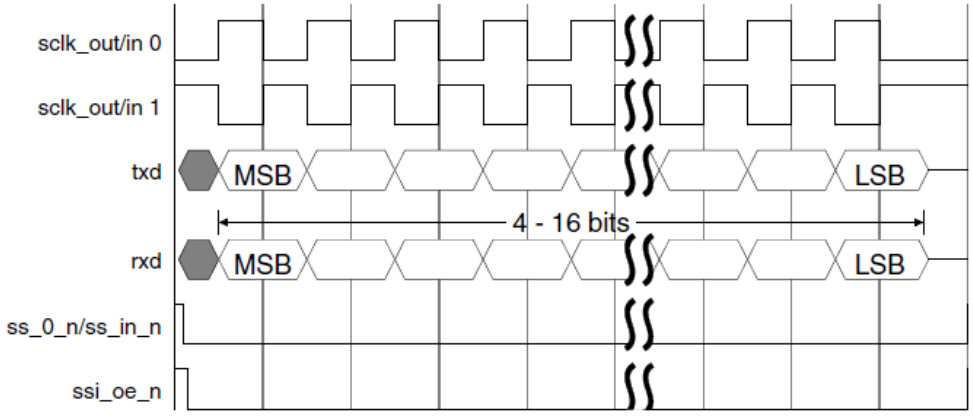

Figure 11 SPI Serial Format (SCPH = 1)

The slave select line is held high when the SPI is idle or disabled.

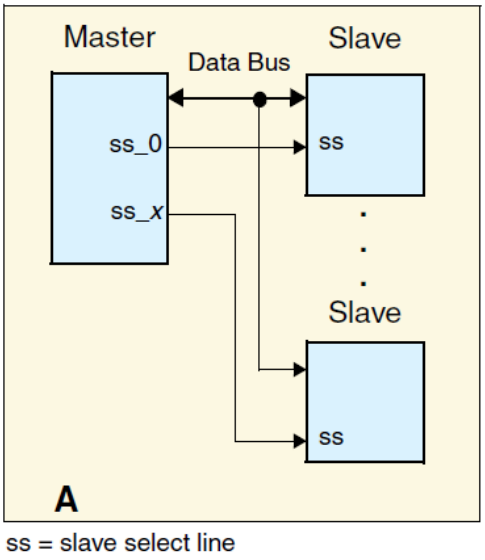

Figure 12 Slave Selection

14.2. Features

- Motorola SPI Interface Operations support
- Support maximum 2 SPI port
- Support Master (SPI1 only), and Slave(SPI0 only) mode
- Support DMA to offload CPU bandwidth
- high speed SPI with baud rate up to 31.25MHz
- Programmable clock bit-rate
- Programmable clock polarity and phase
- Master just support 1 hardware CS, you can use GPIO to control more SPI salve.

15. I2C

15.1. Introduction

The I2C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL).

When the bus is idle, both the SCL and SDA signals are pulled high through internal pull-up resistors. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

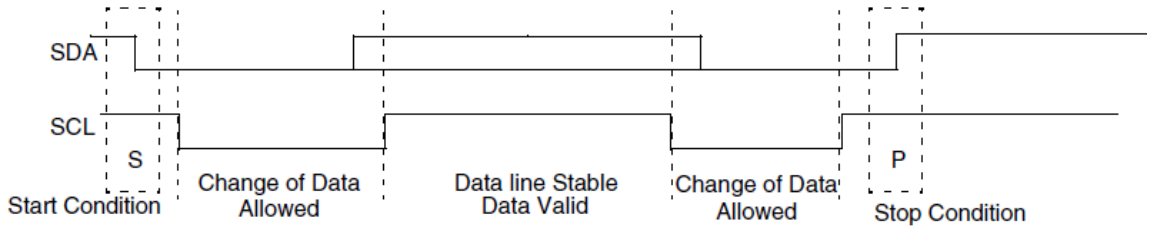

Figure 13 I2C start stop condition

I2C bus carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device.

Devices can also be considered as masters or slaves when performing data transfers. A master is a device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

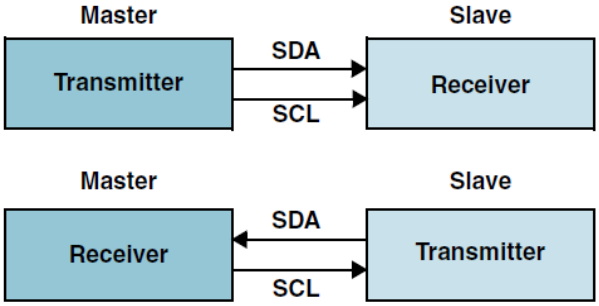

Figure 14 Master/Slave and Transmitter/Receiver Relationships

Ameba-Z can operate in standard mode (with data rates 0 to 100 Kb/s), fast mode (with data rates less than or equal to 400 Kb/s), high-speed mode (with data rates less than or equal to

3.4 Mb/s) are not supported.

Ameba-Z can communicate with devices only of these modes as long as they are attached to the bus. Additionally, fast mode devices are downward compatible. For instance, fast mode devices can communicate with standard mode devices in 0 to 100 Kb/s I2C bus system. However, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I2C bus system as they cannot follow the higher transfer rate and unpredictable states would occur.

There are two address formats: the 7-bit address format and the 10-bit address format.

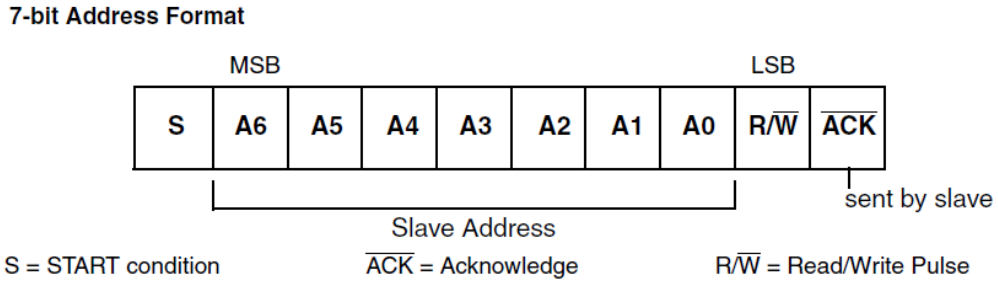

Figure 15 7-bit address format

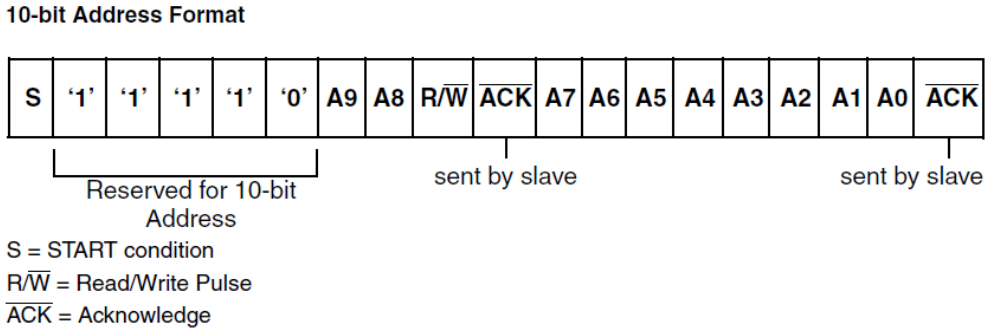

Figure 16 10-bit address format

15.2. Features

- Support maximum 2 I2C port
- Two speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - Not support High-speed mode (<3.4 Mb/s)
- Master or Slave I2C operation

- 7- or 10-bit addressing
- Transmit and receive buffers
- TX and RX DMA support
- Slave mode address match wakeup for power save

16. I2S

16.1. Introduction

I2S（Inter IC Sound）is a standard communication structure using in digital audio systems. Since the digital audio signals in consumer audio market are being processed by a number of VLSI ICs, standardized communication structure could increase system flexibility.

16.2. Features

- Sample bit: 16 bit , 24 bit
- Sample rate: 8K, 16K, 24K, 32K, 48K, 96K, 7.35K, 14.7K, 22.05K, 29.4K, 44.1K, 88.2K
- IIS throughput: 0.512Mbps (16K*32bit) ~ 6.144Mbps (96K*64bit)
- IIS channel number: mono, stereo
- Integrated DMA engine to minimize SW efforts
- Master or slave mode support
- Support Mono and Stereo TX or RX or TX&RX mode
- Not support PCM mode

16.3. Function Description

16.3.1. Clock Type

- SCLK : 6.144MHz, 3.072MHz, 2.048Mz, 1.536MHz, 1.024MHz ,0.512MHz,0.256MHZ
- MCLK :24.576Mhz, 12.288Mz, 8.192MHz, 6.144MHz , 4.096Mhz , 2.048Mhz
- WS(Sample Rate): 96K, 48K, 32K, 24K, 16K, 8K ( )
- MCLK=4SCLK=256WS (24bit)
- MCLK=8SCLK=256WS (16bit)

17. ADC

17.1. Introduction

Ameba-Z integrates one ADC with as many as four channels: One internal channel for thermal, two external normal channels, and one external VBAT channel.

17.2. Feature

- Support 1 internal ADC channel (reserved for internal thermal meter output)
- Support 3 external ADC channel
- Up to 2 sets of 12-bits resolution A/D converter channel configurable
  - Bandwidth 16KHz
  - Input signal range: 0.01V~V_{REF}-0.2V
- 1 16-bits high resolution A/D converter (ADC_CH2 only)
  - Bandwidth 64KHz
  - Input signal range: 0.01V~V_{REF}-0.2V
- Support 0~ 3.3V analog signal sampling
- Support DMA mode
- Support Timer(TIM3) trigger one shot sampling without CPU active for save power
- Pre-configured period to auto-sampling
- Support two wakeup method: buffer threshold and event trigger.
- Support VBAT, 0~5V

	Internal	*PinName*	*Thermal*	*VBAT*	*Voltage*
CH0	Y	N/A	Y	N/A	N/A
CH1	N	GPIOA19/ADC_1	N	N	0~3.3V
CH2	N	VBAT_MEAS	N	Y	0~5V
CH3	N	GPIOA_20/ADC_3	N	N	0~3.3V

18. GDMA

18.1. Introduction

General purpose direct memory access (GDMA) is used to transfer data between peripherals and memory as well as memory to memory without CPU actions.

Ameba-Z integrate two GDMA modules, One GDMA module has 6 channels to manage the data transfer between memory and peripherals.

18.2. Features of GDMA

- Dual port DMA with totally 12 channels
- Single FIFO per channel for source and destination
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support multi block transfer
- Maximum block size is 4095
- Programmable source and destination addresses; address increment, decrement, no change or address auto-reload
- Configurable endian
- Support block level flow control
- DMA interrupt for complete or error

19. WGT (watchdog timer)

19.1. Introduction

The watchdog timer regains control in case of system failure (due to a software error) to increase application reliability. The WDT can generate a reset or an interrupt when the counter reaches a given timeout value.

19.2. Features

- Watch dog timer is count with 32.768KHz/(divfactor+1). Dividing factor is 1~0xFFFF.
- Timeout value: 1ms ~ 8190s
- Configurable reset or interrupt generation with the given timeout value
- Watch dog timer disable/enable/refresh

20. GPIO

20.1. Introduction

Ameba-Z GPIO IP controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

Ameba-Z support two port: PORT_A(0~31) and PORT_B(0~6).

Port A can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge

NOTICE: Both edge interrupt is not support.

The interrupts can be masked by programming the gpio_int_mask register. The interrupt status can be read before masking (called raw status) and after masking.

Whenever Port A is configured for interrupts, the data direction must be set to Input. If the data direction register is reprogrammed to Output, then any pending interrupts are not lost. However, no new interrupts are generated.

If the user has configured Port A to include the interrupt feature, the GPIO can be configured to either include or exclude a debounce capability using the GPIO_DEBOUNCE parameter.

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

20.2. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

- GPIO_DEBOUNCE to remove any spurious glitches

21. Security Engine

21.1. Introduction

The Security engine provides fast and energy efficient hardware encryption and decryption service for Ameba-Z.

21.2. Features

- Provide low SW computing and high performance encryption
- Efficient CPU/DMA access support
- Block size up to 32KB.
- Supported authentication algorithms:
  - MD5
  - SHA-1
  - SHA-2 (SHA-224 / SHA-256)
  - HMAC-MD5
  - HMAC-SHA1
  - HMAC-SHA2
- Supported Encryption / Decryption mechanisms:
  - DES (CBC / ECB)
  - 3DES (CBC / ECB)
  - AES-128 (CBC / ECB / CTR)
  - AES-192 (CBC / ECB / CTR)
  - AES-256 (CBC / ECB / CTR)

22. USOC (USB device)

22.1. Introduction

USOC is USB device controller that is compliant with the USB 2.0 specification.

The USOC module connects SIE to AHB system bus so that USB can work in two modes:

- iNIC mode, all SIE data transfer is through AHB bus.
- NIC mode or Dongle mode, all SIE data transfer is through legacy TDE/RDE interface.

In two modes, register access path are all enabled to get the highest flexibility to configure SIE, or other system block such as WLON/SYSON.

22.2. Features

- Support USB 2.0
- Support HS/FS/LS mode
- Internal DMA support, DMA works based on register settings
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use if Ethernet to WIFI transformation card
- 1.5KByte bulk-in buffer and 1.5KByte bulk-out buffer
- Switch NIC and iNIC mode by register settings
- Interrupt mitigation
- Error handling
- Support Mass storage and network device

23. SDIO/GSPI device

23.1. Introduction

The SDIO Controller supports the Secure Digital I/O communication protocol and Realtek SPI protocol.

23.2. Features

- Support SDIO 2.0 SDR25
- CIS can be configured with internal non-volatile memory for fast card detection
- Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use if Ethernet to WIFI transformation card
- Clock rate variable up to 50 MHz
- Internal DMA support

23.3. Bus Timing Specification

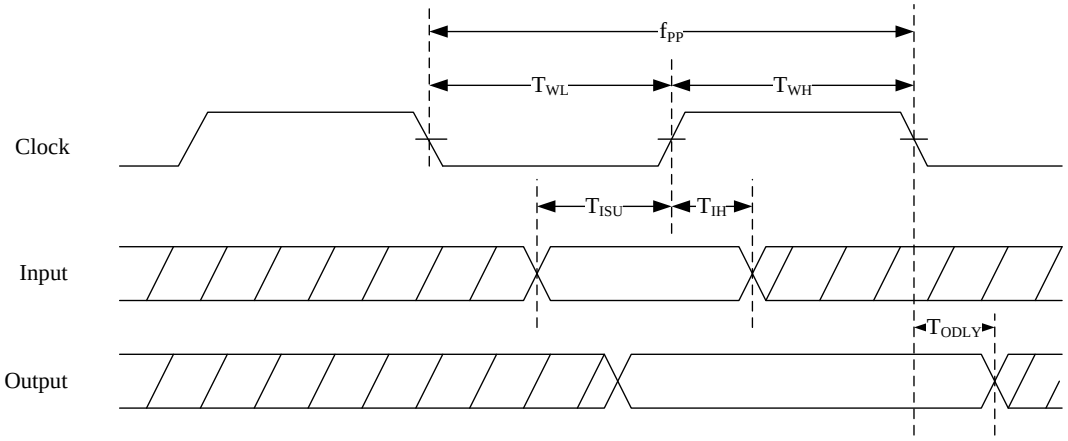

Figure 17 SDIO bus timing

Table 27 SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz

		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

24. Electrical Characteristics

24.1. Temperature Limit Ratings

Table 28 Temperature Limit Ratings

Parameter	*Minimum*	*Maximum*	*Units*
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	0	+125	°C

24.2. Power Supply DC Characteristics

Table 29 Power Supply DC Characteristics

Symbol	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
VA33, VD33IO, SW_HV3	3.3V Supply Voltage	3.0	3.3	3.6	V
VDD_IO	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V
VA12_AFE, VA12_SYN, VA12_RF	1.2V Core Supply Voltage	1.08	1.2	1.32	V
IDD33	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA
IDD_IO	IO Rating Current (including VDD_IO)			200	mA
IDD_IO_33	3.3V IO Rating Current			50	mA

24.3. Digital IO Pin DC Characteristics

24.3.1. Electrical Specifications

Table 30 Typical Digital IO DC Parameters (3.3V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
I_{T+}	Schmitt-trigger High Level		1.78	1.87	1.97	V
I_{T-}	Schmitt-trigger Low Level		1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA

Table 31 Typical Digital IO DC Parameters (1.8V Case)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	CMOS	0.65x Vcc	-	-	V
V_{IL}	Input-Low Voltage	CMOS	-	-	0.35x Vcc	V
V_{OH}	Output-High Voltage	CMOS	Vcc-0.45	-	-	V
V_{OL}	Output-Low Voltage	CMOS	-	-	0.45	V
I_{T+}	Schmitt-trigger High Level		1.02	1.09	1.14	V
I_{T-}	Schmitt-trigger Low Level		0.67	0.73	0.87	V
I_{IL}	Input-Leakage Current	V_{IN}=1.8V or 0	-10	±1	10	μA

25. Mechanical Dimensions

25.1. Package Specification

25.1.1. QFN32

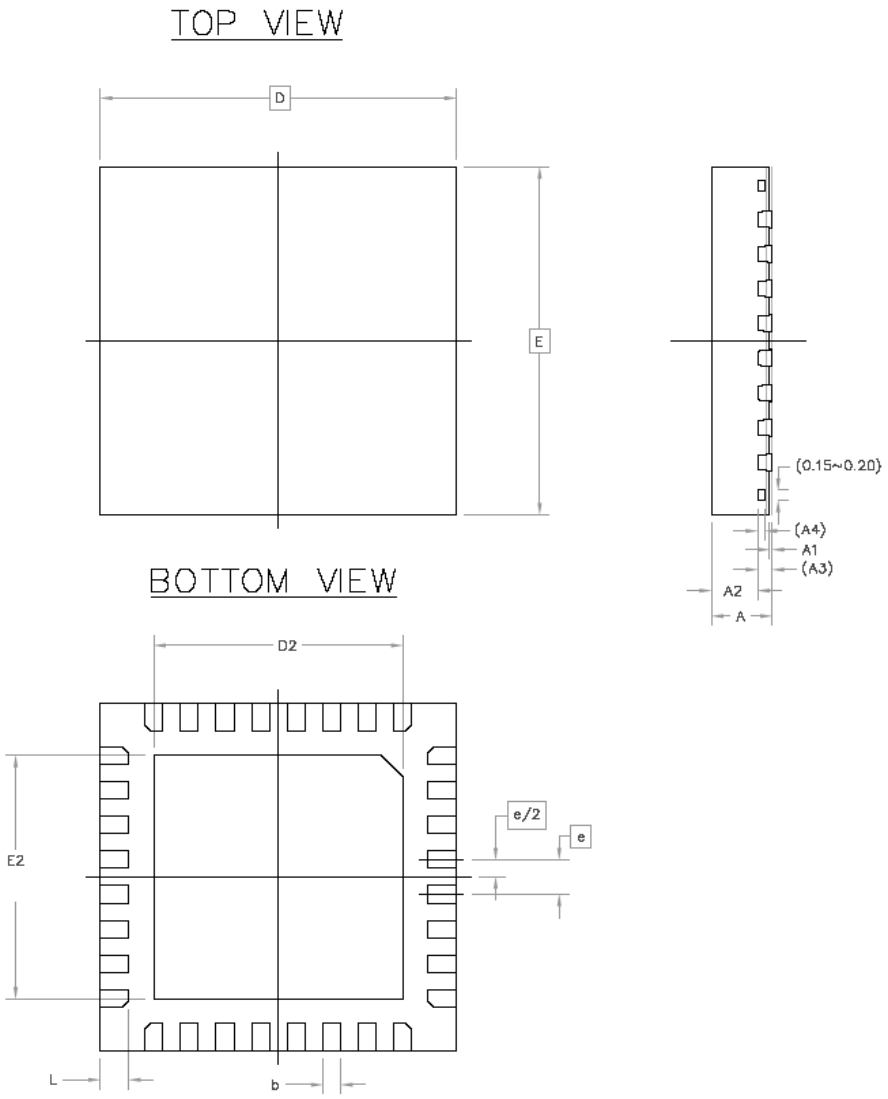

Figure 18 QFN32 Package Specification

Table 32 QFN32 Package Specification

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max

A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
A4	0.10 REF			0.004 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.020 BSC		
D2/E2	3.25	3.50	3.75	0.128	0.138	0.148
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

25.1.2. QFN48

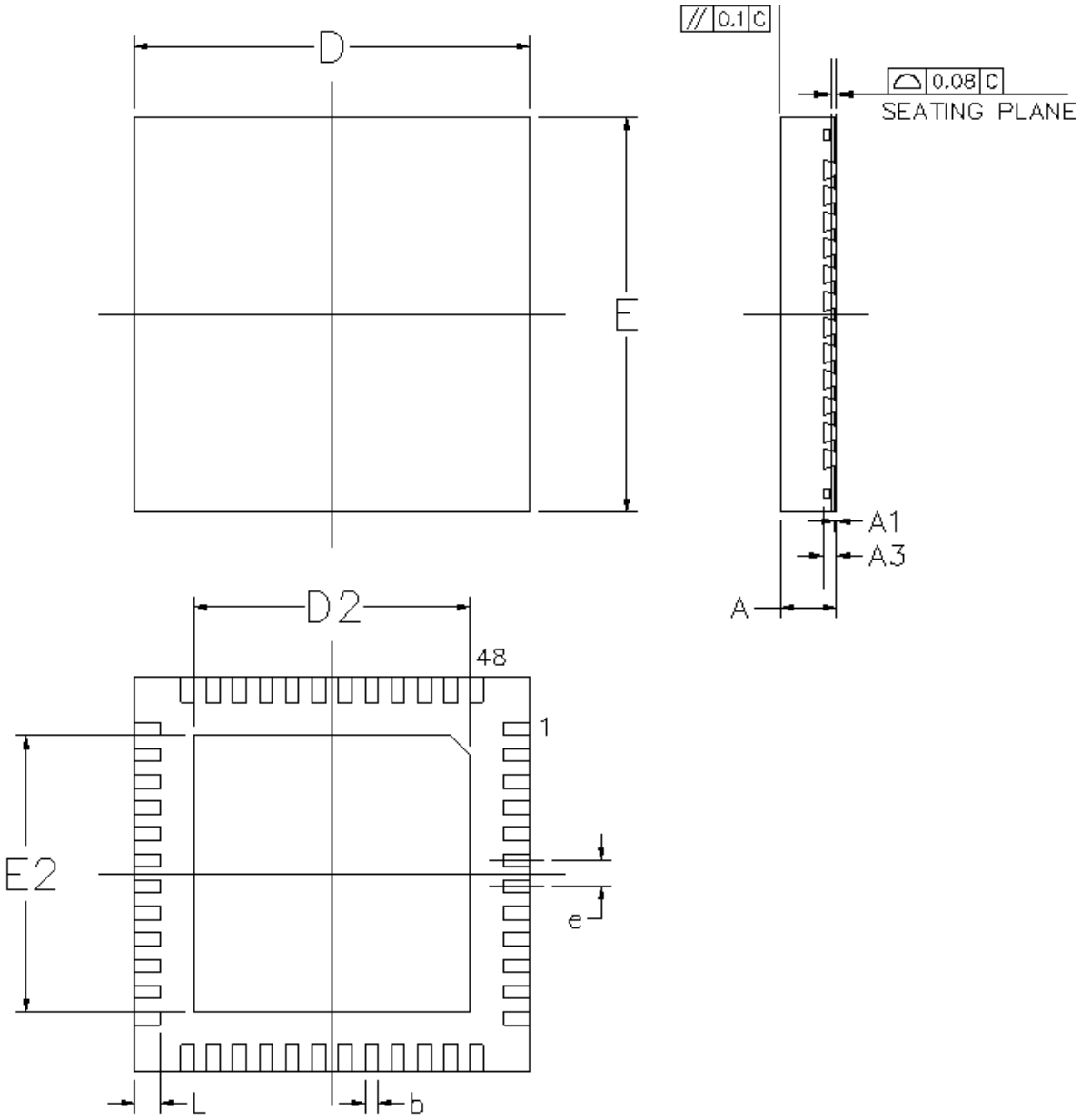

Figure 19 QFN48 Package Specification

Table 33 QFN48 Package Specification

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039

A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.0	4.2	4.5	0.157	0.167	0.177
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

25.1.3. QFN68

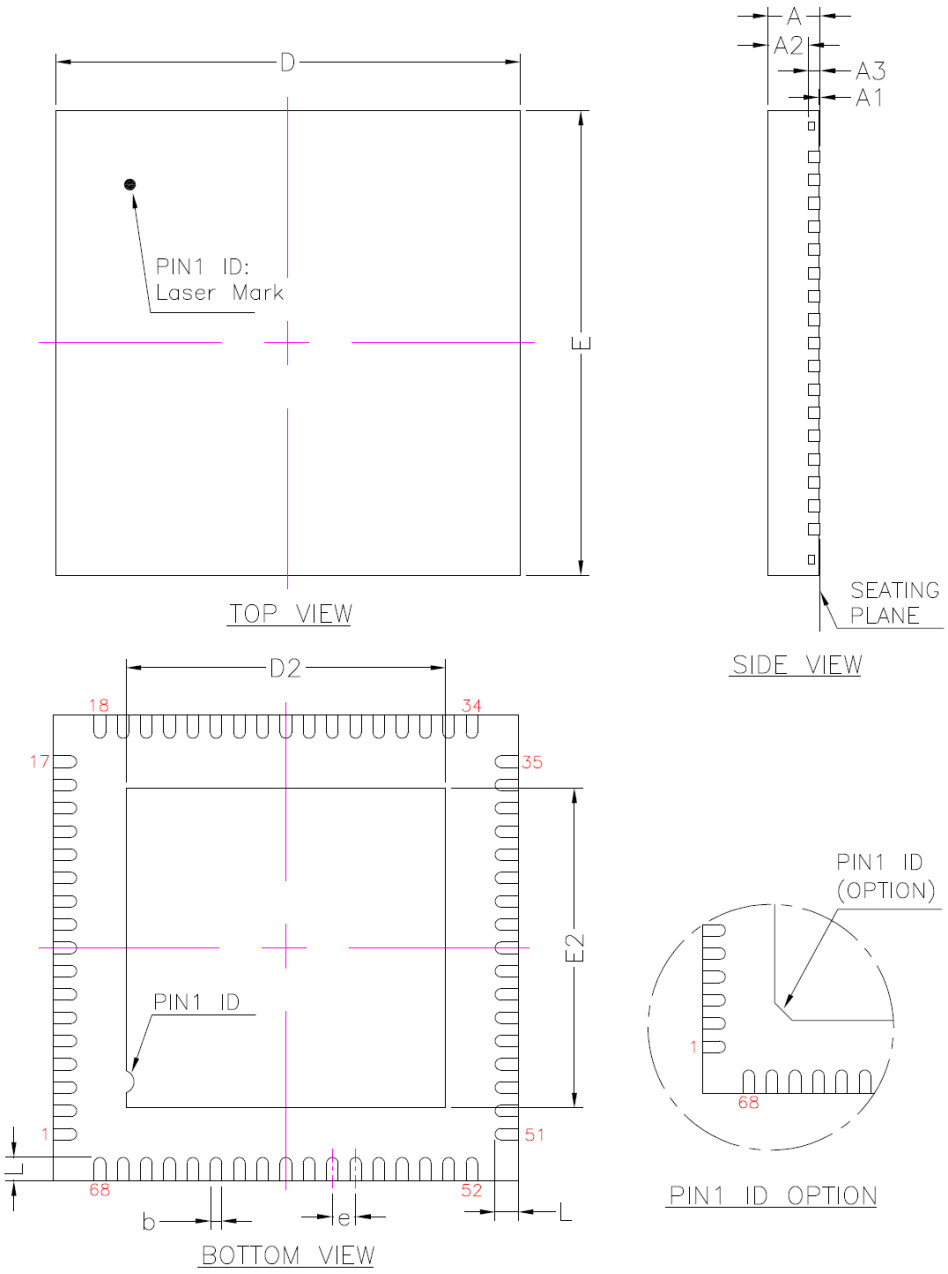

Figure 20 QFN68 Package Specification

Table 34 QFN48 Package Specification

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max

A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3		0.2 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		8.00 BSC			0.315 BSC	
D_2/E_2	4.80	5.05	5.31	0.189	0.199	0.209
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.