UM0401
RTL872xD Datasheet

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This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ORDERING INFORMATION

Part Number	Package	Status
TBD		

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1 Product Overview

1.1 General Description

RTL872xD is a highly integrated single-chip low power dual bands (2.4GHz and 5GHz) Wireless LAN (WLAN) and Bluetooth Low Energy (v5.0) communication controller. It consists of a high-performance MCU (ARM v8m, Cortex-M4F instruction compatible) named KM4, a low power MCU (v8m, Cortex-M0 instruction compatible) named KM0, WLAN (802.11 a/b/g/n) MAC, an 1T1R capable WLAN baseband, RF, Bluetooth and peripherals.

High speed connectivity interfaces, SDIO and USB are provided. There are also audio codec, Key-Scan and touch keys integrated into this IC. Besides, flexible design configures GPIO to different functions according to applications.

RTL872xD also integrates memories (ROM/SRAM/PSRAM) for IoT (Internet of Things) Wi-Fi protocol functions and applications. The user-friendly development kits (SDK and HDK) are supported to customers for developing IoT applications.

The KM4 MCU is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, floating point computation, DSP instructions and a high level of support block integration. The KM4 MCU incorporates a 3-stage pipeline.

The KM0 coprocessor is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the KM4 core. The KM0 coprocessor offers up to 20MHz performance with a simple instruction set and reduced code size.

1.2 System Architecture

The system architecture of RTL872xD is shown in Fig 1-1.

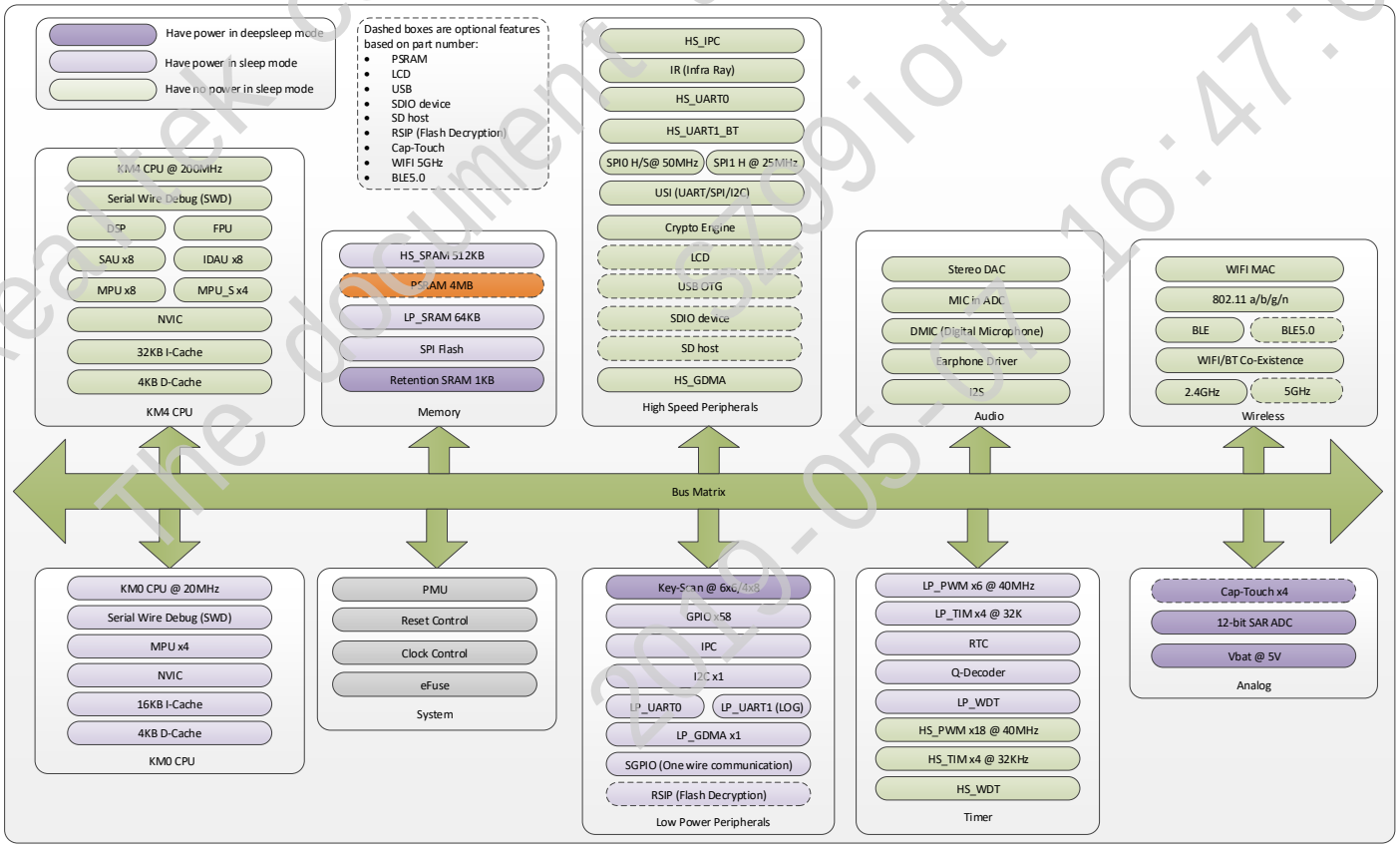


Fig 1-1 System architecture

In RTL872xD, the main system consists of 32-bit multilayer AXI bus matrix that interconnects all the masters and the slaves. The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

A multilayer AXI bus matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slave ports of the matrix to be accessed simultaneously by different bus masters.

APB peripherals are connected to the AXI bus matrix via APB buses using separate slave ports from the multilayer AXI bus matrix. This allows for better performance by reducing collisions between the CPU and the DMA controller, and also for peripherals on the asynchronous bridge to have a fixed clock that does not track the system clock.

1.3 Features

1.3.1 System and Memory

The system and memory features of RTL872xD are listed in Table 1-1.

Table 1-1 System and memory features

Items	Description
processor	● Dual processor core ● KM4: ARM latest v8M architecture with Cortex-M4F instruction compatible ● KM0: ARM latest v8M architecture with Cortex-M0 instruction compatible ● Equal access to address space including SRAM, peripherals and registers.
KM4 CPU	● Cortex-M4F instruction compatible with FPU, DSP and TrustZone-M ● Running at a frequency of up to 200MHz (configurable). ● Floating Point Unit (FPU) and Memory Protection Unit (MPU). ● Built-in Nested Vectored Interrupt Controller (NVIC). ● Non-maskable Interrupt (NMI) with a selection of sources. ● Serial Wire Debug (SWD) with 8 break points and 4 watch points (without Serial Wire Output (SWO) for enhanced debug capabilities). ● System tick timer. ● 32KB I-Cache and 4KB D-Cache.
KM0 CPU	● Cortex-M0 instruction compatible ● Running at a frequency of up to 20MHz. ● Built-in Nested Vectored Interrupt Controller (NVIC). ● Non-maskable Interrupt (NMI) with a selection of sources. ● Serial Wire Debug (SWD) with 4 break points and 2 watch points. ● System tick timer. ● 16KB I-Cache and 4KB D-Cache
KM4 CPU On-Chip memory	● Up to 512KB contiguous main SRAM @200MHz ● Optional 4MB PSRAM for specific parts @ 50MHz, 8bit DDR
KM0 CPU On-Chip memory	● Up to 64KB contiguous main SRAM. ● Up to 1KB retention SRAM for keeping data at power saving modes.
GDMA	● KM4 and KM0 both have a GDMA controller. ● HS-GDMA0 supports six channels with TrustZone-M ● LP-GDMA0 supports six channels without TrustZone-M.
Flash	● SPI/QSPI/QPI flash controller with cache ● Flash In-Circuit Programming (ICP) are supported
General-Purpose I/O (GPIO)	● Up to 64 General-Purpose I/O (GPIO) pins. All GPIOs have configurable pull-up/pull-down resistors. ● GPIO interrupt trigger could be configured with rising, falling or both input edges.
IPC	● Inter-Processor communication

1.3.2 Wireless

The wireless features of RTL872xD are listed in Table 1-2.

Table 1-2 Wireless features

Items	Description
Wi-Fi	● 802.11 a/b/g/n 1x1, 2.4GHz & 5GHz ● Support 20MHz/40MHz up to MCS7 ● Low power architecture ● Support low power Tx/Rx for short range application ● Low power beacon listen mode ● Low power Rx mode ● Very low power suspends mode (DLPS) ● External PA is supported
BT BLE	● Support BLE ● Support both central and peripheral modes ● High power mode (10dbm, share the same PA with Wi-Fi) ● Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna.
BT BLE5.0	Support BLE5.0

1.3.3 Secure

The secure features of RTL872xD are listed in Table 1-3.

Table 1-3 Secure features

Items	Description
Hardware engine	AES/DES/SHA hardware engine
TrustZone	TrustZone-M supported
Secure boot	Secure boot supported
SWD protection	Debug port access protection and prohibition modes
eFuse protection	Security eFuse
RSIP	Flash Decryption on-the-fly

1.3.4 Communication Interface

The communication interface features of RTL872xD are listed in Table 1-4.

Table 1-4 Communication interface features

Items	Description
SD/SDIO	● Support SD card host ● Support SDIO 2.0 SDR25 ● Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode ● Support high performance Ethernet to Wi-Fi transformation ● Clock rate variable up to 50MHz ● Internal DMA support ● SDIO device time consuming from power on to initialization completion: 64.14635ms
USB	● Support USB 2.0 ● Support HS/FS/LS mode ● Internal DMA support, DMA works based on register settings ● 1.5KByte bulk-in buffer and 1.5KByte bulk-out buffer
SPI	● Support Motorola SPI Serial interface operation ● Support master or slave operation mode ● Provide two SPI ports: ■ SPI0 (High speed): configured as master or slave with Max. baud rate: 50MHz.

	■ SPI1 (Normal speed): configured as master with Max. baud rate: 25MHz. ● Support DMA interface for DMA transfer ● Independent masking of interrupts ● FIFO depth – The transmit and receive FIFO buffers 64 words deep. The FIFO width is fixed at 16 bits. ● Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device ● Programmable features: ■ Clock bit-rate – Dynamic control of the serial bit rate of the data transfer; used in only serial-master mode of operation. ■ Data item size (4 to 16 bits) – Item size of each data transfer under the control of the programmer. ■ Configurable clock polarity and phase ■ Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.
UART	● Support UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bit ● Support a very wide range of baud rate ● Support auto flow control ● Support interrupt control ● Support IrDA ● Support loopback mode for test ● Differentiate clock for Tx path and Rx path ● Fractional baud rate generator for Tx path ● Low power mode for Rx path ● Monitor and eliminate Rx baud rate error and own frequency drift automatically for new Rx path ● Support DMA mode ● Option for UART Rx to be DMA flow controller
IR (Infra Ray)	● Support carrier frequency from 25KHz to 500KHz ● Support Duty from 1/2 to 1/5 ● Support IR diode input ● Support IR receiver module input ● 32*4 bytes Tx FIFO ● 32*4 bytes Rx FIFO ● Tx carrier frequency can be configured ● Tx carrier duty cycle can be configured
One wire (SGPIO)	● One wire communication interface for security element ● Timer Mode: ■ Rx and Multiple Timer are 16-bit timer with a 16-bit prescaler. ■ Rx and Multiple Timer can stop, reset, and interrupt by match events. ■ Rx and multiple timer/counter can stop and reset to each other. ● Capture Mode: ■ Rx timer can be captured by capture events. ■ Capture events can be Rx trigger events or the multiple match events. ■ The capture value can be transferred to '0' or '1' by comparing the value. ● Counter Mode: ■ Multiple Counter can count Rx trigger events. ● External Output Mode: ■ External output can set high, low or toggle on the match event. ● Get the serial input: ■ Shift the input value to a 32-bit FIFO by match events. ● Send the serial output: ■ Send the '0'or '1' waveform by shifting the output value of a 32-bit FIFO. This output value decides that the external match uses the match value of group 0 or group 1. ■ Change the output value by using the multiple FIFO data to update the multiple match value. ● Monitor Mode: ■ Monitor the receiving value to make the interrupt in the power saving mode.
I^2C	● Two-wire I^2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)

	● Support one I²C port ● Two Speed mode: ■ Standard (up to 100Kbps) ■ Fast (up to 400Kbps) ● Master or Slave I²C operation ● 7- or 10-bit addressing ● Transmit and receive buffers with depth of 16 ● Tx and Rx DMA support ● Multi-master ability including bus arbitration scheme ● Slave mode address match wakeup for power save (up to 100Kbps) ● Clock stretch in master/slave mode ● 7- or 10-bit combined format transfers ● General Call ● Component parameters for configurable software driver support (programmable SDA hold time, slave address, etc.) ● Filter to eliminate the glitches on signal of SDA and SCL. Programmable digital noise Filter. ● Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)
USI (Universal Serial interface)	● Configured as SPI, UART or I²C ● USI I²C can support High Speed Mode

1.3.5 Audio

The secure features of RTL872xD are listed in Table 1-5.

Table 1-5 Audio features

Items	Description
Audio DAC and earphone driver	● Sampling Frequency: 8/16/32/44.1/48/88.2/96KHz ● Integrates earphone driver ■ 40mW on 16Ω load ■ 20mW on 32Ω load ● Gain Control in DAC Path ■ Gain Step: 0.375dB/step ■ Gain Range: -64.5dB ~ 0dB ● Audio output mode: ■ Line-Out Cap-less mode (QFN88) ■ Line-Out Differential mode (QFN88) ■ Line-Out Single-end mode
Audio ADC	● Sampling Frequency: 8/16/32/44.1/48/88.2/96KHz ● ADC input gain range: ■ Gain Step: 0.375dB/step ■ Gain Range: -17.625dB ~ 30dB (digital) ● MIC input boost gain stage: 0/20/30/40dB (analog) ● Audio Input mode: ■ Line-In ■ Analog MICx2 or Digital MIC x2
I²S	● Sample rate: ■ 8/12/16/24/32/48/64/96/192/384/7.35/11.025/14.7/22.05/29.4/44.1/58.8/88.2/176.4KHz ● I²S channel number: mono, stereo, 5.1 channel ● Sample bit for mono: 16-bit, 32-bit ● Sample bit for stereo & 5.1 channel: 16-bit, 24-bit, 32-bit ● Integrated DMA engine to minimize the software efforts ● Support mono and stereo Tx or Rx or Tx & Rx mode ● Support 5.1 Tx mode (DAC), not support Rx mode (ADC) ● Not support PCM mode

1.3.6 Timer

The timer features of RTL872xD are listed in Table 1-6.

Table 1-6 Timer features

Items	Description
Basic Timers (HS_TIM0 ~ HS_TIM3) (LP_TIM0 ~ LP_TIM3)	● Channels: x1 ● Clock source: 32KHz ● Resolution: 32-bit ● Counter mode: up ● Interrupt generation ● Sleep mode wakeup
PWM Timers (HS_TIM5 & LP_TIM5)	● Channels: HS_TIM5 x18, LP_TIM5 x6 ● Clock source: XTAL ● Resolution: 16-bit ● Prescaler: 8-bit ● Counter mode: up ● Statistics pulse width ● Statistics pulse counter ● Input capture pin: x2 ● Interrupt generation ● LP_TIM5 can work at sleep mode
Pulse Timers (HS_TIM4 & LP_TIM4)	● Channels: HS_TIM5 x18, LP_TIM5 x6 ● Clock source: XTAL ● Resolution: 16-bit ● Prescaler: 8-bit ● Counter mode: up ● One pulse mode ● PWM mode with polarity selection ● Input capture pin: x2 ● Interrupt generation
Real-Time clock (RTC)	● Independent BCD timer/counter ● Time with seconds, minutes, hours, days (12- or 24-hour format) ● Daylight saving compensation programmable by software ● One programmable alarm with interrupt function. The alarm can be triggered by any combination of the time fields. ● Maskable interrupts/events ■ Alarm ● Digital calibration circuit ● Register write protection

1.3.7 Human-computer Interaction

The human-computer interaction features of RTL872xD are listed in Table 1-7.

Table 1-7 Human-computer interaction features

Items	Description
Key-matrix	● Up to 8*8 (64) Keypad Array with use of 16 GPIOs ● Configurable Rows and Columns of Keypad Array ● Hardware debounce with configurable time at each scan ● Configurable Scan Clock, Scan Interval and Release Time ● Support interrupts, provide interrupts mask, interrupts clear, interrupts status ● Multi-keys detect ● Provide FIFO with width of 12 bits and depth of 16 to store Key Press and Release Events ● Support low power mode. Key press event can wakeup CPU from sleep.
Cap-Touch	● Support 4 capacitive sensor channels

	● Automatic channel scan: hardware scan each enabled channel automatically in sequence ● Programmable scan period: sample number and scan interval ● Difference or Absolute threshold judgement mode (with ETC function enable) ■ Automatic environment sensor capacitance tracking and calibration (ETC) ■ Hardware baseline initial automatically ● Automatic baseline and threshold update for different noise environment ● Programmable button debounce function ● Programmable interrupt enabled for each interrupt source ● 4*12 bits FIFO ● Low power consumption
LCD	● Supports Thin Film Transistor (TFT) color display ● LCD refresh rate 30Hz (Max. data rate = 4.6MB/s) ● Support 8-/16-bit MCU I8080 parallel interface ■ Support resolution of 8-/16-bit mode can be (1024x1024) for still picture display ■ Support resolution of 8-bit mode can be (645x645) for animate display when refresh rate is 30F/S ■ Support resolution of 16-bit mode can be (912x912) for animate display when refresh rate is 30F/S ● Support 6-/16-bit RGB parallel interface ■ Support resolution of 6-bit mode is less than (527x527) for animate display when refresh rate is 60F/S ■ Support resolution of 16-bit mode is less than (912x912) for animate display when refresh rate is 60F/S ● Support RGB565 data format for input & output ● Programmable timings for different display panels ● Programmable polarity for HSYNC, VSYNC and Data Enable ● Support DMA frame buffer for RGB/MCU I/F ● Support I/O mode for MCU I/F ● Support LED dot matrix display interface like 04/08/12/75 and so on

1.3.8 Analog

The analog features of RTL872xD are listed in Table 1-8.

Table 1-8 Analog features

Items	Description
Data capture ADC and voltage comparator	● Resolution: 12-bit SAR ● Available channel number ■ 7x external 3.3V channel and 1x 5V channel ■ 3x internal channel ● Configurable input ■ Single-end ■ Differential with predefined channel pair ● Contain 64 FIFO entries which is 16-bit width ● Multi-Channel DMA support ● Multi sampling trigger sources ■ Software ■ Timer ● 1 low power voltage comparator for battery voltage measurement ● Conversion item control or another FIFO level to trigger wakeup circuit

1.4 Peripherals

The peripherals of RTL872xD under different packages are shown in Table 1-9.

Table 1-9 Peripherals under different packages

Item	Peripherals	Comment	QFN48	QFN68		QFN88
			RTL8720DN-VA1 RTL8720DM-VA1	RTL8721DM-VA1	RTL8721DN-VRC	RTL8722DM-VA1
UART	HS_UART0		N	Y	Y	Y

	HS_UART1	Internal for BT	N	N	N	N
	HS_USI_UART		Y	N	N	Y
	LP_UART1	Low power mode wakeup	Y	Y	Y	Y
	LP_UART0	LP_UART0 is LOGUART/low power mode wakeup	Y	Y	Y	Y
SPI	HS_SPI0	Maximum 50MHz/Master/Slave	N	Y	Y	Y
	HS_SPI1	Maximum 25MHz/Master	Y	Y	Y	Y
	HS_USI_SPI	Maximum 25MHz/Master/Slave	Y	Y	Y	Y
RTC_OUT	RTC_OUT		Y	Y	Y	Y
EXT_32K	EXT_32K		Y	Y	Y	Y
LP_TIM4_TRIG	LP_TIM4_TRIG	Timer capture	N	Y	Y	Y
LP_TIM5_TRIG	LP_TIM5_TRIG	Timer capture	N	Y	Y	Y
IR	IR		Y	Y	Y	Y
I²C	LP_I²C	Standard (up to 100Kbps) and fast (up to 400Kbps)	Y	Y	Y	Y
	HS_USI_I2C	Standard/fast/high speed mode (up to 3.33Mbps)	Y	N	N	Y
SDIO	SDIO 2.0 Device	Maximum 50MHz	N	N	N	Y
	SD HOST	Maximum 50MHz	N	N	N	Y
PWM	HS_PWM0 ~ 17		8	11	11	17
	LP_PWM0 ~ 5	Support low power mode	4	6	6	6
I²S	I²S		N	Y	Y	Y
DMIC	DMIC		Y	Y	Y	Y
LCD	LCD	8-bit/16-bit/RGB mode/MCU mode/LED mode	N	N	N	Y
Q-Decoder	Q-Decoder		N	Y	Y	Y
SPGIO	SPGIO		Y	Y	Y	Y
Key-Scan	Key-Scan		4x2/3x3	7x3/5x5	4x8/6x6	4x8/6x6
Wake Pin	Wake Pin	Wake up deepsleep	6	10	12	12
HS_TIM4_TRIG	HS_TIM4_TRIG	Timer capture	Y	Y	Y	Y
HS_TIM5_TRIG	HS_TIM5_TRIG	Timer capture	Y	Y	Y	Y
Analog Pin	USB	USB host (support USB mass storage class) and device	Y	Y	Y	Y
	ADC	0 ~ 3.3V	x3	x7	x7	x7
	VBAT_MEAS	0 ~ 5V	N	Y	Y	Y
	Cap-Touch		N	x4	x4	x4
	Audio Output	Analog audio codec output	N	x2 (Single-End)	x2 (Single-End)	x2 (Differential)/x2 (Single-End) x2 (AUXIN)
	Audio Input	Analog audio codec input	N	x2 (Single-End)	x2 (Single-End)	x1 (Differential)/x2 (Single-End) x2 (AUXIN)

2 Package

2.1 Package Types

There are three package types named QFN48, QFN68 and QFN88 in RTL872xD, the details are shown in Table 2-1.

Table 2-1 Package types

Port Name	QFN48	QFN68		QFN88	Trap
	RTL8720DN-VA1 RTL8720DM-VA1	RTL8721DM-VA1	RTL8721DN-VRC	RTL8722DM-VA1	
PA[0]		√	√	√	
PA[1]				√	
PA[2]		√	√	√	
PA[3]					
PA[4]		√	√	√	
PA[5]				√	
PA[6]				√	
PA[7]	√	√	√	√	UART_DOWNLOAD
PA[8]	√	√	√	√	
PA[9]				√	
PA[10]				√	
PA[11]				√	
PA[12]	√	√	√	√	ICFG0
PA[13]	√	√	√	√	ICFG1
PA[14]	√	√	√	√	ICFG2
PA[15]	√	√	√	√	ICFG3
PA[16]		√	√	√	
PA[17]		√	√	√	
PA[18]		√	√	√	
PA[19]		√	√	√	
PA[20]			√	√	
PA[21]			√	√	
PA[22]				√	
PA[23]				√	
PA[24]				√	
PA[25]	√	√	√	√	
PA[26]	√	√	√	√	
PA[27]	√	√	√	√	NORMAL_MODE_SEL
PA[28]	√	√	√	√	
PA[29]					
PA[30]	√	√	√	√	SPS_SEL
PA[31]				√	
PB[0]				√	
PB[1]	√	√	√	√	
PB[2]	√	√	√	√	
PB[3]	√	√	√	√	
PB[4]		√	√	√	
PB[5]		√	√	√	
PB[6]		√	√	√	
PB[7]		√	√	√	
PB[8]					
PB[9]					
PB[10]					

PB[11]					
PB[12]					
PB[13]	√	√	√	√	
PB[14]	√	√	√	√	
PB[15]					
PB[16]	√	√	√	√	
PB[17]	√	√	√	√	
PB[18]				√	
PB[19]				√	
PB[20]	√			√	
PB[21]	√			√	
PB[22]		√	√	√	
PB[23]		√	√	√	
PB[24]				√	
PB[25]				√	
PB[26]		√	√		
PB[27]					
PB[28]				√	
PB[29]		√	√	√	
PB[30]				√	
PB[31]		√	√	√	

2.1.1 QFN48

The QFN48 pin assignments for RTL8720DN-VA1/RTL8720DM-VA1 are shown in Fig 2-1.

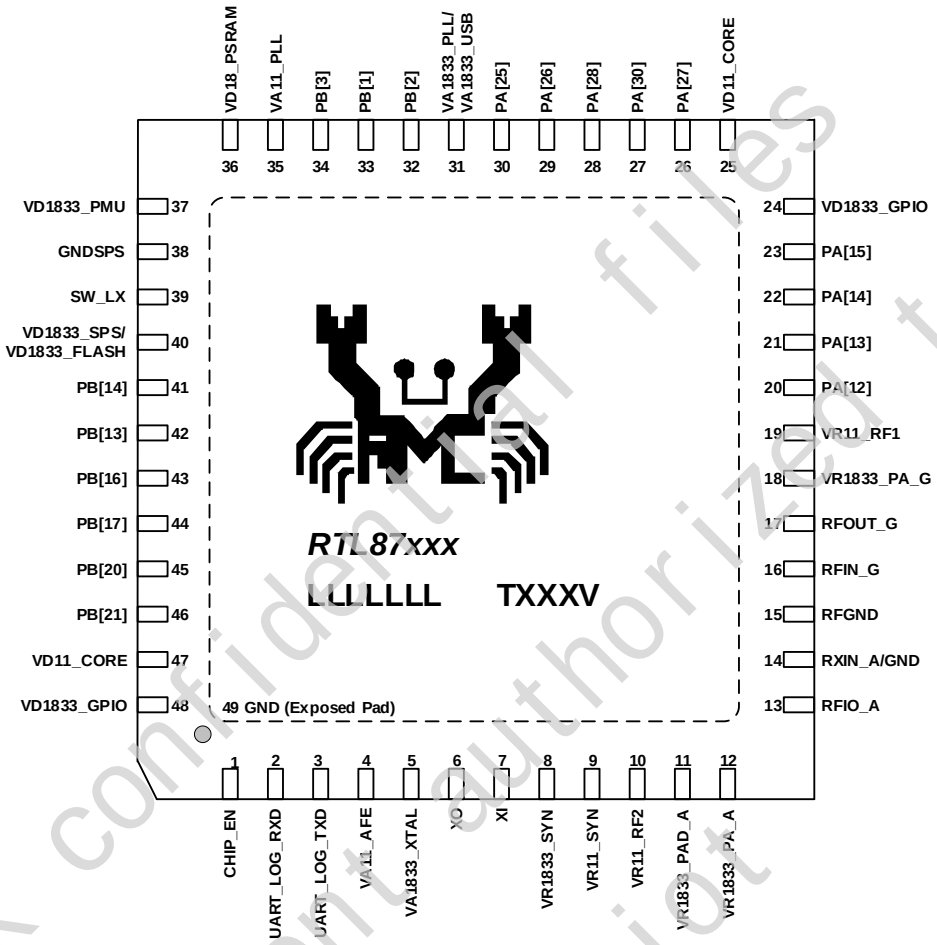


Fig 2-1 QFN48 pin assignments for RTL8720DN-VA1/RTL8720DM-VA1

2.1.2 QFN68

The QFN68 pin assignments for RTL8721DN-VRC are shown in Fig 2-2, and QFN68 pin assignments for RTL8721DM-VA1 are shown in Fig 2-3.

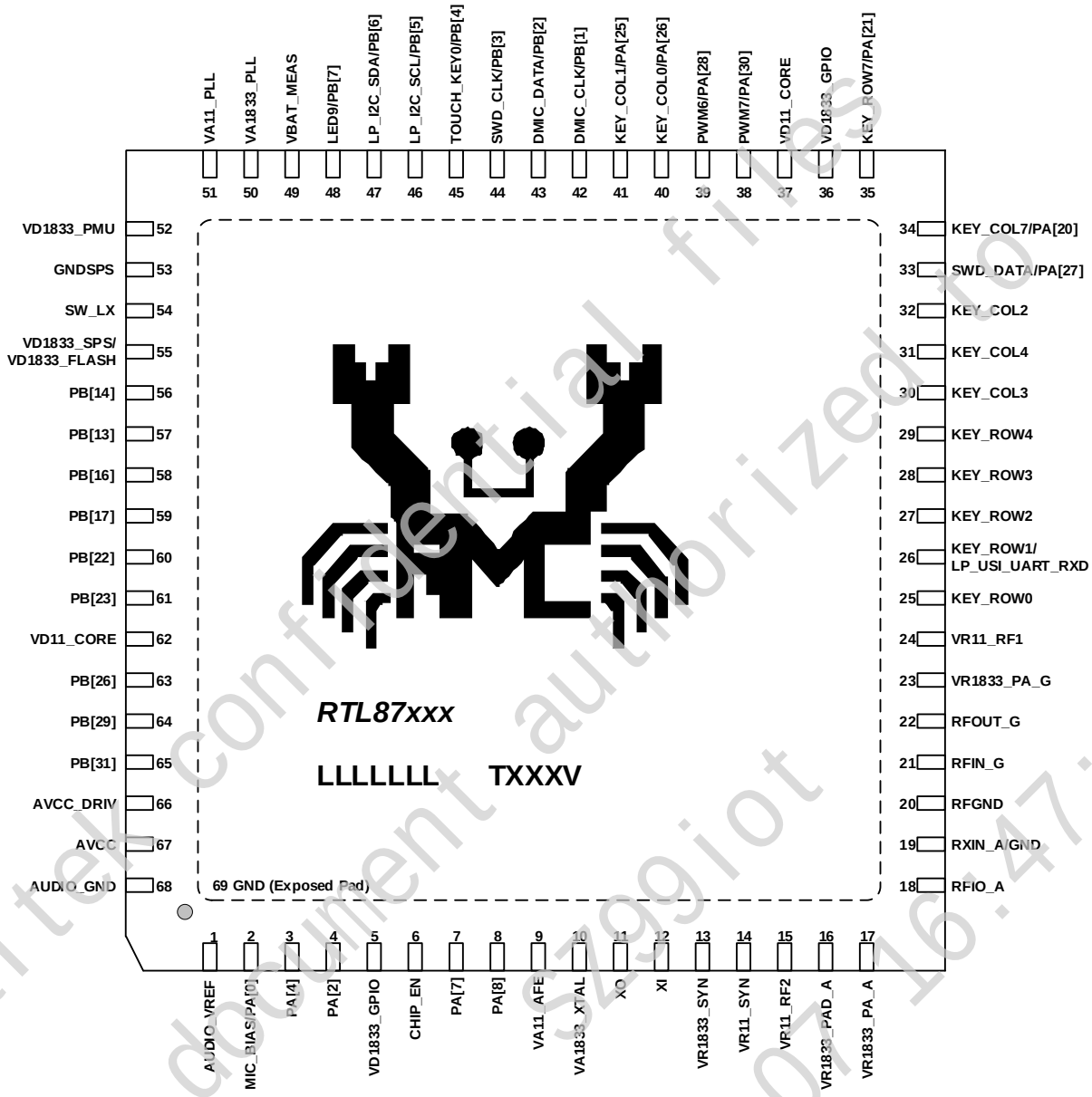


Fig 2-2 QFN68 pin assignments for RTL8721DN-VRC

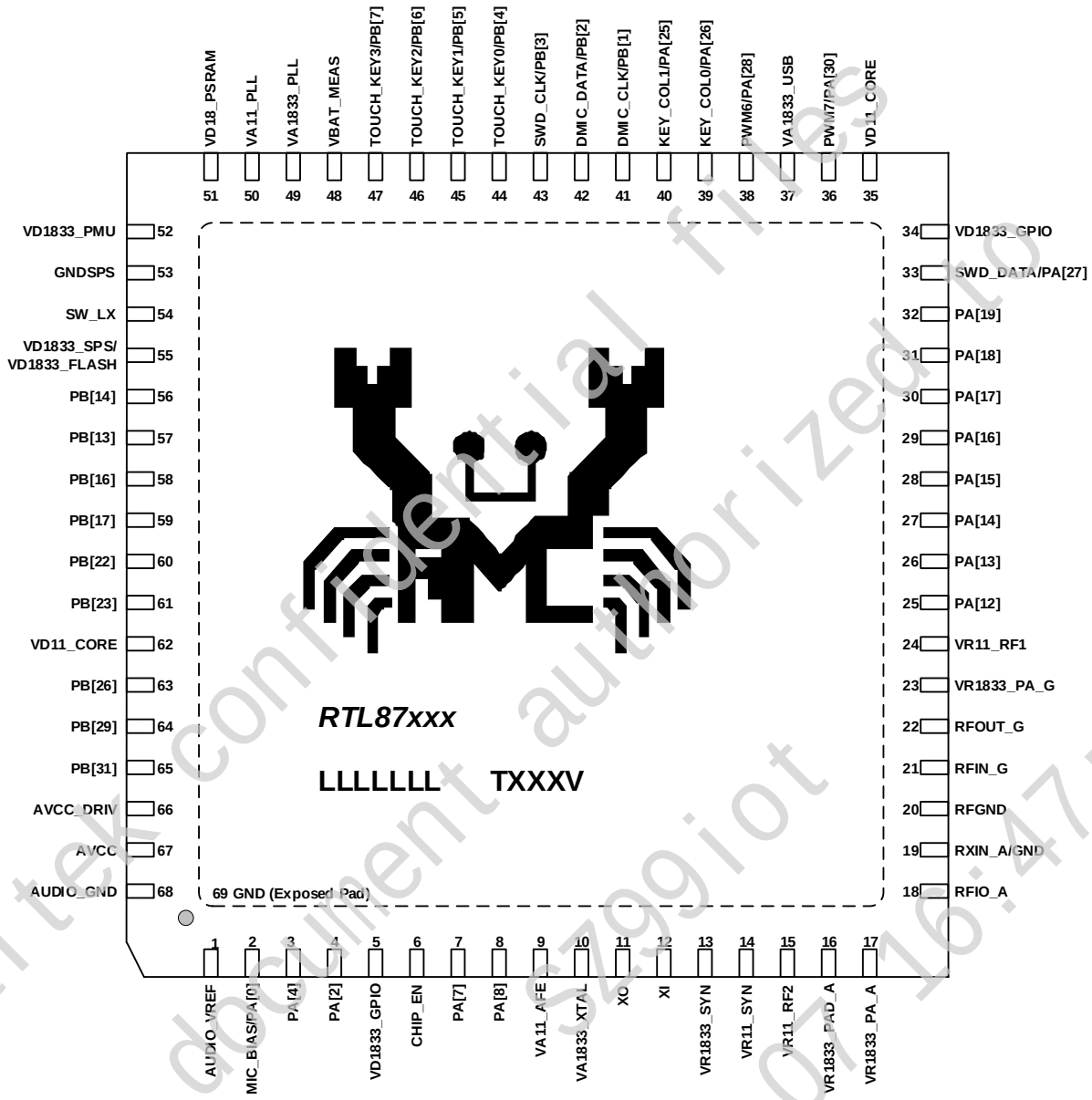


Fig 2-3 QFN68 pin assignment for RTL8721DM-VA1

2.1.3 QFN88

The QFN88 pin assignments for RTL8722DM-VA1 are shown in Fig 2-4.

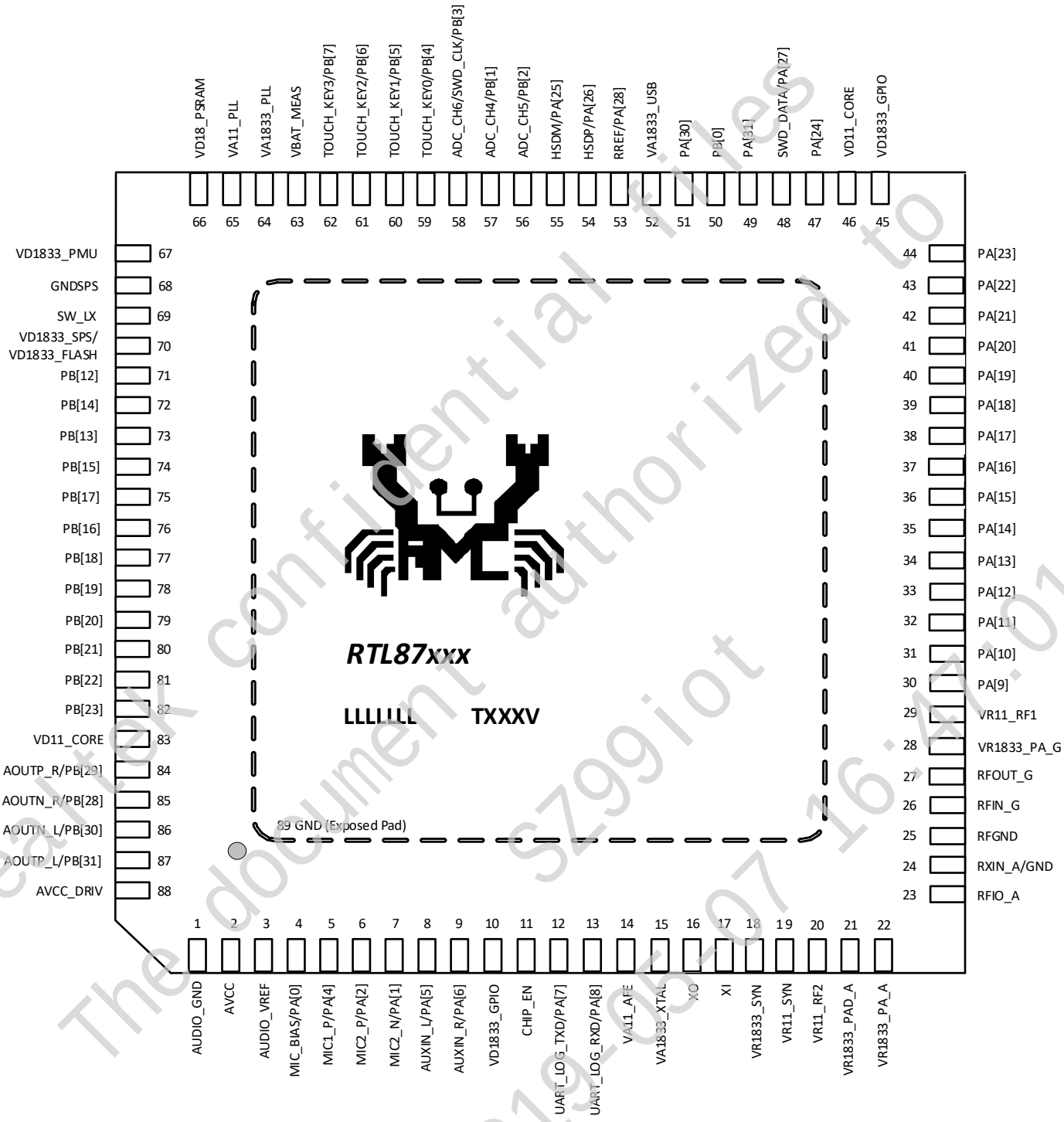


Fig 2-4 QFN88 pin assignments for RTL8722DM-VA1

2.2 Low Power Pins

These pins can work and wakeup MCU under deepsleep mode, as Table 2-2 shows. All these pins are located at Key-Scan pins.

Table 2-2 Low power pins

Pin Name	FUNC_ID28	FUNC_ID29	FUNC_ID30	FUNC_ID31
GPIO	Ext32K	Key-Scan row	Key-Scan column	Wakeup
PA[12]		KEY_ROW0		LGPIO[0]
PA[13]		KEY_ROW1		LGPIO[1]
PA[14]	RTC_OUT	KEY_ROW2		LGPIO[2]
PA[15]	RTC EXT_32K	KEY_ROW3	KEY_COL6	LGPIO[3]
PA[16]		KEY_ROW4	KEY_COL5	LGPIO[0]
PA[17]		KEY_ROW6	KEY_COL3	LGPIO[1]
PA[18]	RTC_OUT	KEY_ROW5	KEY_COL4	LGPIO[2]
PA[19]			KEY_COL2	LGPIO[3]
PA[20]			KEY_COL7	LGPIO[0]
PA[21]		KEY_ROW7		LGPIO[1]
PA[25]			KEY_COL1	LGPIO[2]
PA[26]			KEY_COL0	LGPIO[3]

2.3 Pin Default Configuration

All pins are configured as GPIO without pull resistors except some special function like SWD or LOGUART. The pin default configuration is listed in Table 2-3.

Table 2-3 Pin default configuration

Pin Name	Default Function	Default PU/PD
PA[7]	LOGUART	Internal UP
PA[8]	LOGUART	Internal UP
PA[13]	PA[13]	eFuse Pull Control 0
PA[15]	PA[15]	eFuse Pull Control 1
PA[25]	PA[25]	eFuse Pull Control 2
PA[27]	SWD_DATA when eFuse enable	Internal UP
PA[28]	PA[28]	eFuse Pull Control 3
PA[30]	PA[30]	External UP
PB[1]	PB[1]	eFuse Pull Control 4
PB[3]	SWD_CLK when eFuse enable	No pull
PB[7]	PB[7]	eFuse Pull Control 5
PB[18]	SWD_CLK when eFuse enable, or SD_D2 when eFuse enable SDIO	No pull
PB[19]	SWD_DATA when eFuse enable, or SD_D3 when eFuse enable SDIO	eFuse Pull Control 6
PB[20]	SD_CMD when eFuse enable SDIO	No pull
PB[21]	SD_CLK when eFuse enable SDIO	No pull
PB[22]	SD_D0 when eFuse enable SDIO	eFuse Pull Control 7
PB[23]	SD_D1 when eFuse enable SDIO	No pull

2.4 Trap Pins

The trap pins are listed in Table 2-4.

Table 2-4 Trap pins

Pin Name	Trap Function	Description
PA[7]	UART_DOWNLOAD	Trigger ISP ROM code flash download, low active.
PA[12]	ICFG0	Realtek test mode
PA[13]	ICFG1	Realtek test mode
PA[14]	ICFG2	Realtek test mode
PA[15]	ICFG3	Realtek test mode
PA[27]	NORMAL_MODE_SEL	It is not allowed to pull down when power on, otherwise:

		● Realtek test mode will be selected. ● Boot will fail. When this pin is not pull-down, the state of PA[12] ~ PA[15] can be ignored.
PA[30]	SPS_SEL	● High: SWR mode ● Low: LDO mode

3 Analog Pin Descriptions

The signal type used in RTL872xD are shown in Table 3-1.

Table 3-1 Pin type description

Symbol	Type	Symbol	Type
I	Input pin	O	Output pin
P	Power pin	AH	Analog and digital hybrid programmable pin
PI	Power input pin	PO	Power Output pin

3.1 Power on Trap Pin

The power on trap pins in RTL872xD are shown in Table 3-2.

Table 3-2 Power on trap pins

Symbol	Type	QFN48	QFN68		QFN88	Description
		RTL8720DN-VA1 RTL8720DM-VA1	RTL8721DM-VA1	RTL8721DN-VRC	RTL8722DM-VA1	
NORMAL_MODE_SEL	I	26	33	33	48	Shared with PA[27] ● 1: Normal operation mode ● 0: Enter into test/debug mode
UART_DOWNLOAD	I	3	7	7	12	Shared with PA[7] ● 1: Boot from flash ● 0: Download image from UART
SPS_SEL	I	27	36	38	51	Shared with PA[30] ● 1: Internal 1.1V regulator works at SPS mode ● 0: Internal 1.1V regulator works at LDO mode

3.2 RF Pins

The RF pins in RTL872xD are shown in Table 3-3.

Table 3-3 RF pins

Symbol	Type	QFN48	QFN68	QFN88	Description
RFGND	P	15	20	25	RF ground
RFIO_A	I/O	13	18	23	WL 5GHz RF signal
RXIN_A/GND	I	14	19	24	WL 5GHz RF input signal or RF ground
RFIN_G	I	16	21	26	WL/BT 2.4GHz RF input signal
RFOUT_G	O	17	22	27	WL/BT 2.4GHz RF output signal

3.3 Chip Enable Pin

The chip enable pin in RTL872xD is shown in Table 3-4.

Table 3-4 Chip enable pin

Symbol	Type	QFN48	QFN68	QFN88	Description
CHIP_EN	I	1	6	11	Enable chip ● 1: Enable chip ● 0: Shut down chip

3.4 Power Pins

The power pins in RTL872xD are shown in Table 3-5.

Table 3-5 Power pins

Symbol	Type	QFN48 RTL8720DN-VA1 RTL8720DM-VA1	QFN68 RTL8721DM-VA1	QFN68 RTL8721DN-VRC	QFN88 RTL8722DM-VA1	Description
VA1833_XTAL	P	5	10	10	15	1.8V/3.3V power for Crystal Oscillator
VA11_AFE	P	4	9	9	14	1.1V power for WL/BT Analog Front End
VR1833_SYN	P	8	13	13	18	1.8V/3.3V power for RF Synthesizer
VR11_SYN	P	9	14	14	19	1.1V power for RF Synthesizer
VR1833_PA_A	P	12	17	17	22	1.8V/3.3V power for RF 5G Power amplifier
VR1833_PAD_A	P	11	16	16	21	1.8V/3.3V power for RF
VR11_RF2	P	10	15	15	20	1.1V power for RF 5G path
VR1833_PA_G	P	18	23	23	28	1.8V/3.3V power for RF 2.4G Power amplifier
VR11_RF1	P	19	24	24	29	1.1V power for RF 2.4G path
VD11_CORE	P	47, 25	62, 35	62, 37	83, 46	1.1V power for digital core power
VD1833_SPS/VD1833_FLASH	P	40	55	55	70	1.8V/3.3V power for Flash I/O power and internal regulator input from 1.8V/3.3V to 1.1V
SW_LX	P	39	54	54	69	1.1V power output from Switching/Linear Regulator
GNDSPS	P	38	53	53	68	Ground for Switching/Linear Regulator
VA1833_USB	P	31	37	36	52	3.3V power for USB analog
VA1833_PLL	P	31	49	50	64	1.8V/3.3V power for PLL
VA11_PLL	P	35	50	51	65	1.1V power for PLL
VD18_PSRAM	P	36	51	-	66	1.8V power output from internal Linear regulator for PSRAM
VD1833_PMU	P	37	52	52	67	1.8V/3.3V power for Power Management Unit
AVCC_DRIV	P	-	66	66	88	1.8V/3.3V power supply for internal audio codec LDO.
AVCC	P	-	67	67	2	AVCC output from internal audio codec LDO, add a 1uF cap as close as possible.
AUDIO_VREF	P	-	1	1	3	Codec bandgap reference output, add a 4.7nF cap as close as possible.
MIC_BIAS	P	-	2	2	4	Microphone bias output
VD1833_GPIO	P	24, 48	5, 34	5, 36	10, 45	1.8V/3.3V power for digital GPIO
AUDIO_GND	P	-	68	68	1	Audio ground

3.5 XTAL Pins

The XTAL pins in RTL872xD are shown in Table 3-6.

Table 3-6 XTAL pins

Symbol	Type	QFN48	QFN68	QFN88	Description
XI	I	7	12	17	Input of 40MHz Crystal Clock Reference
XO	O	6	11	16	Output of 40MHz Crystal Clock Reference

3.6 ADC and Cap-Touch Pins

The ADC and Cap-Touch pins in RTL872xD are shown in Table 3-7.

Table 3-7 ADC and Cap-Touch pins

Symbol	Type	QFN48 RTL8720DN-VA1 RTL8720DM-VA1	QFN68 RTL8721DM-VA1	QFN68 RTL8721DN-VRC	QFN88 RTL8722DM-VA1	Description
ADC_0/TOUCH_KEY0	I	-	44	45	59	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_1/TOUCH_KEY1	I	-	45	46	60	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_2/TOUCH_KEY2	I	-	46	47	61	ADC or Cap-Touch input pin, 3.3V tolerance

ADC_3/TOUCH_KEY3	I	-	47	48	62	ADC or Cap-Touch input pin, 3.3V tolerance
ADC_4	I	33	41	42	57	ADC input pin, 3.3V tolerance
ADC_5	I	32	42	43	56	ADC input pin, 3.3V tolerance
ADC_6	I	34	43	44	58	ADC input pin, 3.3V tolerance
VBAT_MEAS	I	-	48	49	63	ADC input pin, 5V tolerance

3.7 USB Pins

The USB pins in RTL872xD are shown in Table 3-8.

Table 3-8 USB pins

Symbol	Type	QFN48	QFN68	QFN68	QFN88	Description
		RTL8720DN-VA1 RTL8720DM-VA1	RTL8721DM-VA1	RTL8721DN-VRC	RTL8722DM-VA1	
HSDP	I/O	29	39	40	54	USB differential bus
HSDM	I/O	30	40	41	55	USB differential bus
RREF	I	28	38	39	53	External reference resistor for USB analog, 1% accuracy

3.8 Audio Codec Pins

The audio codec pins in RTL872xD are shown in Table 3-9.

Table 3-9 Audio codec pins

Symbol	Type	QFN48	QFN68	QFN88	Description
MIC1_P	AH	-	3	5	MIC1 input positive pad. Used as main MIC in dual MIC application. Programmable digital I/O, refer to pinmux table (UM0402 RTL872xD pinmux table).
MIC2_N	AH	-	-	7	MIC2 input negative pad. Used as 2nd MIC in dual MIC application. Programmable digital I/O, refer to pinmux table.
MIC2_P	AH	-	4	6	MIC2 input positive pad. Used as 2nd MIC in dual MIC application. Programmable digital I/O, refer to pinmux table.
AOUTN_R	AH	-	-	85	Right channel analog output negative pad. Programmable digital I/O, refer to pinmux table.
AOUTP_R	AH	-	64	84	Right channel analog output positive pad. Programmable digital I/O, refer to pinmux table.
AOUTN_L	AH	-	NA	86	Left channel analog output negative pad. Programmable digital I/O, refer to pinmux table.
AOUTP_L	AH	-	65	87	Left channel analog output positive pad. Programmable digital I/O, refer to pinmux table.
AUXIN_R	AH	-	-	9	AUX input right channel pad. Programmable digital I/O, refer to pinmux table.
AUXIN_L	AH	-	-	8	AUX input left channel pad. Programmable digital I/O, refer to pinmux table.
AVCC_DRV	PI	-	66	88	1.8V/3.3V power supply for internal audio codec LDO.
MIC_BIAS	PO	-	2	4	Microphone bias output
AUDIO_VREF	PO	-	1	3	Codec bandgap reference output, add a 4.7nF cap as close as possible.
AVCC	PO	-	67	2	AVCC output from internal audio codec LDO, add a 1uF cap as close as possible.
AUDIO_GND	PO	-	68	1	Audio ground

4 Memory Organization

4.1 Introduction

The RTL872xD incorporates several distinct memory regions. Program memory, data memory, registers and I/O ports are organized within the same linear 4Gbytes address space. The bytes are coded in memory in Little-Endian format.

The addressable memory space is divided into multiple main blocks, as shown in Table 4-1. All the memory areas that are not allocated to on-chip memories and peripherals are considered “RSVD” (reserved). For the detailed mapping of available memory and register areas, refer to the following sections.

Table 4-1 Address space main blocks

Base Address	Top Address	Size	Function	Description
0x0000_0000	0x0001_FFFF	128KB	KM0 ITCM ROM (actually 96KB)	32MB: KM0 Memory Address
0x0002_0000	0x0002_7FFF	32KB	KM0 DTCM ROM (actually 16KB)	
0x0002_8000	0x0007_FFFF	352KB	RSVD	
0x0008_0000	0x0008_FFFF	64KB	KM0 SRAM	
0x0009_0000	0x000B_FFFF	192KB	RSVD	
0x000C_0000	0x000C_3FFF	16KB	Retention SRAM (1KB) (The same port with KM0 SRAM)	
0x000C_4000	0x000F_FFFF	240KB	RSVD	
0x0010_0000	0x01FF_FFFF	31MB	RSVD	
0x0200_0000	0x07FF_FFFF	96MB	External PSRAM	224MB: External Memory Address
0x0800_0000	0x0FFF_FFFF	128MB	External FLASH	
0x1000_0000	0x1007_FFFF	512KB	KM4 SRAM	256MB: KM4 Memory Address
0x1008_0000	0x100D_FFFF	384KB	RSVD	
0x100E_0000	0x100E_FFFF	64KB	Extension SRAM0 from Bluetooth	
0x100F_0000	0x100F_FFFF	64KB	Extension SRAM1 from Wi-Fi	
0x1010_0000	0x1013_FFFF	256KB	KM4 ITCM ROM	
0x101C_0000	0x101D_7FFF	96KB	KM4 DTCM ROM	
0x101C_0000	0x101F_FFFF	256KB	RSVD	
0x1020_0000	0x1FFF_FFFF	254MB	RSVD	
0x2000_0000	0x3FFF_FFFF	512MB	RSVD	Reserved
0x4000_0000	0x47FF_FFFF	128MB	KM4 Peripherals	128MB: KM4 Peripherals Address
0x4800_0000	0x4FFF_FFFF	128MB	KM0 Peripherals	128MB: KM4 Peripherals Secure Address
0x5000_0000	0x57FF_FFFF	128MB	KM4 Peripherals Secure	128MB: KM0 Peripherals Address
0x5800_0000	0xFFFF_FFFF	2816MB	RSVD	Reserved

4.2 KM4 Memory Map and Register Boundary Addresses

Table 4-2 gives the boundary addresses of the peripherals available in the KM4 devices.

Table 4-2 KM4 register boundary addresses

Port Name	Security	Base Address	Top Address	Size
KM4_SRAM1	IDAU	0x1000_0000	0x1003_FFFF	256KB
KM4_SRAM2	IDAU	0x1004_0000	0x1007_FFFF	256KB
Extension SRAM	IDAU	0x100E_0000	0x100F_FFFF	128KB
PSRAM Memory	IDAU	0x0200_0000	0x07FF_FFFF	96MB
HS_SYSON	NS	0x4000_0000	0x4000_0FFF	4KB
	S	0x5000_0000	0x5000_0FFF	4KB
HS_TIM0 ~ 3/4/5	NS	0x4000_2000	0x4000_2FFF	4KB
HS_UART0	NS	0x4000_4000	0x4000_4FFF	4KB

HS_IPC	NS	0x4000_6000	0x4000_6FFF	4KB
HS_USI	NS	0x4000_8000	0x4000_83FF	1KB
HS_UART1 (Bluetooth)	NS	0x4000_A000	0x4000_AFFF	4KB
RXI300_KM4	NS	0x4000_C000	0x4000_CFFF	4KB
	S	0x5000_C000	0x5000_CFFF	4KB
HS_SPI1	NS	0x4000_E000	0x4000_E7FF	2KB
Audio Codec	NS	0x4001_0000	0x4001_0FFF	4KB
HS_IR	NS	0x4001_2000	0x4001_2FFF	4KB
PSRAM Controller	NS	0x4001_4000	0x4001_4FFF	4KB
I^2S	NS	0x4002_0000	0x4002_03FF	1KB
Secure Engine	NS	0x4002_2000	0x4002_5FFF	16KB
	S	0x5002_2000	0x5002_5FFF	16KB
SDIO Host	NS	0x4002_6000	0x4002_9FFF	16KB
HS_GDMA0	NS	0x4002_A000	0x4002_BFFF	8KB
	S	0x5002_A000	0x5002_BFFF	8KB
SDIO Device	NS	0x4002_C000	0x4002_FFFF	16KB
USB	NS	0x4003_0000	0x4006_FFFF	256KB
LCD Controller	NS	0x4007_0000	0x4007_4FFF	20KB
HS_SPI0	NS	0x4007_8000	0x4007_87FF	2KB
Wi-Fi	NS	0x4008_0000	0x400A_FFFF	192KB
KM0 BRG	NS	0x0008_0000	0x0008_FFFF	64KB
		0x000C_0000	0x000C_3FFF	16KB
		0x4800_0000	0x4803_FFFF	256KB
Flash Controller	NS	0x4808_0000	0x4808_0FFF	4KB
Flash Memory	IDAU	0x0800_0000	0x0FFF_FFFF	128MB

4.3 KM0 Memory Map and Register Boundary Addresses

Table 4-3 gives the boundary addresses of the peripherals available in the KM0 devices.

Table 4-3 KM0 register boundary addresses

Port Name	Base Address	Top Address	Size
KM0_SRAM	0x0008_0000	0x0008_FFFF	64KB
1KB Retention SRAM	0x000C_0000	0x000C_3FFF	16KB
KM4 BRG	0x1000_0000	0x1007_FFFF	512KB
	0x4000_0000	0x4007_FFFF	512KB
Wi-Fi FW	0x4008_0000	0x400A_FFFF	192KB
LP_SYSON	0x4800_0000	0x4800_0FFF	4KB
LP_TIM0 ~ 3/4/5	0x4800_2000	0x4800_2FFF	4KB
LP_RTC	0x4800_4000	0x4800_43FF	1KB
LP_IPC	0x4800_6000	0x4800_63FF	1KB
Key-Scan	0x4800_A000	0x4800_A3FF	1KB
I^2C0	0x4800_C000	0x4800_C3FF	1KB
UART3	0x4800_E000	0x4800_E3FF	1KB
LP_GDMA0	0x4801_0000	0x4801_07FF	2KB
UART2 (LOGUART)	0x4801_2000	0x4801_23FF	1KB
GPIOA/B	0x4801_4000	0x4801_47FF	2KB
RXI300_KM0	0x4801_8000	0x4801_8FFF	4KB
SGPIO	0x4801_A000	0x4801_AFFF	4KB
Cap-Touch/ADC/Comparator	0x4801_C000	0x4801_CFFF	4KB
Q-Decoder	0x4801_E000	0x4801_EFFF	4KB
Flash Controller	0x4808_0000	0x4808_0FFF	4KB
Flash Memory	0x0800_0000	0x0FFF_FFFF	128MB

4.4 KM4 Embedded SRAM

The KM4 contains up to a total 512KB of contiguous, on-chip static RAM memory. This embedded SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits). It is divided into the following two blocks which can be accessed by both KM4 and KM0.

- KM4 SRAM1 (up to 256KB)
- KM4 SRAM2 (up to 256KB)

Dividing SRAM into two slave ports allows user's program to potentially obtain better performance. For example, simultaneous access to SRAM1 by the CPU and by the system DMA controller does not result in any bus stalls for either master.

Generally speaking, the CPU reads or writes all peripheral data at some point, even when all such data is read from or sent to a peripheral by DMA. So, minimizing stalls is likely to involve putting data to/from different peripherals in RAM on each port.

Alternatively, sequences of data from the same peripheral can be alternated between RAM on each port. This could be helpful if DMA fills or empties a RAM buffer, and signals the CPU before proceeding on to a second buffer. The CPU then tends to access the data while the DMA is using the other RAM.

In power domains, the entire SRAM is also divided into three blocks:

- SRAM_PD1 (up to 256KB)
- SRAM_PD2 (up to 128KB)
- SRAM_PD3 (up to 128KB)

Each block can be disabled or enabled individually in the Power Management Unit (PMU) block to save power, and the entire SRAM can also keep power for quickly resuming from sleep mode when system enters sleep mode.

4.5 KM0 Embedded SRAM

The KM0 features 64KB of system SRAM, the embedded SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits).

This SRAM can be accessed by both KM4 and KM0.

4.6 KM4 Extension SRAM

When Bluetooth is disabled, more 64KB SRAM will be extended. This SRAM can also be accessed by both KM4 and KM0, up to 50MHz*32 bits.

4.7 Retention SRAM

The RTL872xD features 1KB of retention SRAM in order to allow saving data with minimal power usage during deepsleep mode.

This SRAM can be accessed by both KM4 and KM0.

4.8 SPI Flash Memory

The SPI Flash Controller (SPIC) manages CPU I-Code and D-Code accesses to the Flash memory. It implements the erase and program Flash memory operations, and the read/write protection mechanisms. It accelerates code execution with a system of instruction prefetch and cache lines.

4.9 PSRAM

4MB 8IO DDR PSRAM is included in RTL872xD, up to 50MHz DDR.

5 Nested Vectored Interrupt Controller (NVIC)

5.1 Features

All interrupts including the core exceptions are managed by the NVIC. The nested vector interrupt controller NVIC includes the following features:

- Nested Vectored Interrupt Controller that is an integral part of each CPU.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- The NVIC of the KM4 supports:
  - 58 vectored interrupts.
  - 8 programmable interrupt priority levels with hardware priority level masking.
  - Vector table offset register VTOR.
- The NVIC of the KM0 supports:
  - 32 vectored interrupts.
  - 4 programmable interrupt priority levels with hardware priority level masking.
  - Vector table offset register VTOR.
- Support for NMI from any interrupt.

The NVIC and the processor core interface are closely coupled, which enables low latency interrupt processing and efficient processing of late arriving interrupts.

5.2 NVIC Diagram

The diagram of NVIC is shown in Fig 5-1.

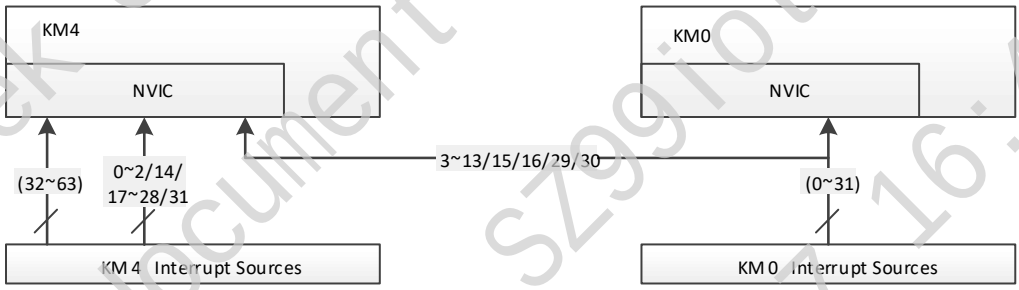


Fig 5-1 NVIC diagram

Most of KM0 interrupt signals are linked to KM4 NVIC at the same interrupt number like LOGUART, and other KM0 interrupt signals are not linked to KM4 NVIC like WDG/RXI300/IPC.

This mechanism let KM4 use KM0's peripheral like it is KM4's peripheral. But if an interrupt signal is shared by KM0 and KM4, just only one CPU can open this interrupt, if not, software will hang.

5.3 NVIC Table

Table 5-1 lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the Vectored Interrupt Controller. Each line may represent more than one interrupt source. The interrupt number does not imply any interrupt priority.

Note: The macro "configLIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY", which is used to define the highest interrupt priority controlled by FreeRTOS, is very important to interrupt. If the interrupt safe FreeRTOS API functions are called by the interrupt service routine, the priority of it must not be higher than this macro. Do not call RTOS _ISR functions from any interrupt that has a higher priority than this macro.

Table 5-1 NVIC table

IRQ	KM4 Name	KM0 Name	Description
	Reset	Reset	Reset
	NMI	NMI	Non-maskable interrupts (external NMI input). The WDG is linked to the NMI vector
	Hard Fault	Hard Fault	All fault conditions if the corresponding fault handler is not enabled
	MemManager Fault	MemManager Fault	Memory management fault; Memory Protection Unit (MPU) violation or access to illegal locations
	Bus Fault	Bus Fault	Bus error; occurs when Advanced High-Performance Bus (AHB) interface receives an error response from a bus slave (also called pre-fetch abort if it is an instruction fetch or data abort if it is a data access)
	Usage Fault	Usage Fault	Exceptions resulting from program error or trying to access coprocessor (the Cortex-M4 does not support a coprocessor)
	RSVD	RSVD	Reserved
	SVC	SVC	Supervisor Call
	Debug Monitor	Debug Monitor	Debug monitor (breakpoints, watch-points, or external debug requests)
	RSVD	RSVD	Reserved
	PendSV	PendSV	Pendable Service Call
	SYSTICK	SYSTICK	System Tick Timer
0	KM4_System_ISR	KM0_System_ISR	● KM4: System ISR include wakeup event, like HS BT/-USB-dev/SDIO-dev/UART0 ● KM0: LS peripheral wakeup event, like GPIO/LUART/I2C0, etc.
1	WDG_ISR_H	WDG_ISR_L	KM4 & KM0 watchdog warning interrupt
2	RXI300_IRQ_H	RXI300_IRQ_L	● KM4 RXI300 platform interrupt ● KM0 RXI300 platform interrupt
3	UART log	UART log	KM4 & KM0 LP_UART0 (LOGUART) interrupt
4	GPIOA	GPIOA	KM4 & KM0 GPIO PortA Interrupt (GPIO IP0 PORTA)
5	RTC	RTC	KM4 & KM0 RTC interrupt
6	I2C0	I2C0	KM4 & KM0 I2C0 interrupt
7	SPI_FLASH	SPI_FLASH	KM4 & KM0 SPI FLASH interrupt
8	GPIOB	GPIOB	KM4 & KM0 GPIO PortB Interrupt (GPIO IP1 PORTA)
9	LUART	LUART	KM4 & KM0 LP_UART1 interrupt
10	Key-Scan	Key-Scan	KM4 & KM0 Key-Scan interrupt
11	Cap-Touch	Cap-Touch	KM4 & KM0 Cap-Touch interrupt
12	BOR2	BOR2	KM4 & KM0 BOR interrupt
13	SGPIO	SGPIO	KM4 & KM0 SGPIO interrupt
14	IPC_KM0	IPC_KM4	IPC interrupt: ● KM0 IPC interrupt KM4 ● KM4 IPC interrupt KM0
15	ADC	ADC	KM4 & KM0 ADC interrupt
16	Q-Decoder	Q-Decoder	KM4 & KM0 Q-Decoder interrupt
17	HTimer0	LTimer0	● KM4 HTimer0 interrupt ● KM0 LTimer0 interrupt
18	HTimer1	LTimer1	● KM4 HTimer1 interrupt ● KM0 LTimer1 interrupt
19	HTimer2	LTimer2	● KM4 HTimer2 interrupt ● KM0 LTimer2 interrupt
20	HTimer3	LTimer3	● KM4 HTimer3 interrupt ● KM0 LTimer3 interrupt
21	HTimer4	LTimer4	● KM4 HTimer4 interrupt ● KM0 LTimer4 interrupt
22	HTimer5	LTimer5	● KM4 HTimer5 interrupt ● KM0 LTimer5 interrupt
23	LCDC	LGDMA0_Channel0	● KM4 LCDC interrupt ● KM0 LGDMA0_Channel0 interrupt
24	USB	LGDMA0_Channel1	● KM4 USB interrupt

			• KM0 LGDMA0_Channel1 interrupt
25	SDIO_DEV	LGDMA0_Channel2	• KM4 SDIO_DEV interrupt • KM0 LGDMA0_Channel2 interrupt
26	SD_HOST	Wi-Fi FISR (0x134) + FESR (0x124)	• KM4 SD_HOST interrupt • KM0 Wi-Fi FISR + FESR interrupt
27	IPSEC	Wi-Fi FTSR (0x13C) + mailbox	• KM4 SD_HOST interrupt • KM0 Wi-Fi FTSR + mailbox interrupt
28	I2S0	LGDMA0_Channel3	• KM4 I2S0 interrupt • KM0 LGDMA0_Channel3 interrupt
29	PWR_DOWN	PWR_DOWN	KM4 & KM0 PWR_DOWN interrupt, this interrupt will be triggered when power down pin push under power down interrupt mode
30	ADC_COMP	ADC_COMP	KM4 & KM0 ADC comparator interrupt
31	WL_DMA	KM4_WAKE_ISR	• KM4 WL_DMA interrupt • KM0: KM4 peripherals wake interrupt, the same as KM4_System_ISR
32	WL_PROTOCOL (0xB4)	-	KM4 WL_PROTOCOL interrupt
33	PSRAMC	-	KM4 PSRAMC interrupt
34	UART0	-	KM4 HS_UART0 interrupt
35	UART1_BT	-	KM4 HS_UART1_BT interrupt
36	SPI0	-	KM4 HS_SPI0 interrupt
37	SPI1	-	KM4 HS_SPI1 interrupt
38	HUSI0	-	KM4 HS_USI0 interrupt
39	IR	-	KM4 IR interrupt
40	BT_SCORE_BOARD	-	KM4 BT_SCORE_BOARD interrupt
41	GDMA0_Channel0	-	KM4 HS_GDMA0_Channel0 interrupt
42	GDMA0_Channel1	-	KM4 HS_GDMA0_Channel1 interrupt
43	GDMA0_Channel2	-	KM4 HS_GDMA0_Channel2 interrupt
44	GDMA0_Channel3	-	KM4 HS_GDMA0_Channel3 interrupt
45	GDMA0_Channel4	-	KM4 HS_GDMA0_Channel4 interrupt
46	GDMA0_Channel5	-	KM4 HS_GDMA0_Channel5 interrupt
47	RSVD	-	Reserved
48	RSVD	-	Reserved
49	RSVD	-	Reserved
50	IPSEC_S	-	KM4 HS_IPSEC TrustZone interrupt
51	RXI300_IRQ_S	-	KM4 HS_RXI300 TrustZone interrupt
52	GDMA0_Channel0_S	-	KM4 HS_GDMA0_Channel0 TrustZone interrupt
53	GDMA0_Channel1_S	-	KM4 HS_GDMA0_Channel1 TrustZone interrupt
54	GDMA0_Channel2_S	-	KM4 HS_GDMA0_Channel2 TrustZone interrupt
55	GDMA0_Channel3_S	-	KM4 HS_GDMA0_Channel3 TrustZone interrupt
56	GDMA0_Channel4_S	-	KM4 HS_GDMA0_Channel4 TrustZone interrupt
57	GDMA0_Channel5_S	-	KM4 HS_GDMA0_Channel5 TrustZone interrupt

6 Wi-Fi Radio Characteristics

6.1 Wi-Fi RF Block Diagram

The Wi-Fi RF block diagram of RTL872xD is given in Fig 6-1.

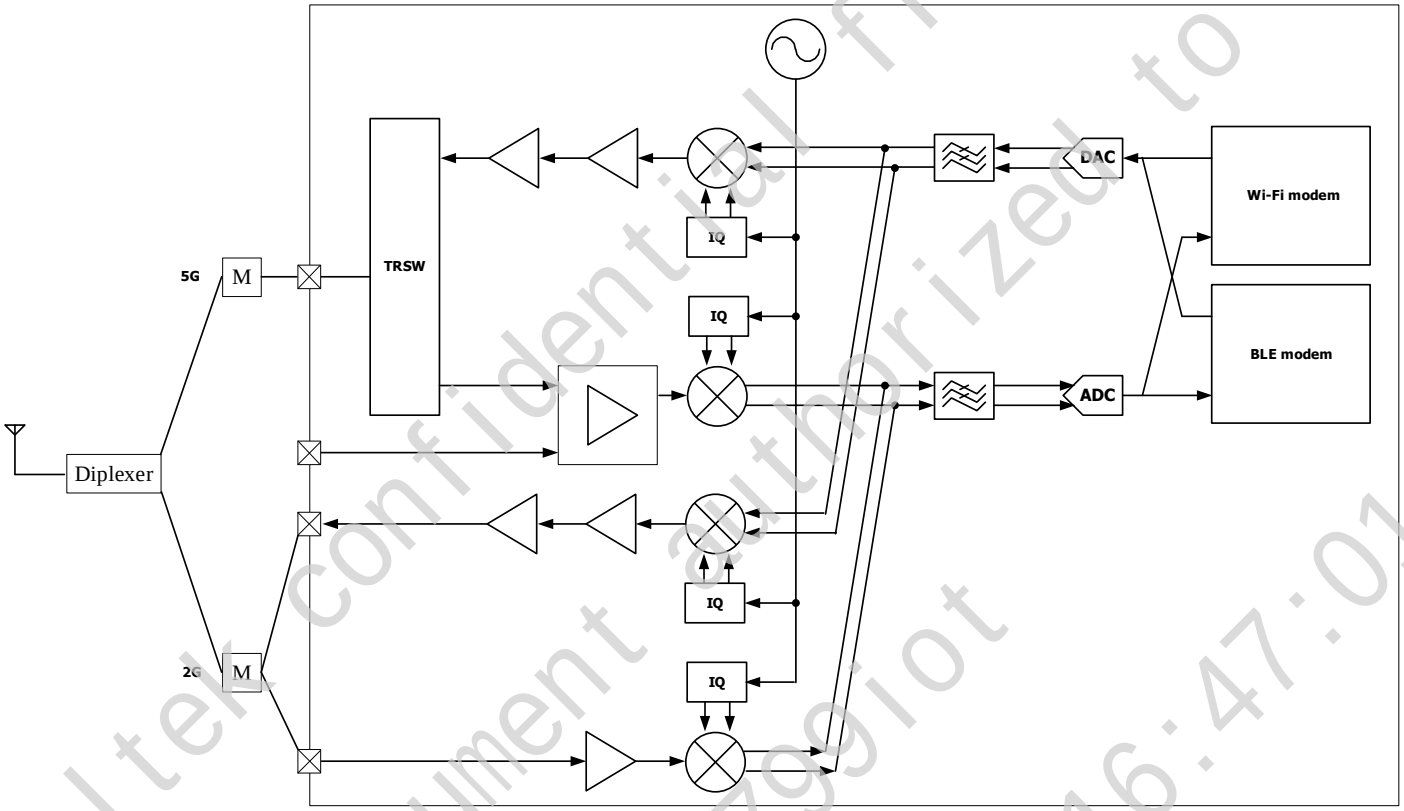


Fig 6-1 Wi-Fi RF block diagram

The radio frequency (RF) specifications of Wi-Fi are described in the tables below. These values are measured on the QFN68 board.

6.2 Wi-Fi 2.4GHz Band RF Receiver Specifications

Parameter	Description	Performance (1.8V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412	-	2484	2412	-	2484	MHz
Rx Sensitivity	1Mbps CCK	-99.5	-98.7	-98	-99.1	-98.6	-97.5	dBm
	2Mbps CCK	-96	-96	-95.5	-97	-95.9	-95.5	
	5.5Mbps CCK	-94.5	-94.4	-93.5	-94.5	-94.2	-93.5	
	11Mbps CCK	-91.5	-91.0	-90	-91.5	-91.1	-90.6	
Rx Sensitivity	BPSK rate 1/2, 6Mbps OFDM	-96	-95.7	-94.5	-96	-95.4	-94.3	dBm
	BPSK rate 3/4, 9Mbps OFDM	-94.5	-94.4	-93	-94.5	-94.3	-93.9	
	QPSK rate 1/2, 12Mbps OFDM	-93	-92.9	-92	-93	-92.9	-92.5	
	QPSK rate 3/4, 18Mbps OFDM	-90.5	-90.3	-89	-91	-90.4	-90	
	16QAM rate 1/2, 24Mbps OFDM	-87	-86.9	-86	-87	-86.8	-86.4	
	16QAM rate 3/4, 36Mbps OFDM	-84	-83.8	-82.5	-84	-83.8	-83.4	

	64QAM rate 1/2, 48Mbps OFDM	-79.5	-79.3	-78.5	-79.5	-79.2	-78.9	
	64QAM rate 3/4, 54Mbps OFDM	-78	-77.9	-76.5	-78.1	-77.8	-77	
Rx Sensitivity BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-95.5	-95.3	-94.5	-95.5	-95.1	-94.1	dBm
	MCS 1, QPSK rate 1/2	-92	-92	-91.5	-92.2	-92	-91.7	
	MCS 2, QPSK rate 3/4	-90	-89.4	-88.5	-90	-89.4	-89	
	MCS 3, 16QAM rate 1/2	-86.5	-86.2	-85.5	-86.5	-85.8	-84	
	MCS 4, 16QAM rate 3/4	-83.5	-82.9	-82	-83.2	-82.9	-82.5	
	MCS 5, 64QAM rate 2/3	-78.5	-78.4	-77.5	-78.5	-78.4	-78	
	MCS 6, 64QAM rate 3/4	-77	-76.8	-76	-77	-76.7	-76.4	
	MCS 7, 64QAM rate 5/6	-76	-75.4	-74	-75.7	-75.4	-75	
Rx Sensitivity BW = 40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-93	-92.5	-92.5	-93	-92.5	-92.2	dBm
	MCS 1, QPSK rate 1/2	-89.5	-89.1	-89	-89.5	-88.7	-87	
	MCS 2, QPSK rate 3/4	-86.5	-86.5	-86	-87	-86.5	-86.4	
	MCS 3, 16QAM rate 1/2	-83.5	-83.4	-83	-83.5	-83.3	-83	
	MCS 4, 16QAM rate 3/4	-80	-80	-79.5	-80	-79.9	-79	
	MCS 5, 64QAM rate 2/3	-75.5	-75.3	-73.5	-75.5	-75.4	-75	
	MCS 6, 64QAM rate 3/4	-74.5	-74	-73	-74.5	-74	-73.9	
	MCS 7, 64QAM rate 5/6	-73	-72.5	-72	-73	-72.5	-72.3	
Maximum Receive Level	6Mbps OFDM	-	0	-	-	0	-	dBm
	54Mbps OFDM	-	0	-	-	0	-	
	MCS 0	-	0	-	-	0	-	
	MCS 7	-	0	-	-	0	-	
Receive Adjacent Channel Rejection	1Mbps CCK	40	43	44	42	43	44	dBm
	11Mbps CCK	39	40	41	39	41	42	
	BPSK rate 1/2, 6Mbps OFDM	39	40	41	39	40	41	
	64QAM rate 3/4, 54Mbps OFDM	20	22	23	20	22	24	
	HT20, MCS 0, BPSK rate 1/2	39	39	40	39	39	40	
	HT20, MCS 7, 64QAM rate 5/6	19	20	21	19	20	21	
	HT40, MCS 0, BPSK rate 1/2	29	30	32	27	29	32	
	HT40, MCS 7, 64QAM rate 5/6	10	11	13	9	10	11	

6.3 Wi-Fi 2.4GHz Band RF Transmitter Specifications

Parameter	Description	Performance (1.8V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412	-	2484	2412	-	2484	MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK	-	14	-	-	21	-	dBm
	11Mbps CCK	-	14	-	-	21	-	dBm
	BPSK rate 1/2, 6Mbps OFDM	-	13	-	-	19	-	dBm
	64QAM rate 3/4, 54Mbps OFDM	-	12	-	-	18	-	dBm
	HT20-MCS 0, BPSK rate 1/2	-	12	-	-	18	-	dBm
	HT20-MCS 7, 64QAM rate 5/6	-	11	-	-	17.5	-	dBm
	HT40-MCS 0, BPSK rate 1/2	-	12	-	-	18	-	dBm
	HT40-MCS 7, 64QAM rate 5/6	-	11	-	-	17.5	-	dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM	-	-	-5	-	-	-5	dB
	64QAM rate 3/4, 54Mbps OFDM	-	-	-25	-	-	-25	dB
	HT20-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	dB
	HT20-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	dB
	HT40-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	dB
	HT40-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	dB
Output power variation[2]	After do power trim at FT	-1.5	-	1.5	-1.5	-	1.5	dBm
Carrier suppression		-	-	-30	-	-	-30	dBm
	2nd harmonic	-	-36	-34	-	-23	-21.9	dBm

Harmonic output power (IC port)	3rd harmonic	-	-26	-24	-	-15	-14	dBm

1. Power level is tested after DPK on.
2. VDD18 voltage is within ±5% of typical value.

6.4 Wi-Fi 5GHz Band RF Receiver Specifications

Parameter	Description	Performance (1.8V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180	-	5825	5180	-	5825	MHz
Rx Sensitivity	BPSK rate 1/2, 6Mbps OFDM	-95	-94.6	-93	-94.5	-93.6	-92	dBm
	BPSK rate 3/4, 9Mbps OFDM	-93.5	-93.2	-92.5	-93.5	-92.8	-91	
	QPSK rate 1/2, 12Mbps OFDM	-92.5	-91.8	-91	-92	-91.5	-90.5	
	QPSK rate 3/4, 18Mbps OFDM	-90	-89.3	-88.5	-90	-89.1	-88	
	16QAM rate 1/2, 24Mbps OFDM	-86.5	-85.8	-85	-86.5	-85.6	-84.5	
	16QAM rate 3/4, 36Mbps OFDM	-83.5	-82.9	-82	-83.5	-82.8	-82	
	64QAM rate 1/2, 48Mbps OFDM	-79	-78.3	-77.5	-79	-78.3	-77.5	
	64QAM rate 3/4, 54Mbps OFDM	-77.5	-76.7	-76	-77.5	-76.7	-76	
Rx Sensitivity BW = 20MHz HT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-94.5	-94.1	-93	-94	-93.3	-91.5	dBm
	MCS 1, QPSK rate 1/2	-91.5	-90.9	-89.5	-91.5	-90.7	-89.5	
	MCS 2, QPSK rate 3/4	-89	-88.4	-87.5	-89	-88.2	-87	
	MCS 3, 16QAM rate 1/2	-86	-85.2	-84.5	-86	-85	-84	
	MCS 4, 16QAM rate 3/4	-82.5	-82.1	-81	-82.6	-81.9	-80.5	
	MCS 5, 64QAM rate 2/3	-78	-77.4	-76.5	-78	-77.1	-76	
	MCS 6, 64QAM rate 3/4	-76.5	-75.7	-75	-76.5	-75.4	-74	
	MCS 7, 64QAM rate 5/6	-75	-74.1	-73	-74.8	-73.7	-72.5	
Rx Sensitivity BW = 40MHz HT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2	-92	-91.3	-90.5	-91.5	-90.6	-88.5	dBm
	MCS 1, QPSK rate 1/2	-88.5	-88.1	-87.5	-88.5	-87.8	-86.5	
	MCS 2, QPSK rate 3/4	-86	-85.4	-85	-85.5	-85.2	-83.5	
	MCS 3, 16QAM rate 1/2	-82.5	-82.2	-81.5	-82.5	-82.1	-81	
	MCS 4, 16QAM rate 3/4	-79	-78.9	-78	-79	-78.7	-78	
	MCS 5, 64QAM rate 2/3	-75	-74.3	-74	-74.5	-74	-73	
	MCS 6, 64QAM rate 3/4	-73.5	-73	-71	-73.5	-72.8	-72	
	MCS 7, 64QAM rate 5/6	-72	-71.6	-71	-72	-71.3	-70.5	
Maximum Receive Level	6Mbps OFDM	-	0	-	-	0	-	dBm
	54Mbps OFDM	-	0	-	-	0	-	
	MCS 0	-	0	-	-	0	-	
	MCS 7	-	0	-	-	0	-	
Receive Adjacent Channel Rejection	BPSK rate 1/2, 6Mbps OFDM	20	21	24	19	21	23	dBm
	64QAM rate 3/4, 54Mbps OFDM	11	12	12	10	11	12	
	HT20, MCS 0, BPSK rate 1/2	19	21	22	19	19	20	
	HT20, MCS 7, 64QAM rate 5/6	7	7	8	7	7	9	
	HT40, MCS 0, BPSK rate 1/2	29	30	31	29	30	31	
	HT40, MCS 7, 64QAM rate 5/6	11	12	14	11	13	14	

6.5 Wi-Fi 5GHz Band RF Transmitter Specifications

Parameter	Description	Performance (1.8V)			Performance (3.3V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180	-	5825	5180	-	5825	MHz
	BPSK rate 1/2, 6Mbps OFDM	-	11	-	-	17	-	dBm
	64QAM rate 3/4, 54Mbps OFDM	-	10	-	-	16	-	dBm

Output power with spectral mask and EVM compliance[1]	HT20-MCS 0, BPSK rate 1/2	-	10	-	-	16	-	dBm
	HT20-MCS 7, 64QAM rate 5/6	-	9	-	-	15	-	dBm
	HT40-MCS 0, BPSK rate 1/2	-	10	-	-	16	-	dBm
	HT40-MCS 7, 64QAM rate 5/6	-	9	-	-	15	-	dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM	-	-	-5	-	-	-5	dB
	64QAM rate 3/4, 54Mbps OFDM	-	-	-25	-	-	-25	dB
	HT20-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	dB
	HT20-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	dB
	HT40-MCS 0, BPSK rate 1/2	-	-	-5	-	-	-5	dB
	HT40-MCS 7, 64QAM rate 5/6	-	-	-28	-	-	-28	dB
Output power variation[2]	After doing power trim at FT	-1.5	-	1.5	-1.5	-	1.5	dBm
Carrier suppression		-	-	-30	-	-	-30	dBm

1. Power level is tested after DPK on.
2. VDD18 voltage is within ±5% of typical value.

7 Electrical Characteristics

7.1 Temperature Limit Ratings

The temperature limit ratings of RTL872xD are listed in Table 7-1.

Table 7-1 Temperature limit ratings

Parameter	Minimum	Maximum	Unit
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	0	+125	°C

7.2 DC Characteristics

The direct current (DC) characteristics of power supply and digital I/O pin are illustrated in the following sections.

7.2.1 Power Supply

The power supply DC characteristics of RTL872xD are shown in Table 7-2.

Table 7-2 Power supply DC characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VA1833_XTAL, VR1833_SYN, VR1833_PAD_A, VR1833_PA_A, VR1833_PA_G, VA1833_USB, VA1833_PLL, VD1833_PMU, VD1833_SPS/VD1833_FLASH, AVCC_DRIV	1.85V or 3.3V Supply Voltage	1.76	1.85, 3.3	3.6	V
VD1833_GPIO	Digital I/O Supply Voltage	0.99	1.8 ~ 3.3	3.6	V
VA11_AFE, VA11_SYN, VA11_RF1, VA11_RF2, VD11_CORE, VA11_PLL	1.1V Core Supply Voltage	1.08	1.1	1.21	V
IDD33	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA
IDD_IO	I/O Rating Current (including VDD_IO)	-	-	200	mA
IDD_IO_33	3.3V I/O Rating Current	-	-	50	mA

7.2.2 Digital I/O Pin

The digital I/O pin DC characteristics of RTL872xD are shown in Table 7-3 and Table 7-4, which illustrate 3.3V and 1.8V respectively.

Table 7-3 Digital I/O pin DC characteristics (3.3V)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
I_{T+}	Schmitt-trigger High Level		1.78	1.87	1.97	V
I_{T-}	Schmitt-trigger Low Level		1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	V_{IN} = 3.3V or 0	-10	±1	10	μA

Table 7-4 Digital I/O pin DC characteristics (1.8V)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input-High Voltage	CMOS	0.65 * Vcc	-	-	V

V_{IL}	Input-Low Voltage	CMOS	-	-	0.35 * Vcc	V
V_{OH}	Output-High Voltage	CMOS	Vcc-0.45	-	-	V
V_{OL}	Output-Low Voltage	CMOS	-	-	0.45	V
I_{T+}	Schmitt-trigger High Level	-	1.02	1.09	1.14	V
I_{T-}	Schmitt-trigger Low Level	-	0.67	0.73	0.87	V
I_{IL}	Input-Leakage Current	V_{IN} = 1.8V or 0	-10	±1	10	μA

7.3 Power State and Power Sequence

The timing specification of power sequence is listed in Table 7-5.

Table 7-5 Timing specification of power sequence

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{PRDY}	VDD*x* ready time	0.6	0.6	1	ms
T_{CLK}	Internal ring clock stable time after VDD1833 ready	1	-	-	ms
T_{core}	LP core power ready time	1.5	1.5	-	ms
T_{boot}	HS MCU boot time	200	200	-	ms
V_{RST}	Shutdown occurs after CHIP_EN lower than this voltage	0	0	0.5 * VDD*x*	V
T_{RST}	The required time that CHIP_EN lower than V_{RST}	1	1	-	ms

Note: VDD*x* is the supply power of VD1833.

7.3.1 Power on or Resuming from Deepsleep Sequence

The timing sequence of power on or resuming from deepsleep is given in Fig 7-1.

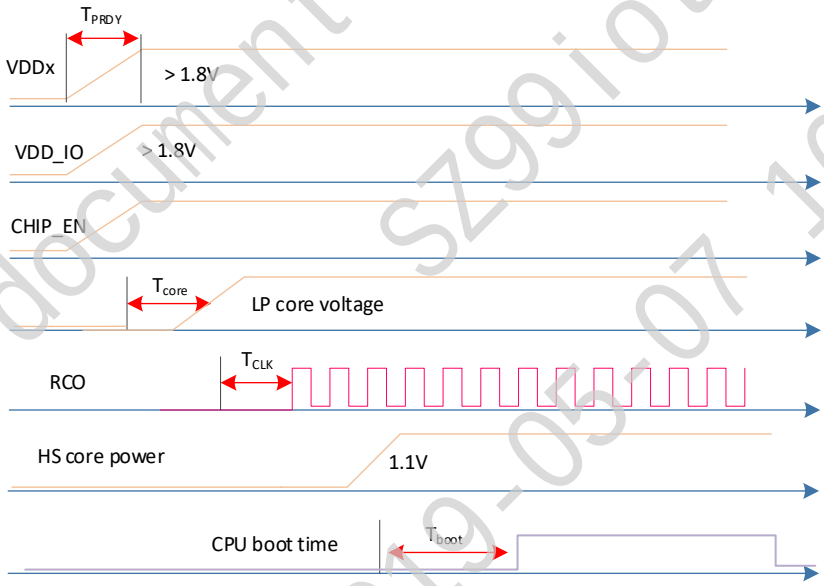


Fig 7-1 Timing sequence of power on or resuming from deepsleep

7.3.2 Shutdown Sequence

The timing sequence of shutdown is illustrated in Fig 7-2.

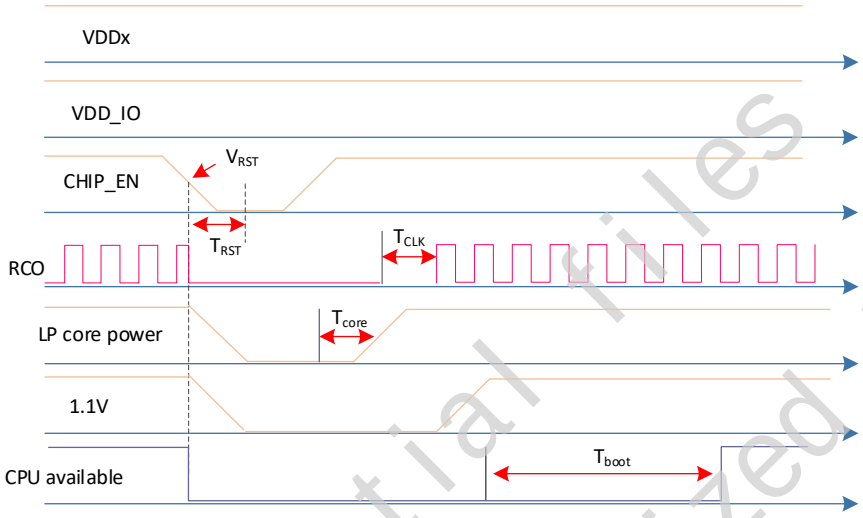
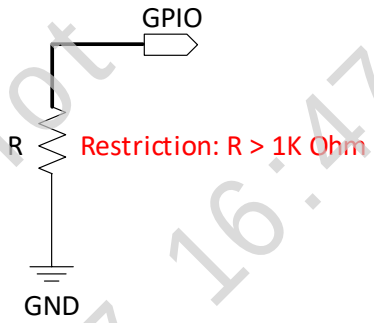


Fig 7-2 Timing sequence of shutdown

7.4 GPIO Pull Low Restriction

When one of the GPIOs listed below needs to be pulled low by a resistor on PCB, the pull low resistor value must > 1K Ohm.

Port Name	Resistor Value	Schematic
PA[7]	R > 1K Ohm	
PA[8]		
PA[9]		
PA[10]		
PA[11]		
PA[12]		
PA[13]		
PA[14]		
PA[15]		
PA[16]		
PA[17]		
PA[18]		
PA[19]		
PA[20]		
PA[21]		
PA[22]		
PA[23]		
PA[24]		
PA[25]		
PA[26]		
PA[27]		
PA[28]		
PA[29]		
PA[30]		
PA[31]		
PB[0]		
PB[1]		
PB[2]		
PB[3]		

PB[8]		
PB[9]		
PB[10]		
PB[11]		
PB[12]		
PB[13]		
PB[14]		
PB[15]		
PB[16]		
PB[17]		
PB[26]		
PB[27]		

8 Package Specifications

8.1 QFN48

The QFN48 package specification of RTL872xD is shown in Fig 8-1 and Table 8-1.

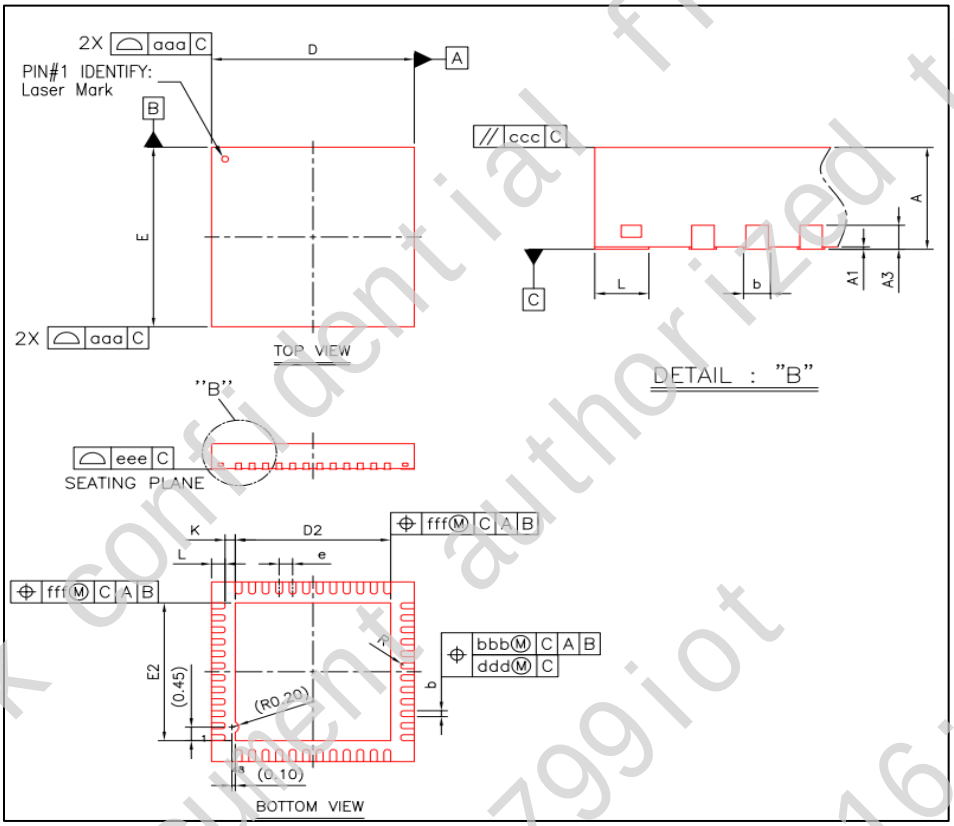


Fig 8-1 QFN48 package specification

Table 8-1 QFN48 package specification

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.8	0.85	0.9	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20REF			0.008REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00BSC			0.236BSC		
E	6.00BSC			0.236BSC		
D2/E2	4.50	4.60	4.70	0.177	0.181	0.185
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		

eee	0.08	0.003
fff	0.10	0.004

Note：

- Controlling dimension: millimeter (mm).
- Reference document: JEDEC MO-220.

8.2 QFN68

The QFN68 package specification of RTL872xD is shown in Fig 8-2 and Table 8-2.

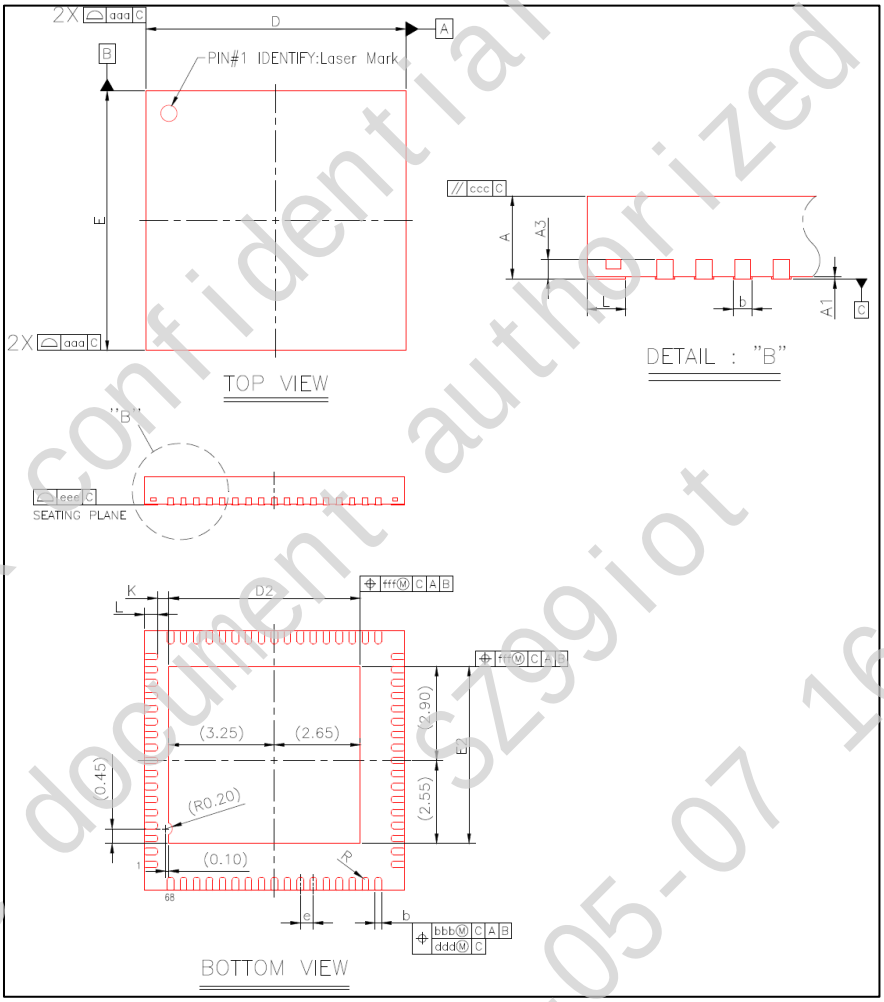


Fig 8-2 QFN68 package specification

Table 8-2 QFN68 package specification

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.10	0.311	0.315	0.319

E	7.90	8.00	8.10	0.311	0.315	0.319
D_2	5.80	5.90	6.00	0.205	0.209	0.213
E_2	5.35	5.45	5.55	0.217	0.220	0.224
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Note:

- Controlling dimension: millimeter (mm).
- Reference document: JEDEC MO-220.

8.3 QFN88

The QFN88 package specification of RTL872xD is shown in Fig 8-3 and Table 8-3.

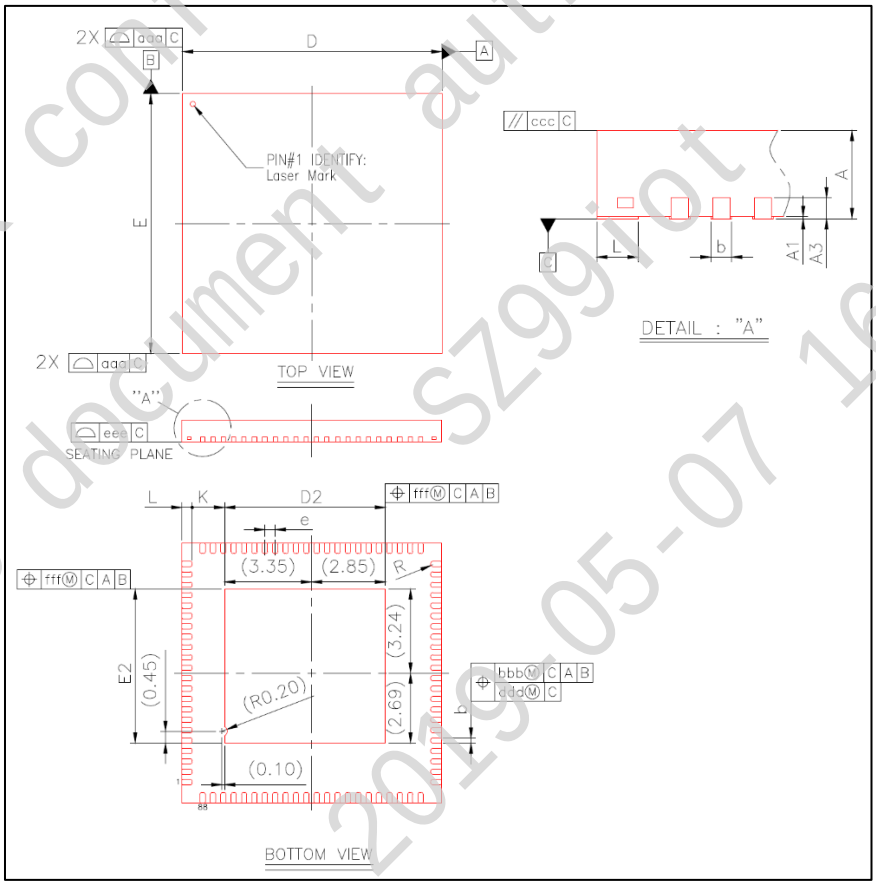


Fig 8-3 QFN88 package specification

Table 8-3 QFN88 package specification

Symbol	Dimension (mm)			Dimension (inch)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D_2	6.10	6.20	6.30	0.240	0.244	0.248
E_2	5.83	5.93	6.03	0.230	0.233	0.237
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Note:

- Controlling dimension: millimeter (mm).
- Reference document: JEDEC MO-220.

Revision History

Date	Version	Description
2019-04-10	v1.7	● Add the chapter: Wi-Fi Radio Characteristics ● Update the table: Timing specification of power sequence ● Update the table: Power supply DC characteristics ● Add the note of interrupt priority ● Add the section: GPIO Pull Low Restriction ● Update the pin assignments for QFN88
2019-02-21	v1.6	● Add RFGND pin to RF pins table ● Add the section: Power State and Power Sequence ● Re-organize the section: DC Characteristics
2019-01-25	v1.5	● Modify the pin name (pin49) of QFN88 package ● Update the memory address
2018-12-26	v1.4	Update the package specification of QFN68
2018-12-20	v1.3	● Update the peripherals under different packages ● Revise the incorrect pin number
2018-12-17	v1.2	Update the description of power pins
2018-12-13	v1.1	● Re-organize the structure of document ● Update package types of RTL872xD and QFN68/QFN88 pin assignments ● Update the operating temperature limit
2018-10-18	v1.0	Add the description about AUDIO_GND
2018-10-09	v0.9	● Add description about SDIO device time consuming ● Unify and normalize the technical items and expression
2018-07-04	v0.8	Add pin default configuration when boot
2018-07-04	v0.7	Change audio & Secure
2018-07-04	v0.6	Change system architecture
2018-07-03	v0.5	Update system architecture
2018-06-29	v0.4	Update power architecture
2018-06-28	v0.3	Add Peripherals
2018-06-27	v0.2	Add all features
2018-06-24	v0.1	Draft version