SPI

The SoC implements two instances of a SPI controller. One controller supports Master operation and another controller supports Slave operation.

1. Signal Descriptions

Table 1. SPI Master 0 Signals

Signal Name	Direction / Type	Description
SPI_M_SCLK	Logic output	Master SPI Clock
SPI_M_TXD	Logic output	Master SPI Transmit data
SPI_M_SS[3:0]	Logic output	Master SPI Slave Selects
SPI_M_RXD	Logic input	Master SPI Receive data

Table 2. SPI Slave 0 Signals

Signal Name	Direction / Type	Description
SPI_S_SCLK	Logic input	Slave SPI Clock
SPI_S_SDIN	Logic input	Slave SPI Receive data
SPI_S_SCS	Logic input	Slave SPI Slave Chip Select
SPI_S_SDOUT	Logic output	Slave SPI Transmit data

NOTE: Signal Names are preliminary and are subject to changes when the “Physical Interfaces” Chapter is populated.

2. Features

The following is a list of the SPI Master features:

- One SPI Master Interface
- Control of up to 4 Slave Selects
- Frame Formats:
  - Motorola SPI*
- Transfer Modes:
  - Transmit & Receive
  - Transmit Only
  - Receive Only
  - EEPROM Read
- Serial Clock Frequencies up to 16 MHz
- 4 bit to 32 bit Frame Size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 8B deep TX and RX FIFO's

The following is a list of the SPI Slave features:

- One SPI Slave Interface
- Frame Formats:
  - Motorola SPI*
- Transfer Modes:
  - Transmit & Receive
  - Transmit Only
  - Receive Only
  - EEPROM Read
- Serial Clock Frequencies up to 41.7 MHz
- 4 bit to 32 bit Frame Size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 8B deep TX and RX FIFO's

3. Memory Mapped IO Registers

Table 3. Summary of SPI Registers—0x40042000..0x400420F0

MEM Address	Default	Instance Name	Name
0x00	0007_0000h	CTRLR0	Control Register 0
0x04	0000_0000h	CTRLR1	Control Register 1
0x08	0000_0000h	SSIENR	SSI Enable Register
0x0C	0000_0000h	MWCR	Microwire Control Register
0x10	0000_0000h	SER	Slave Enable Register
0x14	0000_0000h	BAUDR	Baud Rate Select
0x18	0000_0000h	TXFTLR	Transmit FIFO Threshold Level
0x1C	0000_0000h	RXFTLR	Receive FIFO Threshold Level
0x20	0000_0000h	TXFLR	Transmit FIFO Level Register
0x24	0000_0000h	RXFLR	Receive FIFO Level Register
0x28	0000_0006h	SR	Status Register
0x2C	0000_003Fh	IMR	Interrupt Mask Register
0x30	0000_0000h	ISR	Interrupt Status Register
0x34	0000_0000h	RISR	Raw Interrupt Status Register
0x38	0000_0000h	TXOICR	Transmit FIFO Overflow Interrupt Clear Register
0x3C	0000_0000h	RXOICR	Receive FIFO Overflow Interrupt Clear Register
0x40	0000_0000h	RXUICR	Receive FIFO Underflow Interrupt Clear Register
0x44	0000_0000h	MSTICR	Multi-Master Interrupt Clear Register
0x48	0000_0000h	ICR	Interrupt Clear Register
0x4C	0000_0000h	DMACR	DMA Control Register
0x50	0000_0000h	DMATDLR	DMA Transmit Data Level
0x54	0000_0000h	DMARDLR	DMA Receive Data Level
0x58	0000_0000h	IDR	Identification Register
0x5C	3332_332Ah	SSI_COMP_VERSION	coreKit Version ID register
0x60	0000_0000h	DR0	Data Register
0x64	0000_0000h	DR1	Data Register

MEM Address	Default	Instance Name	Name
0x68	0000_0000h	DR2	Data Register
0x6C	0000_0000h	DR3	Data Register
0x70	0000_0000h	DR4	Data Register
0x74	0000_0000h	DR5	Data Register
0x78	0000_0000h	DR6	Data Register
0x7C	0000_0000h	DR7	Data Register
0x80	0000_0000h	DR8	Data Register
0x84	0000_0000h	DR9	Data Register
0x88	0000_0000h	DR10	Data Register
0x8C	0000_0000h	DR11	Data Register
0x90	0000_0000h	DR12	Data Register
0x94	0000_0000h	DR13	Data Register
0x98	0000_0000h	DR14	Data Register
0x9C	0000_0000h	DR15	Data Register
0xA0	0000_0000h	DR16	Data Register
0xA4	0000_0000h	DR17	Data Register
0xA8	0000_0000h	DR18	Data Register
0xAC	0000_0000h	DR19	Data Register
0xB0	0000_0000h	DR20	Data Register
0xB4	0000_0000h	DR21	Data Register
0xB8	0000_0000h	DR22	Data Register
0xBC	0000_0000h	DR23	Data Register
0xC0	0000_0000h	DR24	Data Register
0xC4	0000_0000h	DR25	Data Register
0xC8	0000_0000h	DR26	Data Register
0xCC	0000_0000h	DR27	Data Register
0xD0	0000_0000h	DR28	Data Register
0xD4	0000_0000h	DR29	Data Register
0xD8	0000_0000h	DR30	Data Register
0xDC	0000_0000h	DR31	Data Register
0xE0	0000_0000h	DR32	Data Register
0xE4	0000_0000h	DR33	Data Register
0xE8	0000_0000h	DR34	Data Register
0xEC	0000_0000h	DR35	Data Register
0xF0	0000_0000h	RX_SAMPLE_DLY	RX Sample Delay Register

3.1.1.1 Control Register 0 (CTRLR0)

This register controls the serial data transfer. It is impossible to write to this register when the SPI Controller is enabled. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 00h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0007_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:21	RO	11'b0	**Reserved 2 (RSVD2)** Reserved		
20:16	RW/L	5'h07	**Data Frame Size in 32-bit mode (DFS_32)** Used to select the data frame length in 32 bit mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32-bits, the receive data is automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. Transmit data must be right-justified by the user before writing into the transmit FIFO. The transmit logic will ignore the upper unused bits when transmitting the data.		
15:12	RW/L	4'h0	**Control Frame Size (CFS)** Control Frame Size. Selects the length of the control word for the Microwire* frame format.		
11	RW/L	1'h0	**Shift Register Loop (SRL)** Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. 0 : Normal Mode Operation 1 : Test Mode Operation		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
			When the SPI Controller is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back.		
10	RW/L	1'h0	**Slave Output Enable (SLV_OE)** Relevant only when the SPI Controller is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality. This bit enables or disables the setting of the ssi_oe_n output from the SPI Controller serial slave. When SLV_OE = 1, the ssi_oe_n output can never be active. When the ssi_oe_n output controls the tri-state buffer on the txd output from the slave, a high impedance state is always present on the slave txd output when SLV_OE = 1. This is useful when the master transmits in broadcast mode (master transmits data to all slave devices). Only one slave may respond with data on the master rxd line. This bit is enabled after reset and must be disabled by software (when broadcast mode is used), if you do not want this device to respond with data. 0 - Slave txd is enabled 1 - Slave txd is disabled		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
9:8	RW/L	2'h0	**Transfer Mode (TMOD)** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the SPI Controller is configured as a master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
7	RW/L	1'h0	**Serial Clock Polarity (SCPOL)** Valid when the frame format (FRF) is set to Motorola SPI*. Used to select the polarity of the inactive serial clock, which is held inactive when the SPI Controller master is not actively transferring data on the serial bus. 0 : Inactive state of serial clock is low 1 : Inactive state of serial clock is high Dependencies: When SSI_HC_FRF=1, SCPOL bit is a read-only bit with its value set by SSI_DFLT_SCPOL.		
6	RW/L	1'h0	**Serial Clock Phase (SCPH)** Valid when the frame format (FRF) is set to Motorola SPI*. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock. 0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit Dependencies: When SSI_HC_FRF=1, SCPH bit is a read-only bit, with its value set by SSI_DFLT_SCPH.		
5:4	RW	2'h0	**Frame Format (FRF)** Selects which serial protocol transfers the data. b00 – Motorola SPI* b01 - Texas Instruments SSP* b10 - National Semiconductors Microwire* b11 – Reserved		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
3:0	RO	4'b0	**Reserved 1 (RSVD1)** Reserved		

3.1.1.2 Control Register 1 (CTRLR1)

This register exists only when the SPI Controller is configured as a master device. When the SPI Controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the SPI Controller is enabled. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 04h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW/L	16'h0	**Number of Data Frames (NDF)** When TMOD = 10 or TMOD = 11, this register field sets the number of data frames to be continuously received by the SPI Controller. The SPI Controller continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the SPI Controller is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the SPI Controller is configured as a serial slave.		

3.1.1.3 SSI Enable Register (SSIENR)

MEM Offset (40042000) 08h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO	31'b0	**Reserved 1 (RSVD1)** Reserved		
0	RW	1'h0	**SSI Enable (SSIENR)** Enables and disables all SPI Controller operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the SPI Controller control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.		

3.1.1.4 Microwire Control Register (MWCR)

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the SPI Controller is enabled. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 0Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:3	RO	29'b0	**Reserved 1 (RSVD1)** Reserved		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
2	RW/L	1'h0	**Microwire Hanshaking (MHS)** Relevant only when the SPI Controller is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the 'busy/ready' handshaking interface for the Microwire protocol. When enabled, the SPI Controller checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register. 0: handshaking interface is disabled 1: handshaking interface is enabled		
1	RW/L	1'h0	**Microwire Control Register (MDD)** Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the SPI Controller MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the SPI Controller MacroCell to the external serial device.		
0	RW/L	1'h0	**Microwire Transfer Mode (MWMOD)** Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received. 0 : non-sequential transfer 1 : sequential transfer		

3.1.1.5 Slave Enable Register (SER)

This register is valid only when the SPI Controller is configured as a master device. When the SPI Controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the SPI Controller master. Up to 16 slave-select output signals are available on the SPI Controller master. You cannot write to this register when SPI Controller is busy.

MEM Offset (40042000) 10h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:4	RO	28'b0	**Reserved 1 (RSVD1)** Reserved		
3:0	RW/L	4'h0	**Slave Select Enable Flag (SER)** Each bit in this register corresponds to a slave select line (ss_x_n]) from the SPI Controller master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set. 1: Selected 0: Not Selected		

3.1.1.6 Baud Rate Select (BAUDR)

This register is valid only when the SPI Controller is configured as a master device. When the SPI Controller is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the SPI Controller is enabled. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 14h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW/L	16'h0	**SSI Clock Divider (SCKDV)** The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz		

3.1.1.7 Transmit FIFO Threshold Level (TXFTLR)

This register controls the threshold value for the transmit FIFO memory. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 18h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:3	RO	29'b0	**Reserved 1 (RSVD1)** Reserved		
2:0	RW	3'b0	**Transmit FIFO Threshold (TXFTLR)** Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. If you attempt to set register field to a value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.		

3.1.1.8 Receive FIFO Threshold Level (RXFTLR)

This register controls the threshold value for the receive FIFO memory. The SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) 1Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:3	RO	29'b0	**Reserved 1 (RSVD1)** Reserved		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
2:0	RW	3'h0	**Receive FIFO Threshold (RFT)** Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.		

3.1.1.9 Transmit FIFO Level Register (TXFLR)

MEM Offset (40042000) 20h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:4	RO	28'b0	**Reserved 1 (RSVD1)** Reserved		
3:0	RO	4'h0	**Transmit FIFO Level (TXTFL)** Contains the number of valid data entries in the transmit FIFO.		

3.1.1.10 Receive FIFO Level Register (RXFLR)

MEM Offset (40042000) 24h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:4	RO	28'b0	**Reserved 1 (RSVD1)** Reserved		
3:0	RO	4'h0	**Receive FIFO Level (RXFLR)** Contains the number of valid data entries in the receive FIFO.		

3.1.1.11 Status Register (SR)

This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

MEM Offset (40042000) 28h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0006h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:7	RO	25'h0	**Reserved 1 (RSVD1)** Reserved		
6	RO	1'h0	**RSVD (RSVD)** Reserved		
5	RO	1'h0	**Transmission Error (TXE)** Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the SPI Controller is configured as a slave device. Data from the previous transmission is resent on the txd line. This bit is cleared when read. 0 : No error 1 : Transmission error		

Bits	Access Type	Default	Description	PowerWell	ResetSignal
4	RO	1'h0	**Receive FIFO Full (RFF)** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 : Receive FIFO is not full 1 : Receive FIFO is full		
3	RO	1'h0	**Receive FIFO Not Empty (RFNE)** Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. 0 : Receive FIFO is empty 1 : Receive FIFO is not empty		
2	RO	1'h1	**Transmit FIFO Empty (TFE)** When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 : Transmit FIFO is not empty 1 : Transmit FIFO is empty		
1	RO	1'h1	**Transmit FIFO Not Full (TFNF)** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0 : Transmit FIFO is full 1 : Transmit FIFO is not full		
0	RO	1'h0	**SSI Busy Flag (BUSY)** When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI Controller is idle or disabled. 0 : SPI Controller is idle or disabled 1 : SPI Controller is actively transferring data		

3.1.1.12 Interrupt Mask Register (IMR)

This read/write register masks or enables all interrupts generated by the SPI Controller.

MEM Offset (40042000) 2Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_003Fh

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:6	RO	26'b0	**Reserved 1 (RSVD1)** Reserved		
5	RO	1'h1	**RSVD (RSVD)** Reserved		
4	RW	1'h1	**Receive FIFO Full Interrupt Mask (RXFIM)** 0 : ssi_rxf_intr interrupt is masked 1 : ssi_rxf_intr interrupt is not masked		
3	RW	1'h1	**Receive FIFO Overflow Interrupt Mask (RXOIM)** 0 : ssi_rxo_intr interrupt is masked 1 : ssi_rxo_intr interrupt is not masked		
2	RW	1'h1	**Receive FIFO Underflow Interrupt Mask (RXUIM)** 0 : ssi_rxu_intr interrupt is masked 1 : ssi_rxu_intr interrupt is not masked		
1	RW	1'h1	**Transmit FIFO Overflow Interrupt Mask (TXOIM)** 0 : ssi_txo_intr interrupt is masked 1 : ssi_txo_intr interrupt is not masked		
0	RW	1'h1	**Transmit FIFO Empty Interrupt Mask (TXEIM)** 0 : ssi_txe_intr interrupt is masked 1 : ssi_txe_intr interrupt is not masked		

3.1.1.13 Interrupt Status Register (ISR)

This register reports the status of the SPI Controller interrupts after they have been masked.

MEM Offset (40042000) 30h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:6	RO	26'b0	**Reserved 1 (RSVD1)** Reserved		
5	RO	1'h0	**RSVD (RSVD)** Reserved		
4	RO	1'h0	**Receive FIFO Full Interrupt Status (RXFIS)** 0 : ssi_rxf_intr interrupt is not active after masking 1 : ssi_rxf_intr interrupt is active after masking		
3	RO	1'h0	**Receive FIFO Overflow Interrupt Status (RXOIS)** 0 : ssi_rxo_intr interrupt is active after masking 1 : ssi_rxo_intr interrupt is not active after masking		
2	RO	1'h0	**Receive FIFO Underflow Interrupt Status (RXUIS)** 0 : ssi_rxu_intr interrupt is not active after masking 1 : ssi_rxu_intr interrupt is active after masking		
1	RO	1'h0	**Transmit FIFO Overflow Interrupt Status (TXOIS)** 0 : ssi_txo_intr interrupt is not active after masking 1 : ssi_txo_intr interrupt is active after masking		
0	RO	1'h0	**Transmit FIFO Empty Interrupt Status (TXEIS)** 0 : ssi_txe_intr interrupt is not active after masking 1 : ssi_txe_intr interrupt is active after masking		

3.1.1.14 Raw Interrupt Status Register (RISR)

This register reports the status of the SPI Controller interrupts prior to masking

MEM Offset (40042000) 34h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:6	RO	26'b0	**Reserved 1 (RSVD1)** Reserved		
5	RO	1'h0	**RSVD (RSVD)** Reserved		
4	RO	1'h0	**Receive FIFO Full Raw Interrupt Status (RXFIR)** 0 : ssi_rxf_intr interrupt is not active prior masking 1 : ssi_rxf_intr interrupt is active prior masking		
3	RO	1'h0	**Receive FIFO Overflow Raw Interrupt Status (RXOIR)** 0 : ssi_rxo_intr interrupt is active prior masking 1 : ssi_rxo_intr interrupt is not active prior masking		
2	RO	1'h0	**Receive FIFO Underflow Raw Interrupt Status (RXUIR)** 0 : ssi_rxu_intr interrupt is not active prior masking 1 : ssi_rxu_intr interrupt is active prior masking		
1	RO	1'h0	**Transmit FIFO Overflow Raw Interrupt Status (TXOIR)** 0 : ssi_txo_intr interrupt is not active prior masking 1 : ssi_txo_intr interrupt is active prior masking		
0	RO	1'h0	**Transmit FIFO Empty Raw Interrupt Status (TXEIR)** 0 : ssi_txe_intr interrupt is not active prior masking 1 : ssi_txe_intr interrupt is active prior masking		

3.1.1.15 Transmit FIFO Overflow Interrupt Clear Register (TXOICR)

MEM Offset (40042000) 38h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO	31'b0	**Reserved 1 (RSVD1)** Reserved		
0	RO/C	1'h0	**Clear Transmit FIFO Overflow Interrupt (TXOICR)** This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.		

3.1.1.16 Receive FIFO Overflow Interrupt Clear Register (RXOICR)

MEM Offset (40042000) 3Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO/C	31'b0	**Reserved 1 (RSVD1)** Reserved		
0	RO/C	1'h0	**Clear Receive FIFO Overflow Interrupt (RXOICR)** This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.		

3.1.1.17 Receive FIFO Underflow Interrupt Clear Register (RXUICR)

MEM Offset (40042000) 40h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO	31'h0	**Reserved 1 (RSVD1)** Reserved		
0	RO/C	1'h0	**Clear Receive FIFO Underflow Interrupt (RXUICR)** This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.		

3.1.1.18 Multi-Master Interrupt Clear Register (MSTICR)

MEM Offset (40042000) 44h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO	31'b0	**Reserved 1 (RSVD1)** Reserved		
0	RO	1'h0	**RSVD (RSVD)** Reserved		

3.1.1.19 Interrupt Clear Register (ICR)

MEM Offset (40042000) 48h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:1	RO	31'b0	**Reserved 1 (RSVD1)** Reserved		
0	RO/C	1'h0	**Interrupt Clear Register (ICR)** This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.		

3.1.1.20 DMA Control Register (DMACR)

The register is used to enable the DMA Controller interface operation.

MEM Offset (40042000) 4Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:2	RO	30'h0	**Reserved 1 (RSVD1)** Reserved		
1	RW	1'h0	**Transmit DMA Enable (TDMAE)** This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled		
0	RW	1'h0	**Receive DMA Enable (RDMAE)** This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled		

3.1.1.21 DMA Transmit Data Level (DMATDLR)

MEM Offset (40042000) 50h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:3	RO	29'h0	**Reserved 1 (RSVD1)** Reserved		
2:0	RW	3'h0	**DMA Transmit Data Level (DMATDL)** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.		

3.1.1.22 DMA Receive Data Level (DMARDLR)

MEM Offset (40042000) 54h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:3	RO	29'b0	**Reserved 1 (RSVD1)** Reserved		
2:0	RW	3'h0	**Receive Data Level (DMARDL)** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.		

3.1.1.23 Identification Register (IDR)

This read-only register is available for use to store a peripheral identification code.

MEM Offset (40042000) 58h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:0	RO	32'h0	**Identification Code (IDCODE)** This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant.		

3.1.1.24 coreKit Version ID register (SSI_COMP_VERSION)

This read-only register stores the specific SPI Controller component version.

MEM Offset (40042000) 5Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 3331_382Ah

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:0	RO	32'h3331338a	**SSI Component Version (SSI_COMP_VERSION)** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. @@jstokes - NOTE : reset value will change with Synopsys release for 32b support		

3.1.1.25 Data Register (DR0)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 60h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.26 Data Register (DR1)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 64h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.27 Data Register (DR2)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 68h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.28 Data Register (DR3)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 6Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.29 Data Register (DR4)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 70h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.30 Data Register (DR5)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 74h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.31 Data Register (DR6)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 78h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.32 Data Register (DR7)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 7Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.33 Data Register (DR8)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 80h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.34 Data Register (DR9)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 84h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.35 Data Register (DR10)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 88h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.36 Data Register (DR11)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 8Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.37 Data Register (DR12)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 90h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.38 Data Register (DR13)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 94h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.39 Data Register (DR14)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 98h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.40 Data Register (DR15)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory
map to facilitate AHB burst transfers. Writing to any of these address locations has the same
effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of
these locations has the same effect as popping data from the receive FIFO onto the prdata
bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) 9Ch
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.41 Data Register (DR16)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) A0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.42 Data Register (DR17)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) A4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.43 Data Register (DR18)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) A8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.44 Data Register (DR19)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) ACh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.45 Data Register (DR20)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) B0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.46 Data Register (DR21)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) B4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.47 Data Register (DR22)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) B8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.48 Data Register (DR23)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) BCh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.49 Data Register (DR24)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) C0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.50 Data Register (DR25)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) C4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.51 Data Register (DR26)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) C8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.52 Data Register (DR27)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) CCh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.53 Data Register (DR28)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) D0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.54 Data Register (DR29)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) D4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.55 Data Register (DR30)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) D8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.56 Data Register (DR31)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) DCh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.57 Data Register (DR32)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) E0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.58 Data Register (DR33)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) E4h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.59 Data Register (DR34)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) E8h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.60 Data Register (DR35)

The SPI Controller data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE : The DR register in the SPI Controller occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the SPI Controller are not addressable.

MEM Offset (40042000) ECh
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:16	RO	16'b0	**Reserved 1 (RSVD1)** Reserved		
15:0	RW	16'h0	**Data Register (DR)** When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer		

3.1.1.61 RX Sample Delay Register (RX_SAMPLE_DLY)

This register controls the number of ssi_clk cycles that are delayed,from the default sample time,before the actual sample of the rxd input signal occurs. It is impossible to write to this register when the SPI Controller is enabled; the SPI Controller is enabled and disabled by writing to the SSIENR register.

MEM Offset (40042000) F0h
Security_PolicyGroup
IntelRsvd False
Size 32 bits
Default 0000_0000h

Bits	Access Type	Default	Description	PowerWell	ResetSignal
31:4	RO	28'h0	**Reserved 1 (RSVD1)** Reserved		
3:0	RW/L	4'h0	**Receive Data Sample Delay (RSD)** This register is used to delay the sample of the rxd input signal. Each value represents a single ssi_clk delay on the sample of the rxd signal. NOTE: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH		