INTEGRATED CIRCUITS LAB REPORT 4

Name: Abhishek Dutta Gupta **Trinity ID: 22312353**

3.1 A brief description of the filter you created in Vivado HLS

A Sobel filter is used for image edge detection. The designed filter in HLS consists of 3 parts

a) Sobel.CPP
b) Sobel.h
c) testbench

Sobel.CPP and Sobel. h converts the image into a grayscale image, applying convolution into the grayscale with the X-axis and Y-axis filters. Finally, it calculates the gradient magnitude and its direction, with edge detection of the image as the output.

The testbench then tests the algorithm by taking an image as an input and exporting an edge-detected filtered image and confirming the design of the filter.

The results of the filter synthesis are attached below:

Synthesis Report for 'sobel_accel'

General Information

Date:	Wed Nov 16 17:51:12 2022
Version:	2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project:	Lab4
Solution:	solution1
Product family:	zynq
Target device:	xc7z020-clg400-1

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	10.575 ns	1.25 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
2087660	2104951	22.078 ms	22.261 ms	2087642	2104922	dataflow

Detail

- Instance
- Loop

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Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	34	-
FIFO	0	-	117	512	-
Instance	9	43	7691	15037	0
Memory	-	-	-	-	-
Multiplexer	-	-	-	36	-
Register	-	-	6	-	-
Total	9	43	7814	15619	0
Available	280	220	106400	53200	0
Utilization (%)	3	19	7	29	0

Detail

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_CONTROL_BUS_AWVALID	in	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_AWREADY	out	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_AWADDR	in	4	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_WVALID	in	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_WREADY	out	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_WDATA	in	32	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_WSTRB	in	4	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_ARVALID	in	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_ARREADY	out	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_ARADDR	in	4	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_RVALID	out	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_RREADY	in	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_RDATA	out	32	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_RRESP	out	2	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_BVALID	out	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_BREADY	in	1	s_axi	CONTROL_BUS	return void
s_axi_CONTROL_BUS_BRESP	out	2	s_axi	CONTROL_BUS	return void
ap_clk	in	1	ap_ctrl_hs	sobel_accel	return value
ap_rst_n	in	1	ap_ctrl_hs	sobel_accel	return value
interrupt	out	1	ap_ctrl_hs	sobel_accel	return value
INPUT_STREAM_TDATA	in	24	axis	INPUT_STREAM_V_data_V	pointer
INPUT_STREAM_TKEEP	in	3	axis	INPUT_STREAM_V_keep_V	pointer
INPUT_STREAM_TSTRB	in	3	axis	INPUT_STREAM_V_strb_V	pointer
INPUT_STREAM_TUSER	in	1	axis	INPUT_STREAM_V_user_V	pointer
INPUT_STREAM_TLAST	in	1	axis	INPUT_STREAM_V_last_V	pointer
INPUT_STREAM_TID	in	1	axis	INPUT_STREAM_V_id_V	pointer

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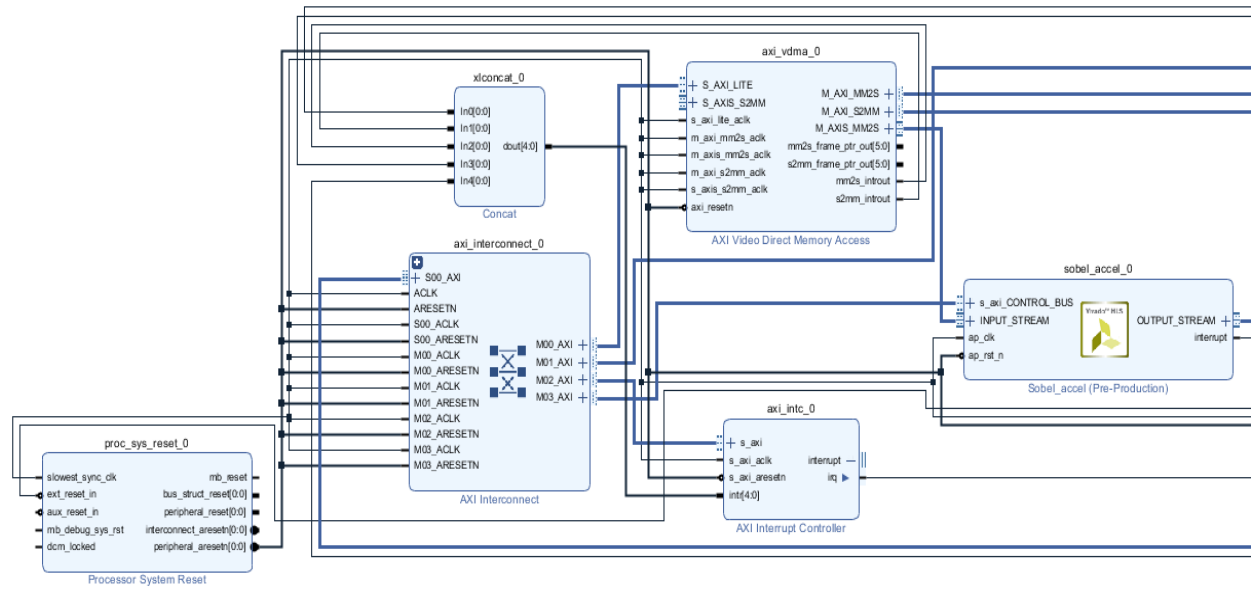
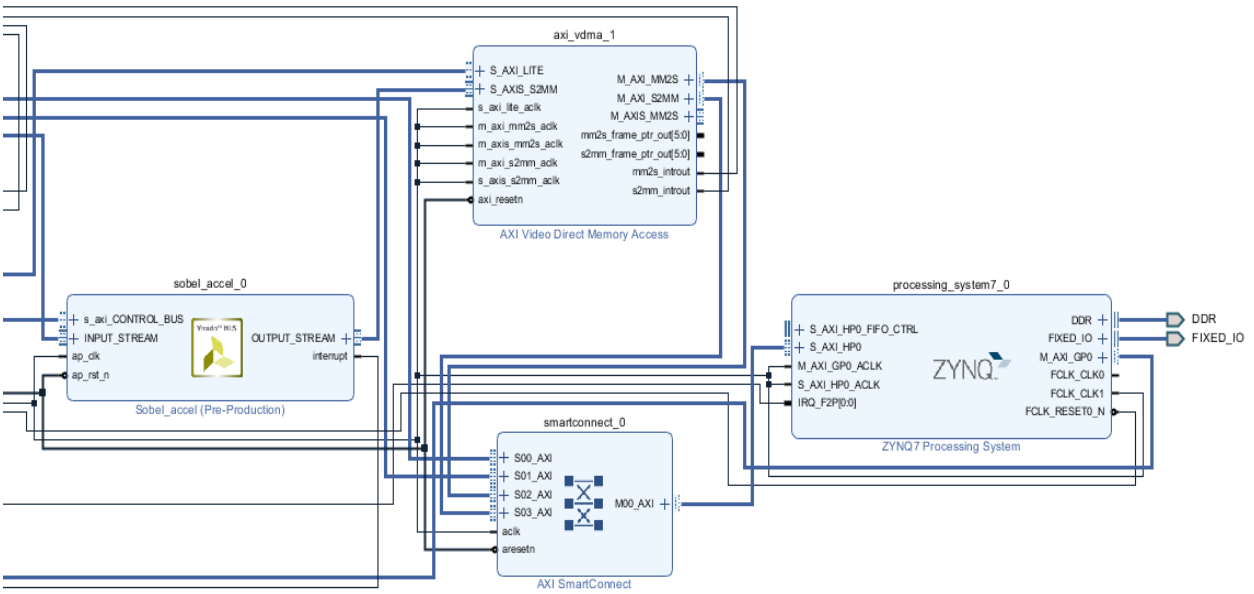
After this, the filter is imported into Vivado 2019.2 as an overlay IP (Sobel_Accel) to create the complete design and generate the bitstream files for uploading to hardware.

3.2 Screenshots of your overlay and describe the role of each IP.





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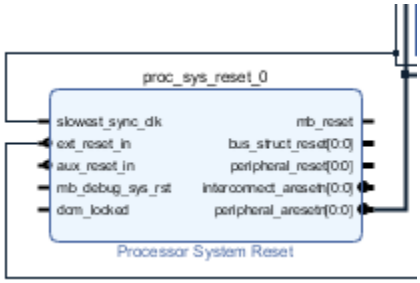
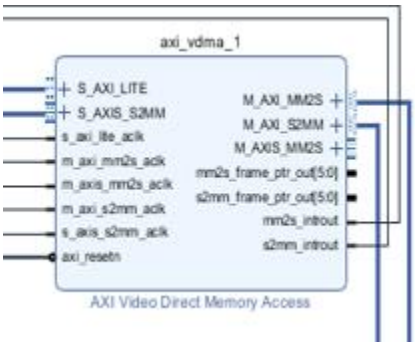
i. Processor System reset: This allows specific changing of parameters to enable/disable features as needed by the processor. Its main functions include power on reset configuration, load equalizing, external reset synchronizations, etc.



ii. AXI Direct Memory Access: It connects to all AXI Smart connects, stream data FIFO and AXI Interconnects. It supplies high bandwidth memory allocation to AXI stream-type targets. Here 2 VDMA's are used (VDMA – 0 & VDMA – 1) both connected to AXI interconnect.

The following changes are made in the VDMA-0 for bitstream generation

1) On the Read Channel Options, Stream Data Width is selected to 24 bits.



iii. Sobel Accel: It is an image-processing kernel that is used for edge detection. It takes in its input/output from the direct memory access, with the control bus supplied from AXI interconnect. This Filter IP is inserted from the HLS Design.

iv. AXI Smart Connect: This provides AXI 4 interfacing, which is address-based interfacing, suitable for register control. It automatically configures and adapts to AXI master and slave IPs.

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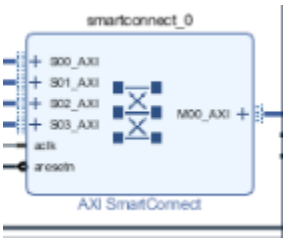
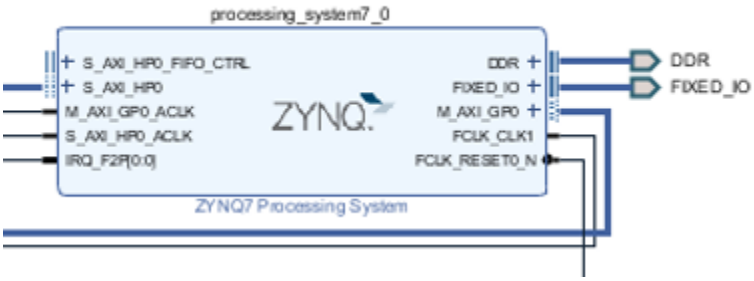


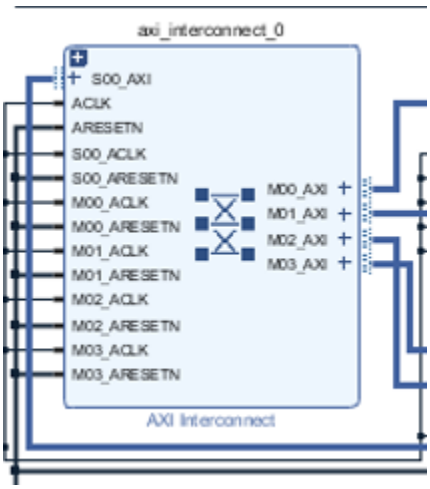
v. Zynq Processor: It is the main processing board that provides software interfaces for all the FIFO Controls, Clock controls, etc. Connections to AXI Smart connect IPs, AXI-interconnect in the overlay is made from the processing system. Moreover, all I/O's are connected to this.

Following changes are made in the IP for bitstream generation

1) Under PS-PL Configuration, HP Slave AXI Interface, S AXI HP0 interface is enabled.
2) Under Clock Configuration, PL Fabric Clock, FCLK_CLK1 is enabled, and the frequency is set to 100 (MHz).
3) Under Interrupts, Fabric Interrupts are enabled and in PL-PS Interrupt Ports, IRQ_F2P [15:0] is enabled.



vi. AXI Interconnect: This provides AXI lite interfacing, which like AXI-4 is an address-based interfacing, but in a simplified manner. It connects one or more AXI master devices to one or more AXI slaves' devices.



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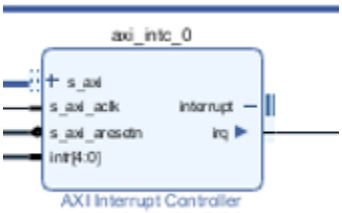
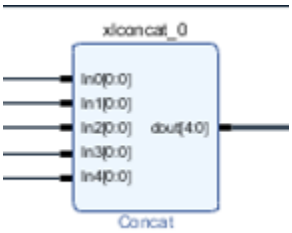
vii. AXI Interrupt Controller: The AXI Interrupt Controller concatenates various interrupt inputs from peripheral devices to a single interrupt output to the system processor. The registers used are accessed through a slave interface. The number of interruptions and other aspects can be tailored to the target system. This is interfaced with the AXI - Interconnect protocol.



viii. Concat: The Concat block basically **concatenates multiple inputs into a single bus output**. The singular interrupt signals from other AXI slaves need to be restructured into a bus because the Interrupt Controller takes only a bus in its input. Here 5 number of ports are used.



3.3 Include the image you used before and after processing.

Fig (1) Image before processing in VIVADO HLS

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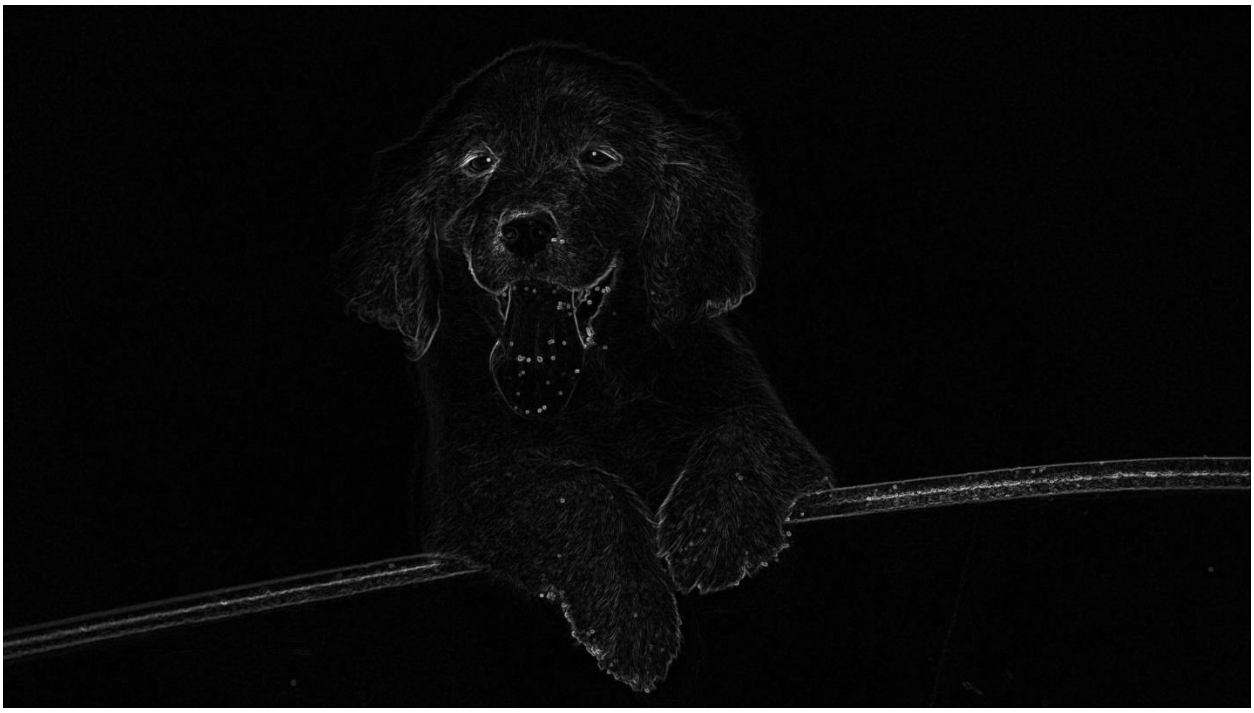

Fig (2) Image after processing in VIVADO HLS

Fig (3) Image before processing in PYNQ hardware implementation

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Fig (4) Image after processing in PYNQ hardware implementation