Dr. Mahalingam College of Engineering and Technology,

Pollachi

(An Autonomous Institution Affiliated to Anna University, Chennai)

Department of Electronics and Communication Engineering

Record Note Book

19ECCN3702 - VLSI LABORATORY

Name	**:**	
Roll No.	**:**	
Branch	**:**	
Class & Section	**:**	

Dr. MAHALINGAM MCET
COLLEGE OF ENGINEERING AND TECHNOLOGY
Enlightening Technical Minds

Dr. Mahalingam College of Engineering and Technology, Pollachi

Record Note Book

19ECCN3702 - VLSI LABORATORY

Name : _____

Roll No. : _____

Branch : _____

Certified that this is the bonafide record of work done by the above student for _____ year B.E. Degree during 20__ to 20__.

_____ _____

Head of the Department Faculty In-charge

Submitted to the Autonomous End Semester Cycle test Practical Examination held on _____

Internal Examiner **External Examiner**

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S.No.	Date	Title of the experiment	Page No.	Marks (out of 75)	Signature with date
			Total		

Course Code: 19ECCN3702	Course Title: VLSI Laboratory		
Course Category: Professional Core	Course Level: Mastery		
L:T:P (Hours/Week) 0 :0: 3	Credits:1.5	Total Contact Hours: 45	Max Marks:100

Prerequisites:

- 19ECCN1302- Digital Principles and System Design

Course Objectives:

The course is intended to:

1. Design and simulate Combinational and sequential circuits.
2. Design and Verify Combinational and Sequential circuits.
3. Implement Combinational and sequential circuits on FPGA.
4. Design and simulate inverter and universal gates using SPICE tool.
5. Perform physical design of inverter and universal gates using SPICE tool.

LIST OF EXPERIMENTS:

1. Design and Simulation of Adders (4 bit Half adder, 4 bit full adder, 4 bit Ripple carry adder).
2. Design and Simulation of Flip-Flops. (S-R Flip-flop, JK Flip-flop, D Flip-flop, T Flip-flop).
3. Design & Verification of 4bit Adder using System Verilog.
4. Design & Verification of D flipflop using System Verilog.
5. FPGA Implementation of 4 bit Synchronous Counter.
6. FPGA Implementation of 4 bit Asynchronous Counter.
7. Schematic design and simulation of Inverter.
8. Schematic design and simulation of 2 input NAND and NOR gate.
9. Layout Design of Inverter.
10. Layout Design of 2 input NAND and NOR gate.

Course Outcomes	Cognitive Level
At the end of this course, students will be able to:	
CO1. Develop and verify functionality of Combinational and sequential circuits.	Apply
CO2. Solve errors in Combinational and Sequential circuit designs.	Apply
CO3. Apply FPGA implementation for combinational and sequential circuits.	Apply
CO4. Construct and simulate inverter and universal gates using SPICE tool.	Apply
CO5. Model physical design of inverter and universal gates using SPICE tool.	Apply

Reference Books:

1. "VLSI Laboratory manual", prepared by the ECE department.
2. Morris Mano.M, "Digital Design", 3rd edition, Prentice Hall of India Pvt.Ltd, / Pearson Education Pvt.Ltd, 2003.

Internal Assessment: (Out of 75 Marks)
Rubrics for Observation:

Criteria	Level of performance			
	Excellent	**Good**	**Satisfactory**	**Needs Improvement**
Preparation	**20**	**17**	**14**	**10**
	Student has very clearly understood the concepts and reflected fully in the responses for pre viva.	Student has very clearly understood the concepts and reflected most of the questions in the responses for pre viva.	Student has clearly understood the concepts and reflected very few of the questions in the responses for pre viva.	Student has not understood the concepts and reflected none of the questions in the responses for pre viva.
Observation & Results	**25**	**22**	**19**	**15**
	Student demonstrates sound knowledge of lab procedures. Student has written all the results and inferences neatly and completely.	Student Demonstrates good knowledge of the lab procedures. Student has written most of the results and inferences neatly and completely.	Student requires help from teacher with some steps in procedures. Student has written part of the results and inferences neatly and completely.	Student often requires help from the teacher to even complete basic procedures. Student has written few of the results and inferences neatly and completely.
Viva Voce	**10**	**8**	**6**	**5**
	The student responded for all questions.	The student responded for most of the questions.	The student responded for part of the questions.	The student responded for few of the questions.

OBSERVATION Criteria	Excellent	Good	Satisfactory	Needs Improvement
Preparation	20	17	14	10
Observation & Results	25	22	19	15
Viva Voce	10	8	6	5
Total	**/55**			

Rubrics for Record:

Criteria	Level of performance			
	Excellent	Good	Satisfactory	Needs Improvement
Neatness	10	8	6	5
	In all the entries in the record, the student has clearly written.	In most of the entries in the record, the student has clearly written.	In some of the entries in the record, the student has clearly written.	In a very few of the entries in the record, the student has clearly written
Submission on time	10	8	6	5
	The student brings the record and gets sign in time.	The student brings the record and gets sign ONE DAY late.	The student brings the record and gets sign THREE DAYS late.	The student brings the record and gets sign a WEEK later.

RECORD Criteria	Excellent	Good	Satisfactory	Needs Improvement
Neatness	10	8	6	5
Submission on time	10	8	6	5
Total	/20			

External Assessment: (100 Marks)

CRITERIA	MARKS
Aim/Apparatus Required	10
Theory/Procedure	20
Coding/Schematic Diagram	40
Output	20
Viva	10
Total	100

* The external mark will be scaled down to 25 marks

Assessment Pattern

Type	Assessment Component	CO No.	Marks	Total mark
Internal Assessment	Record and Observation	1,2,3,4,5	75	75
End Semester Examination	Cycle test	1,2,3,4,5	100	25
			Total	**100**