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Designing A 8-Bit Pipeline ADC Using Cadence Virtuoso

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***Abstract*— The demand for high-performance analog-to-digital converter (ADC) integrated circuits (IC) with optimal resolution, sampling rate, and power consumption is increasing due to emerging applications in wireless communications, broad band transceivers, digital-intermediate frequency (IF) receivers, and numerous digital devices. This research work aims to provide a pipeline ADC design technique with low power consumption, while maintaining high speed and resolution. The aim of our paper is to produce pipeline architecture ADC which has high resolution, fast speed, and low power consumption. In the proposed work the Cadence Virtuoso software tool is used. 180nm, 90nm technology is used to create an 8-bit ADC with 1-bit resolution to each stage. Verilog and pipeline architecture require a 1V supply voltage to function.**

Keywords—Cadence, Virtuoso, Verilog, pipeline architecture.

I. INTRODUCTION

The fundamental components of mixed and analog signal processing are analog to digital converters, or ADCs. Analog signals from the natural world and digital ones from the digital world will be connected by ADCs [1].Continuous signals from electrical circuits are converted to discrete values by analog to digital converters for transmission, estimation, and signal analysis. The main technological differences between ADCs are their variable features, such as resolution, chip size, and power, which change based on the application dynamic range, conversion rate, and usage. ADC is selected for a particular application and utilized in calculations to attain the necessary cost effectiveness [3]. After weighing its characteristics and capabilities, an ADC will be selected for the design according on the system needs or specifications. The most balanced ADC is the pipeline ADC resolution and quickness. With the delta-sigma (ΔΣ) ADC, anti-aliasing protection is intrinsic and dynamic performance is high. The dual-slope ADC computes by contrasting the two slopes, or run-up and run-down times. The pipeline ADC is a cutting-edge, lightning-fast, and power-efficient.[9].The power consumption of the system ranges from pico to mill watts are referred to as ultra-low power electronics. Thus, all systems that must be portable, use less energy, or dissipate as little heat as possible can benefit from the ultra-low power design concepts. [5]

II. LITERATURE REVIEW

A capacitor ratio-independent, power-efficient conversion technique is shown. Number of applications demand high performance data converters. Gainful parameters for sampling rate, resolution, and power dissipation should be present in these data converters. These are the essential ADC requirements for broadband transceivers, wireless communication applications, and several digital gadgets. An operational amplifier is the fundamental building element of a pipeline design. Op amps and pipeline architecture require a 1.8V supply voltage to function [3]. This study describes 8 bits, 20 M samples/s pipeline analog-to-digital converters with a total power dissipation of 75.47 MW, developed in 0.6 µm CMOS technology. Clock management, an operational amplifier, and an exact comparator are some of the circuit techniques employed. Utilizing switched capacitor, samples and multiplying in every phase. Worst-case scenario simulation 0.75 LSB for both DNL and INL. At 5 V dc, the design operates at 44.86 dB.The ADC obtains an SNDR [2]. A challenge in very large scale integrated (VLSI) design is speeding up an analog and mixed mode signal circuit without sacrificing power consumption. To reach all the parameters, this paper effort is being done to design a 12-bit Pipeline A/D converter (ADC) with 400MS/s sample rate. To make room for different applications, the design focuses on figuring out pipeline ADC's high speed and resolution. The main advantages of the pipeline method are its simplicity in terms of implementation, speed gain, and layout design. A suggested technique that multiplies the D/A converter, comparator, sample and hold circuit (S/H), and operational trans conductance amplifier (OTA) is used to construct a pipeline ADC architecture[1].The design and modeling of an 8-bit pipeline analog-to-digital converter (ADC) with 20 Mega-Sample per Second (MSPS) and multiple bits per stage are shown in this study. Digital circuitry in a System-on-Chip (SOC) can be included into the design utilizing the 0.18 µm standard CMOS technology. The architecture of the ADC, individual component circuits, and simulation results are shown [4]. An 8-bit SAR ADC with ultra-low power consumption which can be utilized in biomedical applications is presented in this paper. With 1.8V as the supply voltage, the SAR ADC was developed in O.181lm CMOS technology. The suggested 8-bit SAR-ADC used about 164.97W of electricity [5].Designing a ADC with a

100KS/s sampling rate is the main topic of the study. It is incredibly quick and inexpensive. Technology with precision and resolution that is comparatively medium. This suggests that it has a strong cost-to-speed ratio. When R2R DAC is used in a different way than a traditional ADC, resistor matching is made easier [6] .In the direction of the typical operational amplifier (op-amp). Using two NMOS devices, the gain-enhancement technique separates the op-amp's differential input devices from its cascade devices. As a result, it is possible to increase the open-loop DC gain further without compromising the op-amp's unity-gain bandwidth. This 8-bit pipeline ADC is developed primarily by means of an op-amp, in which the impact of using NMOS devices is analyzed and applied. The 180 nm CMOS Silterra technique was employed in the fabrication. 1.44 mm2 is the silicon area measured by the ADC [7].The method increases the op-amp's feedback factor, which improves performance without changing the signal. Referring to conventional circuits, the bootstrapping action of the level-shifting buffers relaxes important op-amp performance criteria, such as unity-gain bandwidth, noise, open-loop gain, and offset. This lowers the circuits depending on op-amps' power consumption and design complexity. Using this method, pipeline ADC is developed in 65 n m CMOS, requiring 49.7 MW of power with the supply of a 1.2 V power supply to provide 67.0 dB SNDR at 250 MS/s [8].This study describes a low-power, low-area, 8-bit flash ADC.An analogue multiplexer (MUX), a comparator, an encoder, and an SPI (Serial Peripheral Interface) block are the four primary blocks that make up the flash ADC. An easy method for the ADC to communicate with micro controllers is through the SPI block. 180 nm technologies are used in the design and simulation of this mixed-signal circuitry. 128 comparators are used by the 8-bit flash ADC. The input voltage can be anywhere between 0.6V and 1.8V, and the applied input clock is 80 MHz. The average power consumption of the design is 2.81 m W. The layout's entire area is 0.088 mm [9].The study is about an 8 bit self-calibrated D/A converter and low voltage and current mode 9 bit pipeline A/D converter to interface a DSP system. The 1.5 bit stages of the A/D converter are equipped with digital error correction logic. Three LSB fine and five MSB coarse current mode converters make up the D/A converter. The A/D and D/A converters were constructed using 0.35 µm technology and then manufactured. The two converters' performances are contrasted with those of recognized converter structures. The compact chip size and low power consumption of the suggested converters are their key features [10].Noise in transmission affects compressed images, making the receiver's reconstruction of the images more difficult. The design of sub circuits for multiplying DAC utilizing 180nm CMOS technology is presented in this work. Cadence Virtuoso and HSPICE are used in the design, modeling, and performance analysis of the DA, current reference, and amplifier. Sub circuit optimal geometries are calculated, and schematic capture is completed. The outcomes demonstrate that the sub-circuits that were built are appropriate for the implementation of multiplying DACs[11].When sampling at 40 MHz from a 3-V supply, the converter uses 55mW, which comprises a reference circuit and a band gap as well 70mW if digital drivers with a 10-pF load are included [12]. The pipeline ADC is a widely used Nyquist-rate data converter. The quick expansion of its applications like digital video, mobile systems, and high-speed data acquisition are pushing the pipeline ADC architecture towards greater precision, speed, and lower power and supply voltage. The goal of this thesis project is to design and develop a high-speed, low-power pipeline ADC.

III. METHODOLOGY

A. Sample and hold (S/H)

Sample-and-hold (S/H) circuit consists of a MOS switch and a capacitor. The switch serves as a conduit for the input signal, which charges the capacitor. when the transistor gate's clock is high during the sampling mode. To remove any possible loading impact, a differential amplifier stage is frequently used at the S/H circuit's output. In the hold mode, the MOS switch acts as an open circuit to prevent the capacitor from emptying and to sustain the voltage sampled at the time the clock pulse arrived. This shows that during the hold mode, the capacitor holds the input voltage value until the subsequent clock pulse, at which time it charges again. The output can be obtained either at the differential amplifier's output or directly across the capacitor

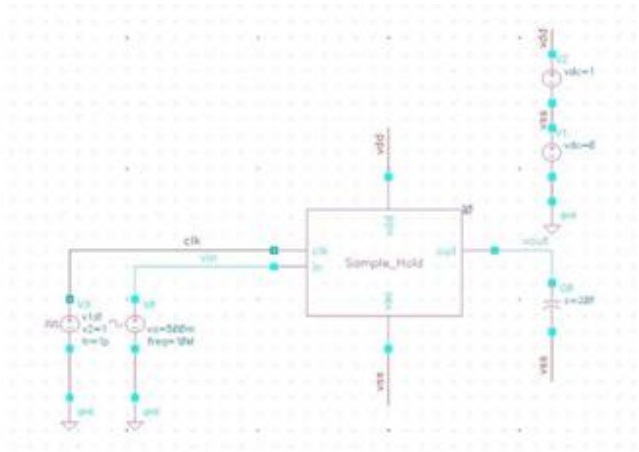

Fig. 1. Sample and Hold circuit

B. Multiplier digital to analog converter (MDAC)

There are numerous approaches of implementing digital-to-analog converters (DAC), each with pros and cons of their own. One of the most common DAC designs is the binary weighted resistor array, which uses resistors of different values to produce the correct output voltage. However, since the area required fitting the additional resistors increases as the number of bits increases, this approach is not appropriate for high-resolution DAC. Furthermore, matching resistor values becomes more challenging as the number of bits increases, which could lead to inaccurate output voltage. Another method for designing a DAC is the weighted capacitor approach, although it too has the disadvantage of having area requirements that increase as the number of bits increases. But this approach usually takes up less space than the binary weighted resistor array. Even with this advantage, it still has trouble producing voltage outputs that are accurate since the values of the capacitors need to match exactly. A new approach to designing a DAC that consumes less power and space than the weighted capacitor technique and binary weighted resistor array is the split capacitor array. Conversely, split capacitor technology increases parasitic capacitance, which can cause the output signal to become more distorted and noisy. Ultimately, the specific application needs and the balance of power, area, and accuracy will dictate which DAC implementation strategy is employed. The DAC block was implemented using the Multiplying DAC network to improve accuracy.

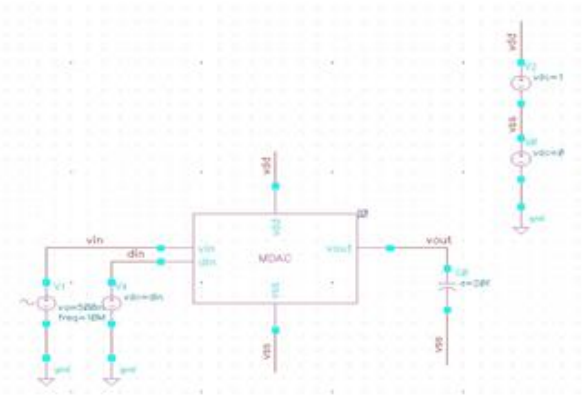

Fig. 2. Multiplier digital to analog converter

C. *Comparator*

The comparator is an important component of the design, and it primary contributors of power consumption. Much care was taken in its design to guarantee that the MOS transistors employed in its construction work in the saturation area, which is necessary for efficient amplification. Additionally, the differential amplifier was employed to lessen the impact of noise, which can degrade the quality of the output signal's comparator's main job is to compare the input voltage to the reference voltage and provide a logic output that is either high or low based on the result of the comparison. Because of its careful design, the comparator has superior operational speed and excellent resolution, making it a very valuable component of this architecture.

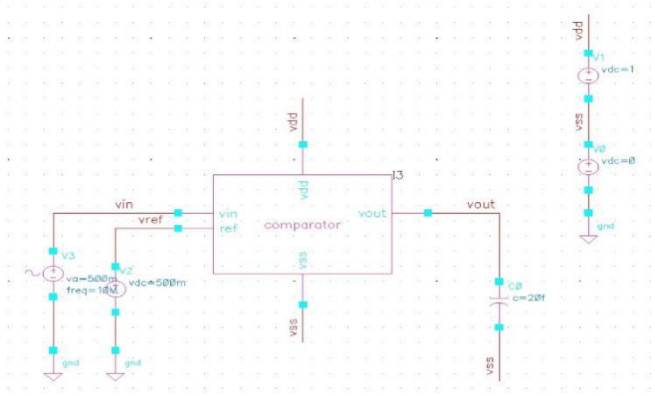

Fig. 3. Comparator

D. *1-bit stage*

Creating an 8-bit pipeline ADC involves combining several stages of 1-bit ADC, each consisting of a sample-and-hold (S/H) circuit, a multiplying digital-to-analog converter (MDAC), and a comparator. Here is a step-by-step explanation of how to combine these components to create a 1-bit stage symbol for an 8-bit pipeline ADC.

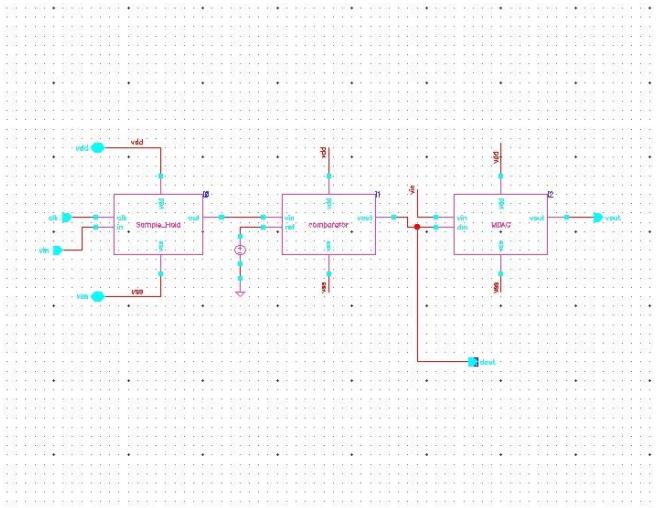

Fig. 4. 1-bit stage

E. *8-bit pipeline*

The 8-bit pipeline ADC works by sequentially resolving each bit of the digital output through a series of 1-bit stages. Each stage captures, holds, and processes the input signal to determine one bit of the final output, while generating a residue signal for the next stage. By cascading eight such stages, the pipeline ADC efficiently converts the input analog signal into an 8-bit digital representation.

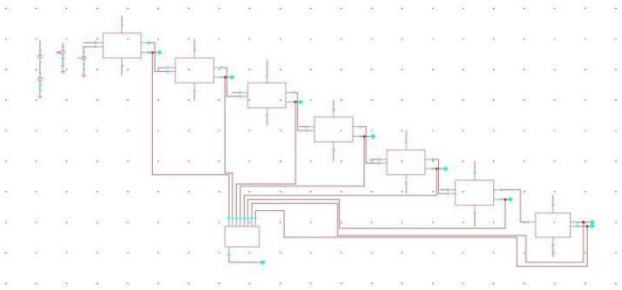

Fig. 5. pipeline ADC

IV. RESULTS AND DISCUSSIONS

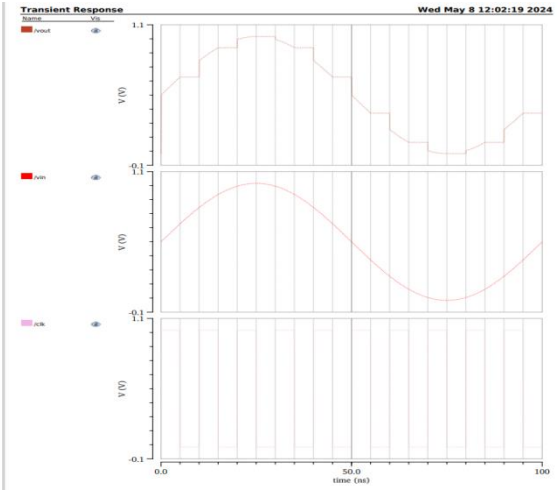

Fig. 6. Sample and Hold graph

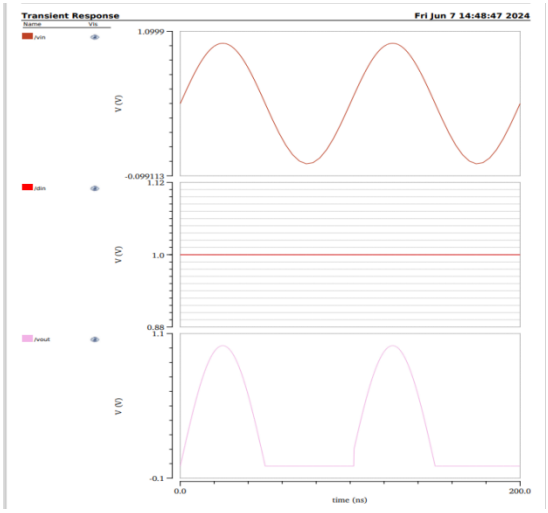

Fig. 7. MDAC

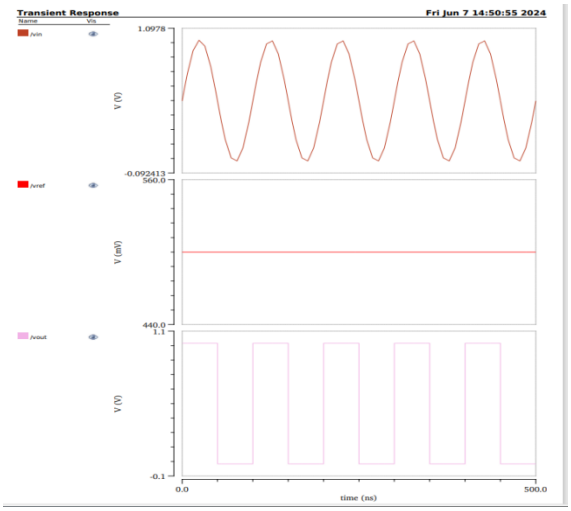

Fig. 8. Comparator

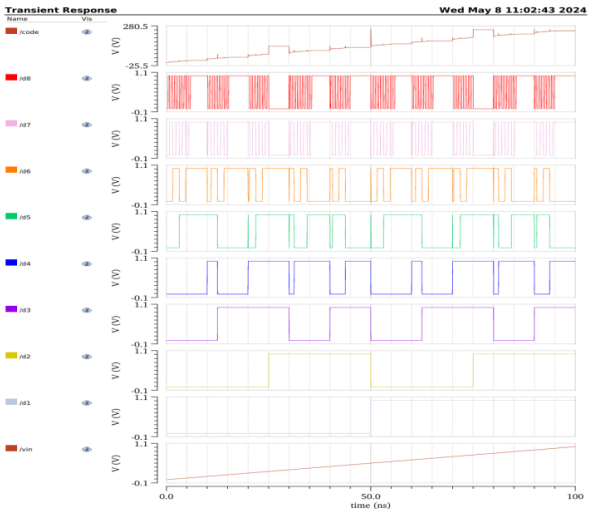

Fig. 9. 8-bit pipeline

The Cadence Virtuoso 180nm and 90nm library was used to create the 8-bit pipeline ADC. Table1 and Table 2 list the ADC readings in terms of delay, power consumption, power supply, time taken for one cycle, and technology.

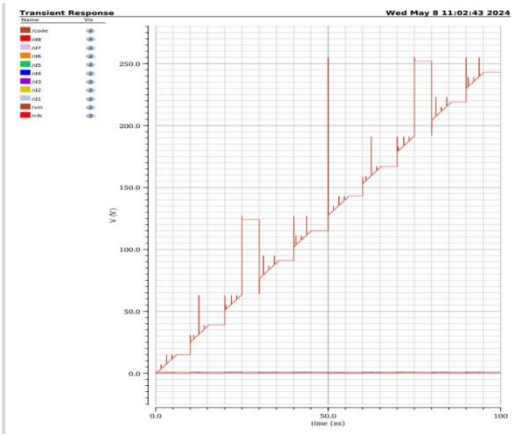

Fig. 10. waveforms for 8 bit ADC

TABLE I. COMPARISON WITH OUR PIPELINE ADC DESIGNS.

	Our work	Our work	Our work	Our work
Technology	180nm	90nm	180nm	90nm
Resolution	8	8	8	8
Input Supply	1V	1V	0.6V	0.6V
Power Consumption	25uW	16uW	6.45mW	4mW
Speed	83MS/sec	160MS/sec	2GS/sec	4GS/sec

TABLE II. COMPARISON WITH OTHER PIPELINE ADC DESIGNS.

	[1]	[2]	[9]	[14]
Technology	90nm	65nm	180nm	180nm
Resolution	10	8	8	12
Input Supply	3	1.2	1.8	1.8
Power Consumption	38mW	110mW	27mW	398mW
Speed	40MS/sec	100MS/sec	8MS/sec	250MS/sec

V. CONCLUSION

The design of an 8-bit pipeline ADC that can be used for power applications is shown in this work. Since the comparator is more powerful than the other components of the ADC, the design was focused on creating a low power comparator and Digital to Analogue Converter (DAC). For 1V supply the ADC's total speed was found to be 83MS/s for 180nm Technology and 160MS/sec for 90nm Technology. For 0.6V supply the ADC'S total speed was for 2GS/sec and 4GS/s for 90nm Technology. The proposed architecture outperformed pervious research work carried out.

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