



CMOS PROJECT

1 : 4 DEMULTIPLEXER

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ROLL NO – BT20ECE053

SUB - CMOS

BRANCH - ECE

SUBMITTED TO -
DR. PARITOSH PESHWE

AIM- Implementation of 1:4 Demux in microwind
and Ngspice.

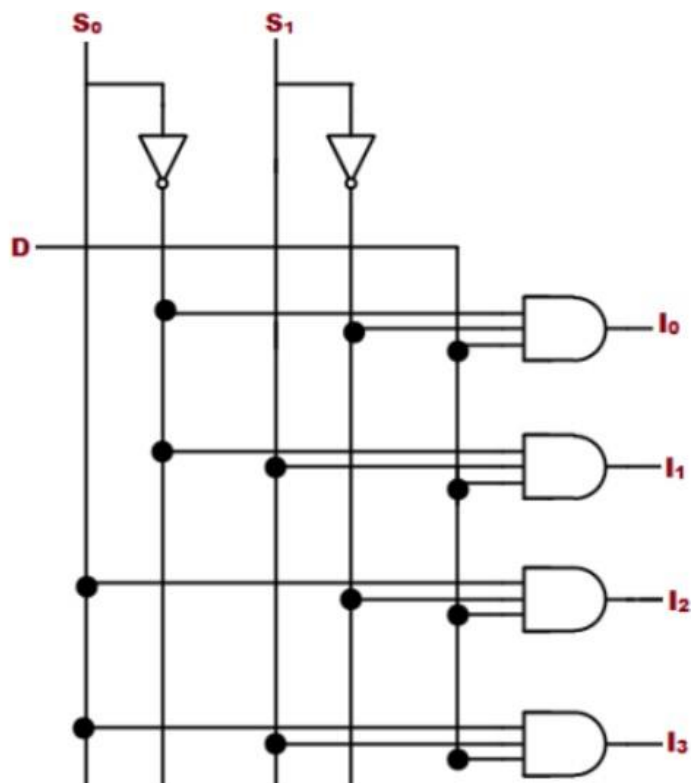
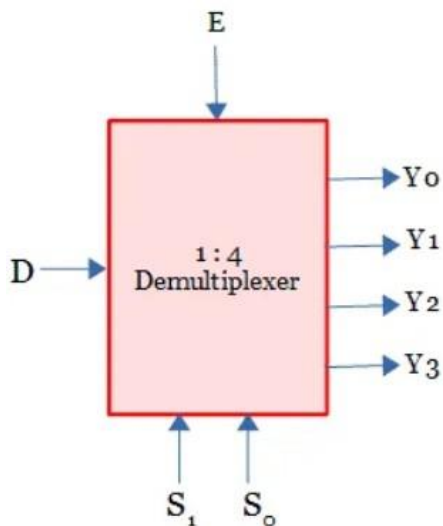
THEORY

1-to-4 Demultiplexer

- A 1-to-4 demultiplexer has a single input (D), two selection lines (S1 and S0) and four outputs (Y0 to Y3).
- The input data goes to any one of the four outputs at a given time for a particular combination of select lines.

- This demultiplexer is also called as a 2-to-4 Demultiplexer, which means that it has two select lines and 4 output lines.

The block diagram of a 1:4 DEMUX



TRUTH TABLE

S1	S0	D	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

IN NETLIST -

Y0 - Output 1 V(31)

Y1- Output 2 V(30)

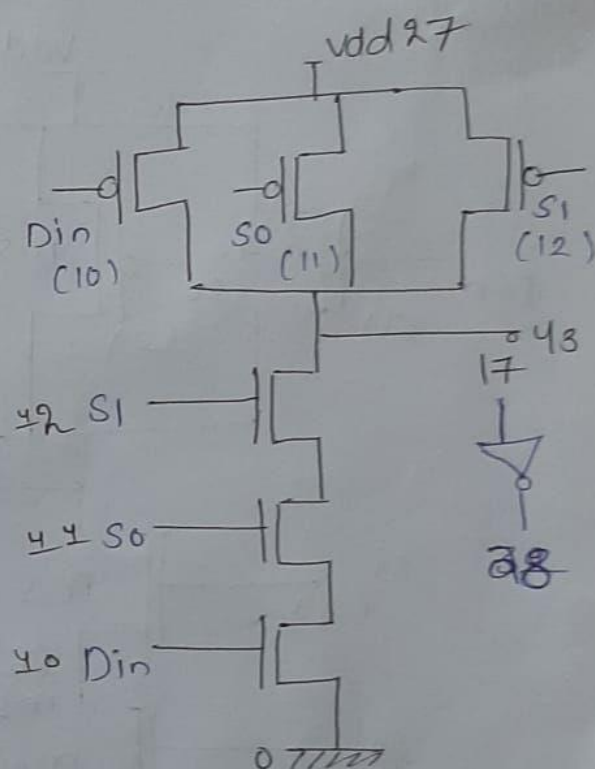
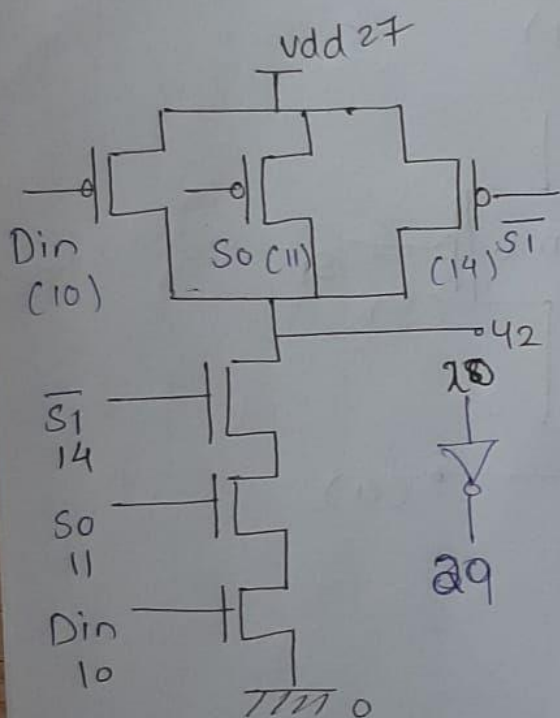
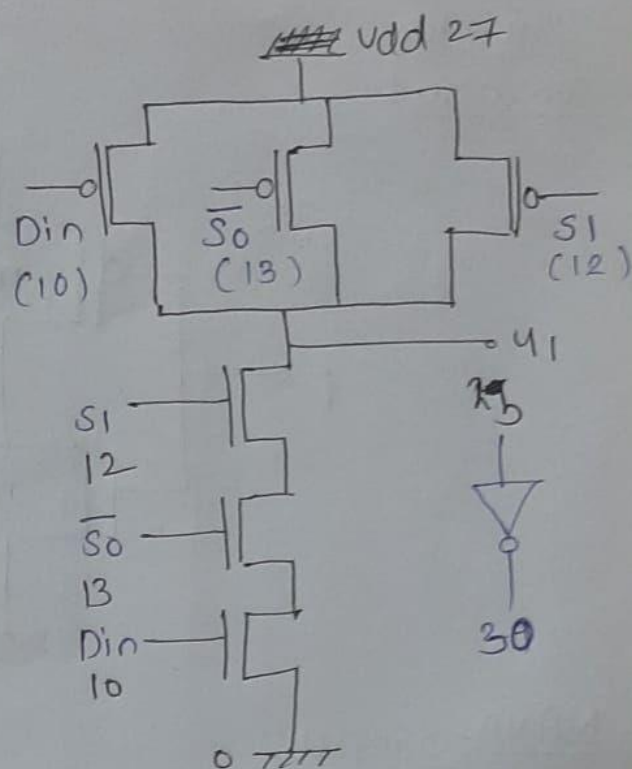
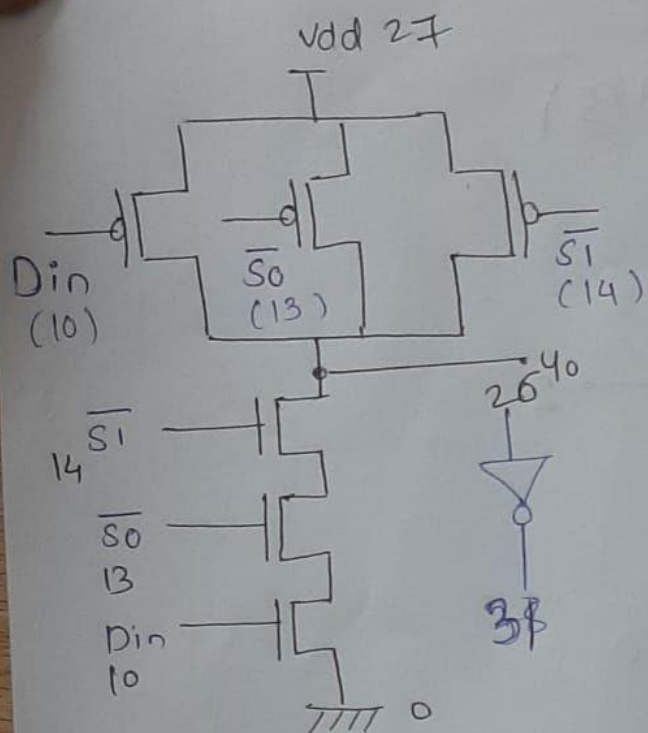
Y2 - Output 3 V(29)

Y3 - Output 4 V(28)

V(10) - Din - which is always 5v.

V(11) - S0

V(12) - S1



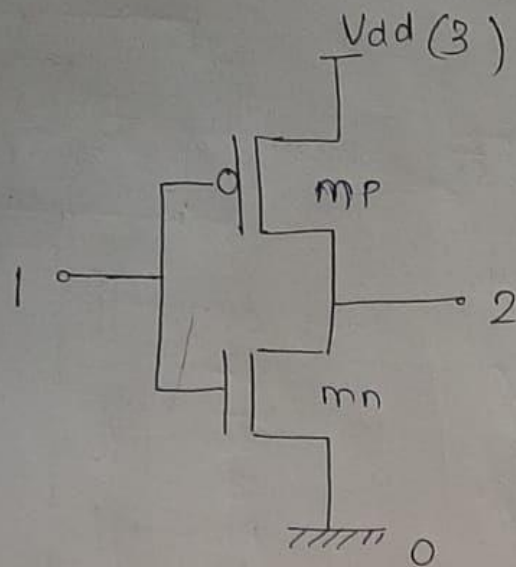
Numbering : ① ground \rightarrow 0

② Din \rightarrow 10 ; S0 \rightarrow 11 ; S1 \rightarrow 12 ; S0 \rightarrow 13 ; S1 \rightarrow 14

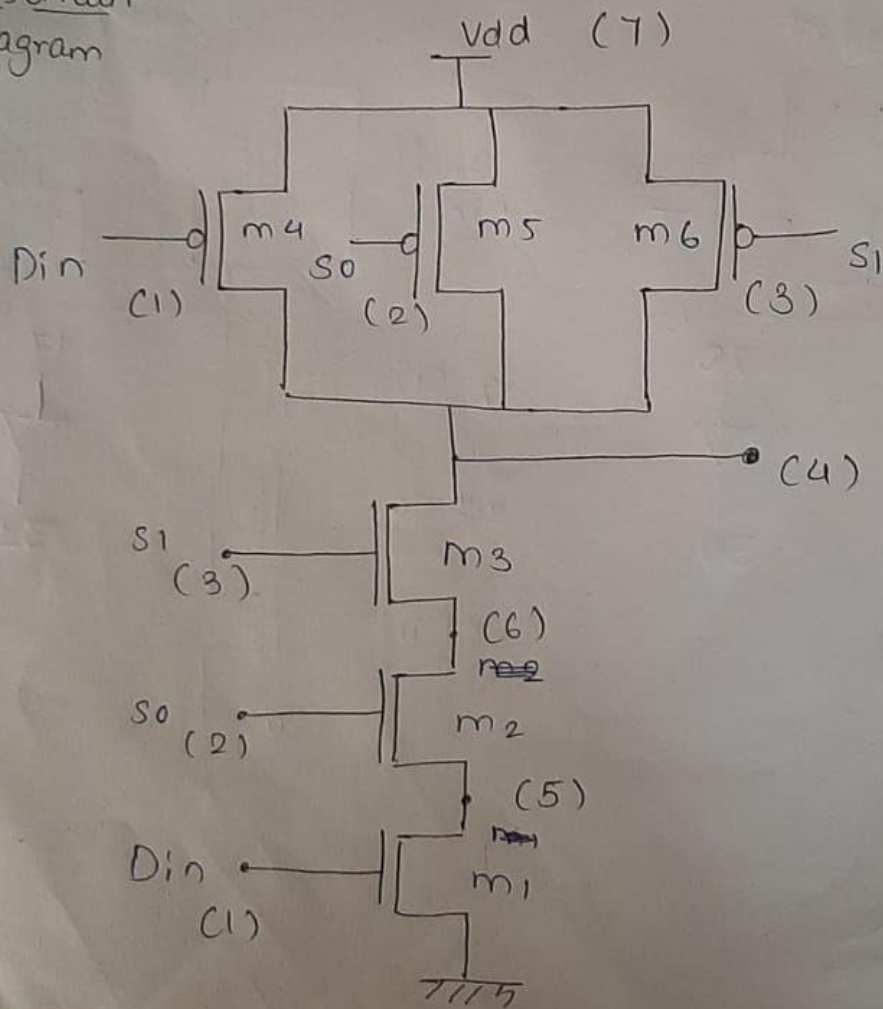
③ VDD \rightarrow 27

④ 40 \rightarrow 26 ; 41 \rightarrow 28 ; 42 \rightarrow 20 ; 43 \rightarrow 17

Inverter
sub circuit



NAND-3 input
subcircuit
diagram



NGSPICE

```
** 1:4 DEMULTIPLEXER
.subckt inverter 1 2 3
mp 2 1 3 3 pmod w=100u l=1u
mn 2 1 0 0 nmod w=40u l=1u
.model pmod pmos Vto=-1V Kp=80u
.model nmod nmos Vto=1V Kp=200u
.ends

.subckt nand_gate 1 2 3 4 7
m1 5 1 0 0 nmod w=40u l=10u
m2 6 2 5 0 nmod w=40u l=10u
m3 4 3 6 0 nmod w=40u l=10u
m4 4 1 7 7 pmod w=100u l=10u
m5 4 2 7 7 pmod w=100u l=10u
m6 4 3 7 7 pmod w=100u l=10u
.model pmod pmos Vto=-1V Kp=80u
.model nmod nmos Vto=1V Kp=200u
ends

Vdd 27 0 dc 5V
Va 10 0 dc 5V
Vb 11 0 pulse ( 0 5 0 0 0 8ns 16ns)
Vc 12 0 pulse ( 0 5 0 0 0 4ns 8ns)
xa 11 13 27 inverter
xb 12 14 27 inverter

xnand_s1 10 11 12 17 27 nand_gate
xnand_s2 10 11 14 20 27 nand_gate
xnand_s3 10 13 12 23 27 nand_gate
xnand_s4 10 13 14 26 27 nand_gate

xc 17 31 27 inverter
xd 20 30 27 inverter
xe 23 29 27 inverter
xf 26 28 27 inverter

.tran 0.1ns 100ns
.control
run
plot V(10)
plot V(11)
plot V(12)
plot V(31)
plot V(30)
plot V(29)
plot V(28)
.endc
.end
```

```
demux.cir - Notepad

File Edit View

** 1:4 DEMULTIPLEXER

.subckt inverter 1 2 3
mp 2 1 3 3 pmod w=100u l=1u
mn 2 1 0 0 nmod w=40u l=1u
.model pmod pmos Vto=-1V Kp=80u
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.ends

.subckt nand_gate 1 2 3 4 7
m1 5 1 0 0 nmod w=40u l=10u
m2 6 2 5 0 nmod w=40u l=10u
m3 4 3 6 0 nmod w=40u l=10u
m4 4 1 7 7 pmod w=100u l=10u
m5 4 2 7 7 pmod w=100u l=10u
m6 4 3 7 7 pmod w=100u l=10u
.model pmod pmos Vto=-1V Kp=80u
.model nmod nmos Vto=1V Kp=200u
.ends

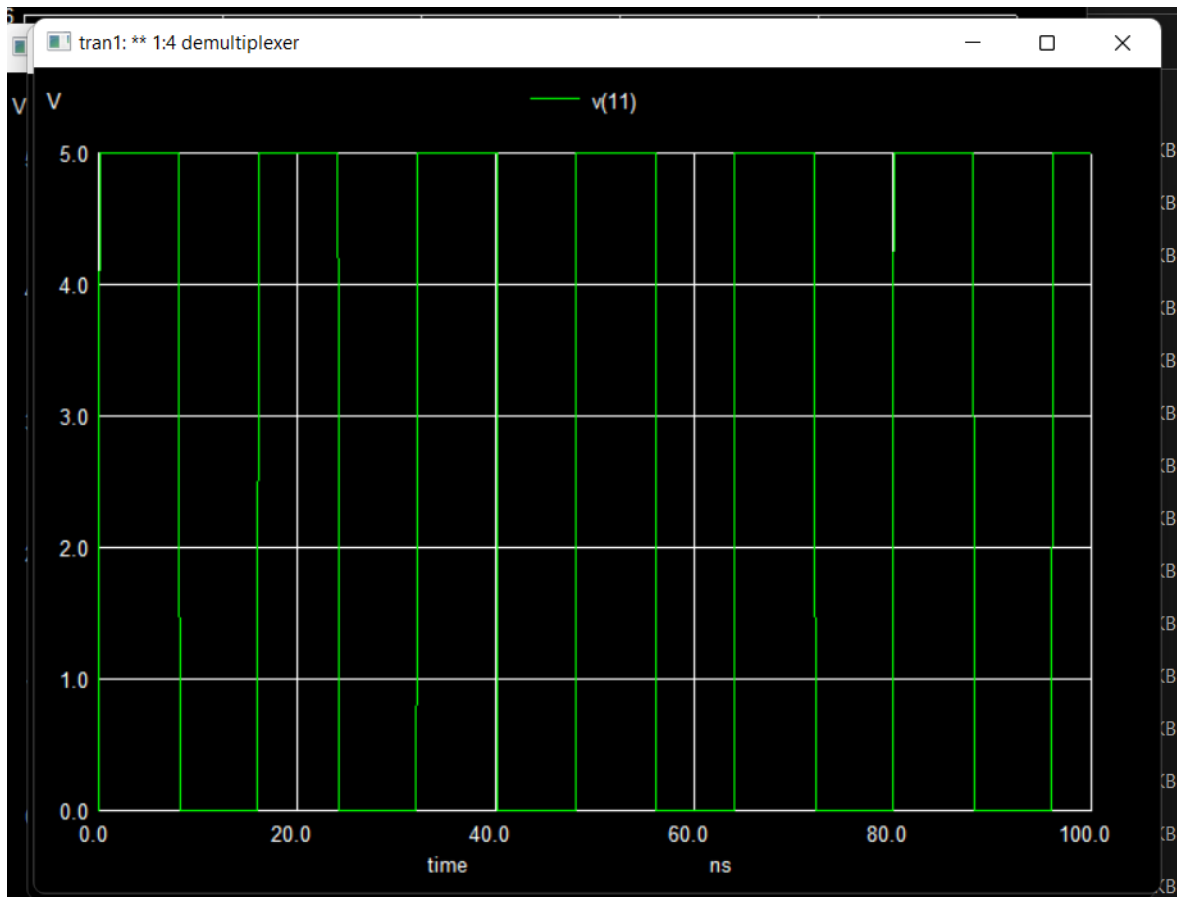
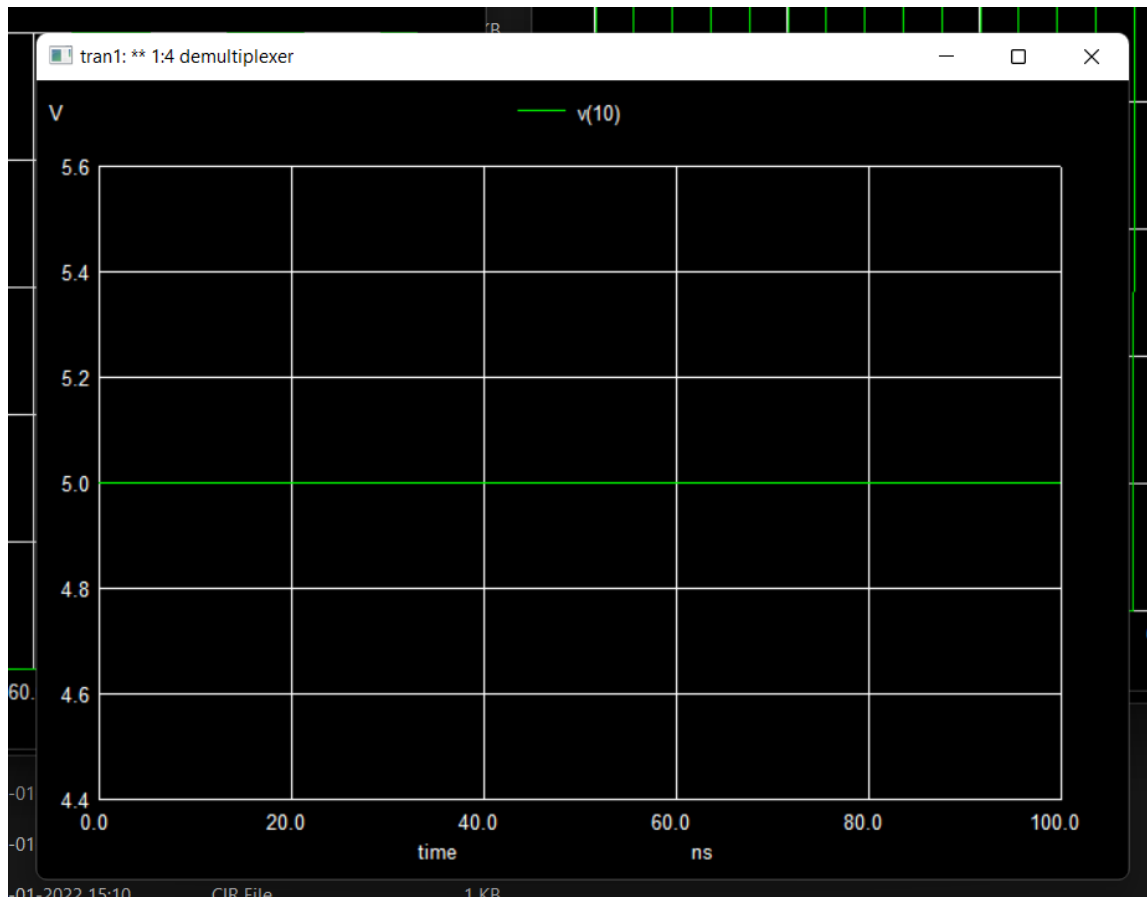
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xa 11 13 27 inverter
xb 12 14 27 inverter

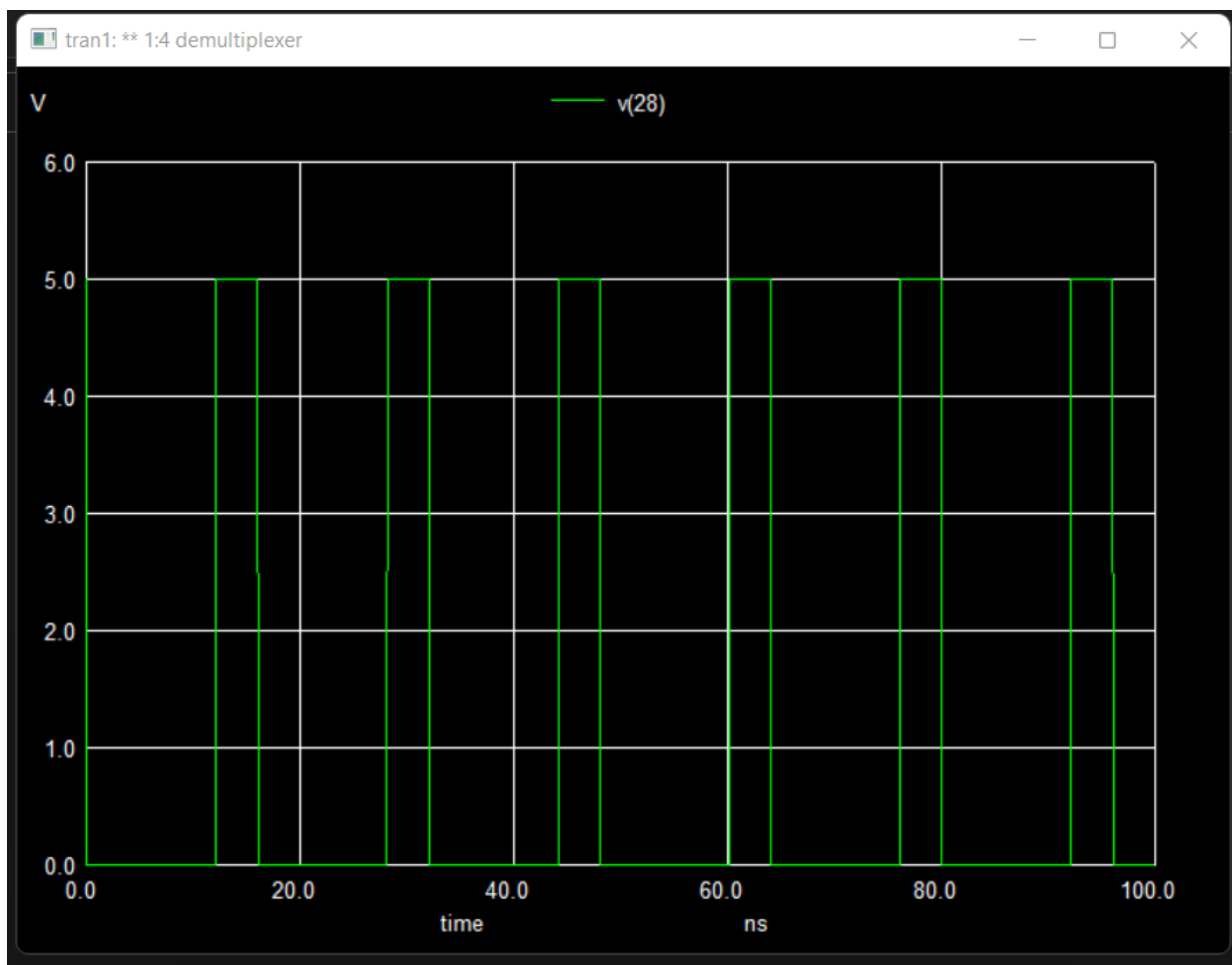
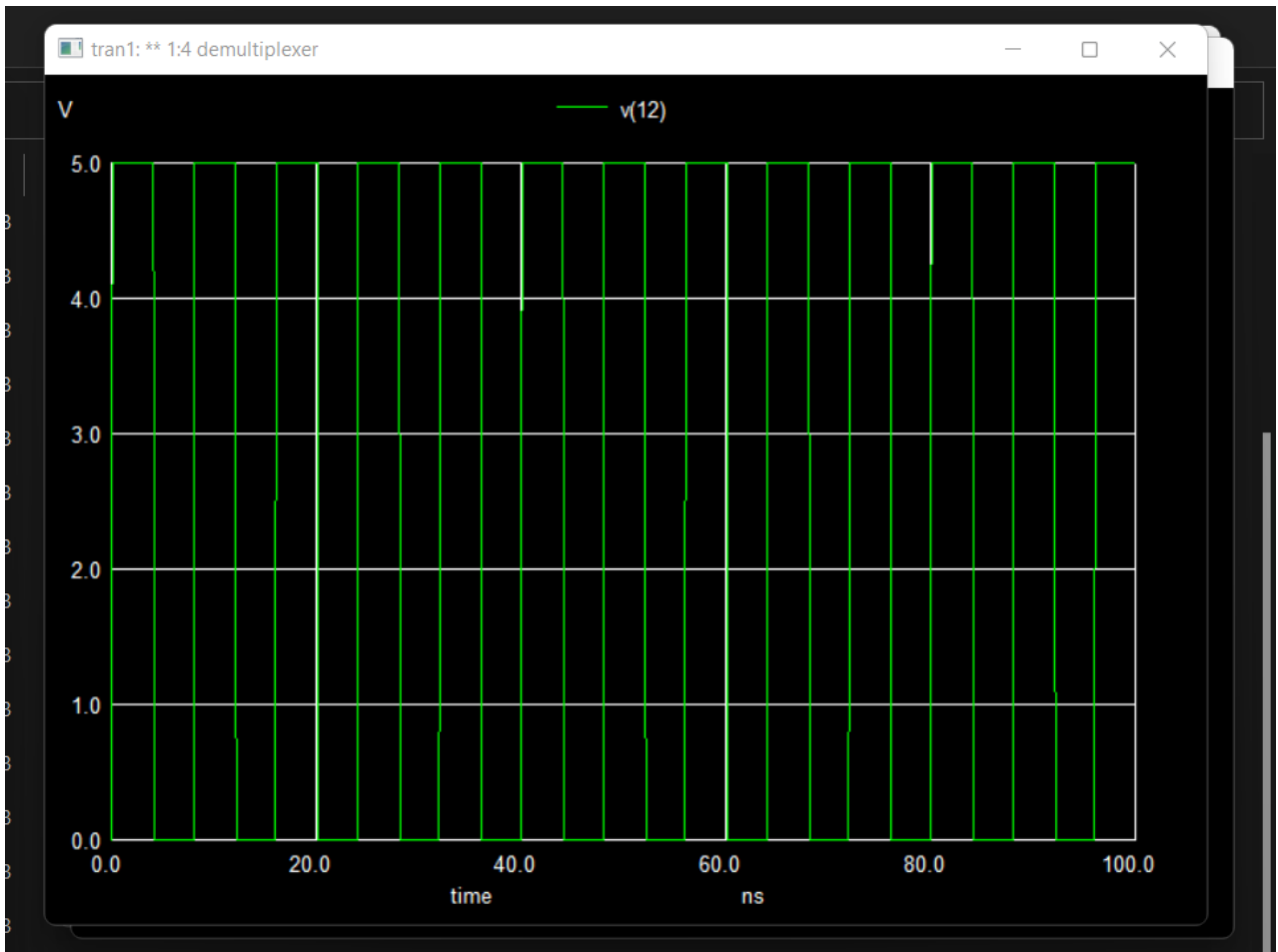
xnand_s1 10 11 12 17 27 nand_gate
xnand_s2 10 11 14 20 27 nand_gate
xnand_s3 10 13 12 23 27 nand_gate
xnand_s4 10 13 14 26 27 nand_gate

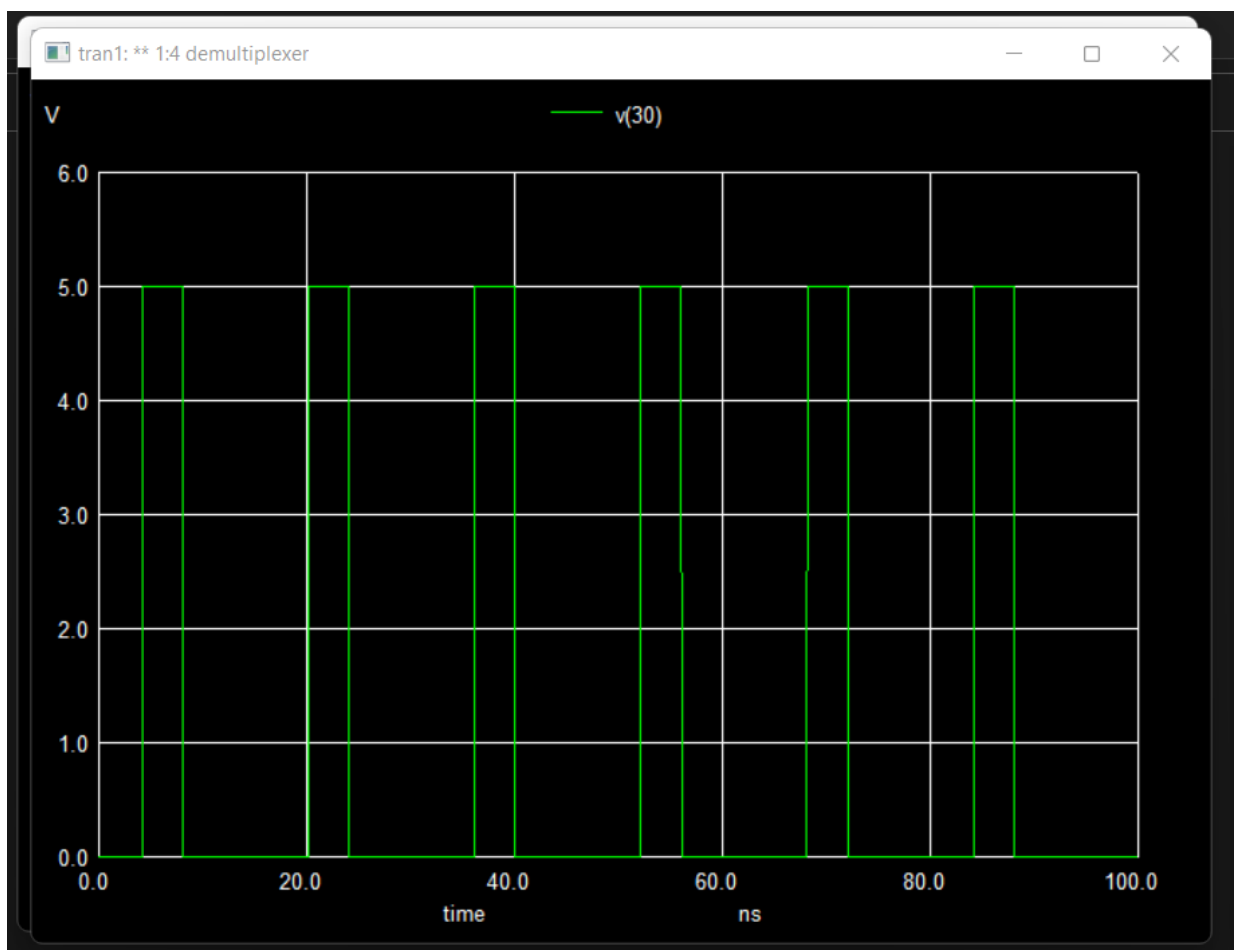
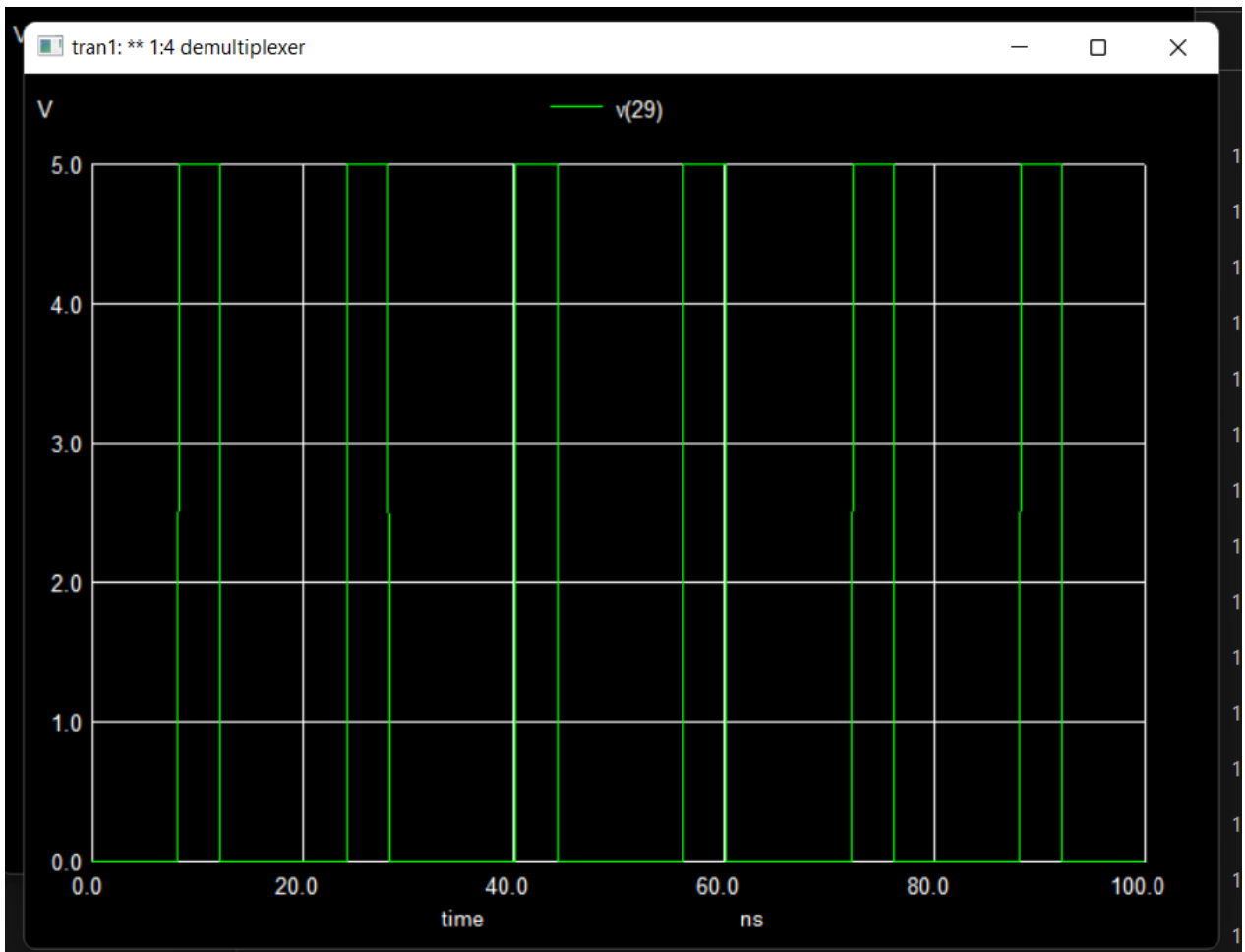
xc 17 31 27 inverter
xd 20 30 27 inverter
xe 23 29 27 inverter
xf 26 28 27 inverter

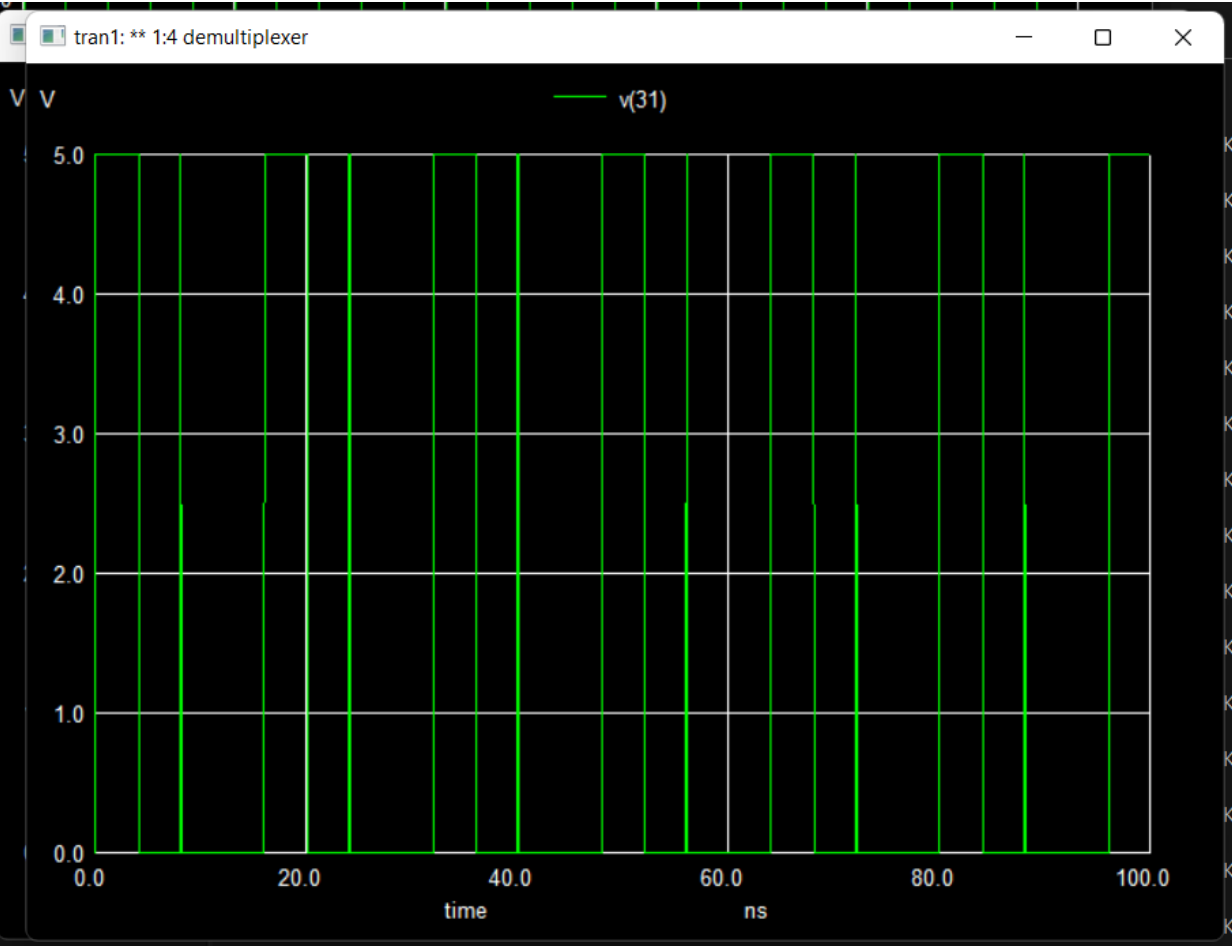
.tran 0.1ns 100ns
.control
run
plot V(10)
plot V(11)
plot V(12)
plot V(31)
plot V(30)
plot V(29)
plot V(28)
.endc
.end
```

NGSPICE OUTPUT

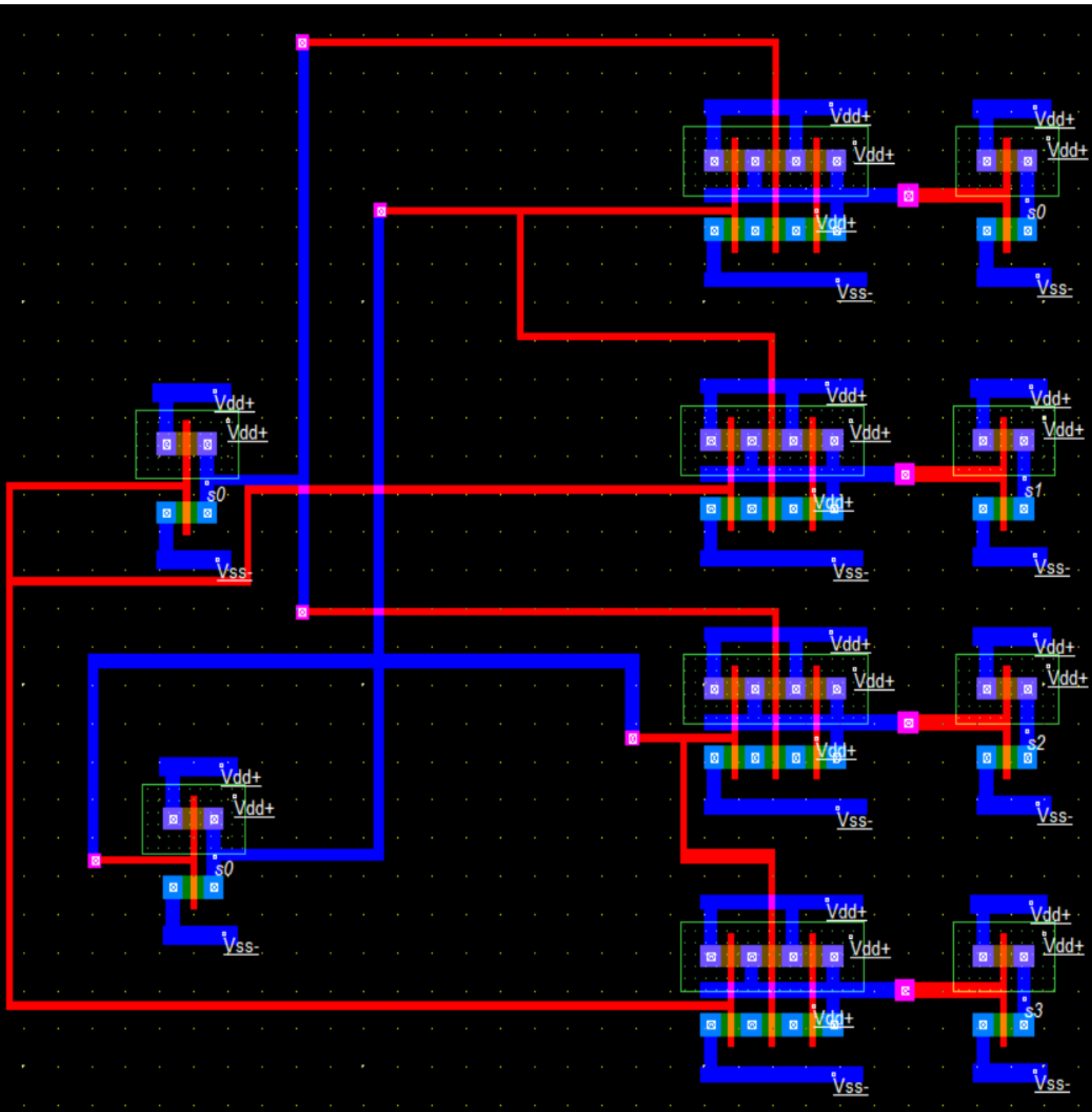




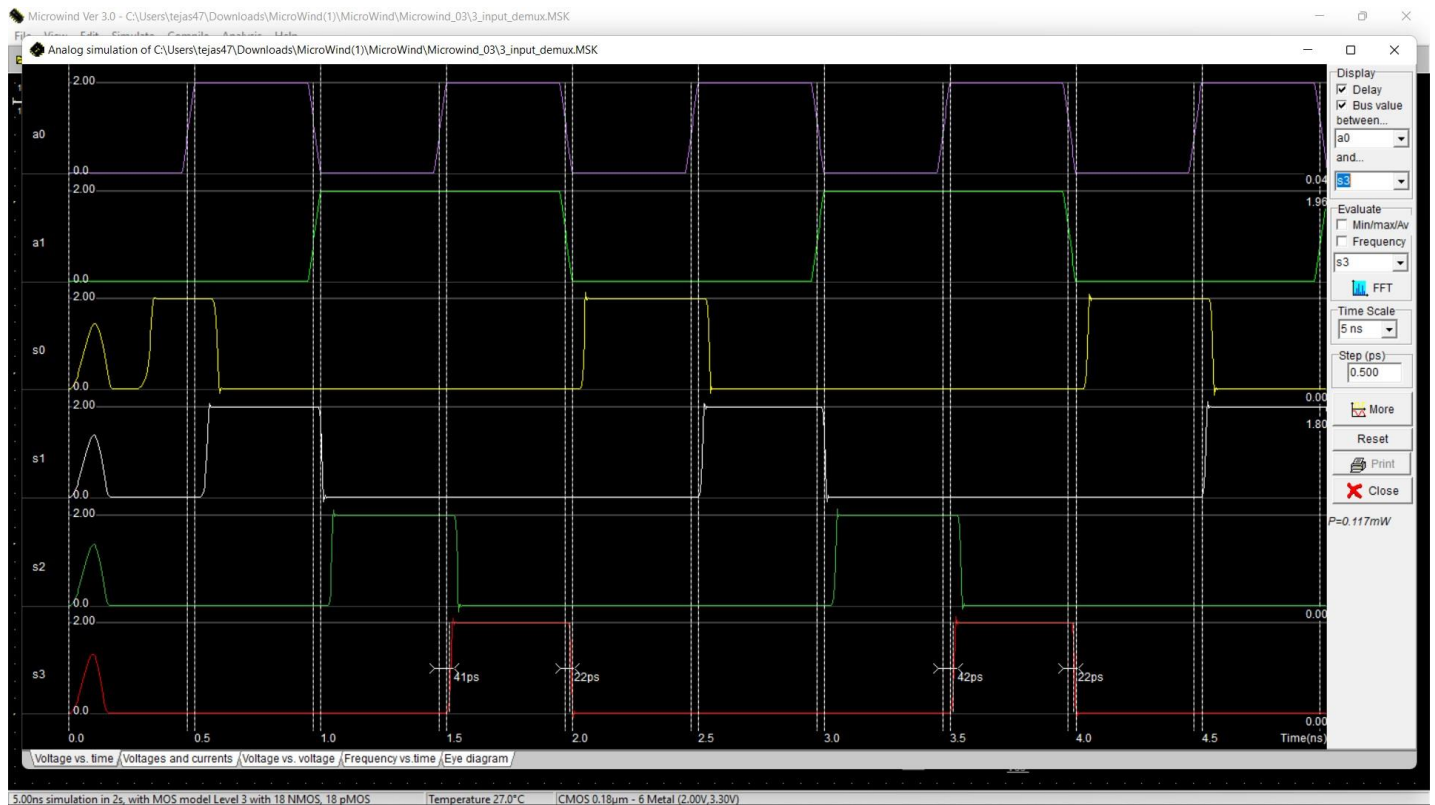




MICROWIND



MICROWIND OUTPUT



CONCLUSION -

Successfully got the output for 1:4 Demultiplexer in Ngspice as well as MicroWind

THANK YOU