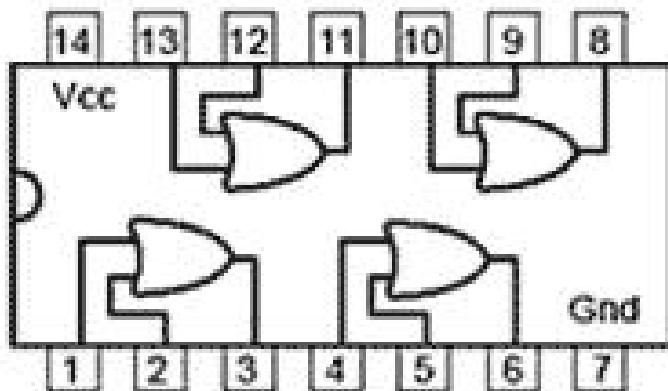
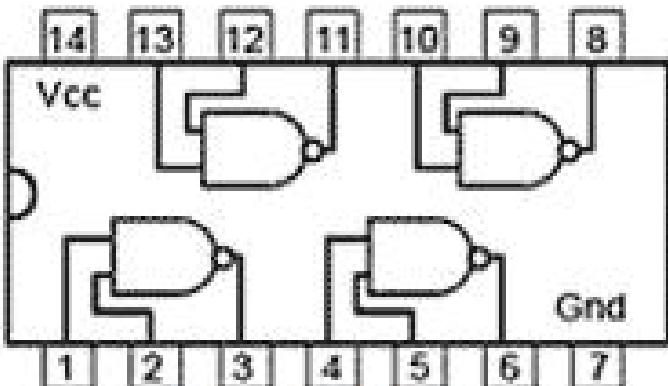


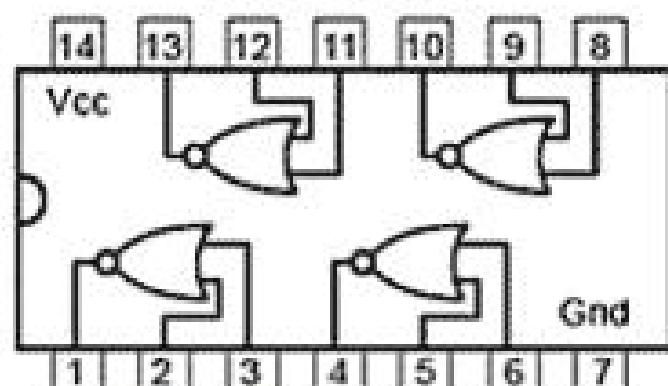
**7408 Quad 2 input  
AND Gates**



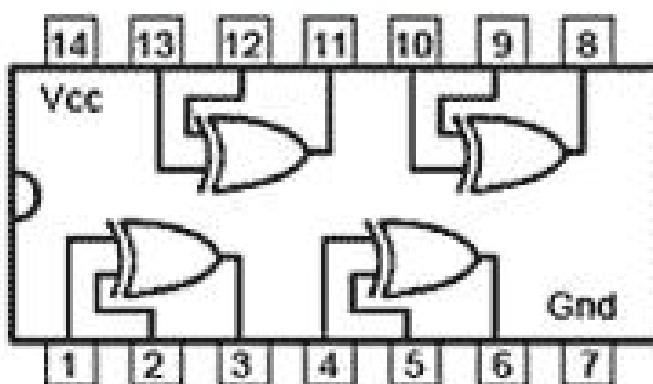
**7432 Quad 2 input  
OR Gates**



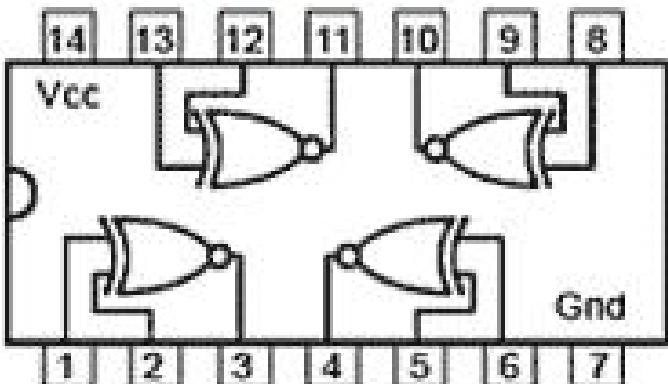
**7400 Quad 2 input  
NAND Gates**



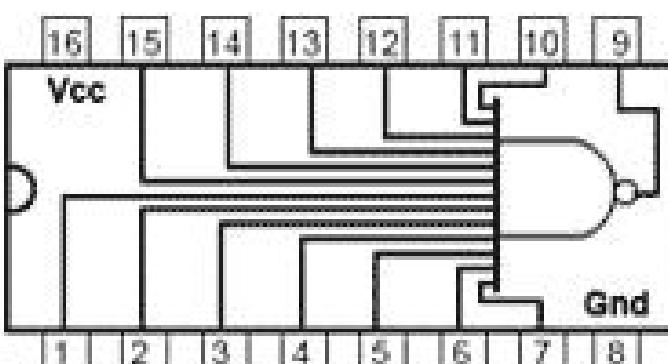
**7402 Quad 2 input  
NOR Gates**



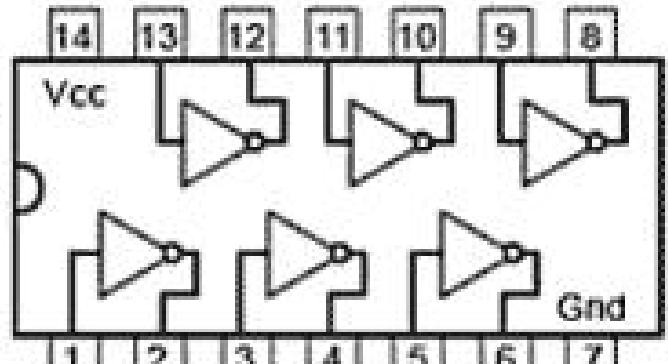
**7486 Quad 2 input  
XOR Gates**



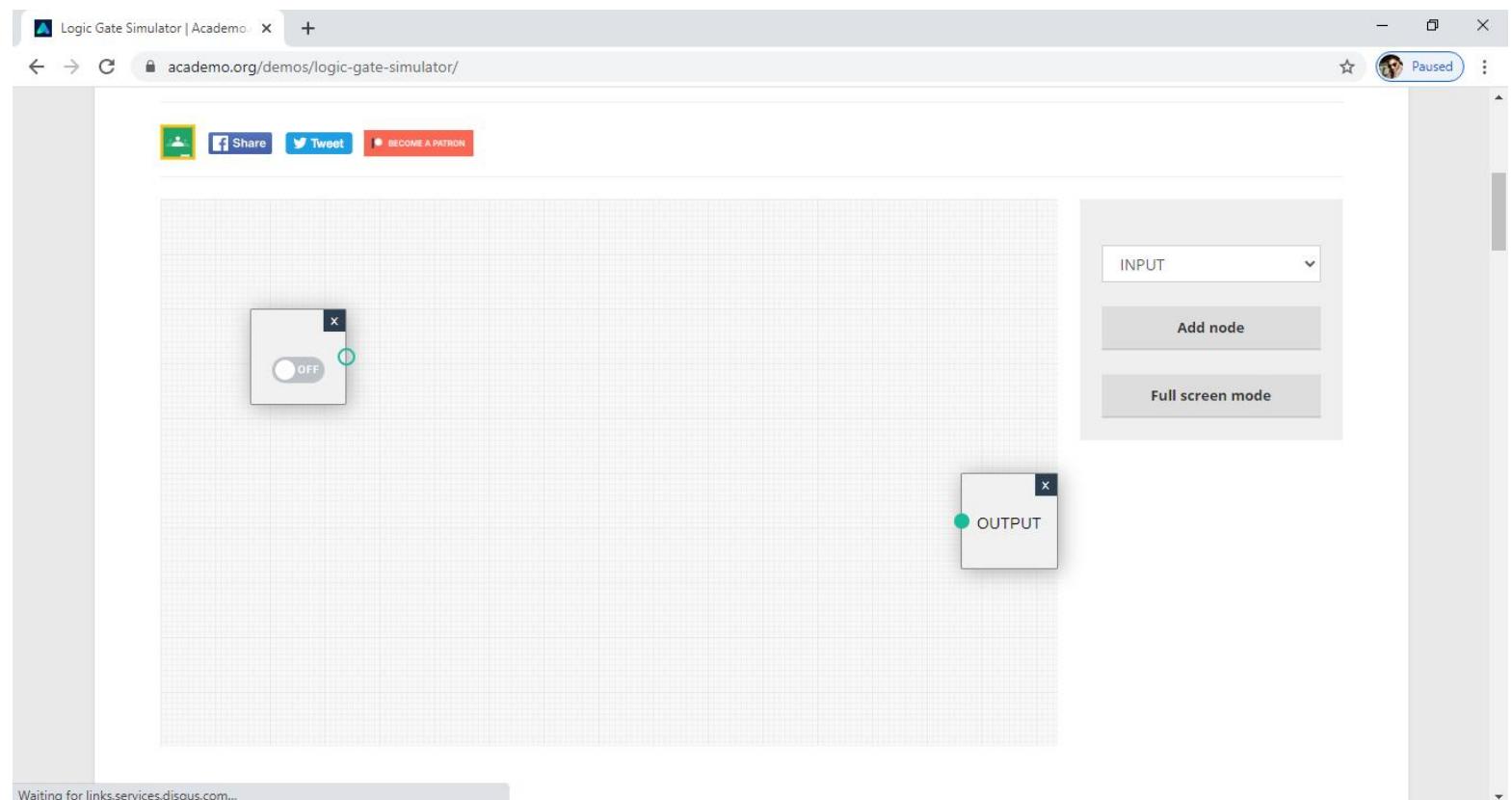
**747266 Quad 2 input  
XNOR Gates**

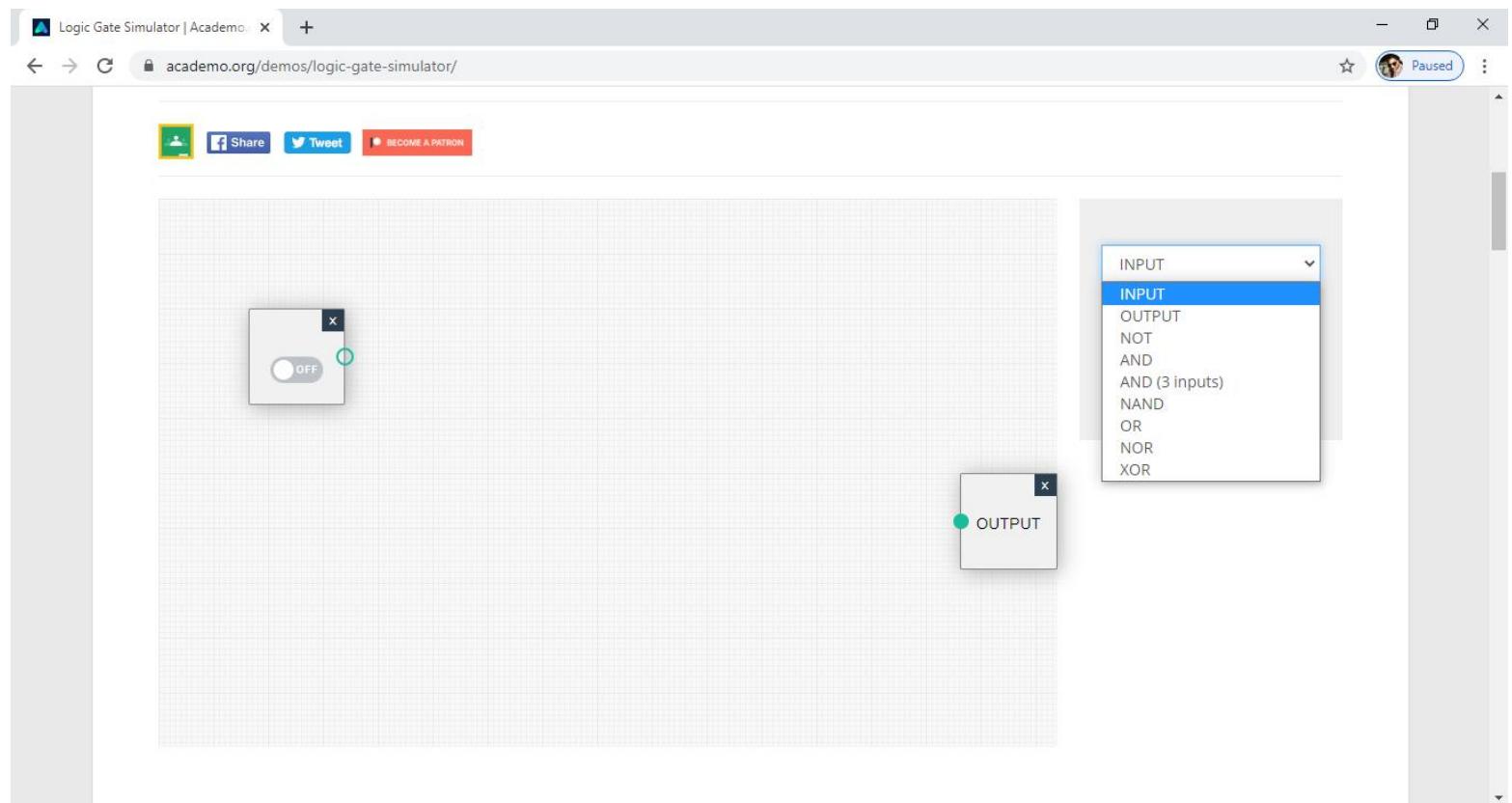


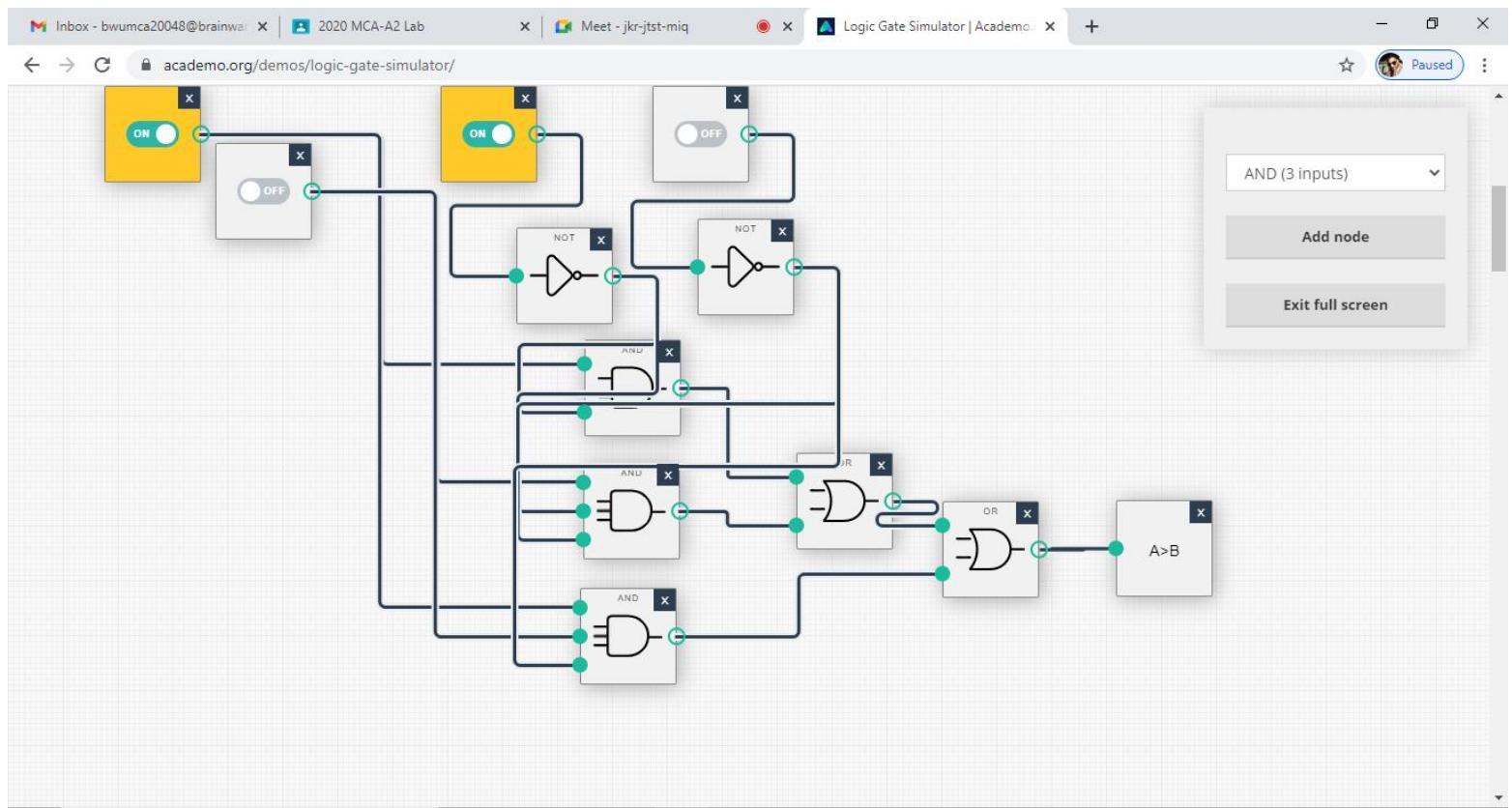
**74133 Single 13 input  
NAND Gate**

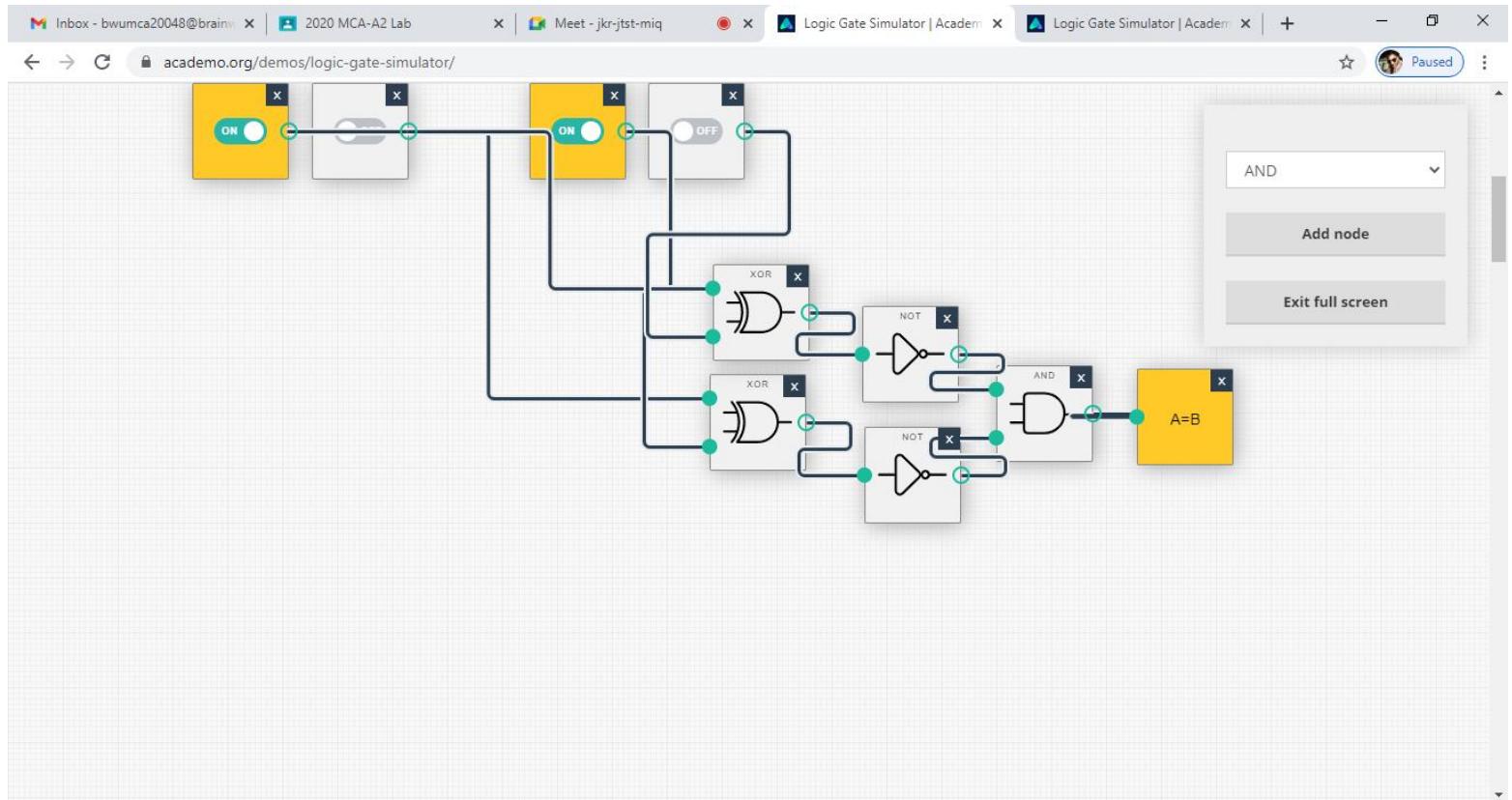


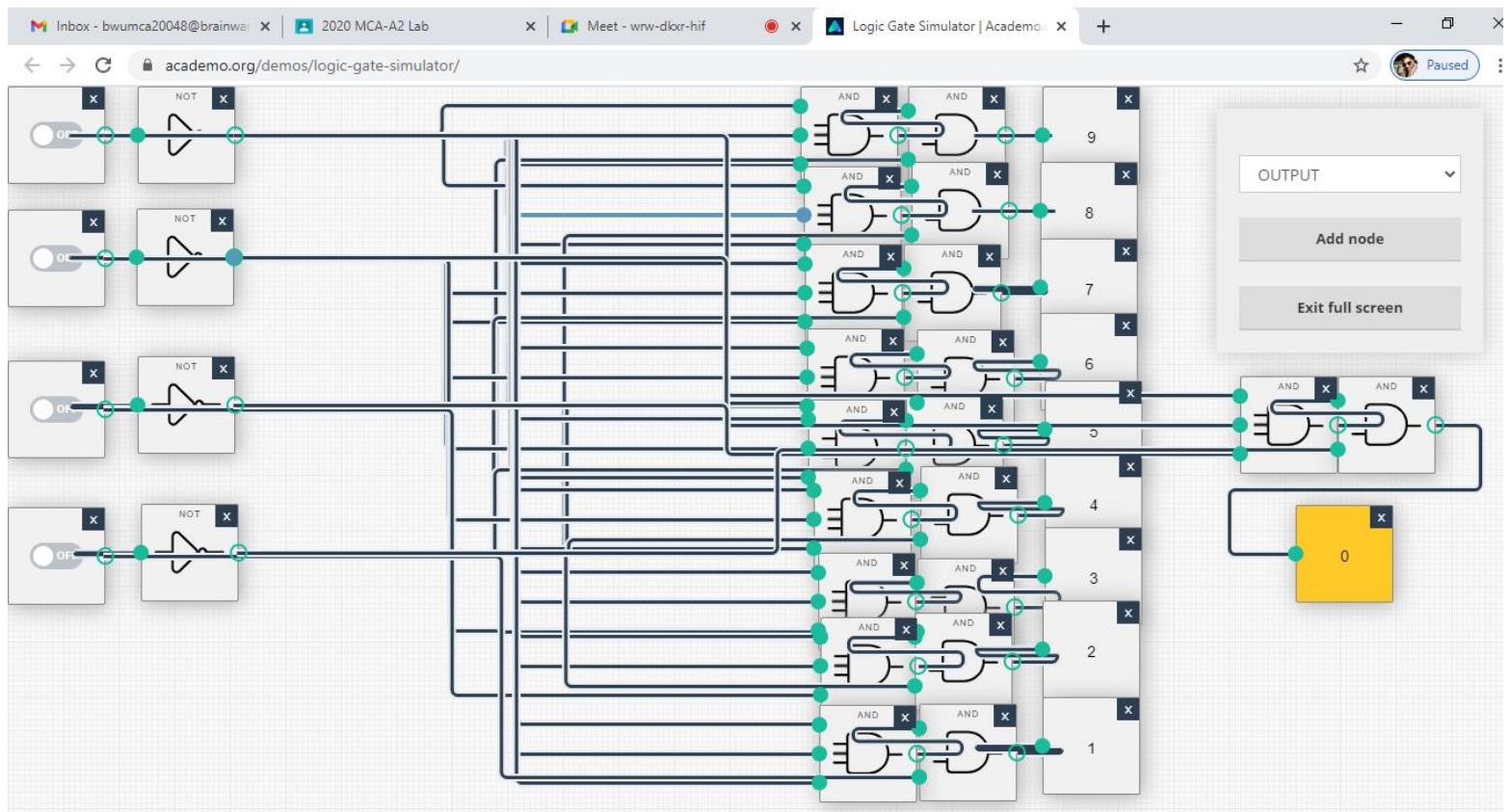
**7404 Hex NOT Gates  
(Inverters)**

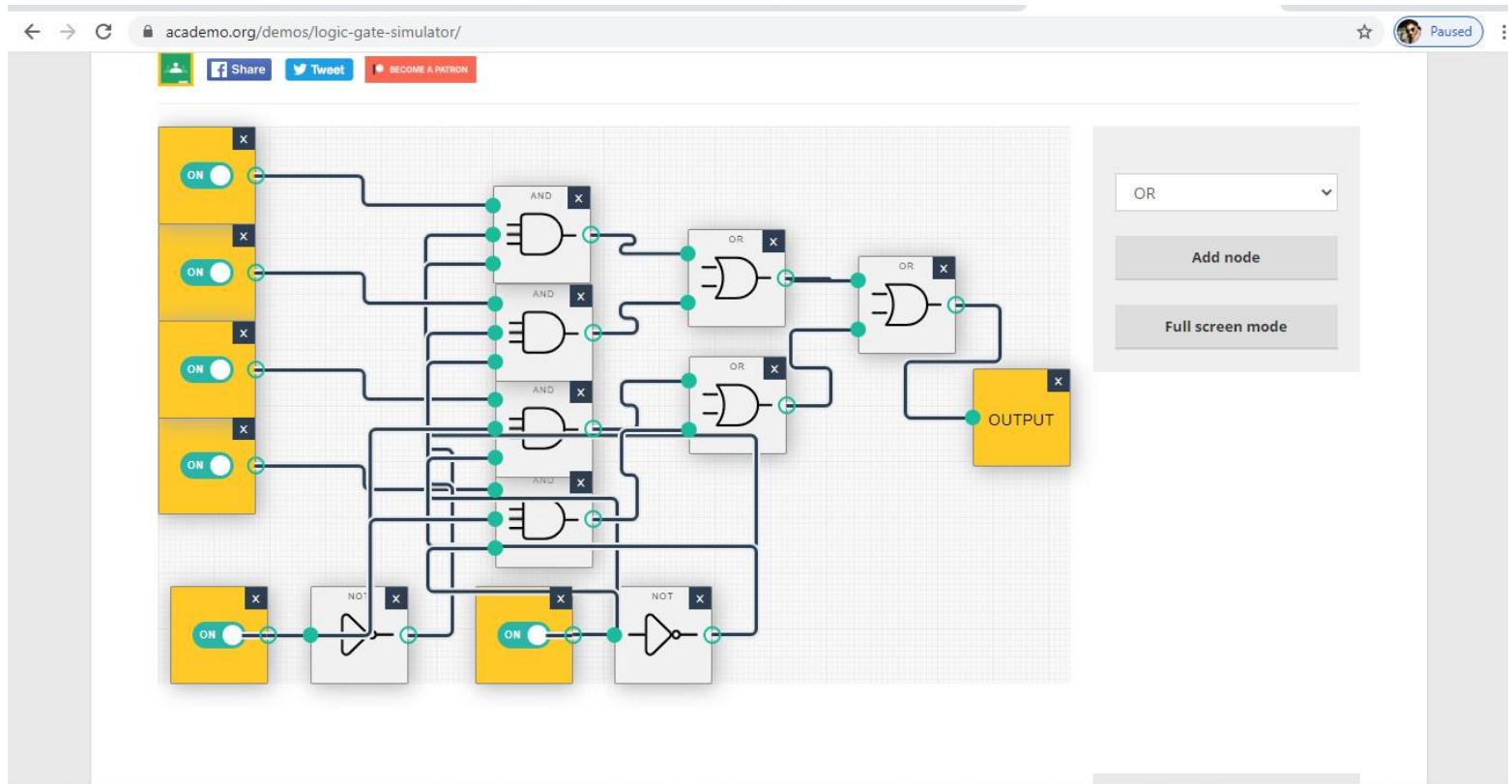


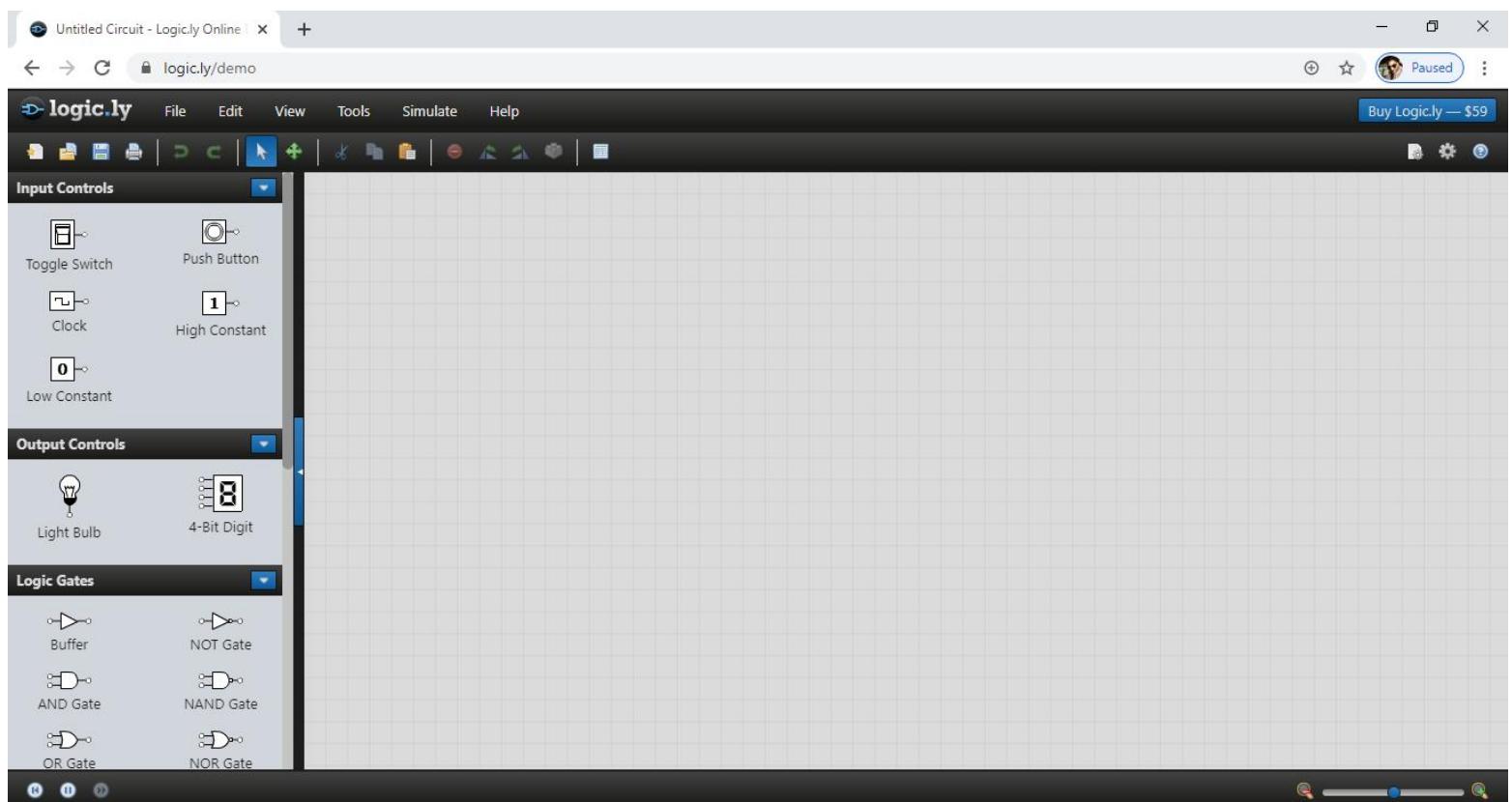


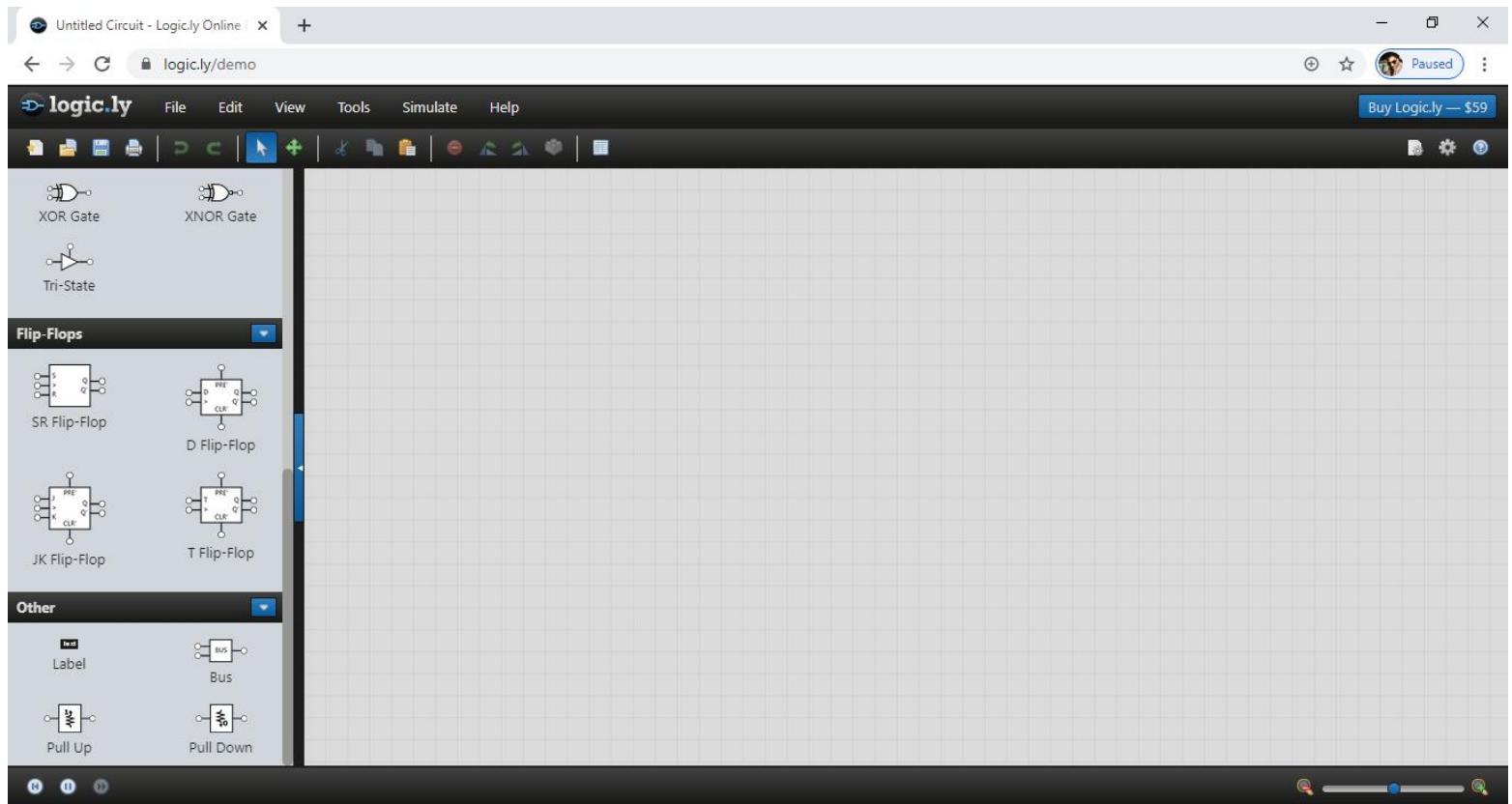












## **54LS00/DM54LS00/DM74LS00 Quad 2-Input NAND Gates**

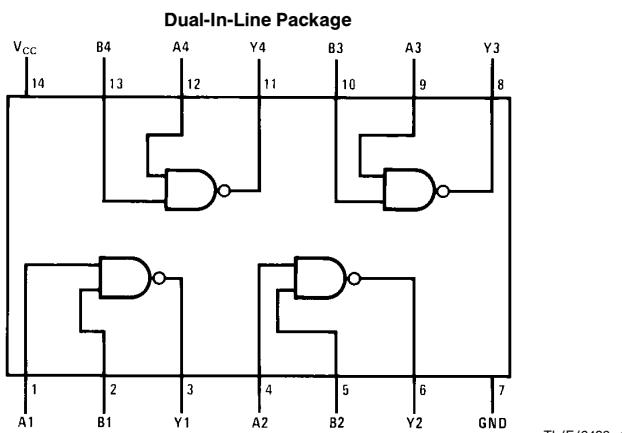
### **General Description**

This device contains four independent gates each of which performs the logic NAND function.

### **Features**

- Alternate Military/Aerospace device (54LS00) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### **Connection Diagram**



TL/F/6439-1

**Order Number 54LS00DMQB, 54LS00FMQB, 54LS00LMQB, DM54LS00J, DM54LS00W, DM74LS00M or DM74LS00N  
See NS Package Number E20A, J14A, M14A, N14A or W14B**

### **Function Table**

$$Y = \overline{AB}$$

| <b>Inputs</b> |          | <b>Output</b> |
|---------------|----------|---------------|
| <b>A</b>      | <b>B</b> | <b>Y</b>      |
| L             | L        | H             |
| L             | H        | H             |
| H             | L        | H             |
| H             | H        | L             |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS00 |     |      | DM74LS00 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                  |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 0.8             | 1.6   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 2.4             | 4.4   | mA    |

## Switching Characteristics

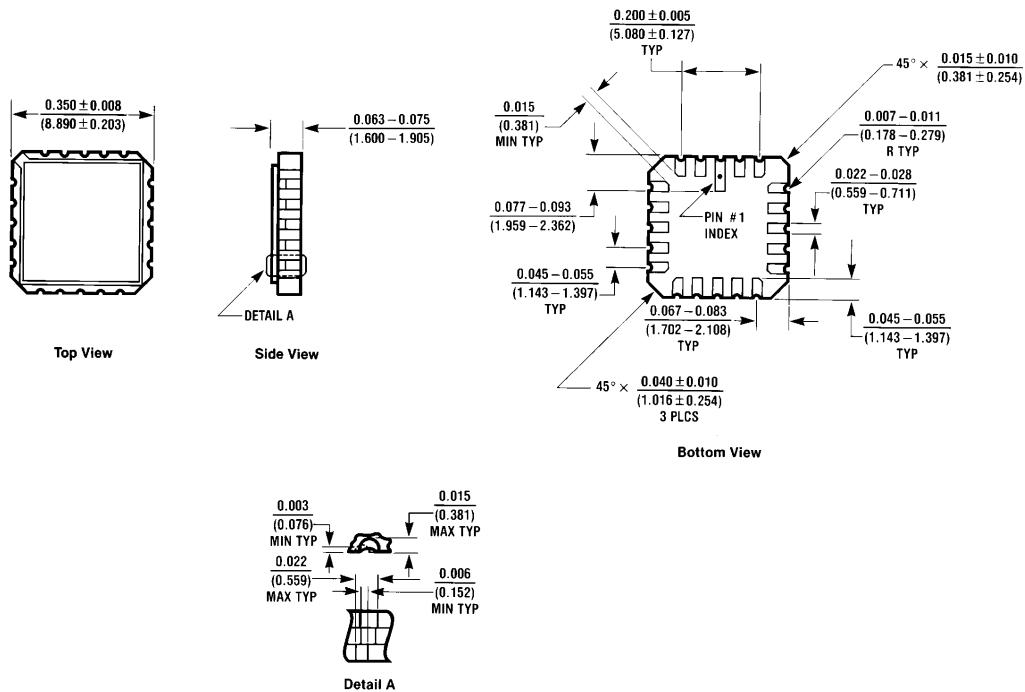
 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 10  | 4                      | 15  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 10  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

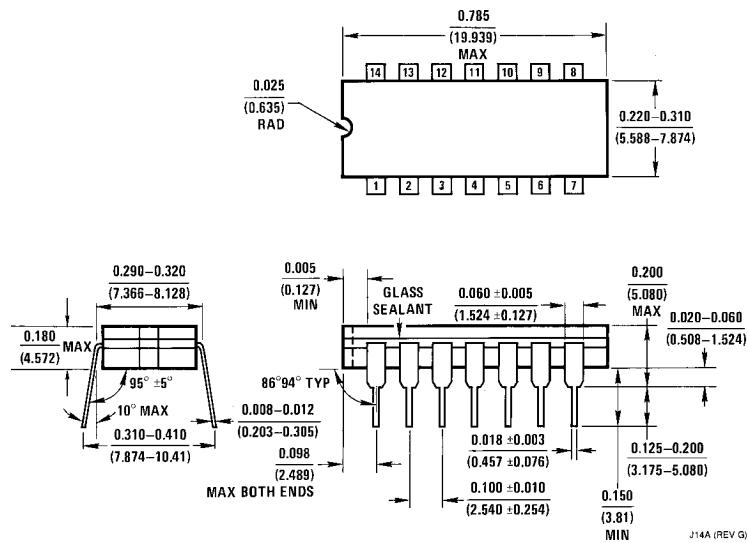
## Physical Dimensions inches (millimeters)



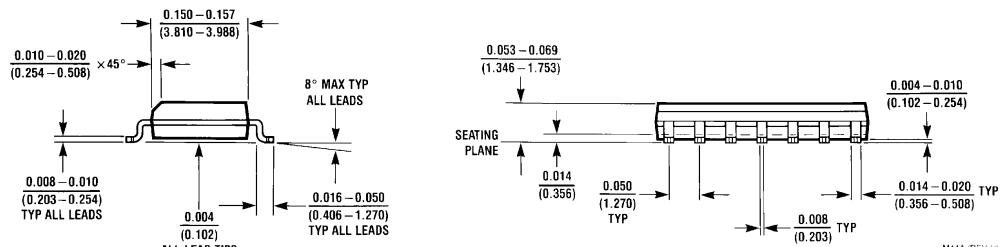
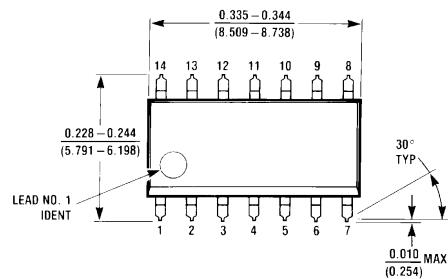
Ceramic Leadless Chip Carrier Package (E)  
 Order Number 54LS00LMQB  
 NS Package Number E20A

E20A (REV D)

**Physical Dimensions** inches (millimeters)

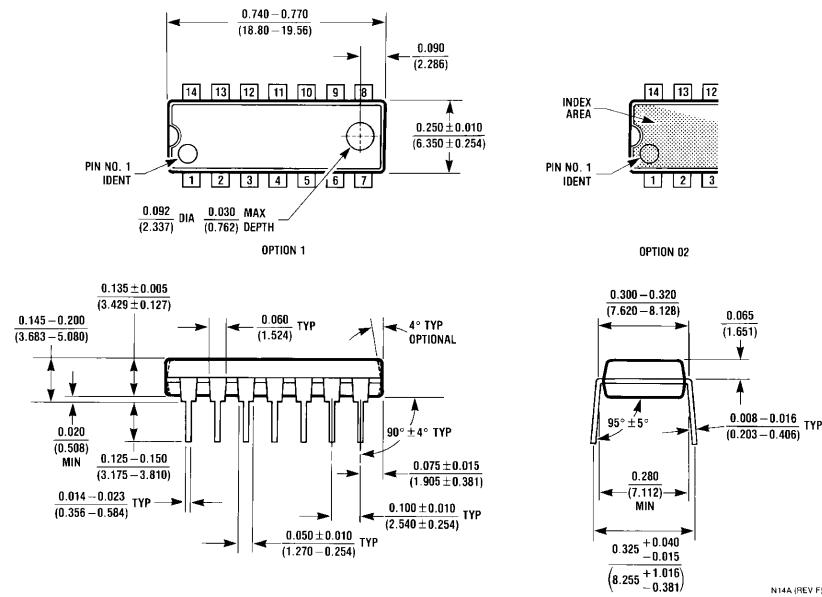


14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS00DMQB or DM54LS00J  
NS Package Number J14A



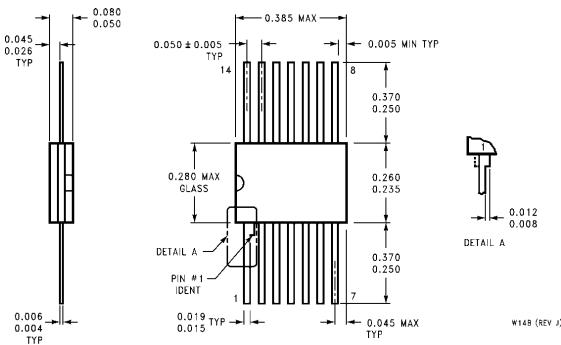
14-Lead Small Outline Molded Package (M)  
Order Number DM74LS00M  
NS Package Number M14A

## Physical Dimensions inches (millimeters) (Continued)



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS00N  
NS Package Number N14A

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number 54LS00FMQB or DM54LS00W**  
**NS Package Number W14B**

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|--|--|---|---|
|--|--|---|---|

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## 54LS02/DM54LS02/DM74LS02 Quad 2-Input NOR Gates

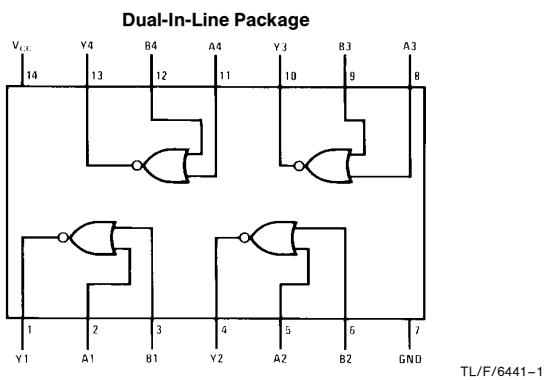
### General Description

This device contains four independent gates each of which performs the logic NOR function.

### Features

- Alternate Military/Aerospace device (54LS02) is available. Contact a National Semiconductor Sales Office/Distributor for specifications

### Connection Diagram



TL/F/6441-1

Order Number 54LS02DMQB, 54LS02FMQB, 54LS02LMQB, DM54LS02J, DM54LS02W, DM74LS02M or DM74LS02N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### Function Table

$$Y = \overline{A + B}$$

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | H      |
| L      | H | L      |
| H      | L | L      |
| H      | H | L      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS02 |     |      | DM74LS02 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol            | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|-------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>    | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>   | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 | 3.4             |       | V     |
|                   |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>   | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     | 0.25            | 0.4   | V     |
|                   |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                   |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>    | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>   | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>   | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.40 | mA    |
| I <sub>OS</sub>   | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                   |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>ICCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 1.6             | 3.2   | mA    |
| I <sub>ICCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 2.8             | 5.4   | mA    |

## Switching Characteristics

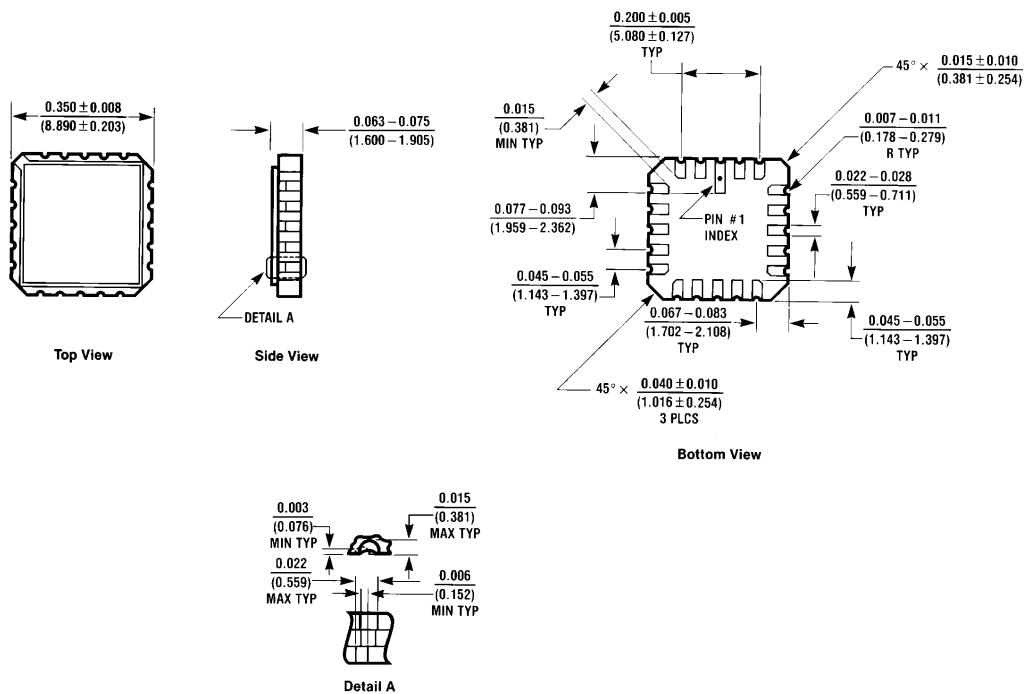
at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output |                        | 13  |                        | 18  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output |                        | 10  |                        | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

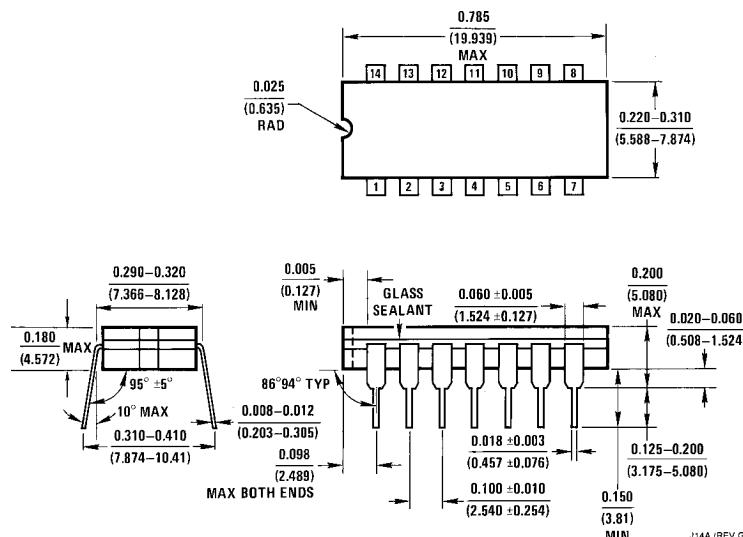
## Physical Dimensions inches (millimeters)



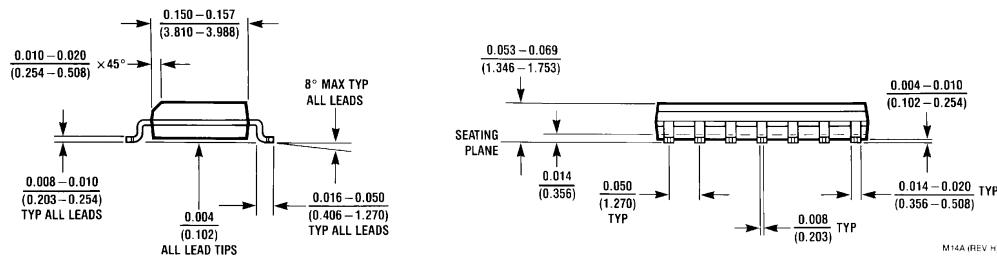
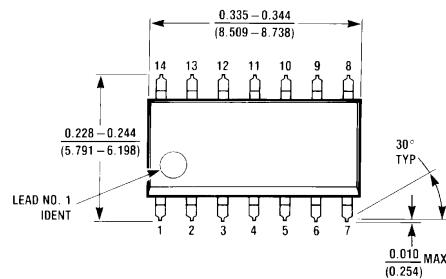
Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS02LMQB  
NS Package Number E20A

E20A (REV D)

## **Physical Dimensions** inches (millimeters) (Continued)

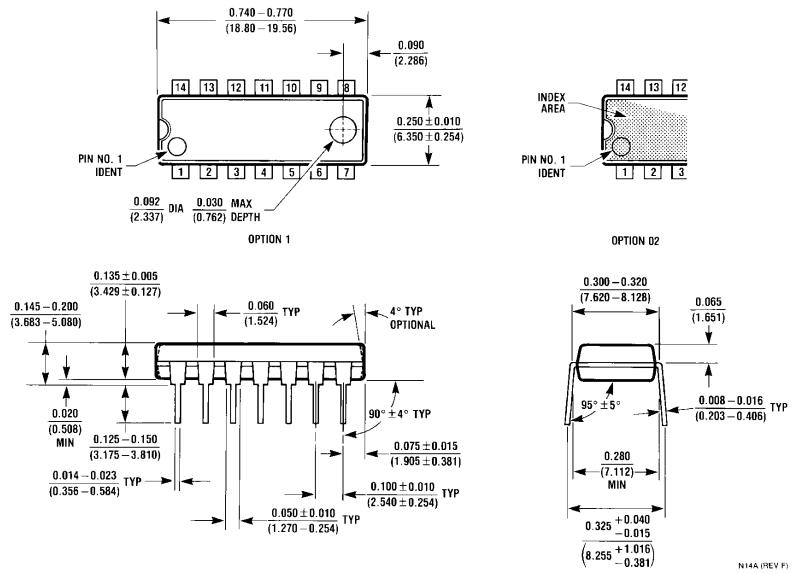


**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS02DMQB or DM54LS02J  
NS Package Number J14A**

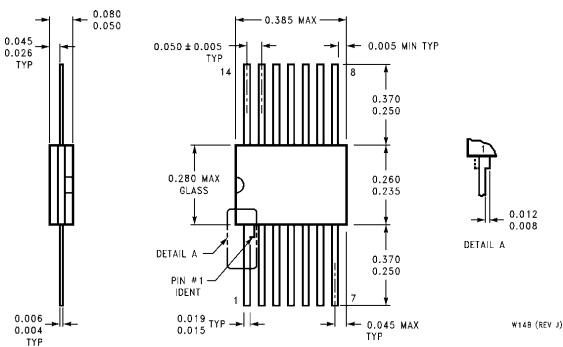


**14-Lead Small Outline Molded Package (M)  
Order Number DM74LS02M  
NS Package Number M14A**

## Physical Dimensions inches (millimeters) (Continued)



**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number 54LS02FMB or DM54LS02W**  
**NS Package Number W14B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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National Semiconductor

June 1989

# 54LS03/DM54LS03/DM74LS03 Quad 2-Input NAND Gates with Open-Collector Outputs

## 54LS03/DM54LS03/DM74LS03 Quad 2-Input NAND Gates with Open-Collector Outputs

### General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

### Features

- Alternate Military/Aerospace device (54LS03) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

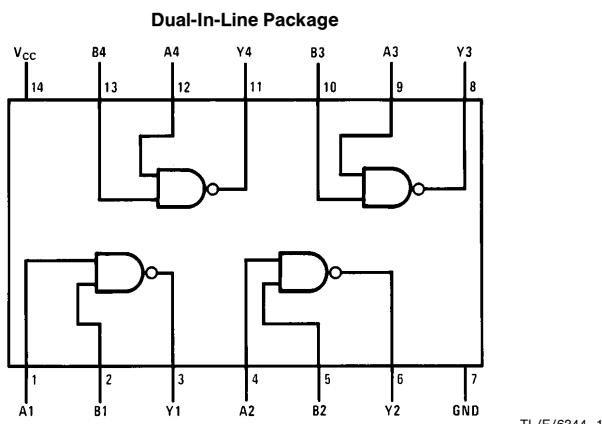
$$R_{MIN} = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where:  $N_1(I_{OH})$  = total maximum output high current for all outputs tied to pull-up resistor

$N_2(I_{IH})$  = total maximum input high current for all inputs tied to pull-up resistor

$N_3(I_{IL})$  = total maximum input low current for all inputs tied to pull-up resistor

### Connection Diagram



Order Number 54LS03DMQB, 54LS03FMQB, 54LS03LMQB,  
DM54LS03J, DM54LS03W, DM74LS03M or DM74LS03N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

### Function Table

$$Y = \overline{AB}$$

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | H      |
| L      | H | H      |
| H      | L | H      |
| H      | H | L      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Output Voltage                       | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS03 |     |     | DM74LS03 |     |      | Units |
|-----------------|--------------------------------|----------|-----|-----|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |     | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7 |          |     | 0.8  | V     |
| V <sub>OH</sub> | High Level Output Voltage      |          |     | 5.5 |          |     | 5.5  | V     |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4   |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125 | 0        |     | 70   | °C    |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

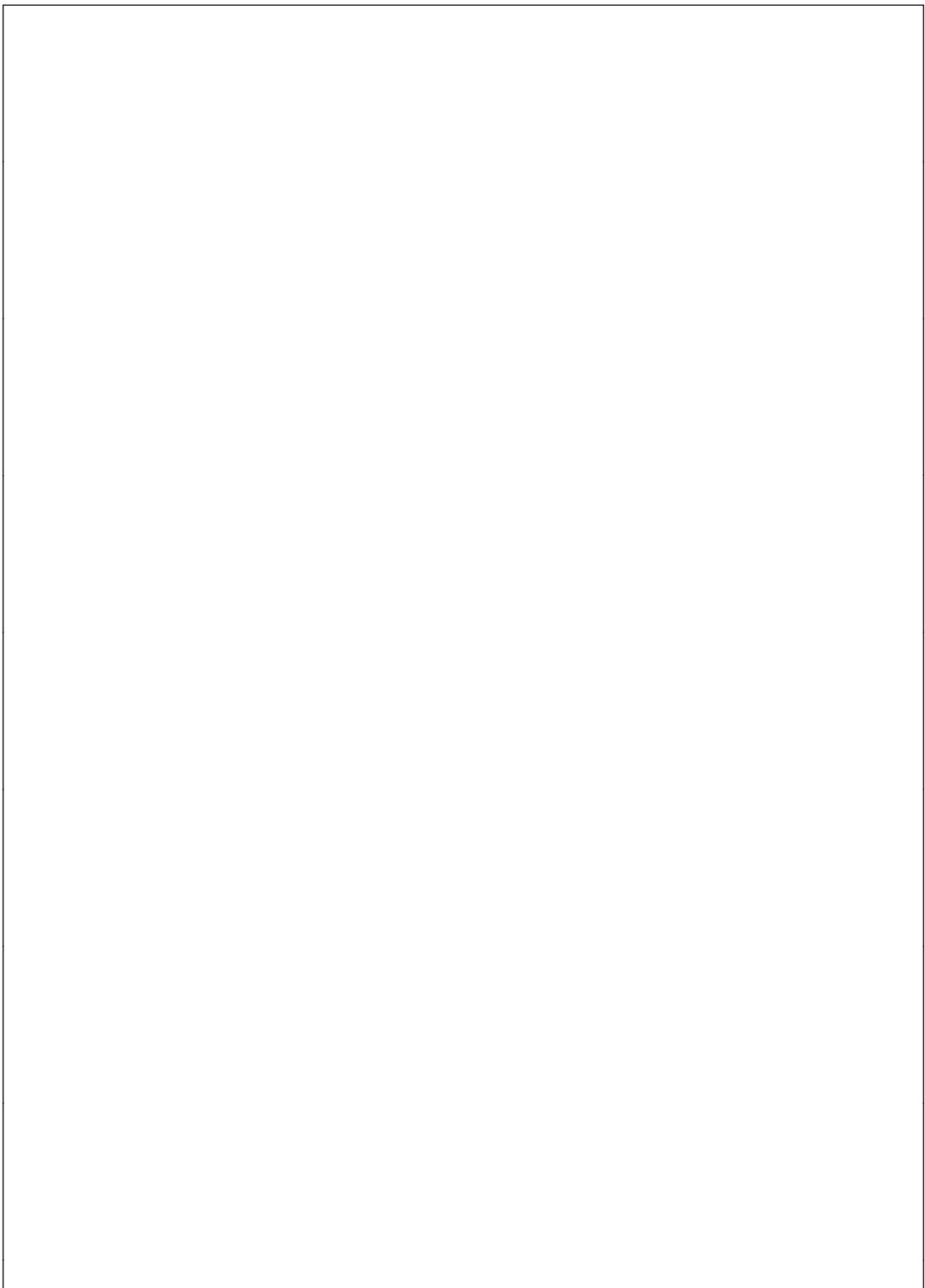
| Symbol           | Parameter                         | Conditions   |      | Min  | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|------|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |      |                 | −1.5  | V     |
| I <sub>CEx</sub> | High Level Output Current         | V <sub>CC</sub> = Min, V <sub>O</sub> = 5.5V,<br>V <sub>IL</sub> = Max |      |      |                 | 100   | μA    |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min |      | DM54 | 0.25            | 0.4   | V     |
|                  |                                   |  |      | DM74 | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |      | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |      |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |      |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |      |                 | −0.36 | mA    |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |      | 0.8             | 1.6   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |      | 2.4             | 4.4   | mA    |

## Switching Characteristics

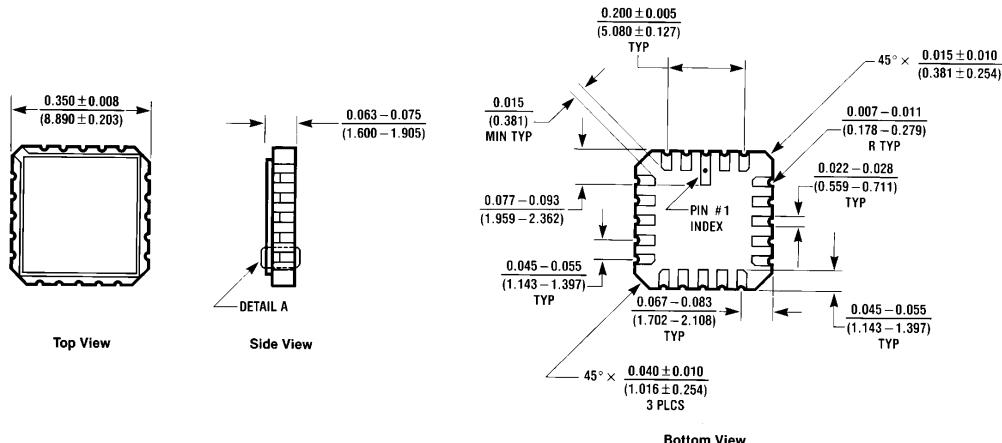
at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 6                      | 20  | 20                     | 45  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 15  | 4                      | 20  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

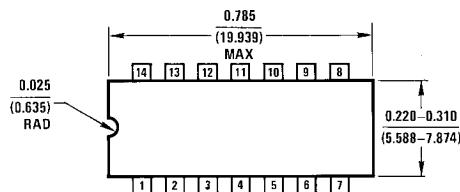


## **Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS03LMQB  
NS Package Number E20A**

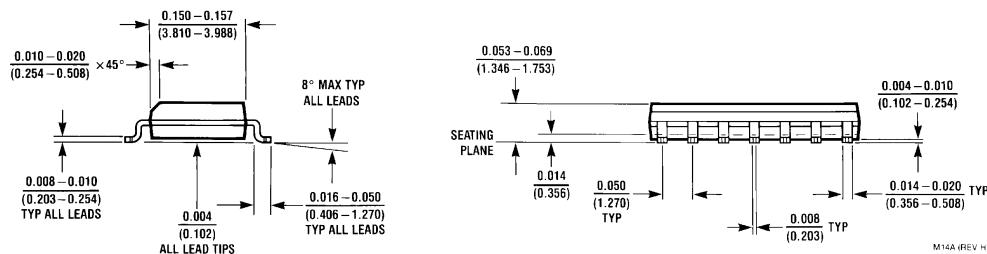
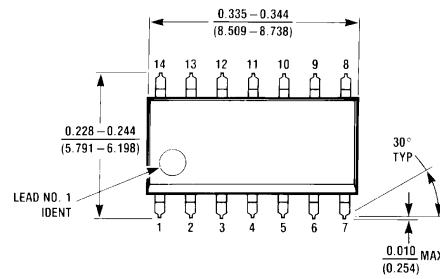
E20A (REV D)



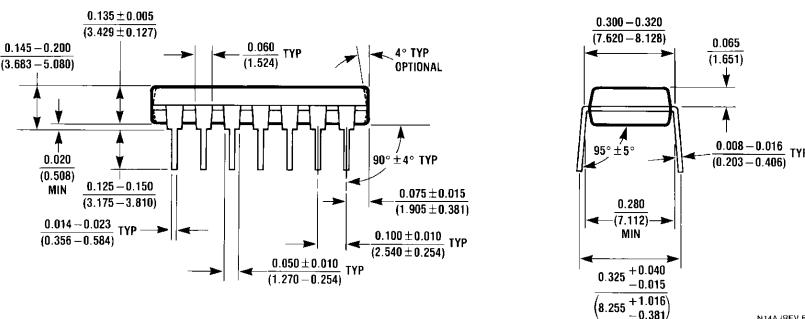
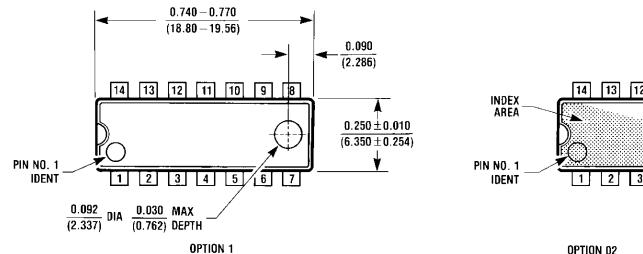
This technical drawing illustrates a cross-section of a glass sealant application. The top horizontal dimension is labeled **0.005** (0.127) MIN. The central vertical dimension is labeled **GLASS SEALANT**. The width of the sealant layer is specified as **0.060 ± 0.005** (1.524 ± 0.127). The total height of the assembly is indicated by two parallel lines at the top, labeled **0.200** (5.080) MAX and **0.020 - 0.060** (0.508 - 1.524). On the left side, a dimension of **86° 94° TYP** is shown. Below this, a dimension of **0.008 - 0.012** (0.203 - 0.305) is given, followed by **0.098** (2.489) and **MAX BOTH ENDS**. On the right side, a dimension of **0.125 - 0.200** (3.175 - 5.080) is shown, followed by **0.100 ± 0.010** (2.540 ± 0.254), **0.150** (3.81), and **MIN**.

**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS03DMQB or DM54LS03J  
NS Package Number J14A**

## Physical Dimensions inches (millimeters) (Continued)

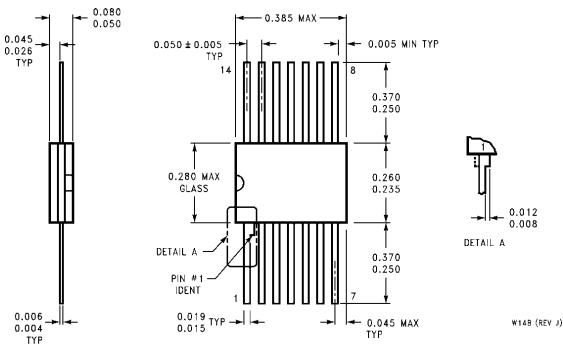


**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS03M  
NS Package Number M14A



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS03N  
NS Package Number N14A

## **Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)  
Order Number 54LS03FMQB or DM54LS03W  
NS Package Number W14B**

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  2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

|   |   |  |  |
|---|---|--|--|
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|---|---|--|--|



National Semiconductor

June 1989

# 54LS04/DM54LS04/DM74LS04 Hex Inverting Gates

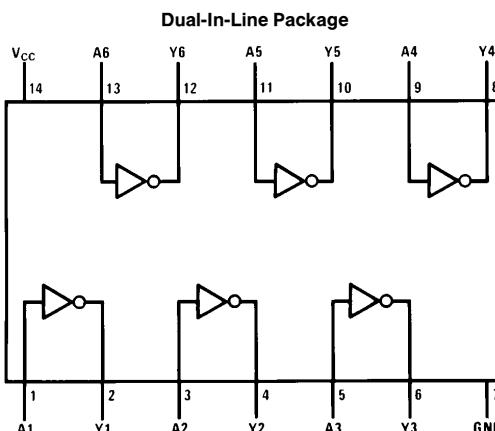
## General Description

This device contains six independent gates each of which performs the logic INVERT function.

## Features

- Alternate Military/Aerospace device (54LS04) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

## Connection Diagram



TL/F/6345-1

Order Number 54LS04DMQB, 54LS04FMQB, 54LS04LMQB, DM54LS04J, DM54LS04W, DM74LS04M or DM74LS04N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$Y = \bar{A}$$

| Input | Output |
|-------|--------|
| A     | Y      |
| L     | H      |
| H     | L      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS04 |     |      | DM74LS04 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol            | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|-------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>    | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>   | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 | 3.4             |       | V     |
|                   |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>   | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     | 0.25            | 0.4   | V     |
|                   |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                   |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>    | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>   | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>   | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>   | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                   |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>ICCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 1.2             | 2.4   | mA    |
| I <sub>ICCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 3.6             | 6.6   | mA    |

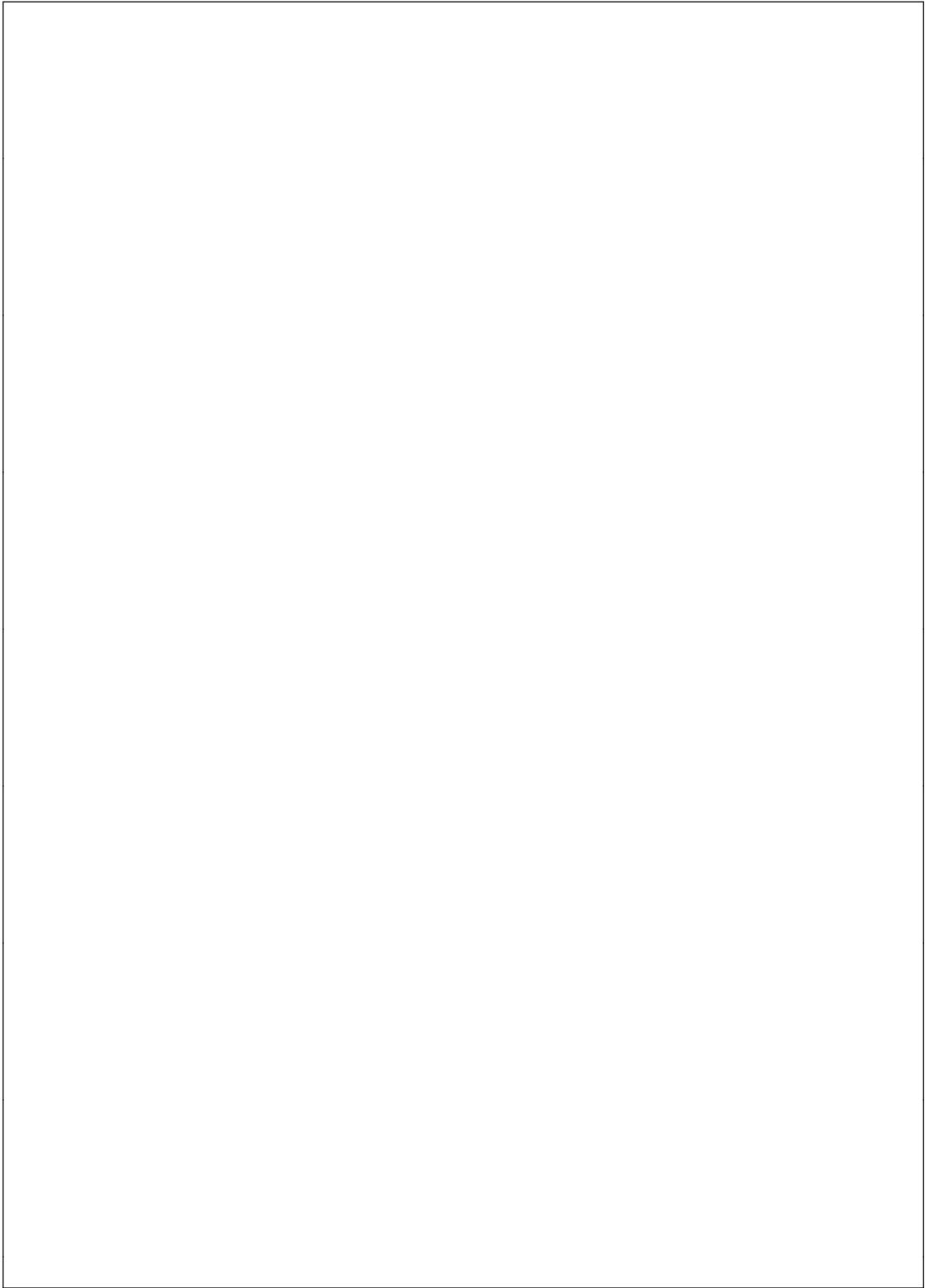
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

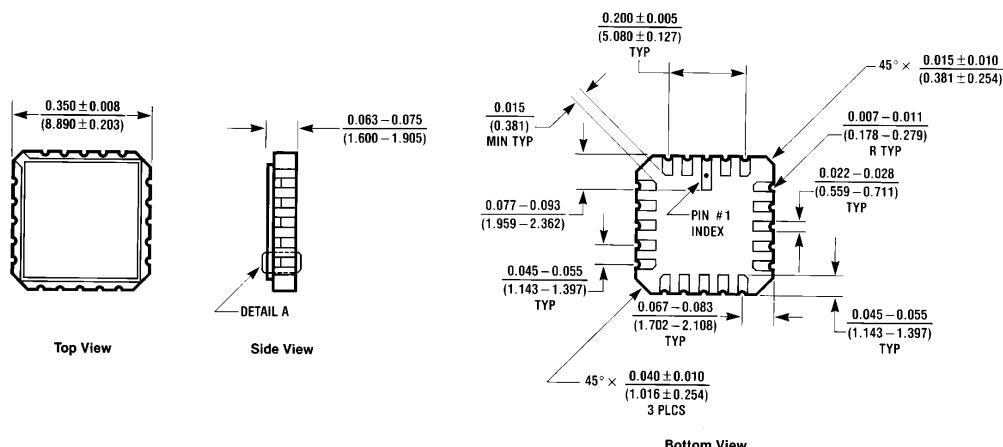
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 10  | 4                      | 15  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 10  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

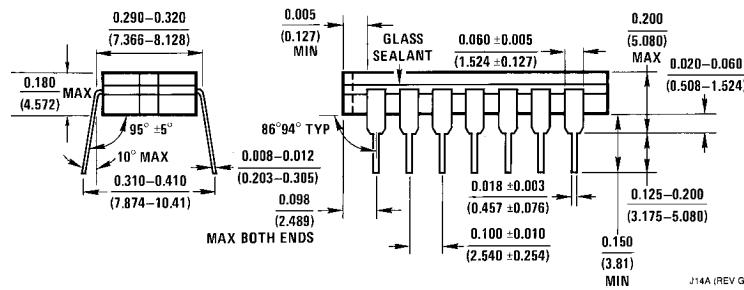
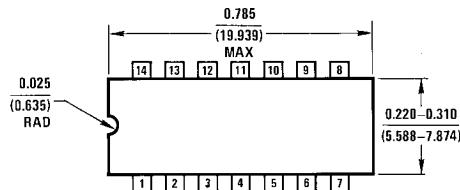


## **Physical Dimensions** inches (millimeters)



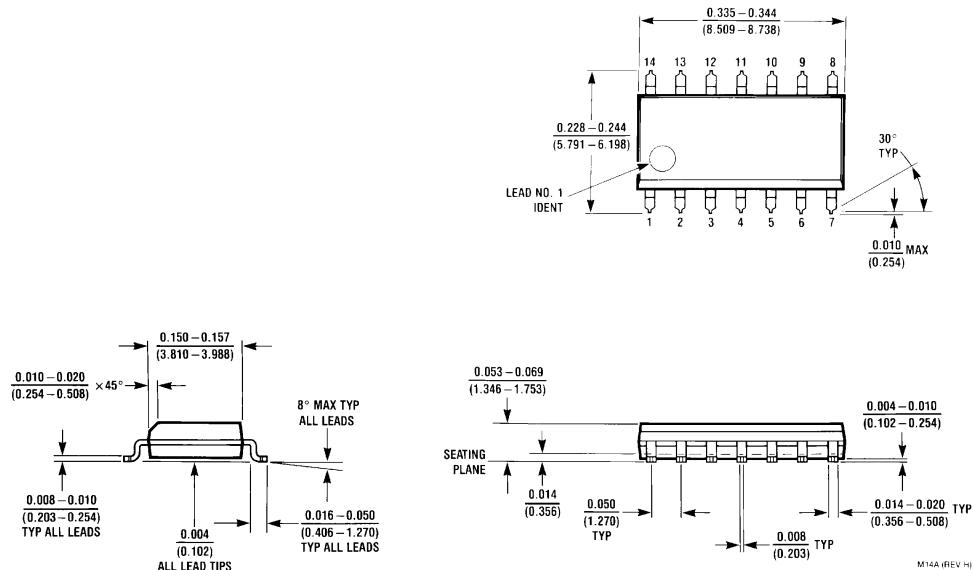
**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS04LMQB  
NS Package Number E20A**

E20A (REV D)

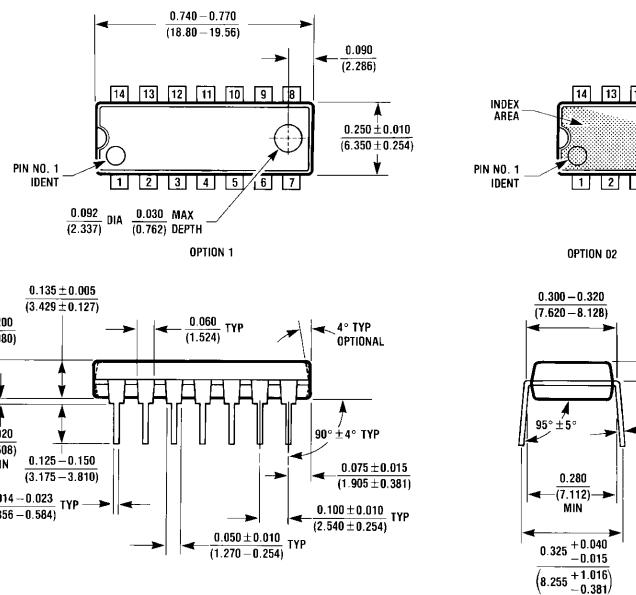


**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS04DMQB or DM54LS04J  
NS Package Number J14A**

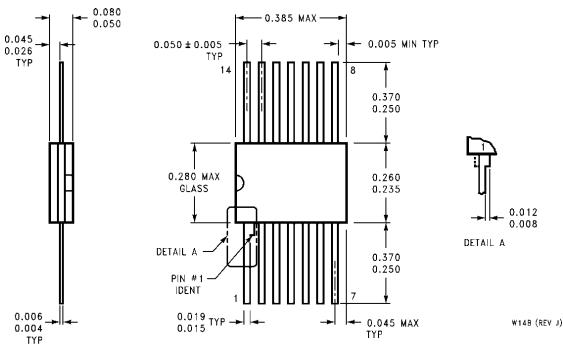
## **Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Small Outline Molded Package (M)  
Order Number DM74LS04M  
NS Package Number M14A**



**14-Lead Molded Dual-In-Line Package (N)  
Order Number DM74LS04N  
NS Package Number N14A**

**Physical Dimensions** inches (millimeters) (Continued)

**14-Lead Ceramic Flat Package (W)**  
Order Number 54LS04FMQB or DM54LS04W  
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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Fax: 81-043-299-2408

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Datasheets for electronic components.

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[http://www.ti.com/corp/docs/investor\\_relations/pr\\_09\\_23\\_2011\\_national\\_semiconductor.html](http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html)

This file is the datasheet for the following electronic components:

DM74LS04J - <http://www.ti.com/product/dm74ls04j?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM54LS04J - <http://www.ti.com/product/dm54ls04j?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM74LS04E - <http://www.ti.com/product/dm74ls04e?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM74LS04M - <http://www.ti.com/product/dm74ls04m?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM74LS04N - <http://www.ti.com/product/dm74ls04n?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM74LS04W - <http://www.ti.com/product/dm74ls04w?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM54LS04E - <http://www.ti.com/product/dm54ls04e?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM54LS04N - <http://www.ti.com/product/dm54ls04n?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM54LS04W - <http://www.ti.com/product/dm54ls04w?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

DM54LS04M - <http://www.ti.com/product/dm54ls04m?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

74LS04 - <http://www.ti.com/product/74ls04?HQS=TI-null-null-dscatalog-df-pf-null-wwe>



National Semiconductor

June 1989

# 54LS05/DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

## 54LS05/DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

### General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

### Features

- Alternate Military/Aerospace device (54LS05) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

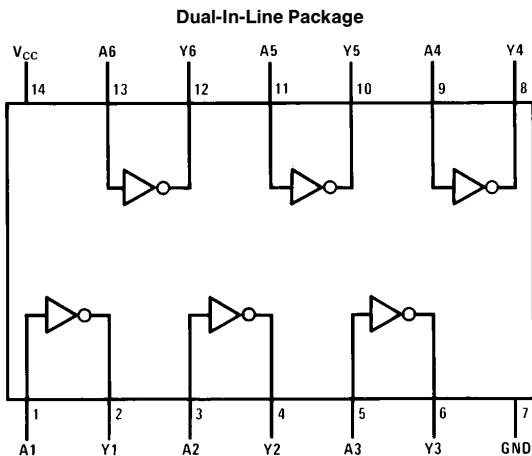
$$R_{MIN} = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where:  $N_1(I_{OH})$  = total maximum output high current for all outputs tied to pull-up resistor

$N_2(I_{IH})$  = total maximum input high current for all inputs tied to pull-up resistor

$N_3(I_{IL})$  = total maximum input low current for all inputs tied to pull-up resistor

### Connection Diagram



TL/F/6346-1

Order Number 54LS05DMQB, 54LS05FMB, DM54LS05J, DM54LS05W, DM74LS05M or DM74LS05N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

### Function Table

$$Y = \bar{A}$$

| Input | Output |
|-------|--------|
| A     | Y      |
| L     | H      |
| H     | L      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Output Voltage                       | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS05 |     |     | DM74LS05 |     |      | Units |
|-----------------|--------------------------------|----------|-----|-----|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |     | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7 |          |     | 0.8  | V     |
| V <sub>OH</sub> | High Level Output Voltage      |          |     | 5.5 |          |     | 5.5  | V     |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4   |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125 | 0        |     | 70   | °C    |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions  |      | Min  | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|---|------|------|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                        |      |      |                 | −1.5  | V     |
| I <sub>CEx</sub> | High Level Output Current         | V <sub>CC</sub> = Min, V <sub>O</sub> = 5.5V<br>V <sub>IL</sub> = Max |      |      |                 | 100   | μA    |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IH</sub> = Min |      | DM54 | 0.25            | 0.4   | V     |
|                  |                                   | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IH</sub> = Min |      | DM74 | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                         | DM74 |      | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                            |      |      |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                          |      |      |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                          |      |      |                 | −0.36 | mA    |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max   |      |      | 1.2             | 2.4   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max   |      |      | 3.6             | 6.6   | mA    |

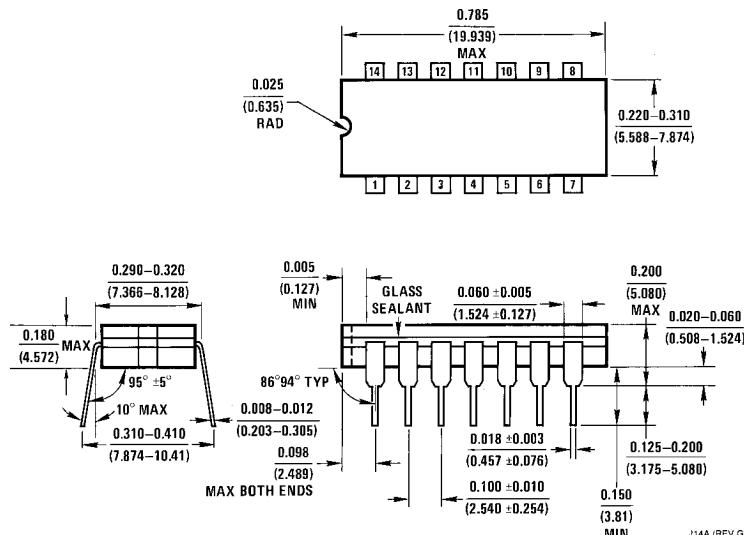
## Switching Characteristics

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

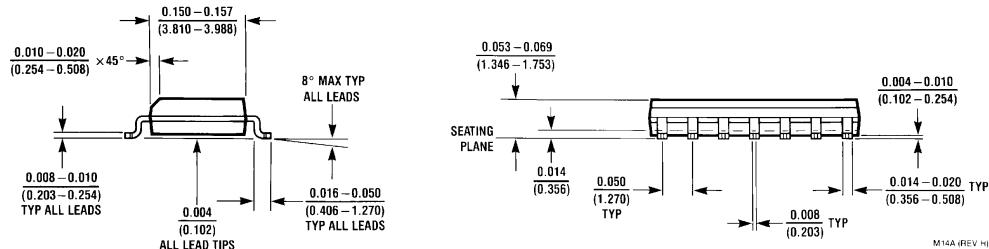
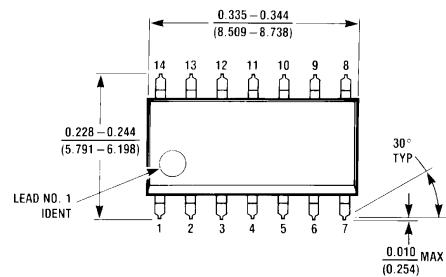
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 6                      | 20  | 20                     | 45  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 15  | 4                      | 20  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Physical Dimensions** inches (millimeters)



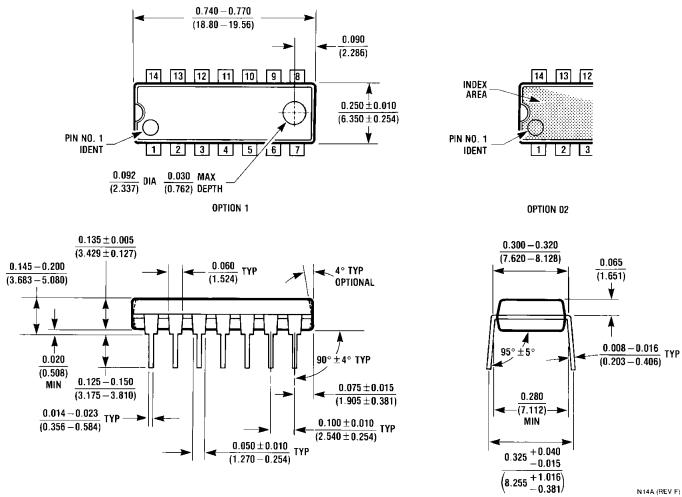
**14-Lead Ceramic Dual-In-Line Package (J)**  
Order Number 54LS05DMQB or DM54LS05J  
NS Package Number J14A



**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS05M  
NS Package Number M14A

# 54LS05/DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

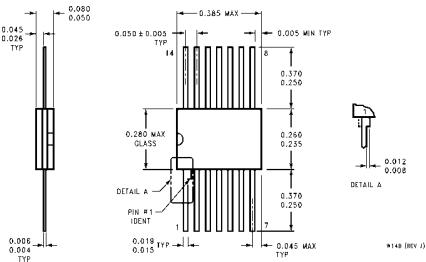
## Physical Dimensions inches (millimeters) (Continued)



**14-Lead Molded Dual-In-Line Package (N)**

Order Number DM74LS05N

NS Package Number N14A



**14-Lead Ceramic Flat Package (W)**

Order Number 54LS05FMQB or DM54LS05W

NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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## 54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

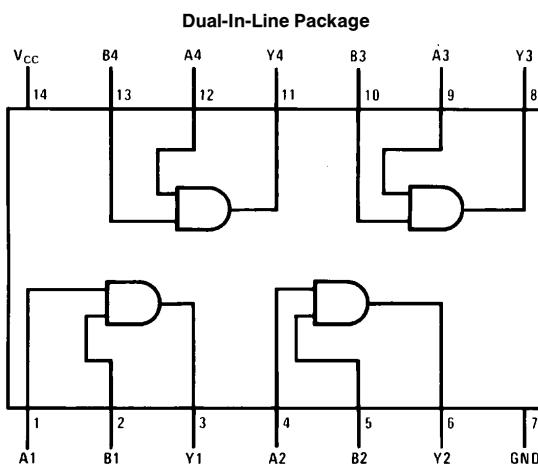
### General Description

This device contains four independent gates each of which performs the logic AND function.

### Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### Connection Diagram



TL/F/6347-1

**Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N  
See NS Package Number E20A, J14A, M14A, N14A or W14B**

### Function Table

$$Y = AB$$

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | L      |
| H      | L | L      |
| H      | H | H      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS08 |     |      | DM74LS08 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                  |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 2.4             | 4.8   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 4.4             | 8.8   | mA    |

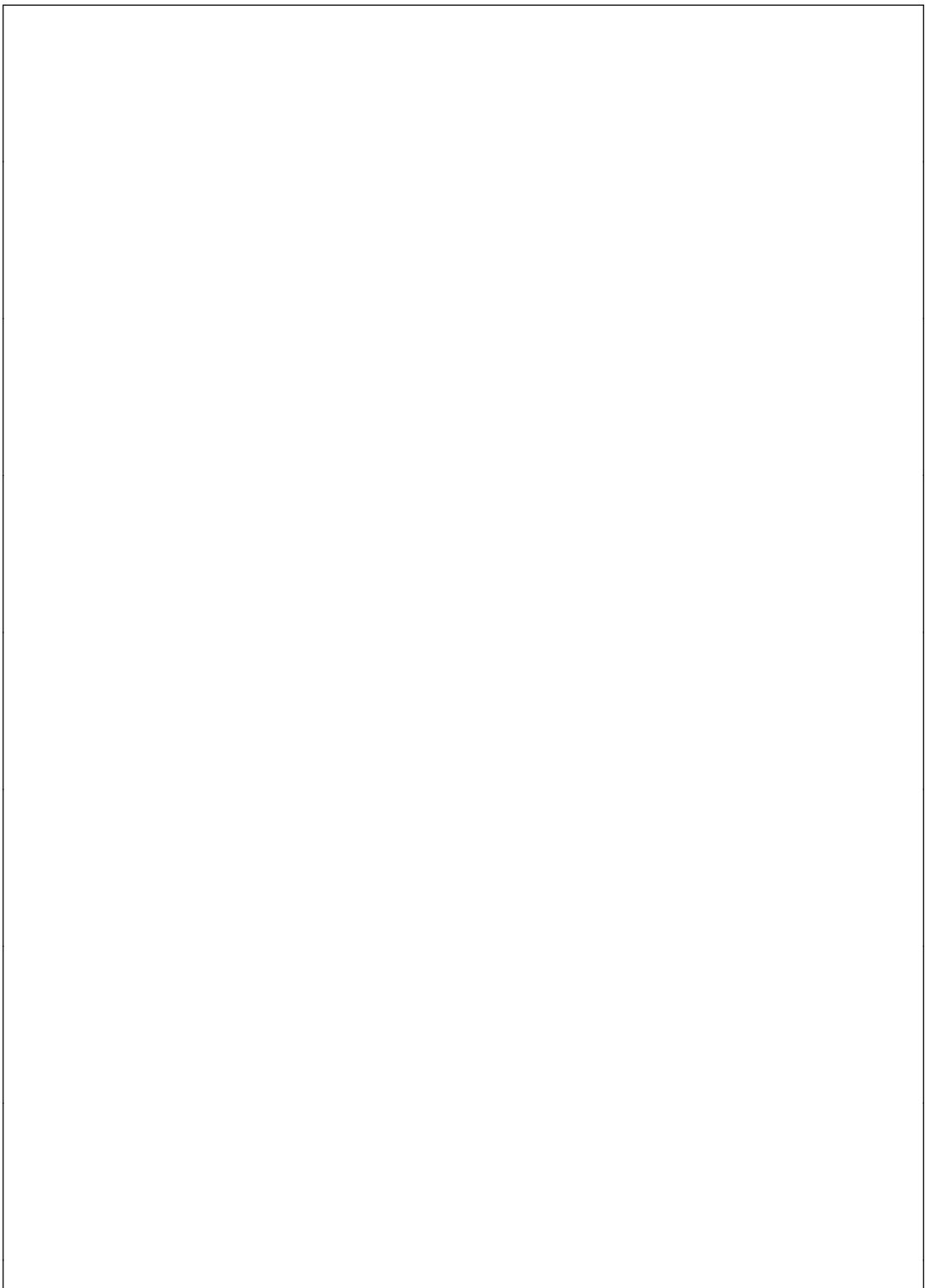
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

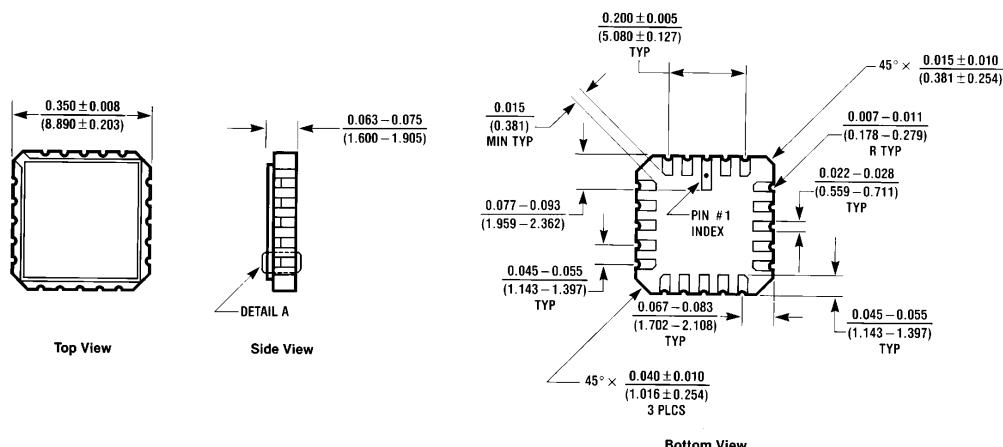
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 4                      | 13  | 6                      | 18  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 11  | 5                      | 18  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

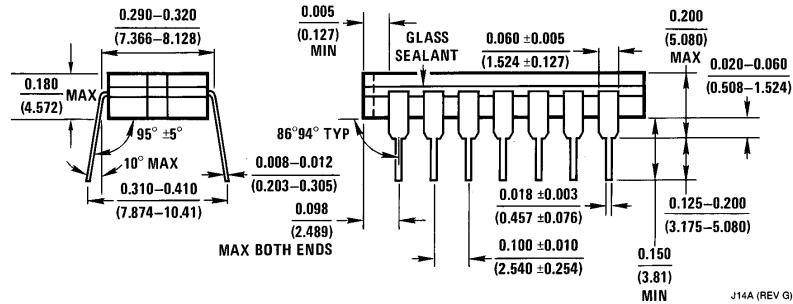
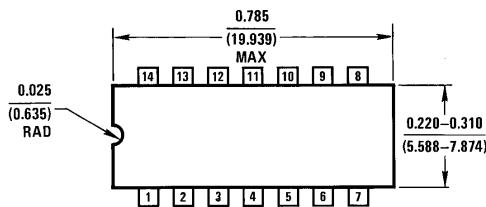


## **Physical Dimensions** inches (millimeters)



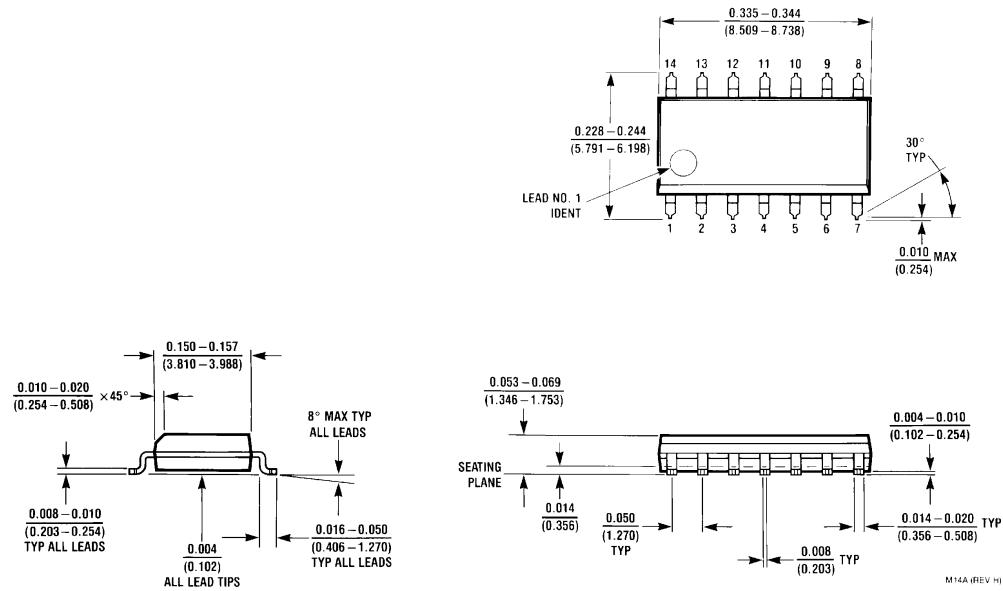
**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS08LMQB  
NS Package Number E20A**

E20A (REV D)

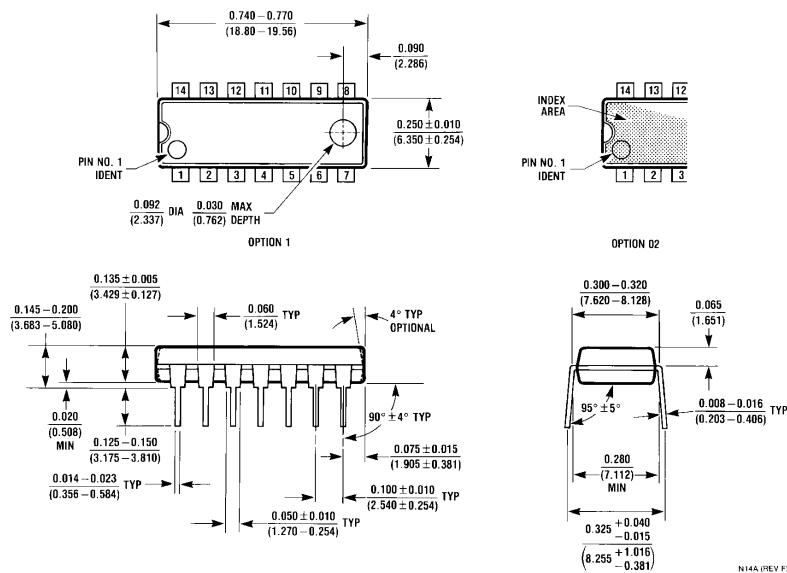


**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS08DMQB or DM54LS08J  
NS Package Number J14A**

## **Physical Dimensions** inches (millimeters) (Continued)

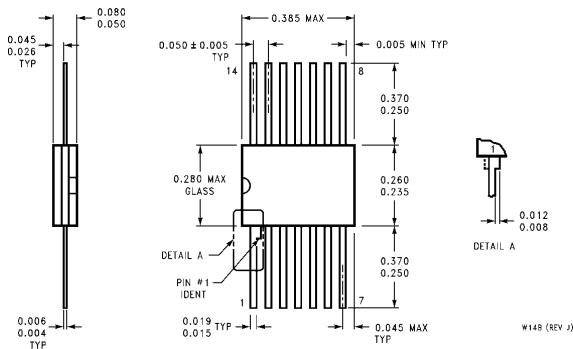


**14-Lead Small Outline Molded Package (M)  
Order Number DM74LS08M  
NS Package Number M14A**



**14-Lead Molded Dual-In-Line Package (N)  
Order Number DM74LS08N  
NS Package Number N14A**

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
Order Number 54LS08FMB or DM54LS08W  
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

|   |   |  |  |
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|---|---|--|--|

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## **54LS10/DM54LS10/DM74LS10** **Triple 3-Input NAND Gates**

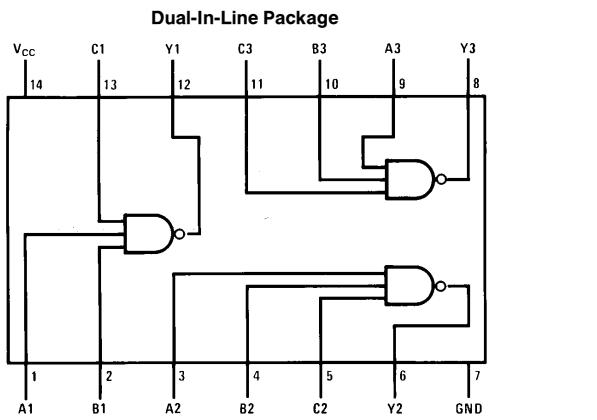
### **General Description**

This device contains three independent gates each of which performs the logic NAND function.

### **Features**

- Alternate Military/Aerospace device (54LS10) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### **Connection Diagram**



TL/F/6349-1

Order Number 54LS10DMQB, 54LS10FMBQ, 54LS10LMQB,  
 DM54LS10J, DM54LS10W, DM74LS10M or DM74LS10N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### **Function Table**

$$Y = \overline{ABC}$$

| Inputs |   |   | Output |
|--------|---|---|--------|
| A      | B | C | Y      |
| X      | X | L | H      |
| X      | L | X | H      |
| L      | X | X | H      |
| H      | H | H | L      |

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS10 |     |      | DM74LS10 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                  |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 0.6             | 1.2   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 1.8             | 3.3   | mA    |

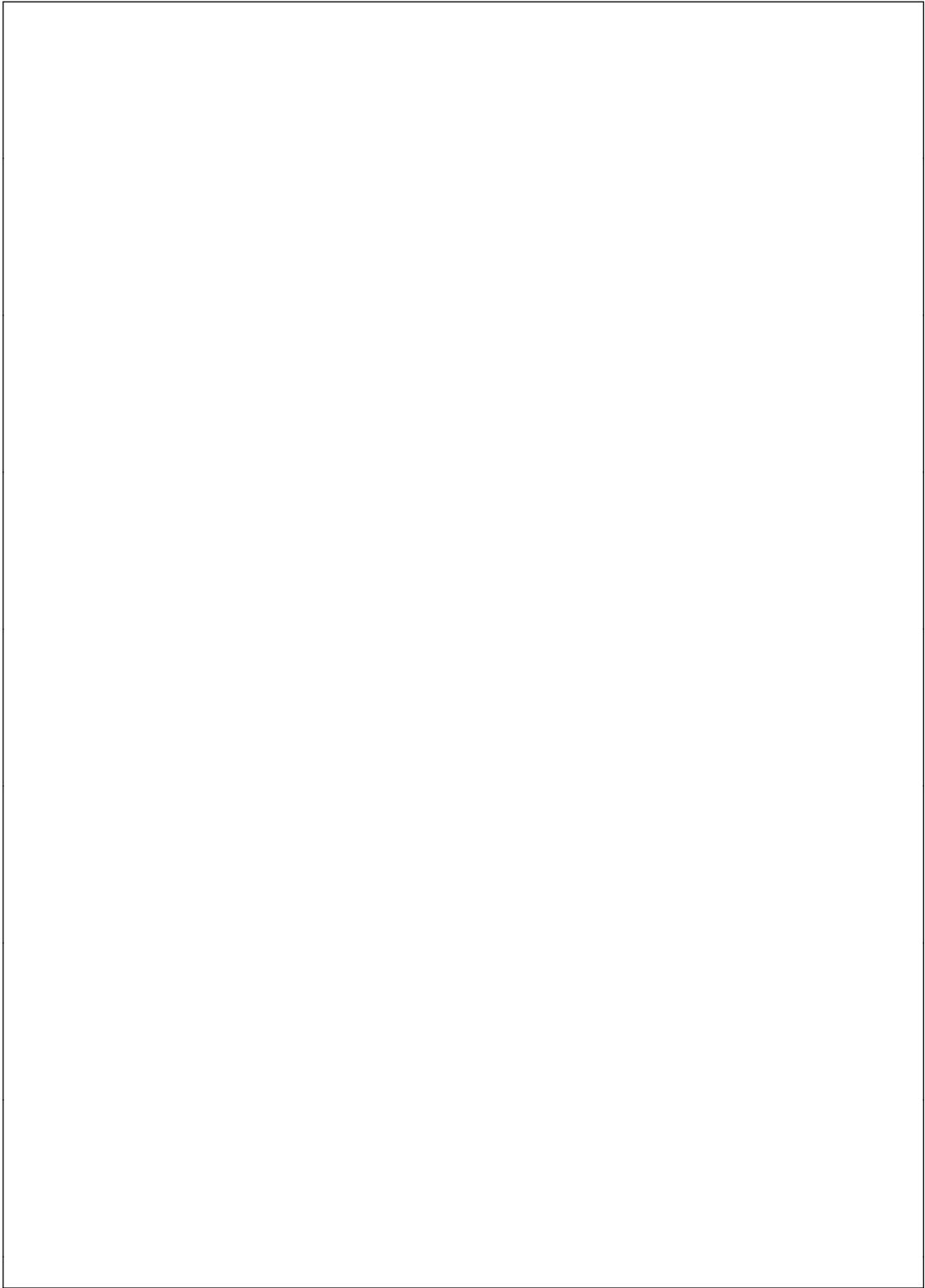
## Switching Characteristics

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

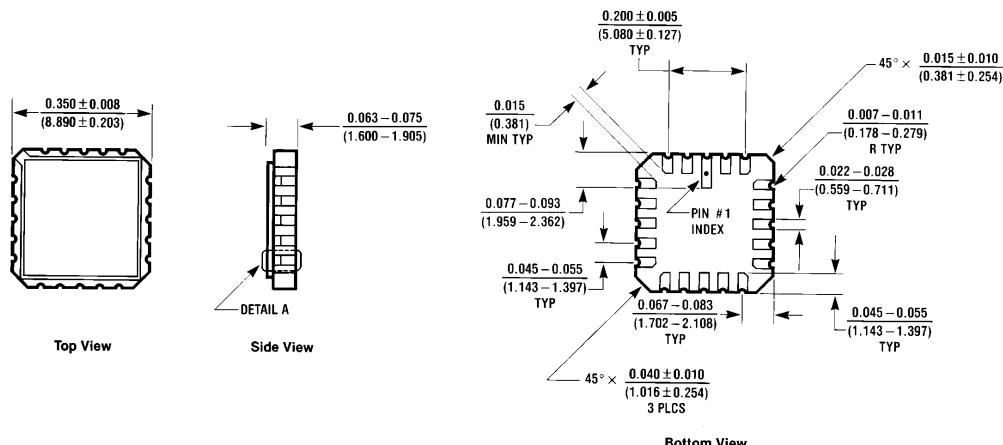
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 10  | 4                      | 15  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 10  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

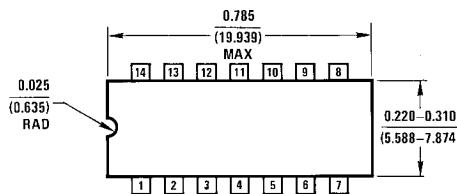


## Physical Dimensions inches (millimeters)



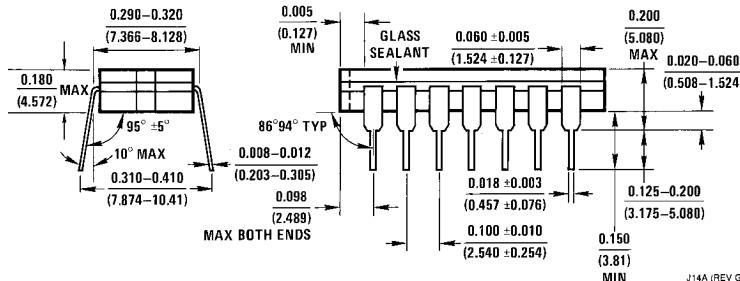
**Ceramic Leadless Chip Carrier Package (E)**  
Order Number 54LS10LMQB  
NS Package Number E20A

E20A (REV D)

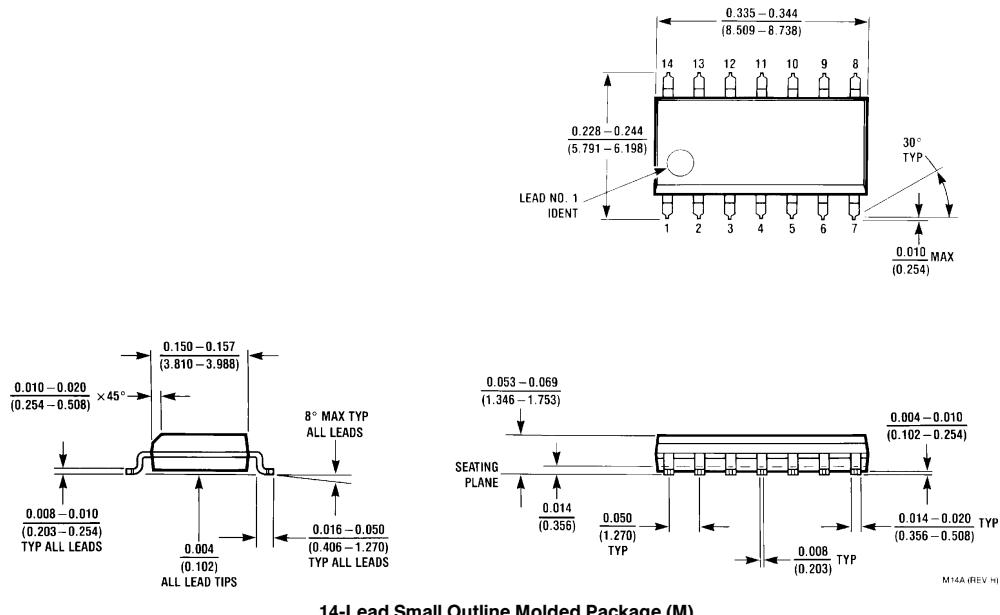


**14-Lead Ceramic Dual-In-Line Package (J)**  
Order Number 54LS10DMQB or DM54LS10J  
NS Package Number J14A

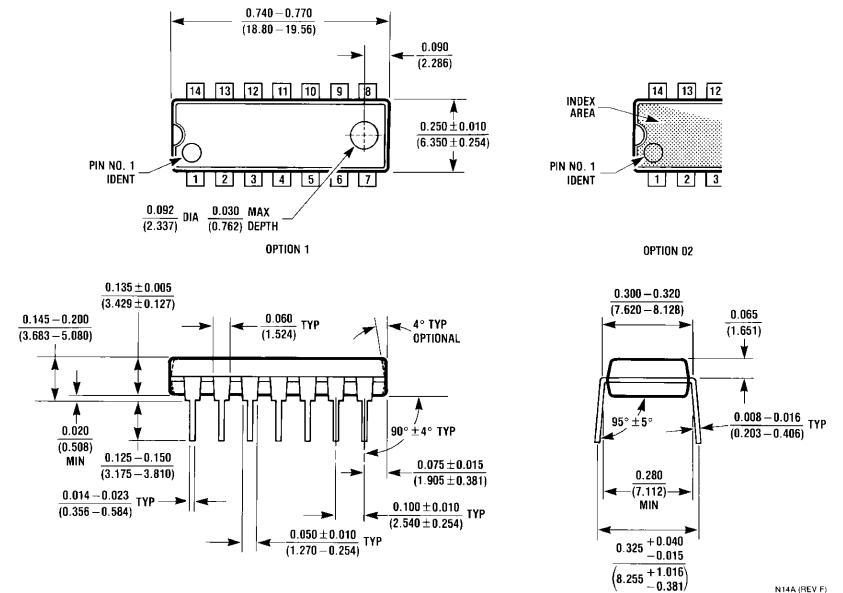
J14A (REV G)



**Physical Dimensions** inches (millimeters) (Continued)

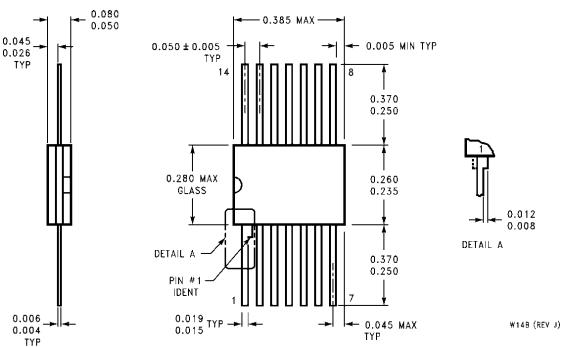


**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS10M  
NS Package Number M14A



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS10N  
NS Package Number N14A

### Physical Dimensions inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
Order Number 54LS10FMQB or DM54LS10W  
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

## General Description

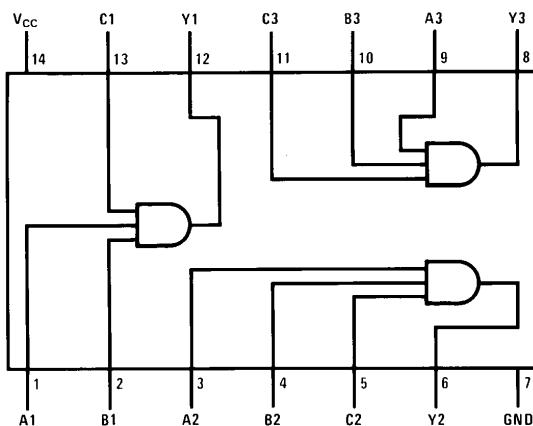
This device contains three independent gates each of which performs the logic AND function.

## Features

- Alternate military/aerospace device (54LS11) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

## Connection Diagram

Dual-In-Line Package



TL/F/6350-1

Order Number 54LS11DMQB, 54LS11FMQB, 54LS11LMQB,  
DM54LS11J, DM54LS11W, DM74LS11M or DM74LS11N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$Y = ABC$$

| Inputs |   |   | Output |
|--------|---|---|--------|
| A      | B | C | Y      |
| X      | X | L | L      |
| X      | L | X | L      |
| L      | X | X | L      |
| H      | H | H | H      |

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | –55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | –65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS11 |     |      | DM74LS11 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | –0.4 |          |     | –0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | –55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions  |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|---|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA                        |      |     |                 | –1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max<br>V <sub>IH</sub> = Min | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |   | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IL</sub> = Max | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |   | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                         | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                            |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                          |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                          |      |     |                 | –0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                     | DM54 | –20 |                 | –100  | mA    |
|                  |                                   |   | DM74 | –20 |                 | –100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max   |      |     | 1.8             | 3.6   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max   |      |     | 3.3             | 6.6   | mA    |

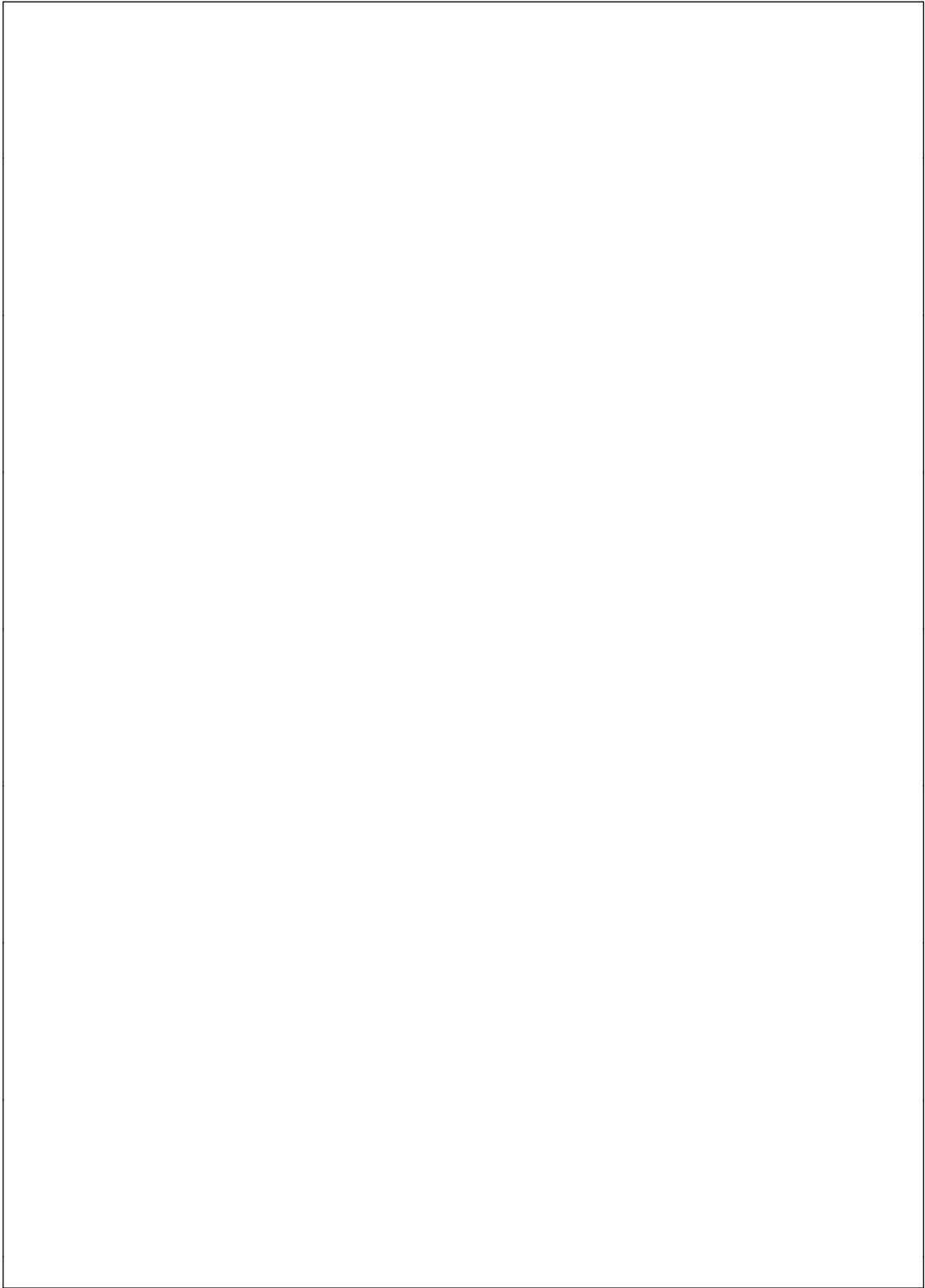
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

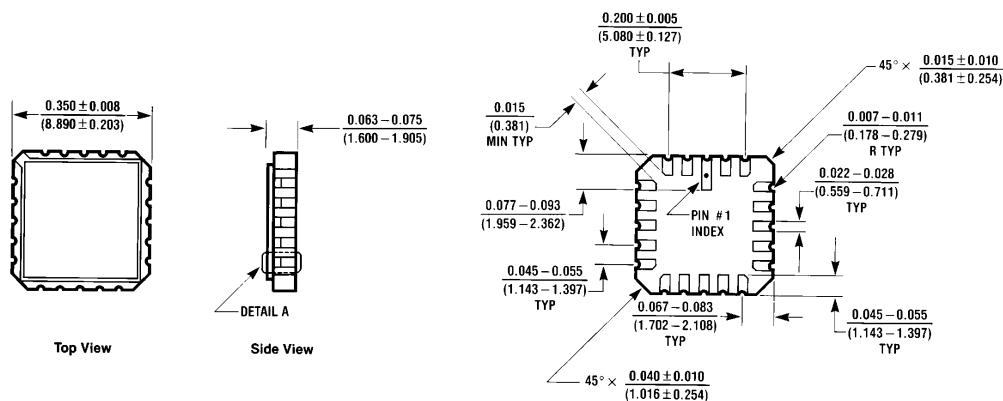
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 4                      | 13  | 6                      | 18  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 11  | 5                      | 18  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

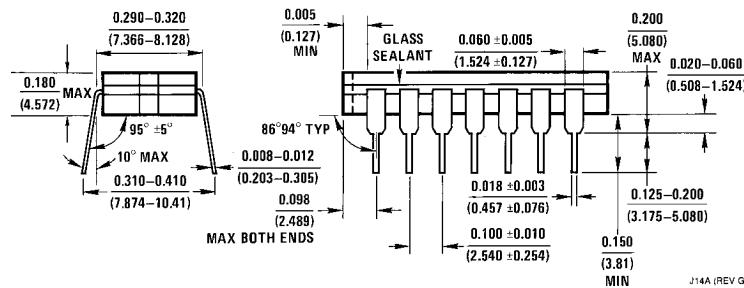
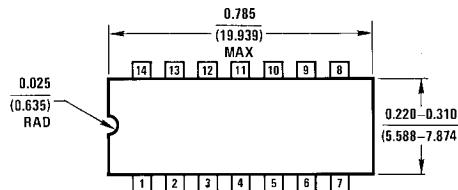


## **Physical Dimensions** inches (millimeters)



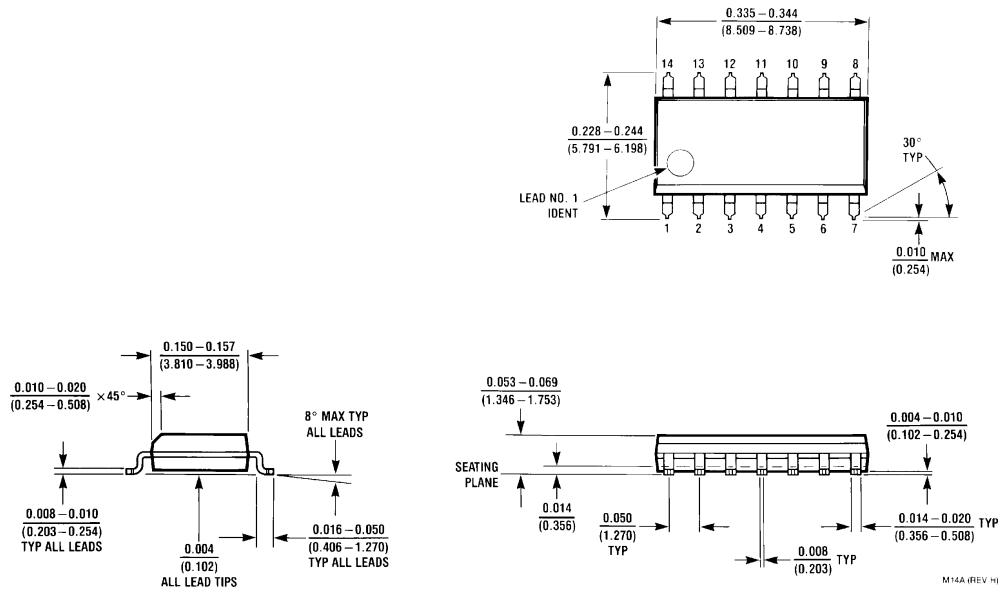
**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS11LMQB  
NS Package Number E20A**

E20A (REV D)

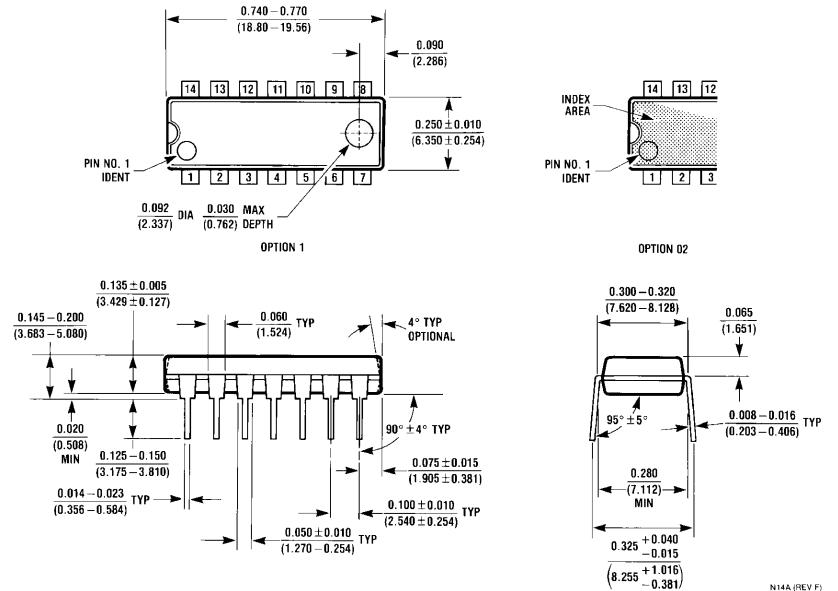


**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS11DMQB or DM54LS11J  
NS Package Number J14A**

## Physical Dimensions inches (millimeters) (Continued)

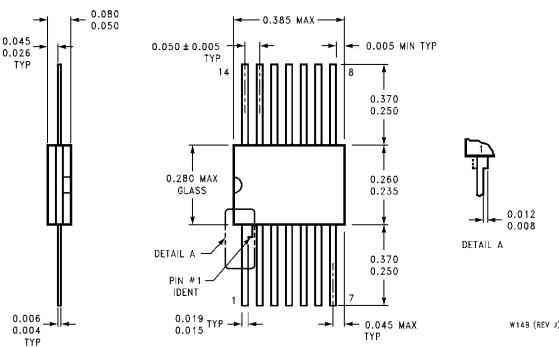


**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS11M  
NS Package Number M14A



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS11N  
NS Package Number N14A

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number 54LS11FMQB or DM54LS11W**  
**NS Package Number W14B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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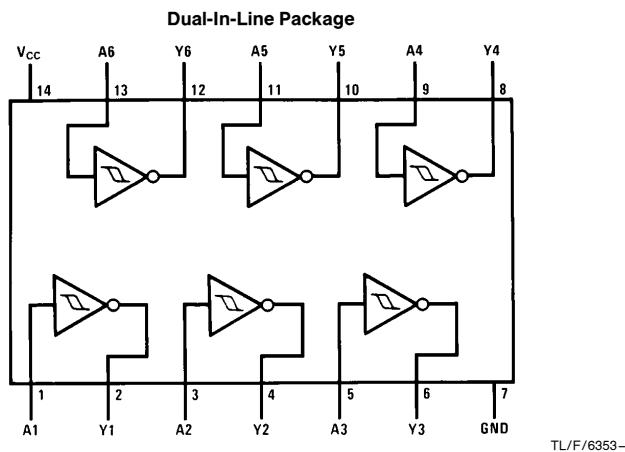
**National Semiconductor  
Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

## 54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

### General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

### Connection Diagram



Order Number 54LS14DMQB, 54LS14FMQB,  
 54LS14LMQB, DM74LS14M or DM74LS14N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### Function Table

$$Y = \bar{A}$$

| Input | Output |
|-------|--------|
| A     | Y      |
| L     | H      |
| H     | L      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| 54LS                                 | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                                       | 54LS14 |     |      | DM74LS14 |     |      | Units |
|-----------------|---|--------|-----|------|----------|-----|------|-------|
|                 |   | Min    | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                                  | 4.5    | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>T+</sub> | Positive-Going Input Threshold Voltage (Note 1) | 1.5    | 1.6 | 2.0  | 1.4      | 1.6 | 1.9  | V     |
| V <sub>T−</sub> | Negative-Going Input Threshold Voltage (Note 1) | 0.6    | 0.8 | 1.1  | 0.5      | 0.8 | 1    | V     |
| HYS             | Input Hysteresis (Note 1)                       | 0.4    | 0.8 |      | 0.4      | 0.8 |      | V     |
| I <sub>OH</sub> | High Level Output Current                       |        |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current                        |        |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature                  | −55    |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                                 | Conditions   |      | Min | Typ (Note 2) | Max  | Units |
|------------------|---|--|------|-----|--------------|------|-------|
| V <sub>I</sub>   | Input Clamp Voltage                       | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |              | −1.5 | V     |
| V <sub>OH</sub>  | High Level Output Voltage                 | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max<br>V <sub>IIL</sub> = Max | 54LS | 2.5 | 3.4          |      | V     |
|                  |   |  | DM74 | 2.7 | 3.4          |      |       |
| V <sub>OL</sub>  | Low Level Output Voltage                  | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IH</sub> = Min  | 54LS |     | 0.25         | 0.4  | V     |
|                  |   |  | DM74 |     | 0.35         | 0.5  |       |
|                  |   | V <sub>CC</sub> = Min, I <sub>OL</sub> = 4 mA                          | DM74 |     | 0.25         | 0.4  |       |
| I <sub>T+</sub>  | Input Current at Positive-Going Threshold | V <sub>CC</sub> = 5V, V <sub>I</sub> = V <sub>T+</sub>                 | DM74 |     | −0.14        |      | mA    |
| I <sub>T−</sub>  | Input Current at Negative-Going Threshold | V <sub>CC</sub> = 5V, V <sub>I</sub> = V <sub>T−</sub>                 | DM74 |     | −0.18        |      | mA    |
| I <sub>I</sub>   | Input Current @ Max Input Voltage         | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             | DM74 |     |              | 0.1  | mA    |
|                  |   | V <sub>CC</sub> = Max, V <sub>I</sub> = 10.0V                          | 54LS |     |              |      |       |
| I <sub>IH</sub>  | High Level Input Current                  | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |              | 20   | μA    |
| I <sub>IL</sub>  | Low Level Input Current                   | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |              | −0.4 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current              | V <sub>CC</sub> = Max (Note 3)   | 54LS | −20 |              | −100 | mA    |
|                  |   |  | DM74 | −20 |              | −100 |       |
| I <sub>CCH</sub> | Supply Current with Outputs High          | V <sub>CC</sub> = Max  |      |     | 8.6          | 16   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low           | V <sub>CC</sub> = Max  |      |     | 12           | 21   | mA    |

Note 1: V<sub>CC</sub> = 5V.

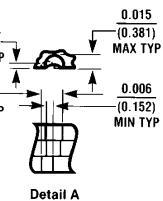
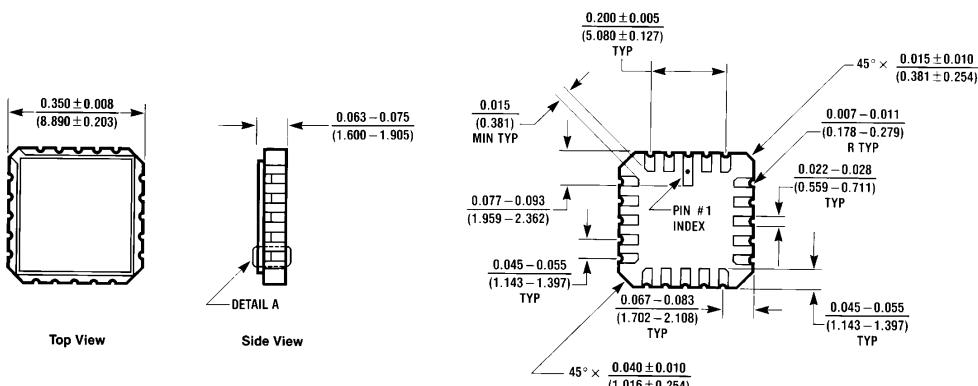
Note 2: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Switching Characteristics** at  $V_{CC} = 5V$  and  $T_A = 25^{\circ}C$  (See Section 1 for Test Waveforms and Output Load)

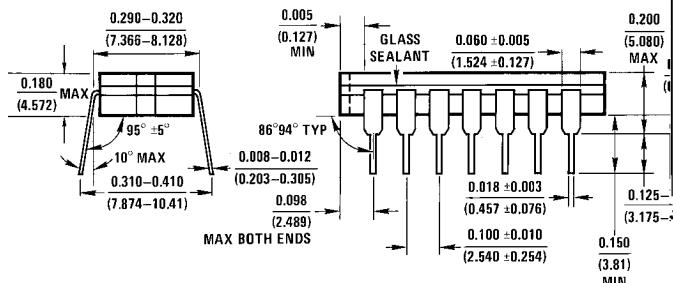
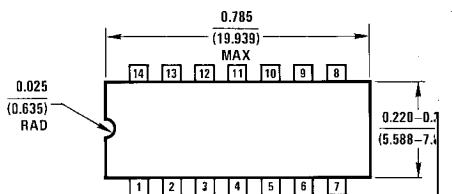
| Symbol    | Parameter  | $R_L = 2\text{ k}\Omega$ |     |                      |     | Units |  |
|-----------|--|--------------------------|-----|----------------------|-----|-------|--|
|           |  | $C_L = 15\text{ pF}$     |     | $C_L = 50\text{ pF}$ |     |       |  |
|           |  | Min                      | Max | Min                  | Max |       |  |
| $t_{PLH}$ | Propagation Delay Time<br>Low to High Level Output | 5                        | 22  | 8                    | 25  | ns    |  |
| $t_{PHL}$ | Propagation Delay Time<br>High to Low Level Output | 5                        | 22  | 10                   | 33  | ns    |  |

## Physical Dimensions inches (millimeters)



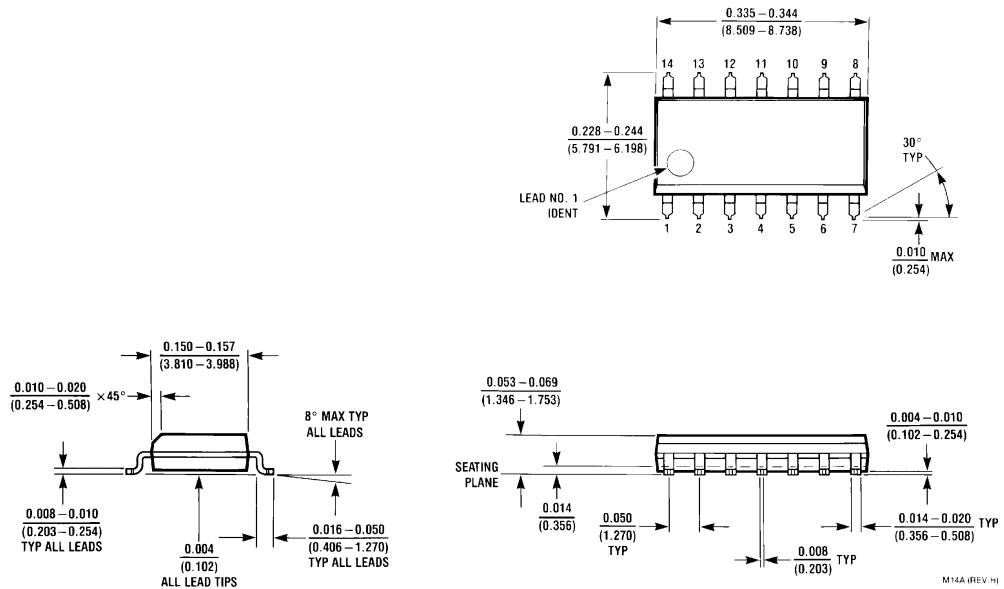
Ceramic Leadless Chip Carrier (E)  
Order Number 54LS14LMQB  
NS Package Number E20A

E20A (REV D)



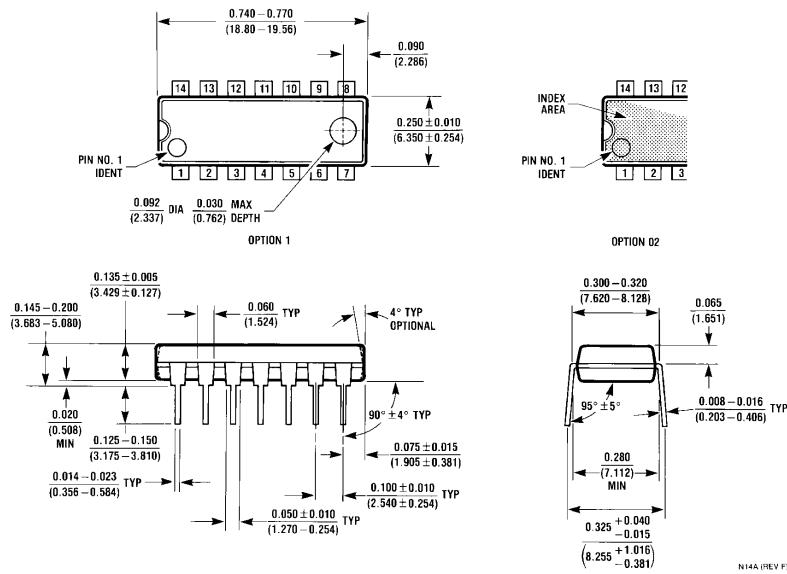
14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS14DMQB  
NS Package Number J14A

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS14M  
NS Package Number M14A

M14A (REV H)

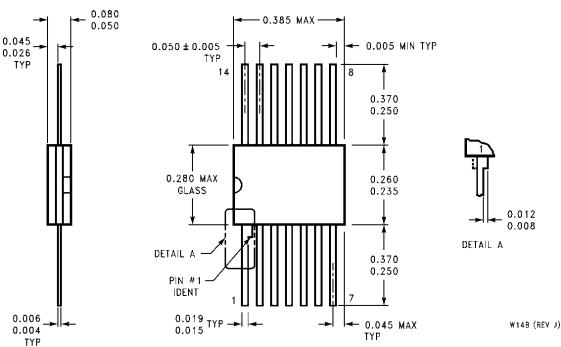


**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS14N  
NS Package Number N14A

N14A (REV F)

# 54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

## Physical Dimensions inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)  
Order Number 54LS14FMQB  
NS Package Number W14B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

|  |   |  |  |
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|--|---|--|--|

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## **54LS20/DM54LS20/DM74LS20 Dual 4-Input NAND Gates**

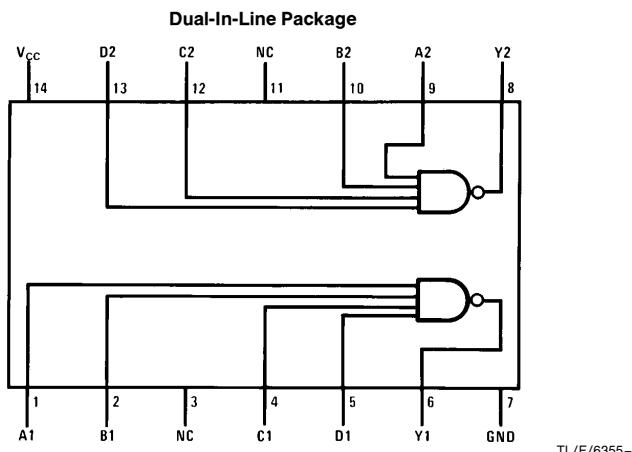
### **General Description**

This device contains two independent gates each of which performs the logic NAND function.

### **Features**

- Alternate Military/Aerospace device (54LS20) is available. Contact a National Semiconductor Sales Office/Distributor for specifications

### **Connection Diagram**



TL/F/6355-1

Order Number 54LS20DMQB, 54LS20FMQB, 54LS20LMQB,  
 DM54LS20J, DM54LS20W, DM74LS20M or DM74LS20N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### **Function Table**

$$Y = \overline{ABCD}$$

| Inputs |   |   |   | Output |
|--------|---|---|---|--------|
| A      | B | C | D | Y      |
| X      | X | X | L | H      |
| X      | X | L | X | H      |
| X      | L | X | X | H      |
| L      | X | X | X | H      |
| H      | H | H | H | L      |

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS20 |     |      | DM74LS20 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                  |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 0.4             | 0.8   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 1.2             | 2.2   | mA    |

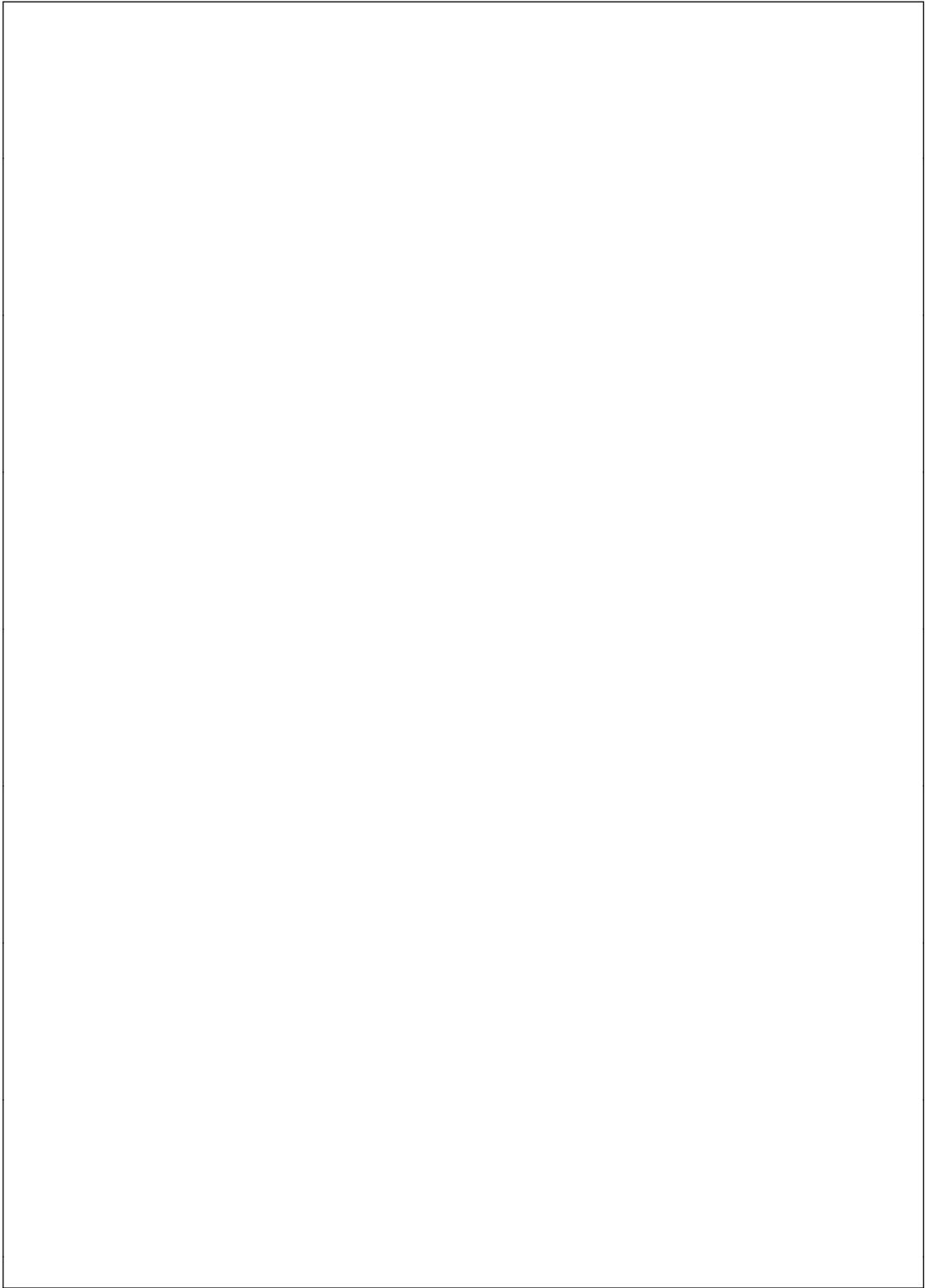
## Switching Characteristics

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

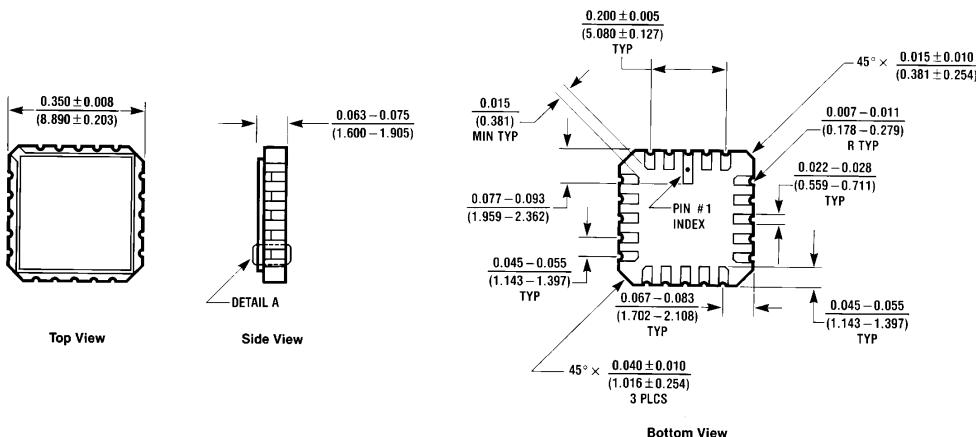
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 10  | 4                      | 15  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 10  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

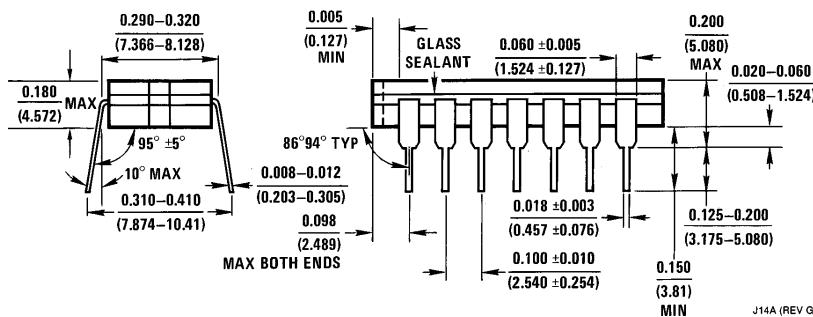
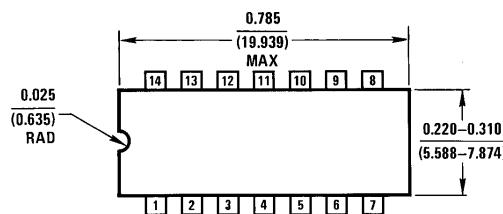


## Physical Dimensions inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)**  
Order Number 54LS20LMQB  
NS Package Number E20A

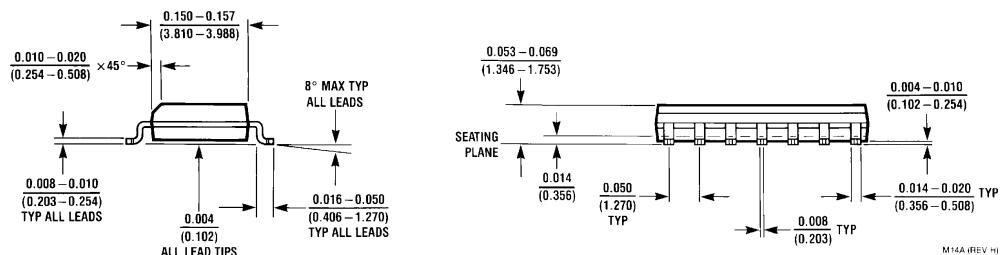
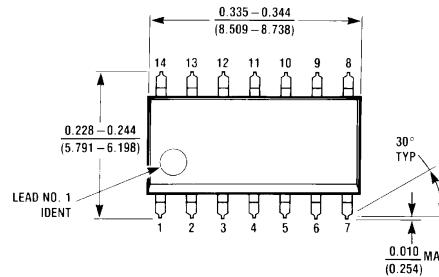
E20A (REV D)



**14-Lead Ceramic Dual-In-Line Package (J)**  
Order Number 54LS20DMQB or DM54LS20J  
NS Package Number J14A

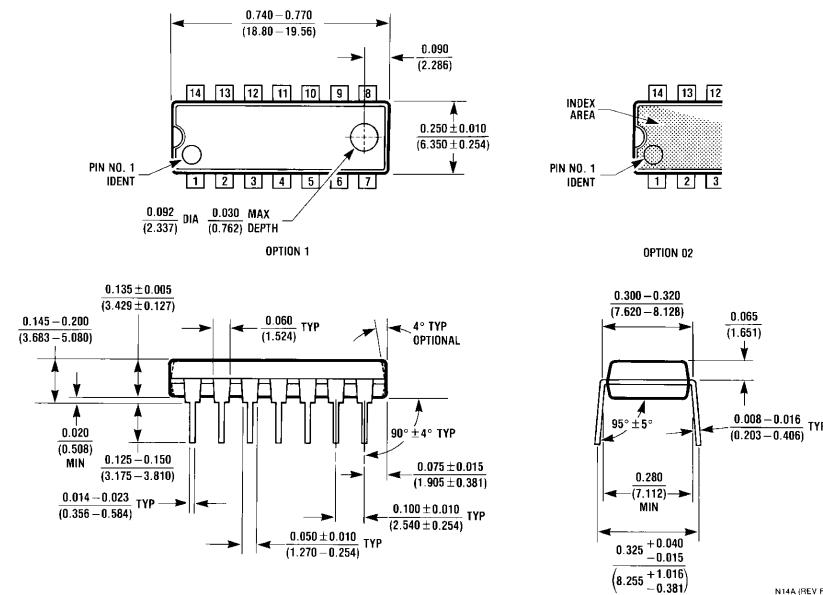
J14A (REV G)

**Physical Dimensions** inches (millimeters) (Continued)



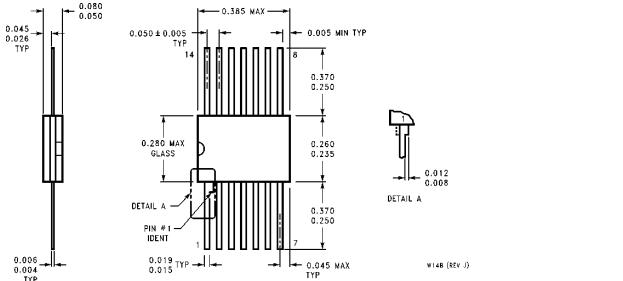
**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS20M  
NS Package Number M14A

M14A (REV H)



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS20N  
NS Package Number N14A

N14A (REV F)

**Physical Dimensions** inches (millimeters) (Continued)

**14-Lead Ceramic Flat Package (W)**  
Order Number 54LS20FMB or DM54LS20W  
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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|---|---|--|--|

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## 54LS21/DM54LS21/DM74LS21 Dual 4-Input AND Gates

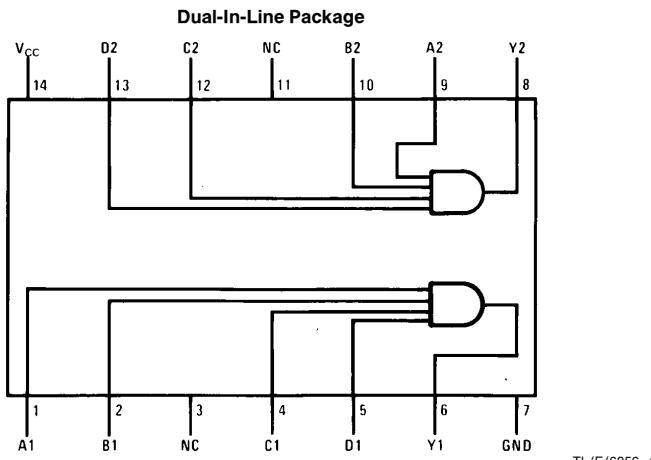
### General Description

This device contains two independent gates each of which performs the logic AND function.

### Features

- Alternate Military/Aerospace device (54LS21) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### Connection Diagram



TL/F/6356-1

Order Number 54LS21DMQB, 54LS21FMQB, 54LS21LMQB,  
 DM54LS21J, DM54LS21W, DM74LS21M or DM74LS21N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### Function Table

**Y = ABCD**

| Inputs |   |   |   | Output |
|--------|---|---|---|--------|
| A      | B | C | D | Y      |
| X      | X | X | L | L      |
| X      | X | L | X | L      |
| X      | L | X | X | L      |
| L      | X | X | X | L      |
| H      | H | H | H | H      |

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | −55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS21 |     |      | DM74LS21 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |                 | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 | 2.5 | 3.4             |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4             |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 |     | 0.25            | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35            | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25            | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |                 | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                      | DM54 | −20 |                 | −100  | mA    |
|                  |                                   |  | DM74 | −20 |                 | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 1.2             | 2.4   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 2.2             | 4.4   | mA    |

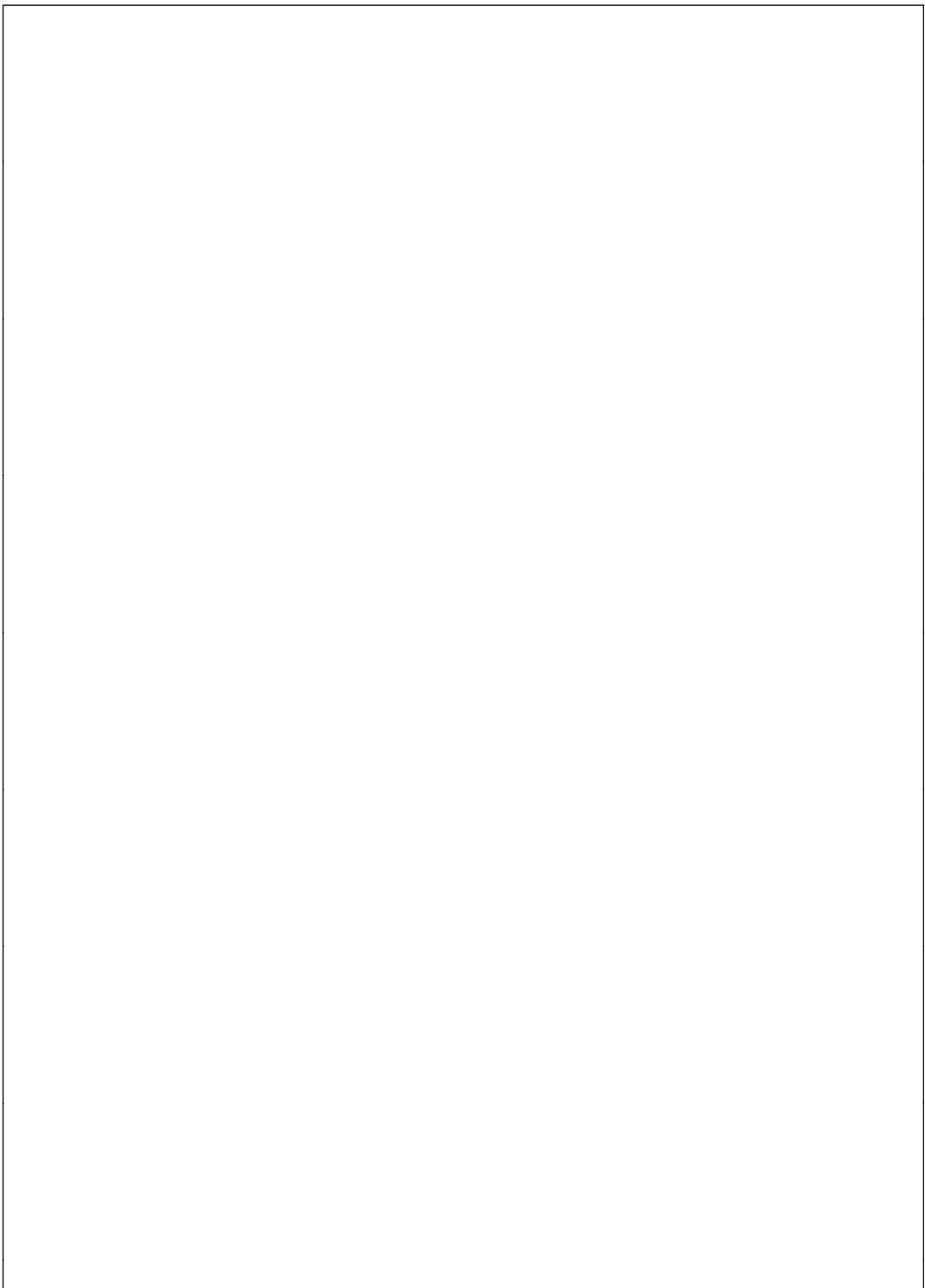
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

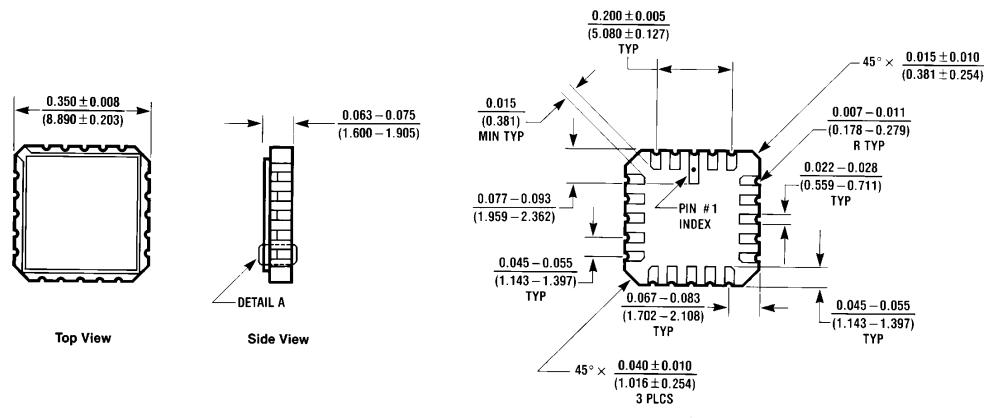
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 4                      | 13  | 6                      | 18  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 11  | 5                      | 18  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

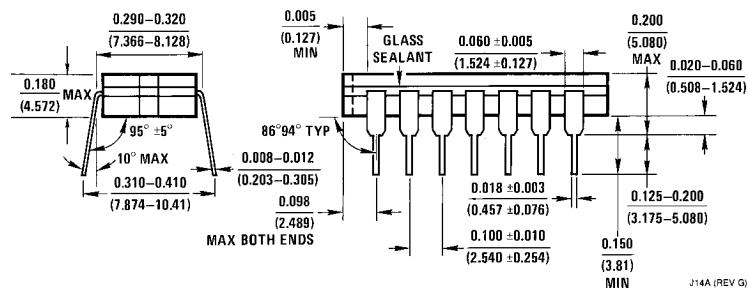
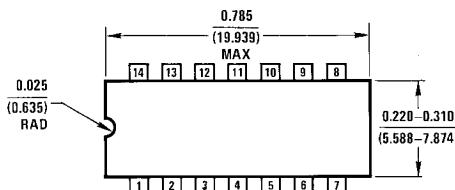


## **Physical Dimensions** inches (millimeters)



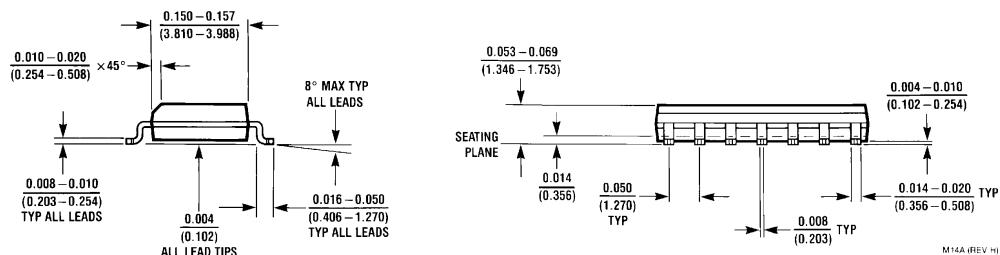
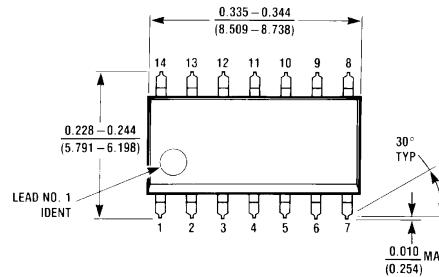
**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS20LMQB  
NS Package Number E20A**

E20A (REV D)



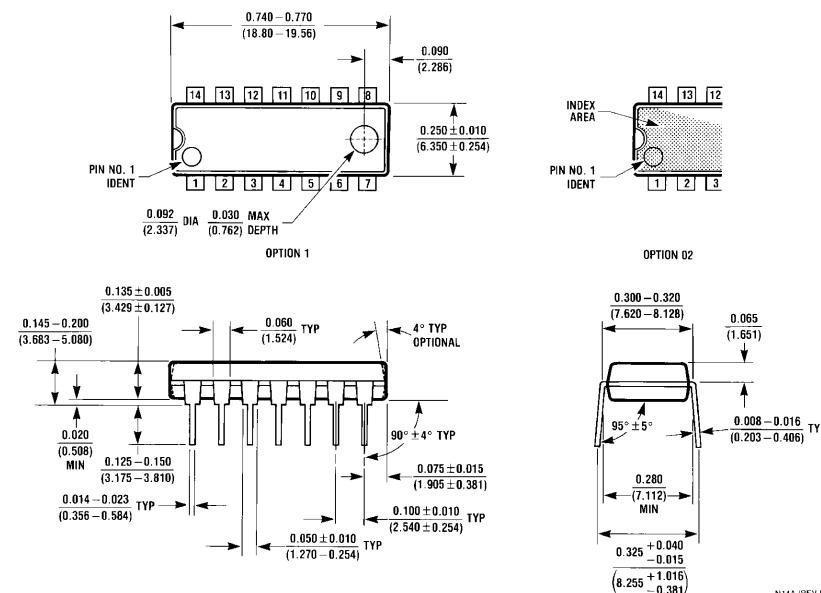
**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS20DMQB or DM54LS21J  
NS Package Number J14A**

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS21M  
NS Package Number M14A

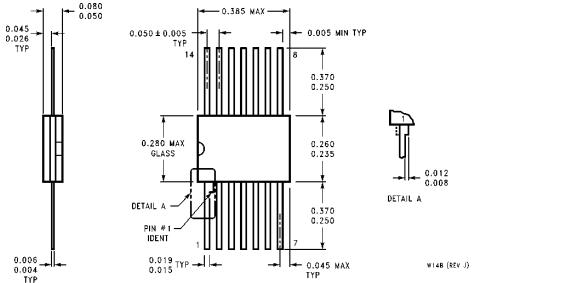
M14A (REV H)



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS21N  
NS Package Number N14A

N14A (REV F)

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number 54LS21FMB or DM54LS21W**  
**NS Package Number W14B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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Fax: (852) 2736-9960

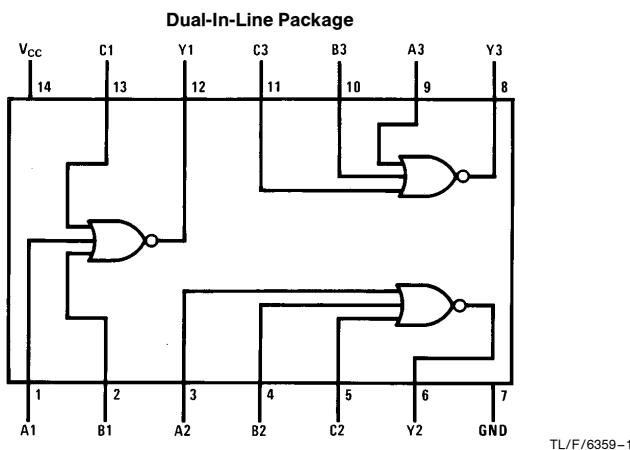
**National Semiconductor  
Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

## **DM54LS27/DM74LS27 Triple 3-Input NOR Gates**

### **General Description**

This device contains three independent gates each of which performs the logic NOR function.

### **Connection Diagram**



**Order Number DM54LS27J, DM54LS27W,  
DM54LS27E, DM74LS27M or DM74LS27N  
See NS Package Number E20A, J14A, M14A, N14A or W14B**

### **Function Table**

$$Y = \overline{A + B + C}$$

| Inputs |   |   | Output |
|--------|---|---|--------|
| A      | B | C | Y      |
| L      | L | L | H      |
| X      | X | H | L      |
| X      | H | X | L      |
| H      | X | X | L      |

H = High Logic Level  
L = Low Logic Level  
X = Either Low or High Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|   |                 |
|---|-----------------|
| Supply Voltage  | 7V              |
| Input Voltage   | 7V              |
| Operating Free Air Temperature Range<br>DM54LS and 54LS | −55°C to +125°C |
| DM74LS  | 0°C to +70°C    |

Storage Temperature Range −65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS27 |     |      | DM74LS27 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | −0.4 |          |     | −0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | −55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions   |      | Min | Typ (Note 1) | Max   | Units |
|------------------|-----------------------------------|--|------|-----|--------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA                         |      |     |              | −1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max,<br>V <sub>IL</sub> = Max | DM54 | 2.5 |              |       | V     |
|                  |                                   |  | DM74 | 2.7 | 3.4          |       |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max,<br>V <sub>IH</sub> = Min | DM54 |     |              | 0.4   | V     |
|                  |                                   |  | DM74 |     | 0.35         | 0.5   |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                          | DM74 |     | 0.25         | 0.4   |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                             |      |     |              | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                           |      |     |              | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                           |      |     |              | −0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max (Note 2)   | DM54 | −20 |              | −100  | mA    |
|                  |                                   |  | DM74 | −20 |              | −100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max  |      |     | 2            | 4     | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max  |      |     | 3.4          | 6.8   | mA    |

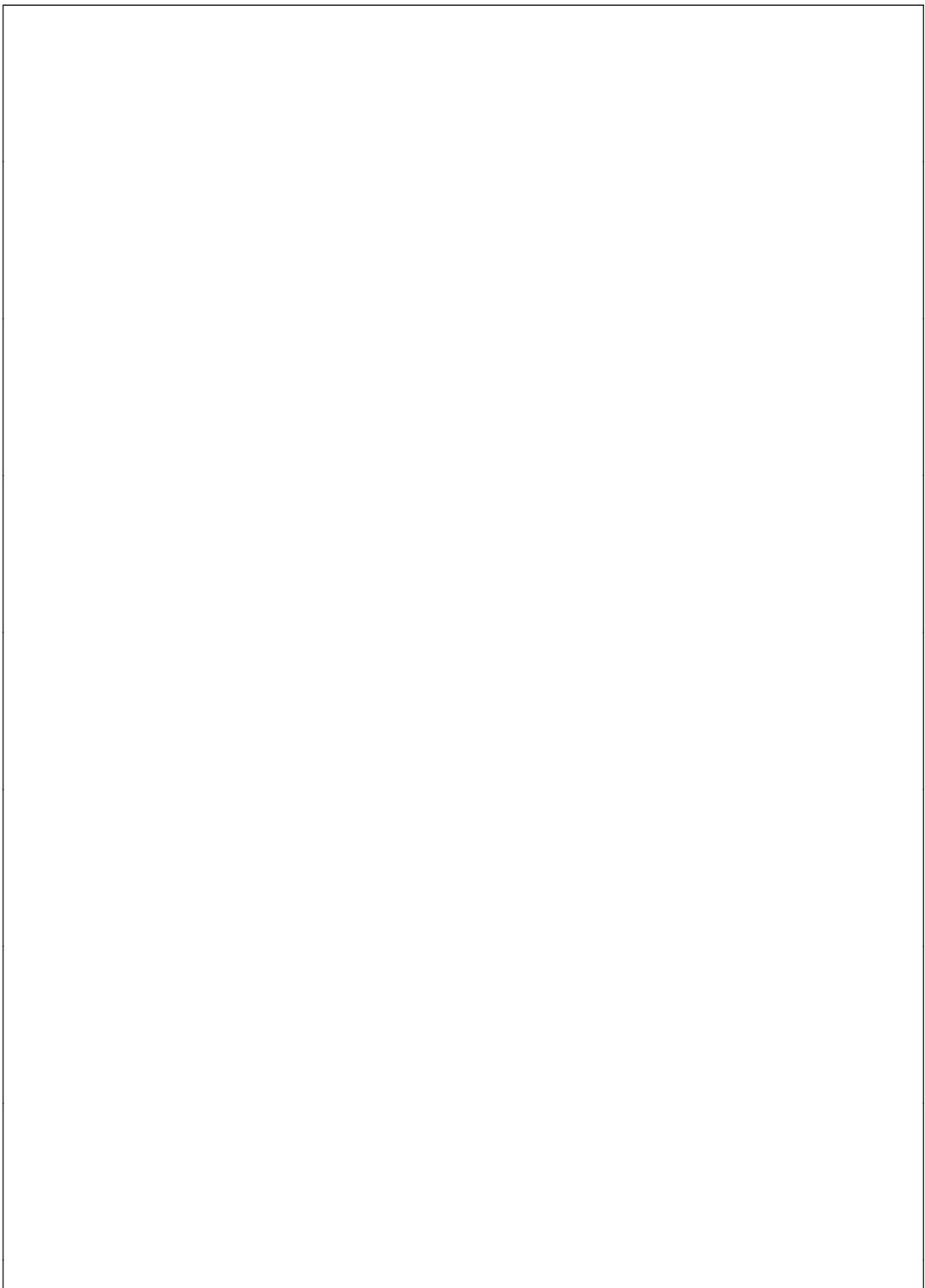
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

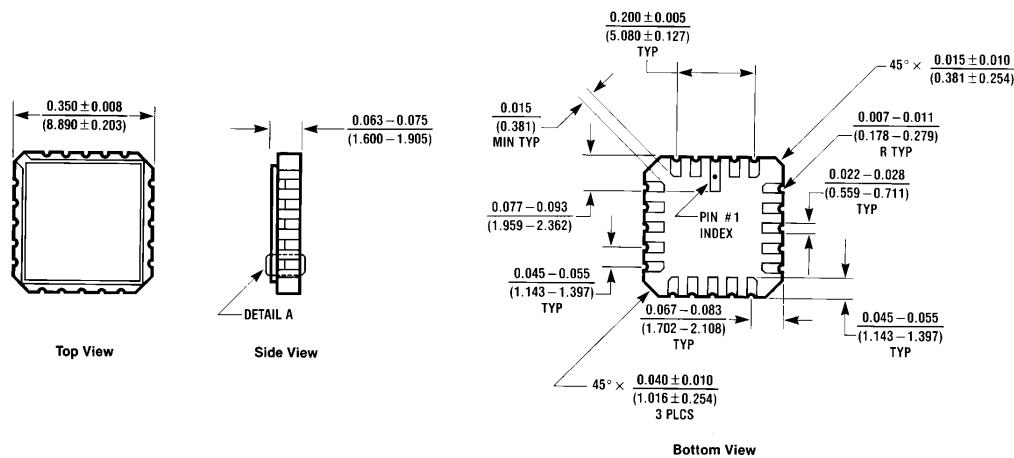
| Symbol           | Parameter                                       | DM54                   |     | DM74                   |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|------------------------|-----|-------|--|
|                  |   | R <sub>L</sub> = 2 kΩ  |     |                        |     |                        |     |       |  |
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 13  | 3                      | 13  | 5                      | 18  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 13  | 3                      | 10  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

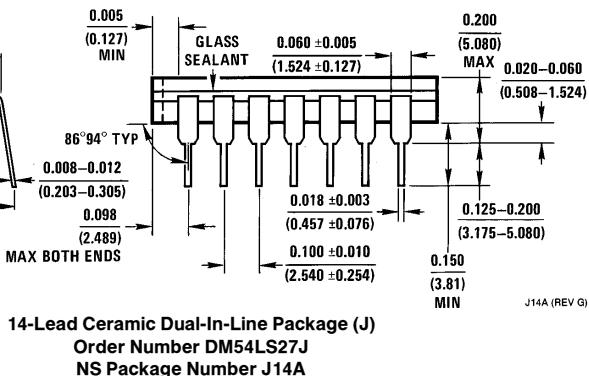
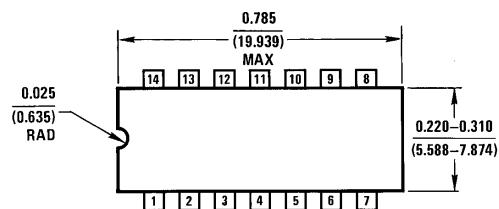


## Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)  
Order Number DM54LS27E  
NS Package Number E20A

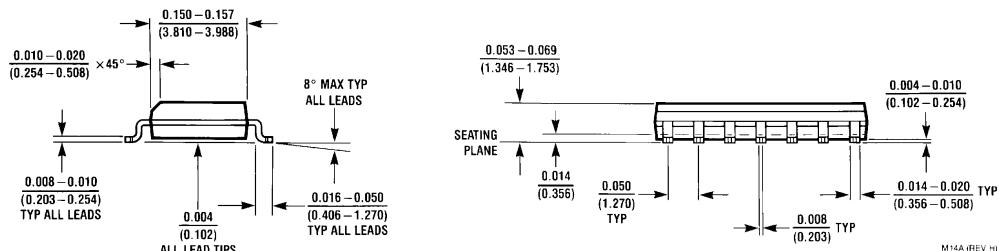
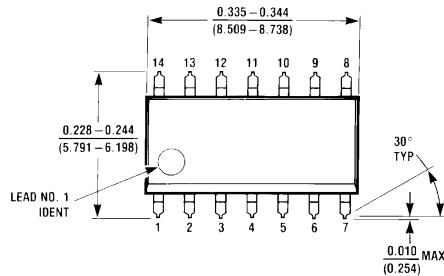
E20A (REV D)



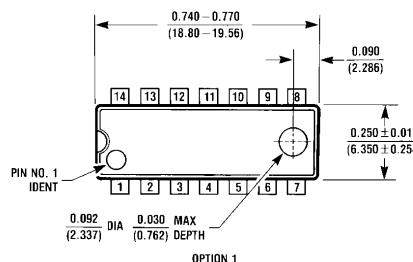
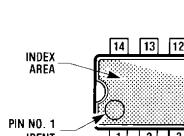
14-Lead Ceramic Dual-In-Line Package (J)  
Order Number DM54LS27J  
NS Package Number J14A

J14A (REV G)

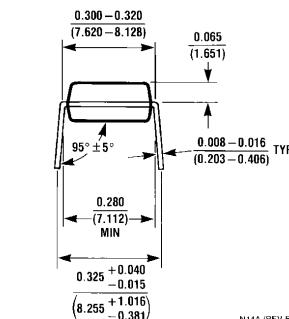
## Physical Dimensions inches (millimeters) (Continued)



**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS27M  
NS Package Number M14A



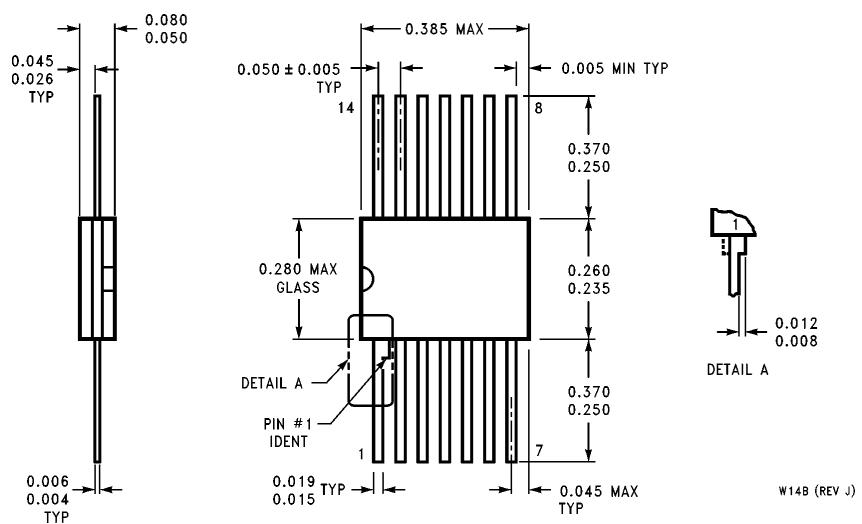
OPTION 1



N14A (REV F)

**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS27N  
NS Package Number N14A

## **Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)  
Order Number DM54LS27W  
NS Package Number W14B**

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  2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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|---|---|--|--|

## **54LS32/DM54LS32/DM74LS32** **Quad 2-Input OR Gates**

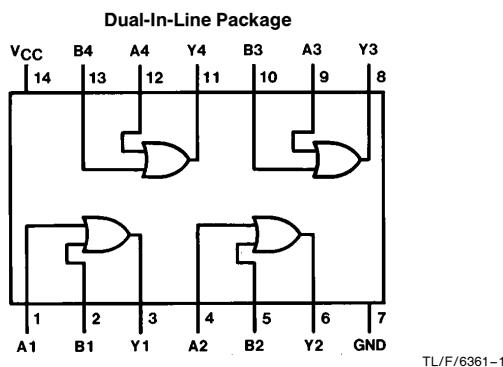
### **General Description**

This device contains four independent gates each of which performs the logic OR function.

### **Features**

- Alternate Military/Aerospace device (54LS32) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### **Connection Diagram**



TL/F/6361-1

Order Number 54LS32DMQB, 54LS32FMQB, 54LS32LMQB,  
 DM54LS32J, DM54LS32W, DM74LS32M or DM74LS32N  
 See NS Package Number E20A, J14A, M14A, N14A or W14B

### **Function Table**

$$Y = A + B$$

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | H      |
| H      | L | H      |
| H      | H | H      |

H = High Logic Level

L = Low Logic Level

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 7V              |
| Operating Free Air Temperature Range |                 |
| DM54LS and 54LS                      | -55°C to +125°C |
| DM74LS                               | 0°C to +70°C    |
| Storage Temperature Range            | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol          | Parameter                      | DM54LS32 |     |      | DM74LS32 |     |      | Units |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|-------|
|                 |                                | Min      | Nom | Max  | Min      | Nom | Max  |       |
| V <sub>CC</sub> | Supply Voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V     |
| V <sub>IH</sub> | High Level Input Voltage       | 2        |     |      | 2        |     |      | V     |
| V <sub>IL</sub> | Low Level Input Voltage        |          |     | 0.7  |          |     | 0.8  | V     |
| I <sub>OH</sub> | High Level Output Current      |          |     | -0.4 |          |     | -0.4 | mA    |
| I <sub>OL</sub> | Low Level Output Current       |          |     | 4    |          |     | 8    | mA    |
| T <sub>A</sub>  | Free Air Operating Temperature | -55      |     | 125  | 0        |     | 70   | °C    |

## Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

| Symbol           | Parameter                         | Conditions  |  | Min  | Typ<br>(Note 1) | Max   | Units |
|------------------|-----------------------------------|---|--|------|-----------------|-------|-------|
| V <sub>I</sub>   | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA                        |  |      |                 | -1.5  | V     |
| V <sub>OH</sub>  | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max<br>V <sub>IH</sub> = Min |  | DM54 | 2.5             | 3.4   | V     |
|                  |                                   | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IL</sub> = Max |  | DM74 | 2.7             | 3.4   |       |
| V <sub>OL</sub>  | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max<br>V <sub>IL</sub> = Max |  | DM54 |                 | 0.25  | V     |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                         |  | DM74 |                 | 0.35  |       |
|                  |                                   | I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min                         |  | DM74 |                 | 0.25  |       |
| I <sub>I</sub>   | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 7V                            |  |      |                 | 0.1   | mA    |
| I <sub>IH</sub>  | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V                          |  |      |                 | 20    | μA    |
| I <sub>IL</sub>  | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V                          |  |      |                 | -0.36 | mA    |
| I <sub>OS</sub>  | Short Circuit Output Current      | V <sub>CC</sub> = Max<br>(Note 2)                                     |  | DM54 | -20             | -100  | mA    |
|                  |                                   | V <sub>CC</sub> = Max<br>(Note 2)                                     |  | DM74 | -20             | -100  |       |
| I <sub>CCH</sub> | Supply Current with Outputs High  | V <sub>CC</sub> = Max   |  |      | 3.1             | 6.2   | mA    |
| I <sub>CCL</sub> | Supply Current with Outputs Low   | V <sub>CC</sub> = Max   |  |      | 4.9             | 9.8   | mA    |

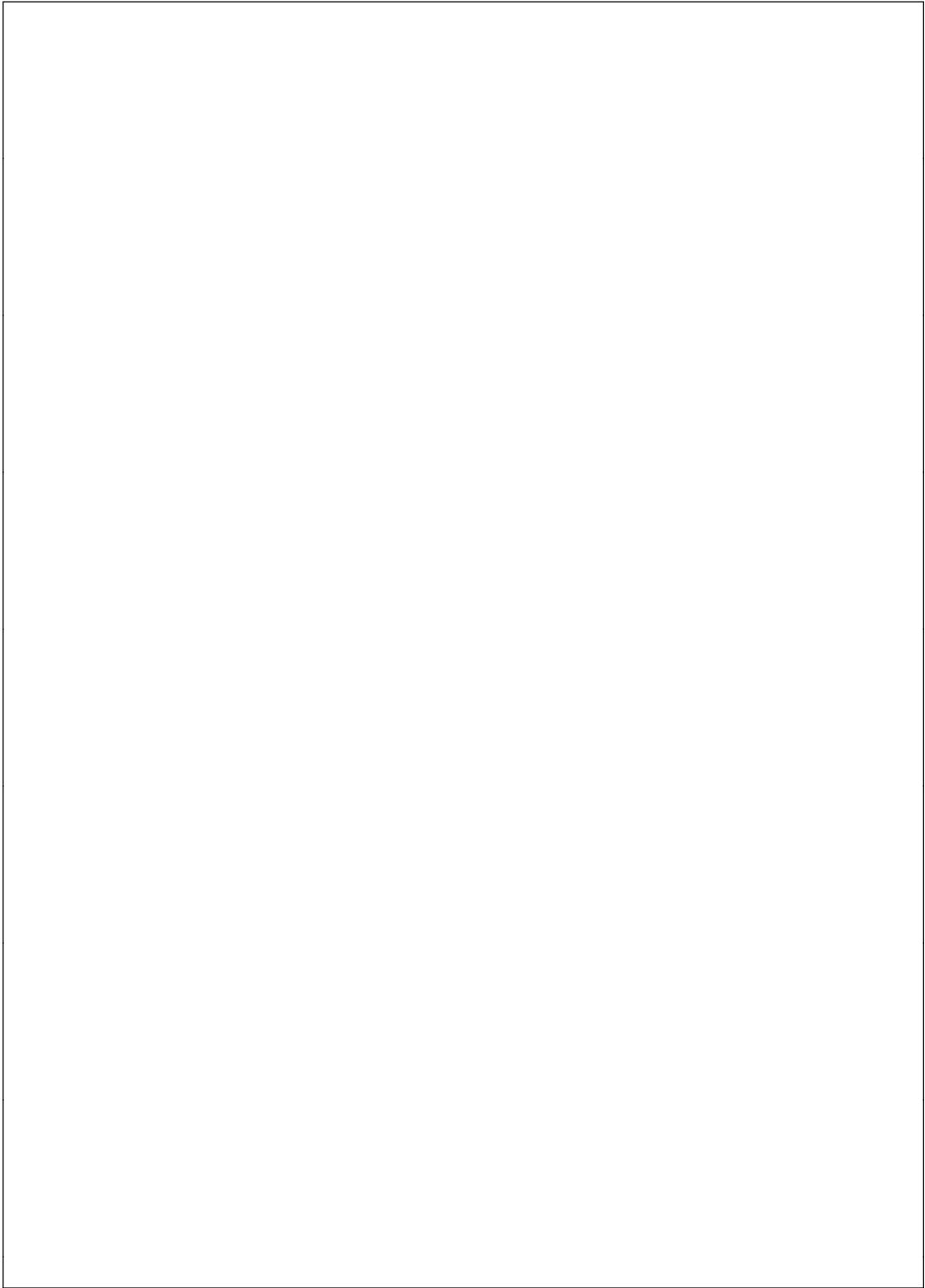
## Switching Characteristics

 at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C (See Section 1 for Test Waveforms and Output Load)

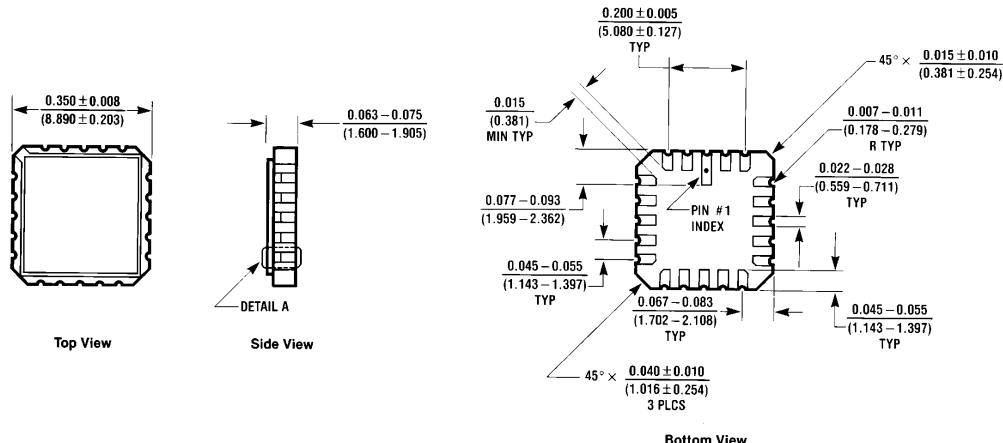
| Symbol           | Parameter                                       | R <sub>L</sub> = 2 kΩ  |     |                        |     | Units |  |
|------------------|---|------------------------|-----|------------------------|-----|-------|--|
|                  |   | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     |       |  |
|                  |   | Min                    | Max | Min                    | Max |       |  |
| t <sub>PLH</sub> | Propagation Delay Time Low to High Level Output | 3                      | 11  | 4                      | 15  | ns    |  |
| t <sub>PHL</sub> | Propagation Delay Time High to Low Level Output | 3                      | 11  | 4                      | 15  | ns    |  |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

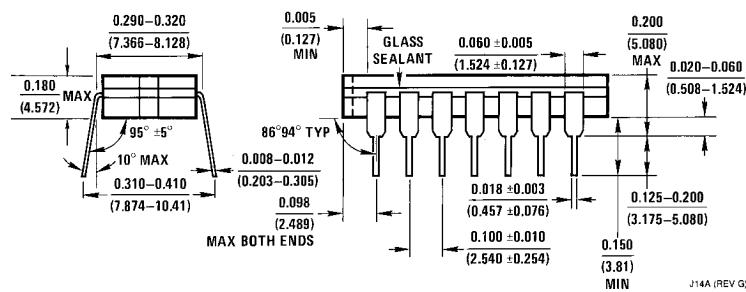
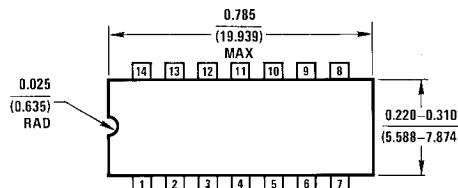


## **Physical Dimensions** inches (millimeters)



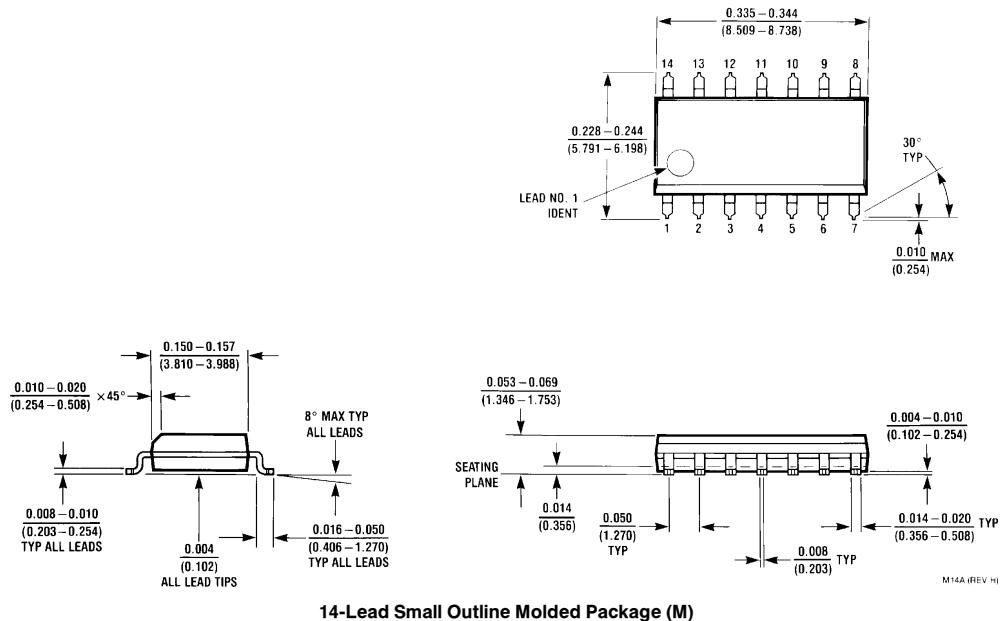
**Ceramic Leadless Chip Carrier Package (E)  
Order Number 54LS32LMQB  
NS Package Number E20A**

E20A (REV D)

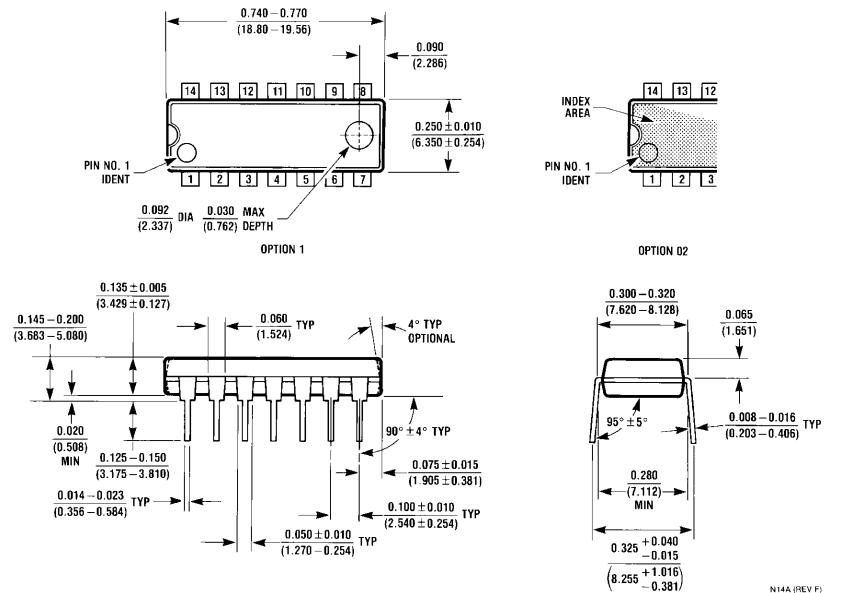


**14-Lead Ceramic Dual-In-Line Package (J)  
Order Number 54LS32DMQB or DM54LS32J  
NS Package Number J14A**

**Physical Dimensions** inches (millimeters)

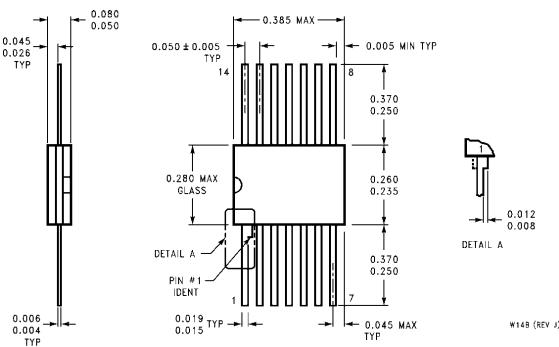


**14-Lead Small Outline Molded Package (M)**  
Order Number DM74LS32M  
NS Package Number M14A



**14-Lead Molded Dual-In-Line Package (N)**  
Order Number DM74LS32N  
NS Package Number N14A

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
Order Number 54LS32FMQB or DM54LS32W  
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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# Double Data Rate (DDR) SDRAM

**MT46V128M4 – 32 Meg x 4 x 4 banks**

**MT46V64M8 – 16 Meg x 8 x 4 banks**

**MT46V32M16 – 8 Meg x 16 x 4 banks**

## Features

- $V_{DD} = 2.5V \pm 0.2V$ ,  $V_{DDQ} = 2.5V \pm 0.2V$   
 $V_{DD} = 2.6V \pm 0.1V$ ,  $V_{DDQ} = 2.6V \pm 0.1V$  (DDR400)<sup>1</sup>
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto refresh
  - 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL\_2 compatible)
- Concurrent auto precharge option is supported
- <sup>t</sup>RAS lockout supported (<sup>t</sup>RAP = <sup>t</sup>RCD)

## Options

|                       |  | Marking          |
|-----------------------|--|------------------|
| • Configuration       | – 128 Meg x 4 (32 Meg x 4 x 4 banks)     | 128M4            |
|                       | – 64 Meg x 8 (16 Meg x 8 x 4 banks)      | 64M8             |
|                       | – 32 Meg x 16 (8 Meg x 16 x 4 banks)     | 32M16            |
| • Plastic package     | – 66-pin TSOP                            | TG               |
|                       | – 66-pin TSOP (Pb-free)                  | P                |
|                       | – 60-ball FBGA (10mm x 12.5mm)           | FN <sup>2</sup>  |
|                       | – 60-ball FBGA (10mm x 12.5mm) (Pb-free) | BN <sup>2</sup>  |
|                       | – 60-ball FBGA (8mm x 12.5mm)            | CV <sup>3</sup>  |
|                       | – 60-ball FBGA (8mm x 12.5mm) (Pb-free)  | CY <sup>3</sup>  |
| • Timing – cycle time | – 5ns @ CL = 3 (DDR400)                  | -5B              |
|                       | – 6ns @ CL = 2.5 (DDR333) (FBGA only)    | -6 <sup>2</sup>  |
|                       | – 6ns @ CL = 2.5 (DDR333) (TSOP only)    | -6T <sup>2</sup> |
| • Self refresh        | – Standard                               | None             |
|                       | – Low-power self refresh                 | L                |
| • Temperature rating  | – Commercial (0°C to +70°C)              | None             |
|                       | – Industrial (-40°C to +85°C)            | IT               |
| • Revision            | – x4, x8, x16                            | :F               |
|                       | – x4, x8, x16                            | :J               |

Notes: 1. DDR400 devices operating at  $\leq$  DDR333 conditions can use  $V_{DD}/V_{DDQ} = 2.5V \pm 0.2V$ .  
 2. Available only on Revision F.  
 3. Available only on Revision J.

**Table 1: Key Timing Parameters**

CL = CAS (READ) latency; data-out window is MIN clock rate with 50% duty cycle at CL = 2, CL = 2.5, or CL = 3

| Speed Grade | Clock Rate (MHz) |          |        | Data-Out Window | Access Window       | DQS-DQ Skew |
|-------------|------------------|----------|--------|-----------------|---------------------|-------------|
|             | CL = 2           | CL = 2.5 | CL = 3 |                 |                     |             |
| -5B         | 133              | 167      | 200    | 1.6ns           | $\pm 0.70\text{ns}$ | 0.40ns      |
| -6          | 133              | 167      | n/a    | 2.1ns           | $\pm 0.70\text{ns}$ | 0.40ns      |
| 6T          | 133              | 167      | n/a    | 2.0ns           | $\pm 0.70\text{ns}$ | 0.45ns      |
| -75E/-75Z   | 133              | 133      | n/a    | 2.5ns           | $\pm 0.75\text{ns}$ | 0.50ns      |
| -75         | 100              | 133      | n/a    | 2.5ns           | $\pm 0.75\text{ns}$ | 0.50ns      |

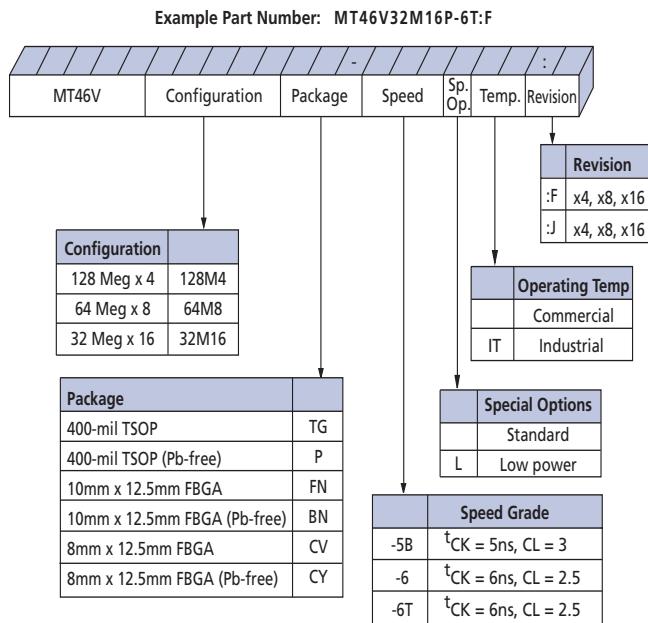
**Table 2: Addressing**

| Parameter      | 128 Meg x 4          | 64 Meg x 8           | 32 Meg x 16          |
|----------------|----------------------|----------------------|----------------------|
| Configuration  | 32 Meg x 4 x 4 banks | 16 Meg x 8 x 4 banks | 8 Meg x 16 x 4 banks |
| Refresh count  | 8K                   | 8K                   | 8K                   |
| Row address    | 8K (A0–A12)          | 8K (A0–A12)          | 8K (A0–A12)          |
| Bank address   | 4 (BA0, BA1)         | 4 (BA0, BA1)         | 4 (BA0, BA1)         |
| Column address | 4K (A0–A9, A11, A12) | 2K (A0–A9, A11)      | 1K (A0–A9)           |

**Table 3: Speed Grade Compatibility**

| Marking          | PC3200 (3-3-3) | PC2700 (2.5-3-3) | PC2100 (2-2-2) | PC2100 (2-3-3) | PC2100 (2.5-3-3) | PC1600 (2-2-2) |
|------------------|----------------|------------------|----------------|----------------|------------------|----------------|
| -5B <sup>1</sup> | Yes            | Yes              | Yes            | Yes            | Yes              | Yes            |
| -6               | —              | Yes              | Yes            | Yes            | Yes              | Yes            |
| -6T              | —              | Yes              | Yes            | Yes            | Yes              | Yes            |
| -75E             | —              | —                | Yes            | Yes            | Yes              | Yes            |
| -75Z             | —              | —                | —              | Yes            | Yes              | Yes            |
| -75              | —              | —                | —              | —              | Yes              | Yes            |
|                  | <b>-5B</b>     | <b>-6/-6T</b>    | <b>-75E</b>    | <b>-75Z</b>    | <b>-75</b>       | <b>-75</b>     |

Notes: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of -5B device operating at slower speed grades is  $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$ .

**Figure 1: 512Mb DDR SDRAM Part Numbers**


### FBGA Part Number System

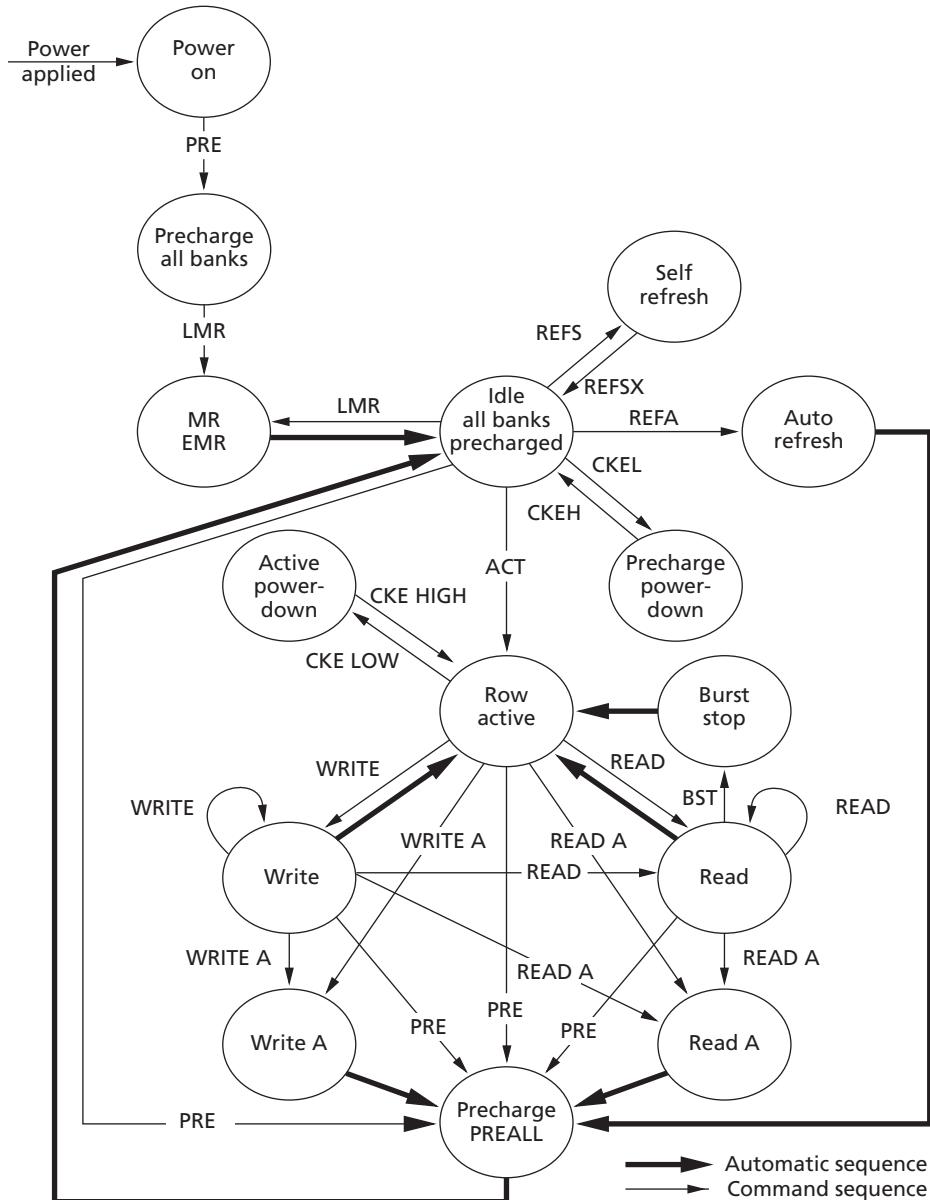
Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: [www.micron.com](http://www.micron.com).

**Table of Contents**

|   |     |
|---|-----|
| State Diagram .....                             | .4  |
| Functional Description .....                    | .5  |
| General Notes .....                             | .5  |
| Functional Block Diagrams.....                  | .6  |
| Pin and Ball Assignments and Descriptions ..... | .8  |
| Package Dimensions .....                        | .12 |
| Electrical Specifications – IDD .....           | .15 |
| Electrical Specifications – DC and AC.....      | .20 |
| Notes.....                                      | .37 |
| Commands .....                                  | .45 |
| DESELECT .....                                  | .49 |
| NO OPERATION (NOP).....                         | .49 |
| LOAD MODE REGISTER (LMR) .....                  | .49 |
| ACTIVE (ACT) .....                              | .50 |
| READ .....                                      | .51 |
| WRITE .....                                     | .52 |
| PRECHARGE (PRE) .....                           | .53 |
| BURST TERMINATE (BST).....                      | .53 |
| AUTO REFRESH (AR).....                          | .53 |
| SELF REFRESH .....                              | .53 |
| Operations .....                                | .54 |
| INITIALIZATION .....                            | .54 |
| REGISTER DEFINITION.....                        | .57 |
| ACTIVE .....                                    | .61 |
| READ .....                                      | .62 |
| WRITE .....                                     | .74 |
| PRECHARGE .....                                 | .87 |
| AUTO REFRESH .....                              | .89 |
| SELF REFRESH .....                              | .90 |
| Power-down (CKE Not Active) .....               | .92 |

## State Diagram

**Figure 2: Simplified State Diagram**



ACT = ACTIVE  
 BST = BURST TERMINATE  
 CKEH = Exit power-down  
 CKEL = Enter power-down  
 EMR = Extended mode register  
 LMR = LOAD MODE REGISTER  
 MR = Mode register

PRE = PRECHARGE  
 PREALL = PRECHARGE all banks  
 READ A = READ with auto precharge  
 REFA = AUTO REFRESH  
 REFS = Enter self refresh  
 REFSX = Exit self refresh  
 WRITE A = WRITE with auto precharge

**Note:** This diagram represents operations within a single bank only and does not capture concurrent operations in other banks.

## Functional Description

The DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single  $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK.

Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which may then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL\_2. All full-drive option outputs are SSTL\_2, Class II compatible.

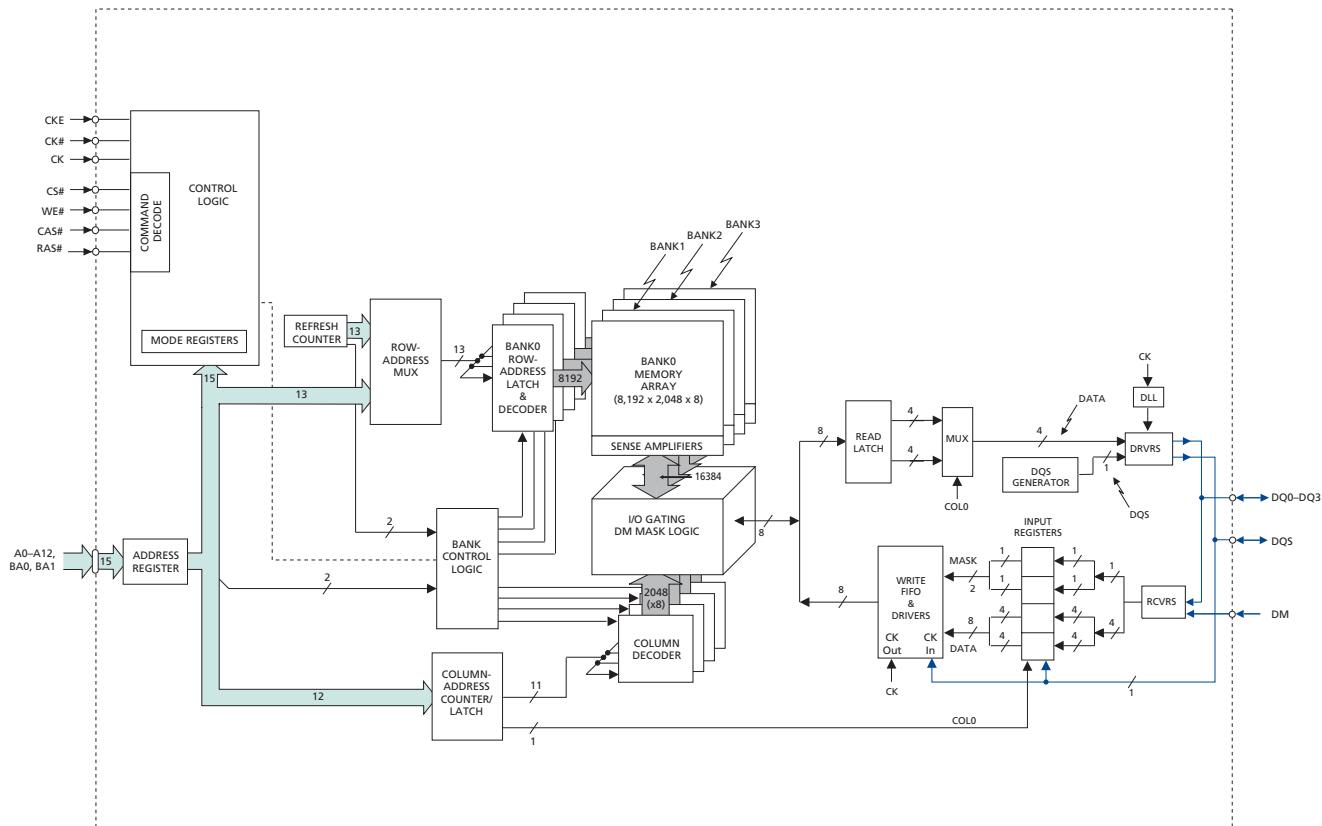
## General Notes

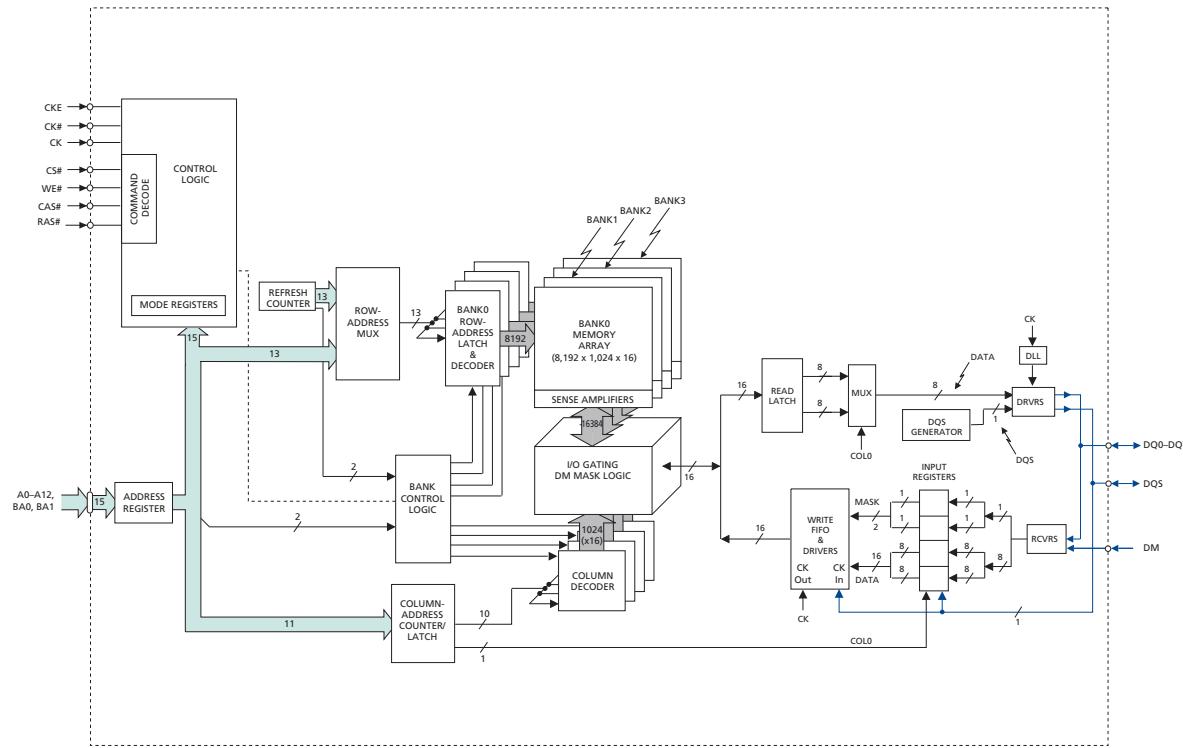
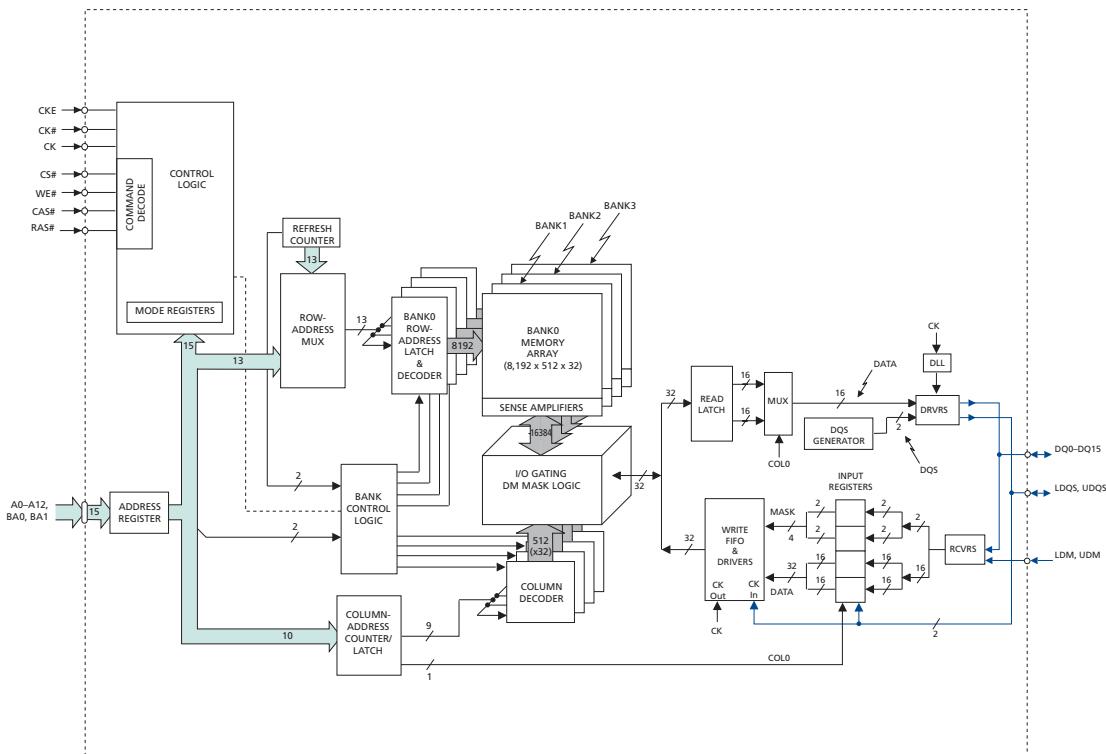
- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ[7:0]) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]) DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

## Functional Block Diagrams

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a 4-bank DRAM.

**Figure 3: 128 Meg x 4 Functional Block Diagram**



**Figure 4: 64 Meg x 8 Functional Block Diagram**

**Figure 5: 32 Meg x 16 Functional Block Diagram**


## Pin and Ball Assignments and Descriptions

**Figure 6: 66-Pin TSOP Pin Assignment (Top View)**

| x4               | x8               | x16              |     | x16 | x8               | x4               |
|------------------|------------------|------------------|-----|-----|------------------|------------------|
| V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | 1 • | 66  | V <sub>SS</sub>  | V <sub>SS</sub>  |
| NF               | DQ0              | DQ0              | 2   | 65  | DQ15             | DQ7              |
| V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>DDQ</sub> | 3   | 64  | V <sub>SSQ</sub> | V <sub>SSQ</sub> |
| NC               | NC               | DQ1              | 4   | 63  | DQ14             | NC               |
| DQ0              | DQ1              | DQ2              | 5   | 62  | DQ13             | DQ6              |
| V <sub>SSQ</sub> | V <sub>SSQ</sub> | V <sub>SSQ</sub> | 6   | 61  | V <sub>DDQ</sub> | V <sub>DDQ</sub> |
| NC               | NC               | DQ3              | 7   | 60  | DQ12             | NC               |
| NF               | DQ2              | DQ4              | 8   | 59  | DQ11             | DQ5              |
| V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>DDQ</sub> | 9   | 58  | V <sub>SSQ</sub> | V <sub>SSQ</sub> |
| NC               | NC               | DQ5              | 10  | 57  | DQ10             | NC               |
| DQ1              | DQ3              | DQ6              | 11  | 56  | DQ9              | DQ4              |
| V <sub>SSQ</sub> | V <sub>SSQ</sub> | V <sub>SSQ</sub> | 12  | 55  | V <sub>DDQ</sub> | V <sub>DDQ</sub> |
| NC               | NC               | DQ7              | 13  | 54  | DQ8              | NC               |
| NC               | NC               | NC               | 14  | 53  | NC               | NC               |
| V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>DDQ</sub> | 15  | 52  | V <sub>SSQ</sub> | V <sub>SSQ</sub> |
| NC               | NC               | LDQS             | 16  | 51  | UDQS             | DQS              |
| NC               | NC               | NC               | 17  | 50  | DNU              | DNU              |
| V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | 18  | 49  | V <sub>REF</sub> | V <sub>REF</sub> |
| DNU              | DNU              | DNU              | 19  | 48  | V <sub>SS</sub>  | V <sub>SS</sub>  |
| NC               | NC               | LDM              | 20  | 47  | UDM              | DM               |
| WE#              | WE#              | WE#              | 21  | 46  | CK#              | CK#              |
| CAS#             | CAS#             | CAS#             | 22  | 45  | CK               | CK               |
| RAS#             | RAS#             | RAS#             | 23  | 44  | CKE              | CKE              |
| CS#              | CS#              | CS#              | 24  | 43  | NC               | NC               |
| NC               | NC               | NC               | 25  | 42  | A12              | A12              |
| BA0              | BA0              | BA0              | 26  | 41  | A11              | A11              |
| BA1              | BA1              | BA1              | 27  | 40  | A9               | A9               |
| A10/AP           | A10/AP           | A10/AP           | 28  | 39  | A8               | A8               |
| A0               | A0               | A0               | 29  | 38  | A7               | A7               |
| A1               | A1               | A1               | 30  | 37  | A6               | A6               |
| A2               | A2               | A2               | 31  | 36  | A5               | A5               |
| A3               | A3               | A3               | 32  | 35  | A4               | A4               |
| V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | 33  | 34  | V <sub>SS</sub>  | V <sub>SS</sub>  |

**Figure 7: 60-Ball FBGA Ball Assignment (Top View)**

**x4 (Top View)**

| 1    | 2    | 3   | 4 | 5 | 6 | 7    | 8    | 9    |
|------|------|-----|---|---|---|------|------|------|
| VssQ | NF   | Vss | A |   |   | VDD  | NF   | VDDQ |
| NC   | VDDQ | DQ3 | B |   |   | DQ0  | VssQ | NC   |
| NC   | VssQ | NF  | C |   |   | NF   | VDDQ | NC   |
| NC   | VDDQ | DQ2 | D |   |   | DQ1  | VssQ | NC   |
| NC   | VssQ | DQS | E |   |   | NC   | VDDQ | NC   |
| VREF | Vss  | DM  | F |   |   | NC   | VDD  | DNu  |
|      | CK   | CK# | G |   |   | WE#  | CAS# |      |
|      | A12  | CKE | H |   |   | RAS# | CS#  |      |
|      | A11  | A9  | J |   |   | BA1  | BA0  |      |
|      | A8   | A7  | K |   |   | A0   | A10  |      |
|      | A6   | A5  | L |   |   | A2   | A1   |      |
|      | A4   | Vss | M |   |   | VDD  | A3   |      |

**x8 (Top View)**

| 1    | 2    | 3   | 4 | 5 | 6 | 7    | 8    | 9    |
|------|------|-----|---|---|---|------|------|------|
| VssQ | DQ7  | Vss | A |   |   | VDD  | DQ0  | VDDQ |
| NC   | VDDQ | DQ6 | B |   |   | DQ1  | VssQ | NC   |
| NC   | VssQ | DQ5 | C |   |   | DQ2  | VDDQ | NC   |
| NC   | VDDQ | DQ4 | D |   |   | DQ3  | VssQ | NC   |
| NC   | VssQ | DQS | E |   |   | NC   | VDDQ | NC   |
| VREF | Vss  | DM  | F |   |   | NC   | VDD  | DNu  |
|      | CK   | CK# | G |   |   | WE#  | CAS# |      |
|      | A12  | CKE | H |   |   | RAS# | CS#  |      |
|      | A11  | A9  | J |   |   | BA1  | BA0  |      |
|      | A8   | A7  | K |   |   | A0   | A10  |      |
|      | A6   | A5  | L |   |   | A2   | A1   |      |
|      | A4   | Vss | M |   |   | VDD  | A3   |      |

**x16 (Top View)**

| 1    | 2    | 3    | 4 | 5 | 6 | 7    | 8    | 9    |
|------|------|------|---|---|---|------|------|------|
| VssQ | DQ15 | Vss  | A |   |   | VDD  | DQ0  | VDDQ |
| DQ14 | VDDQ | DQ13 | B |   |   | DQ2  | VssQ | DQ1  |
| DQ12 | VssQ | DQ11 | C |   |   | DQ4  | VDDQ | DQ3  |
| DQ10 | VDDQ | DQ9  | D |   |   | DQ6  | VssQ | DQ5  |
| DQ8  | VssQ | UDQS | E |   |   | LDQS | VDDQ | DQ7  |
| VREF | Vss  | UDM  | F |   |   | LDM  | VDD  | DNu  |
|      | CK   | CK#  | G |   |   | WE#  | CAS# |      |
|      | A12  | CKE  | H |   |   | RAS# | CS#  |      |
|      | A11  | A9   | J |   |   | BA1  | BA0  |      |
|      | A8   | A7   | K |   |   | A0   | A10  |      |
|      | A6   | A5   | L |   |   | A2   | A1   |      |
|      | A4   | Vss  | M |   |   | VDD  | A3   |      |

**Table 4: Pin and Ball Descriptions**

| FBGA Numbers  | TSOP Numbers   | Symbol  | Type  | Description   |
|---|--|---|-------|---|
| K7, L8, L7,<br>M8, M2, L3,<br>L2, K3, K2,<br>J3, K8,<br>J2, H2                | 29, 30, 31,<br>32, 35, 36,<br>37, 38, 39,<br>40, 28<br>41, 42            | A0, A1, A2,<br>A3, A4, A5,<br>A6, A7, A8,<br>A9, A10,<br>A11, A12 | Input | <b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.  |
| J8, J7  | 26, 27   | BA0, BA1  | Input | <b>Bank address inputs:</b> BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER (LMR) command.  |
| G2, G3  | 45, 46   | CK, CK#   | Input | <b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.   |
| H3  | 44   | CKE   | Input | <b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V <sub>DD</sub> is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only. |
| H8  | 24   | CS#   | Input | <b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.  |
| F3<br>F7, F3  | 47<br>20,47  | DM<br>LDM, UDM  | Input | <b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ[7:0] and UDM is DM for DQ[15:8]. Pin 20 is a NC on x4 and x8.   |
| H7, G8,<br>G7   | 23, 22,<br>21  | RAS#, CAS#,<br>WE#  | Input | <b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered.   |
| A8, B9, B7,<br>C9, C7, D9,<br>D7, E9, E1,<br>D3, D1, C3,<br>C1, B3, B1,<br>A2 | 2, 4, 5,<br>7, 8, 10,<br>11, 13, 54,<br>56, 57, 59,<br>60, 62, 63,<br>65 | DQ[2:0]<br>DQ[5:3]<br>DQ[8:6]<br>DQ[11:9]<br>DQ[14:12]<br>DQ15    | I/O   | <b>Data input/output:</b> Data bus for x16.   |
| A8, B7, C7,<br>D7, D3, C3,<br>B3, A2  | 2, 5, 8,<br>11, 56, 59,<br>62, 65  | DQ[2:0]<br>DQ[5:3]<br>DQ6, DQ7                                    | I/O   | <b>Data input/output:</b> Data bus for x8.  |
| B7, D7, D3,<br>B3   | 5, 11, 56,<br>62   | DQ[2:0]<br>DQ3  | I/O   | <b>Data input/output:</b> Data bus for x4.  |

**Table 4: Pin and Ball Descriptions (continued)**

| FBGA Numbers                                    | TSOP Numbers   | Symbol              | Type   | Description  |
|---|--|---------------------|--------|--|
| E3<br>E7<br>E3                                  | 51<br>16<br>51   | DQS<br>LDQS<br>UDQS | I/O    | <b>Data strobe:</b> Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ[7:0] and UDQS is DQS for DQ[15:8]. Pin 16 (E7) is NC on x4 and x8. |
| F8, M7, A7                                      | 1, 18, 33  | V <sub>DD</sub>     | Supply | <b>Power supply:</b> 2.5V ±0.2V. (2.6V ±0.1V for DDR400).  |
| B2, D2, C8,<br>E8, A9                           | 3, 9, 15, 55,<br>61  | V <sub>DDQ</sub>    | Supply | <b>DQ power supply:</b> 2.5V ±0.2V (2.6V ±0.1V for DDR400). Isolated on the die for improved noise immunity.   |
| F1  | 49   | V <sub>REF</sub>    | Supply | SSTL_2 reference voltage.  |
| A3, F2, M3                                      | 34, 48, 66   | V <sub>SS</sub>     | Supply | Ground.  |
| A1, C2, E2,<br>B8, D8                           | 6, 12, 52,<br>58, 64   | V <sub>SSQ</sub>    | Supply | <b>DQ ground:</b> Isolated on the die for improved noise immunity.   |
| –   | 14, 17, 25,<br>43, 53  | NC                  | –      | <b>No connect for x16:</b> These pins should be left unconnected.  |
| B1, B9, C1,<br>C9, D1, D9,<br>E1, E7, E9,<br>F7 | 4, 7, 10,<br>13, 14, 16,<br>17, 20, 25,<br>43, 53, 54,<br>57, 60, 63 | NC                  | –      | <b>No connect for x8:</b> These pins should be left unconnected.   |
| B1, B9, C1,<br>C9, D1, D9,<br>E1, E7, E9,<br>F7 | 4, 7, 10, 13,<br>14, 16, 17,<br>20, 25, 43,<br>53, 54, 57,<br>60, 63 | NC                  | –      | <b>No connect for x4:</b> These pins should be left unconnected.   |
| A2, A8, C3,<br>C7                               | 2, 8, 59, 65   | NF                  | –      | <b>No function for x4:</b> These pins should be left unconnected.  |
| F9  | 19, 50   | DNU                 | –      | <b>Do not use:</b> Must float to minimize noise on V <sub>REF</sub>  |

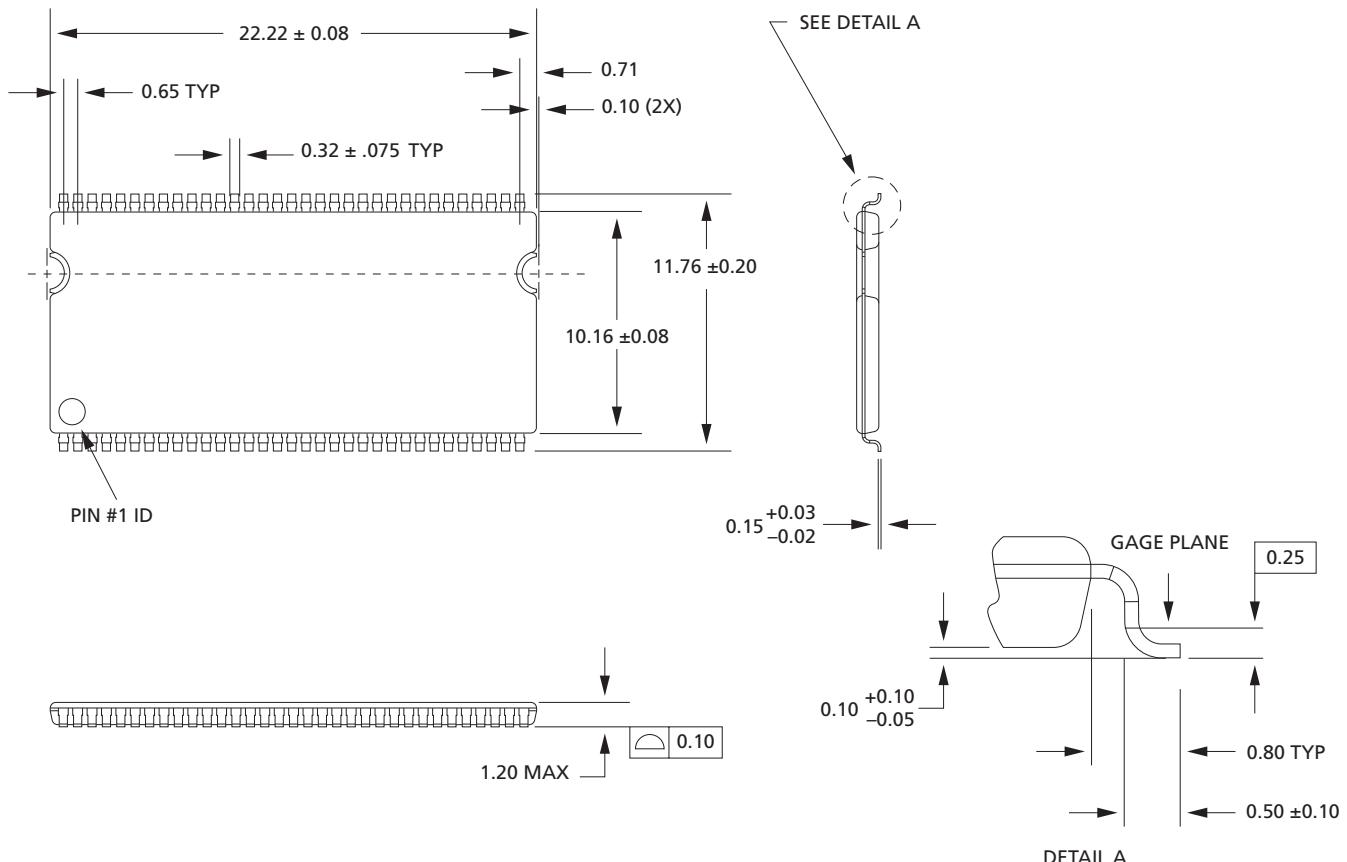
**Table 5: Reserved NC Pin and Ball Descriptions**

NC pins not listed may also be reserved for other uses; this table defines NC pins of importance

| TSOP Numbers | Symbol | Type  | Description                        |
|--------------|--------|-------|------------------------------------|
| 17           | A13    | Input | Address input A13 for 1Gb devices. |

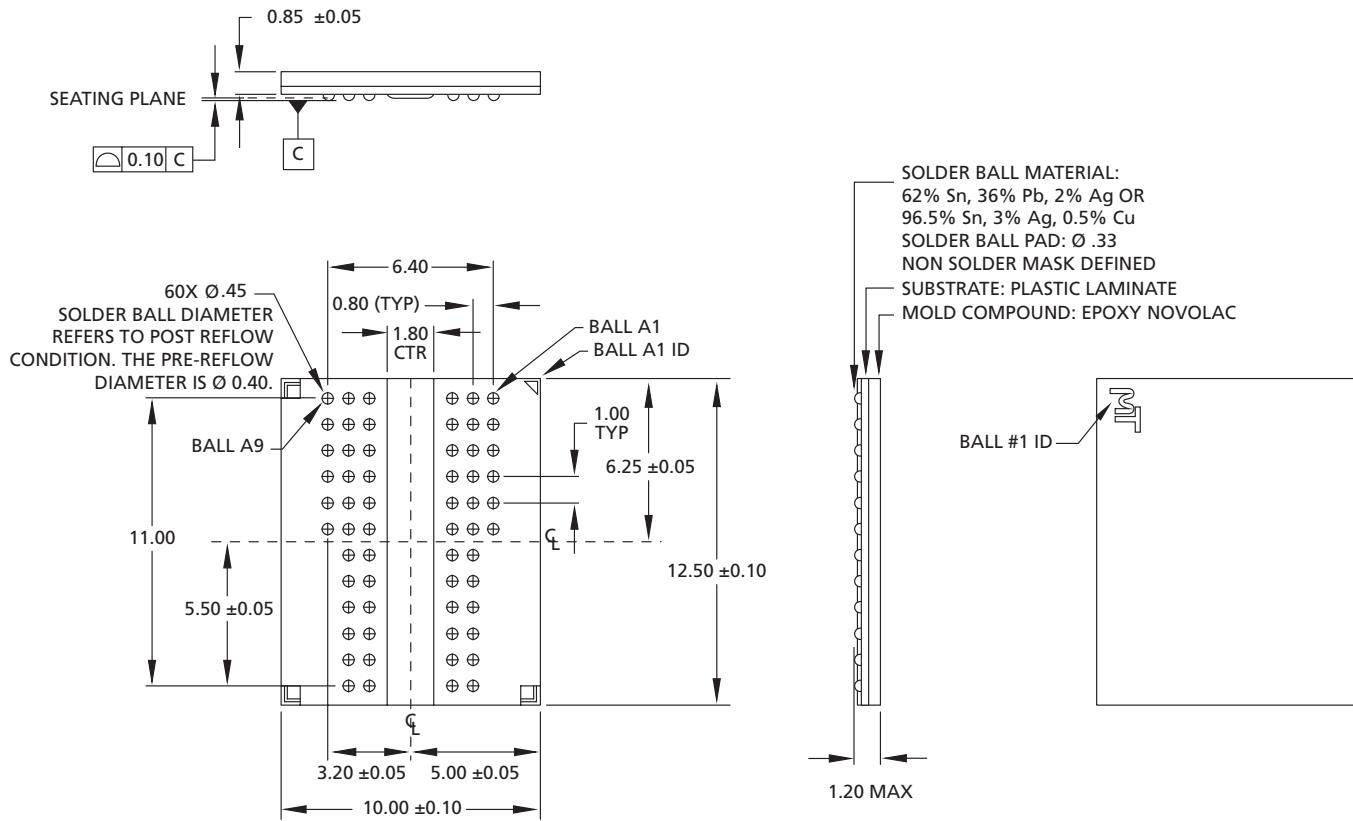
## Package Dimensions

**Figure 8: 66-Pin Plastic TSOP (400 mil)**



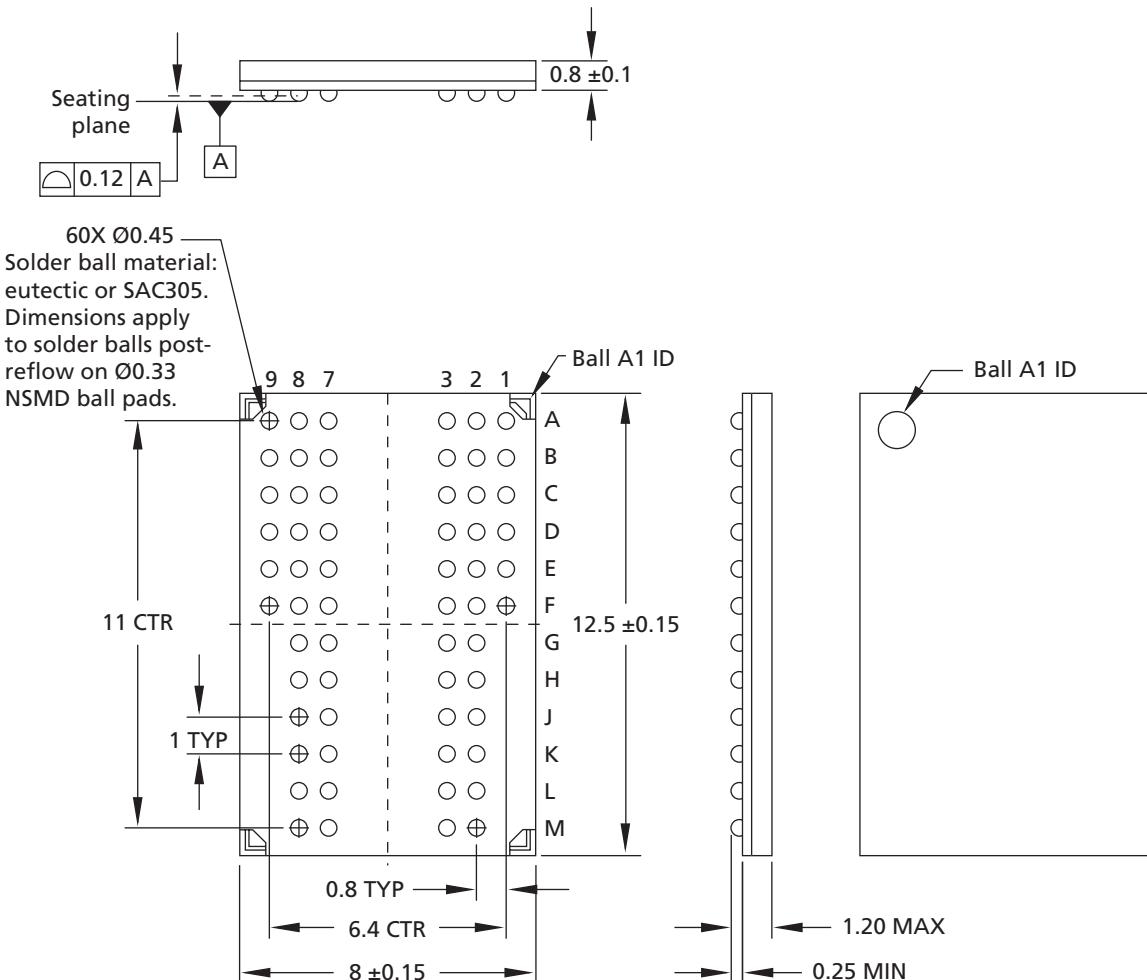
- Notes:**
1. All dimensions are in millimeters.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
  3. Not all packages will have the half moon shaped notches as shown.

**Figure 9: 60-Ball FBGA (10mm x 12.5mm)**



**Notes:** 1. All dimensions are in millimeters.  
2. Topside part marking decoder can be found on Micron's Web site.

**Figure 10: 60-Ball FBGA (8mm x 12.5mm)**



- Notes:**
1. All dimensions are in millimeters.
  2. Topside part marking decoder can be found on Micron's Web site.

## Electrical Specifications – I<sub>DD</sub>

**Table 6: I<sub>DD</sub> Specifications and Conditions (x4, x8) Die Revision F Only**

V<sub>DDQ</sub> = 2.6V ± 0.1V, V<sub>DD</sub> = 2.6V ± 0.1V (-5B); V<sub>DDQ</sub> = 2.5V ± 0.2V, V<sub>DD</sub> = 2.5V ± 0.2V (-6, -6T, -75E, -75Z, -75); 0°C ≤ T<sub>A</sub> ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

| Parameter/Condition  | Symbol                    | -5B               | -6/6T | -75E | -75Z/-75 | Units | Notes  |        |
|--|---------------------------|-------------------|-------|------|----------|-------|--------|--------|
| <b>Operating one-bank active-precharge current:</b><br>$t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles                         | I <sub>DD0</sub>          | 155               | 130   | 130  | 115      | mA    | 23, 48 |        |
| <b>Operating one-bank active-read-precharge current:</b><br>Burst = 4; $t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle  | I <sub>DD1</sub>          | 185               | 160   | 160  | 145      | mA    | 23, 48 |        |
| <b>Precharge power-down standby current:</b> All banks idle; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = (LOW)   | I <sub>DD2P</sub>         | 5                 | 5     | 5    | 5        | mA    | 24, 33 |        |
| <b>Idle standby current:</b> CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM                               | I <sub>DD2F</sub>         | 55                | 45    | 45   | 40       | mA    | 51     |        |
| <b>Active power-down standby current:</b> One bank active; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = LOW   | I <sub>DD3P</sub>         | 45                | 35    | 35   | 30       | mA    | 24, 33 |        |
| <b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}$ (MAX); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle       | I <sub>DD3N</sub>         | 60                | 50    | 50   | 45       | mA    | 23     |        |
| <b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); I <sub>OUT</sub> = 0mA   | I <sub>DD4R</sub>         | 190               | 165   | 165  | 145      | mA    | 23, 48 |        |
| <b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle                    | I <sub>DD4W</sub>         | 195               | 175   | 155  | 135      | mA    | 23     |        |
| <b>Auto refresh burst current:</b>   | $t_{RFC} = t_{RFC}$ (MIN) | I <sub>DD5</sub>  | 345   | 290  | 290      | 280   | mA     | 50     |
|  | $t_{RFC} = 7.8\mu s$      | I <sub>DD5A</sub> | 11    | 10   | 10       | 10    | mA     | 28, 50 |
|  | $t_{RFC} = 1.95\mu s$     | I <sub>DD5A</sub> | 16    | 15   | 15       | 15    | mA     | 28, 50 |
| <b>Self refresh current:</b> CKE ≤ 0.2V  | Standard                  | I <sub>DD6</sub>  | 5     | 5    | 5        | mA    | 12     |        |
|  | Low power (L)             | I <sub>DD6A</sub> | 3     | 3    | 3        | mA    | 12     |        |
| <b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}$ (MIN); Address and control inputs change only during active READ or WRITE commands | I <sub>DD7</sub>          | 450               | 405   | 400  | 350      | mA    | 23, 49 |        |

**Table 7: I<sub>DD</sub> Specifications and Conditions (x16) Die Revision F Only**

$V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  (-5B);  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  (-6, -6T, -75E, -75Z, -75);  $0^\circ C \leq T_A \leq 70^\circ C$ ; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

| Parameter/Condition  | Symbol                    | -5B               | -6/6T | -75E | -75Z/-75 | Units | Notes  |        |
|--|---------------------------|-------------------|-------|------|----------|-------|--------|--------|
| <b>Operating one-bank active-precharge current:</b><br>$t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles                         | I <sub>DD0</sub>          | 155               | 130   | 130  | 115      | mA    | 23, 48 |        |
| <b>Operating one-bank active-read-precharge current:</b><br>Burst = 4; $t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); $I_{OUT} = 0mA$ ; Address and control inputs changing once per clock cycle  | I <sub>DD1</sub>          | 195               | 160   | 160  | 145      | mA    | 23, 48 |        |
| <b>Precharge power-down standby current:</b> All banks idle; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = (LOW)   | I <sub>DD2P</sub>         | 5                 | 5     | 5    | 5        | mA    | 24, 33 |        |
| <b>Idle standby current:</b> CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM   | I <sub>DD2F</sub>         | 55                | 45    | 45   | 40       | mA    | 51     |        |
| <b>Active power-down standby current:</b> One bank active; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = LOW   | I <sub>DD3P</sub>         | 45                | 35    | 35   | 30       | mA    | 24, 33 |        |
| <b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}$ (MAX); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle       | I <sub>DD3N</sub>         | 60                | 50    | 50   | 45       | mA    | 23     |        |
| <b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); $I_{OUT} = 0mA$  | I <sub>DD4R</sub>         | 210               | 165   | 165  | 145      | mA    | 23, 48 |        |
| <b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle                    | I <sub>DD4W</sub>         | 215               | 195   | 160  | 135      | mA    | 23     |        |
| <b>Auto refresh burst current:</b>   | $t_{RFC} = t_{RFC}$ (MIN) | I <sub>DD5</sub>  | 345   | 290  | 290      | 280   | mA     | 50     |
|  | $t_{RFC} = 7.8\mu s$      | I <sub>DD5A</sub> | 11    | 10   | 10       | 10    | mA     | 28, 50 |
|  | $t_{RFC} = 1.95\mu s$     | I <sub>DD5A</sub> | 16    | 15   | 15       | 15    | mA     | 28, 50 |
| <b>Self refresh current:</b> CKE $\leq 0.2V$   | Standard                  | I <sub>DD6</sub>  | 6     | 5    | 5        | 5     | mA     | 12     |
|  | Low power (L)             | I <sub>DD6A</sub> | 4     | 3    | 3        | 3     | mA     | 12     |
| <b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}$ (MIN); Address and control inputs change only during active READ or WRITE commands | I <sub>DD7</sub>          | 480               | 405   | 400  | 350      | mA    | 23, 49 |        |

**Table 8: I<sub>DD</sub> Specifications and Conditions (x4, x8) Die Revision J Only**

V<sub>DDQ</sub> = 2.6V ±0.1V, V<sub>DD</sub> = 2.6V ±0.1V (-5B); V<sub>DDQ</sub> = 2.5V ±0.2V, V<sub>DD</sub> = 2.5V ±0.2V (-6, -6T,);  
0°C ≤ T<sub>A</sub> ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

| Parameter/Condition  | Symbol                    | -5B               | -6/6T | Units | Notes  |
|--|---------------------------|-------------------|-------|-------|--------|
| <b>Operating one-bank active-precharge current:</b><br>$t_{RC} = t_{CK}$ (MIN); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles                         | I <sub>DD0</sub>          | 75                | 65    | mA    | 23, 48 |
| <b>Operating one-bank active-read-precharge current:</b><br>Burst = 4; $t_{RC} = t_{CK}$ (MIN); $t_{CK} = t_{CK}$ (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle  | I <sub>DD1</sub>          | 85                | 75    | mA    | 23, 48 |
| <b>Precharge power-down standby current:</b> All banks idle; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = (LOW)   | I <sub>DD2P</sub>         | 5                 | 5     | mA    | 24, 33 |
| <b>Idle standby current:</b> CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM                               | I <sub>DD2F</sub>         | 23                | 23    | mA    | 51     |
| <b>Active power-down standby current:</b> One bank active; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = LOW   | I <sub>DD3P</sub>         | 18                | 14    | mA    | 24, 33 |
| <b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}$ (MAX); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle       | I <sub>DD3N</sub>         | 40                | 38    | mA    | 23     |
| <b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); I <sub>OUT</sub> = 0mA   | I <sub>DD4R</sub>         | 120               | 85    | mA    | 23, 48 |
| <b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle                    | I <sub>DD4W</sub>         | 120               | 95    | mA    | 23     |
| <b>Auto refresh burst current:</b>   | $t_{RFC} = t_{RFC}$ (MIN) | I <sub>DD5</sub>  | 120   | 105   | mA     |
|  | $t_{RFC} = 7.8\mu s$      | I <sub>DD5A</sub> | 8     | 8     | mA     |
| <b>Self refresh current:</b> CKE ≤ 0.2V  | Standard                  | I <sub>DD6</sub>  | 5     | 5     | mA     |
|  | Low power (L)             | I <sub>DD6A</sub> | 3     | 3     | mA     |
| <b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}$ (MIN); Address and control inputs change only during active READ or WRITE commands | I <sub>DD7</sub>          | 230               | 210   | mA    | 23, 49 |

**Table 9: I<sub>DD</sub> Specifications and Conditions (x16) Die Revision J Only**

$V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  (-5B);  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  (-6, -6T);  
 $0^\circ C \leq T_A \leq 70^\circ C$ ; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

| Parameter/Condition  | Symbol                    | -5B               | -6/6T | Units | Notes  |        |
|--|---------------------------|-------------------|-------|-------|--------|--------|
| <b>Operating one-bank active-precharge current:</b><br>$t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles                         | I <sub>DD0</sub>          | 75                | 65    | mA    | 23, 48 |        |
| <b>Operating one-bank active-read-precharge current:</b><br>Burst = 4; $t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); $I_{OUT} = 0mA$ ; Address and control inputs changing once per clock cycle  | I <sub>DD1</sub>          | 85                | 75    | mA    | 23, 48 |        |
| <b>Precharge power-down standby current:</b> All banks idle; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = (LOW)   | I <sub>DD2P</sub>         | 5                 | 5     | mA    | 24, 33 |        |
| <b>Idle standby current:</b> CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM   | I <sub>DD2F</sub>         | 23                | 23    | mA    | 51     |        |
| <b>Active power-down standby current:</b> One bank active; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = LOW   | I <sub>DD3P</sub>         | 18                | 14    | mA    | 24, 33 |        |
| <b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}$ (MAX); $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle       | I <sub>DD3N</sub>         | 40                | 38    | mA    | 23     |        |
| <b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); $I_{OUT} = 0mA$  | I <sub>DD4R</sub>         | 125               | 95    | mA    | 23, 48 |        |
| <b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle                    | I <sub>DD4W</sub>         | 120               | 95    | mA    | 23     |        |
| <b>Auto refresh burst current:</b>   | $t_{RFC} = t_{RFC}$ (MIN) | I <sub>DD5</sub>  | 125   | 110   | mA     | 50     |
|  | $t_{RFC} = 7.8\mu s$      | I <sub>DD5A</sub> | 8     | 8     | mA     | 28, 50 |
| <b>Self refresh current:</b> CKE $\leq 0.2V$   | Standard                  | I <sub>DD6</sub>  | 5     | 5     | mA     | 12     |
|  | Low power (L)             | I <sub>DD6A</sub> | 3     | 3     | mA     | 12     |
| <b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}$ (MIN); Address and control inputs change only during active READ or WRITE commands | I <sub>DD7</sub>          | 230               | 210   | mA    | 23, 49 |        |

**Table 10: I<sub>DD</sub> Test Cycle Times**

Values reflect number of clock cycles for each test

| I <sub>DD</sub> Test | Speed Grade | Clock Cycle Time | t <sub>RRD</sub> | t <sub>RCD</sub> | t <sub>RAS</sub> | t <sub>RP</sub> | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>REFI</sub> | CL  |
|----------------------|-------------|------------------|------------------|------------------|------------------|-----------------|-----------------|------------------|-------------------|-----|
| I <sub>DD0</sub>     | -75/75Z     | 7.5ns            | n/a              | n/a              | 6                | 3               | 9               | n/a              | n/a               | n/a |
|                      | -75E        | 7.5ns            | n/a              | n/a              | 6                | 2               | 8               | n/a              | n/a               | n/a |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | 7                | 3               | 10              | n/a              | n/a               | n/a |
|                      | -5B         | 5ns              | n/a              | n/a              | 8                | 3               | 11              | n/a              | n/a               | n/a |
| I <sub>DD1</sub>     | -75         | 7.5ns            | n/a              | n/a              | 6                | 3               | 9               | n/a              | n/a               | 2.5 |
|                      | -75Z        | 7.5ns            | n/a              | n/a              | 6                | 3               | 9               | n/a              | n/a               | 2   |
|                      | -75E        | 7.5ns            | n/a              | n/a              | 6                | 2               | 8               | n/a              | n/a               | 2   |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | 7                | 3               | 10              | n/a              | n/a               | 2.5 |
|                      | -5B         | 5ns              | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 3   |
| I <sub>DD4R</sub>    | -75         | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 2.5 |
|                      | -75Z        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 2   |
|                      | -75E        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 2   |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 2.5 |
|                      | -5B         | 5ns              | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | 3   |
| I <sub>DD4W</sub>    | -75         | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | n/a |
|                      | -75Z        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | n/a |
|                      | -75E        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | n/a |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | n/a |
|                      | -5B         | 5ns              | n/a              | n/a              | n/a              | n/a             | n/a             | n/a              | n/a               | n/a |
| I <sub>DD5</sub>     | -75/75Z     | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | 10               | 10                | n/a |
|                      | -75E        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | 9                | 9                 | n/a |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | n/a              | n/a             | n/a             | 12               | 12                | n/a |
|                      | -5B         | 5ns              | n/a              | n/a              | n/a              | n/a             | n/a             | 14               | 14                | n/a |
| I <sub>DD5A</sub>    | -75/75Z     | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | 10               | 1,029             | n/a |
|                      | -75E        | 7.5ns            | n/a              | n/a              | n/a              | n/a             | n/a             | 10               | 1,029             | n/a |
|                      | -6/-6T      | 6ns              | n/a              | n/a              | n/a              | n/a             | n/a             | 12               | 1,288             | n/a |
|                      | -5B         | 5ns              | n/a              | n/a              | n/a              | n/a             | n/a             | 14               | 1,546             | n/a |
| I <sub>DD7</sub>     | -75         | 7.5ns            | 2                | 3                | n/a              | 3               | 10              | n/a              | n/a               | 2.5 |
|                      | -75Z        | 7.5ns            | 2                | 3                | n/a              | 3               | 10              | n/a              | n/a               | 2   |
|                      | -75E        | 7.5ns            | 2                | 3                | n/a              | 2               | 8               | n/a              | n/a               | 2   |
|                      | -6/-6T      | 6ns              | 2                | 3                | n/a              | 3               | 10              | n/a              | n/a               | 2.5 |
|                      | -5B         | 5ns              | 2                | 3                | n/a              | 3               | 11              | n/a              | n/a               | 3   |

## Electrical Specifications – DC and AC

Stresses greater than those listed in Table 11 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 11: Absolute Maximum Ratings**

| Parameter   | Min   | Max              | Units |
|---|-------|------------------|-------|
| $V_{DD}$ supply voltage relative to $V_{SS}$      | -1V   | 3.6V             | V     |
| $V_{DDQ}$ supply voltage relative to $V_{SS}$     | -1V   | 3.6V             | V     |
| $V_{REF}$ and inputs voltage relative to $V_{SS}$ | -1V   | 3.6V             | V     |
| I/O pins voltage relative to $V_{SS}$             | -0.5V | $V_{DDQ} + 0.5V$ | V     |
| Storage temperature (plastic)                     | -55   | 150              | °C    |
| Short circuit output current                      | -     | 50               | mA    |

**Table 12: DC Electrical Characteristics and Operating Conditions (-5B)**

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;  $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$

| Parameter/Condition  | Symbol   | Min                   | Max                   | Units | Notes      |
|--|--|-----------------------|-----------------------|-------|------------|
| Supply voltage   | $V_{DD}$   | 2.5                   | 2.7                   | V     | 37, 42     |
| I/O supply voltage   | $V_{DDQ}$  | 2.5                   | 2.7                   | V     | 37, 42, 45 |
| I/O reference voltage  | $V_{REF}$  | $0.49 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V     | 7, 45      |
| I/O termination voltage (system)   | $V_{TT}$   | $V_{REF} - 0.04$      | $V_{REF} + 0.04$      | V     | 8, 45      |
| Input high (logic 1) voltage   | $V_{IH(DC)}$   | $V_{REF} + 0.15$      | $V_{DD} + 0.3$        | V     | 29         |
| Input low (logic 0) voltage  | $V_{IL(DC)}$   | -0.3                  | $V_{REF} - 0.15$      | V     | 29         |
| Input leakage current:<br>Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 1.35V$<br>(All other pins not under test = 0V) | $I_I$  | -2                    | 2                     | µA    |            |
| Output leakage current:<br>(DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )  | $I_{OZ}$   | -5                    | 5                     | µA    |            |
| Full-drive option output levels (x4, x8, x16):   | High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ ) | $I_{OH}$              | -16.8                 | -     | mA         |
|  | Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )            | $I_{OL}$              | 16.8                  | -     | mA         |
| Reduced-drive option output levels:  | High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ ) | $I_{OHR}$             | -9                    | -     | mA         |
|  | Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )            | $I_{OLR}$             | 9                     | -     | mA         |
| Ambient operating temperatures   | Commercial   | $T_A$                 | 0                     | 70    | °C         |
|  | Industrial   | $T_A$                 | -40                   | 85    | °C         |

**Table 13: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)**

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$ 

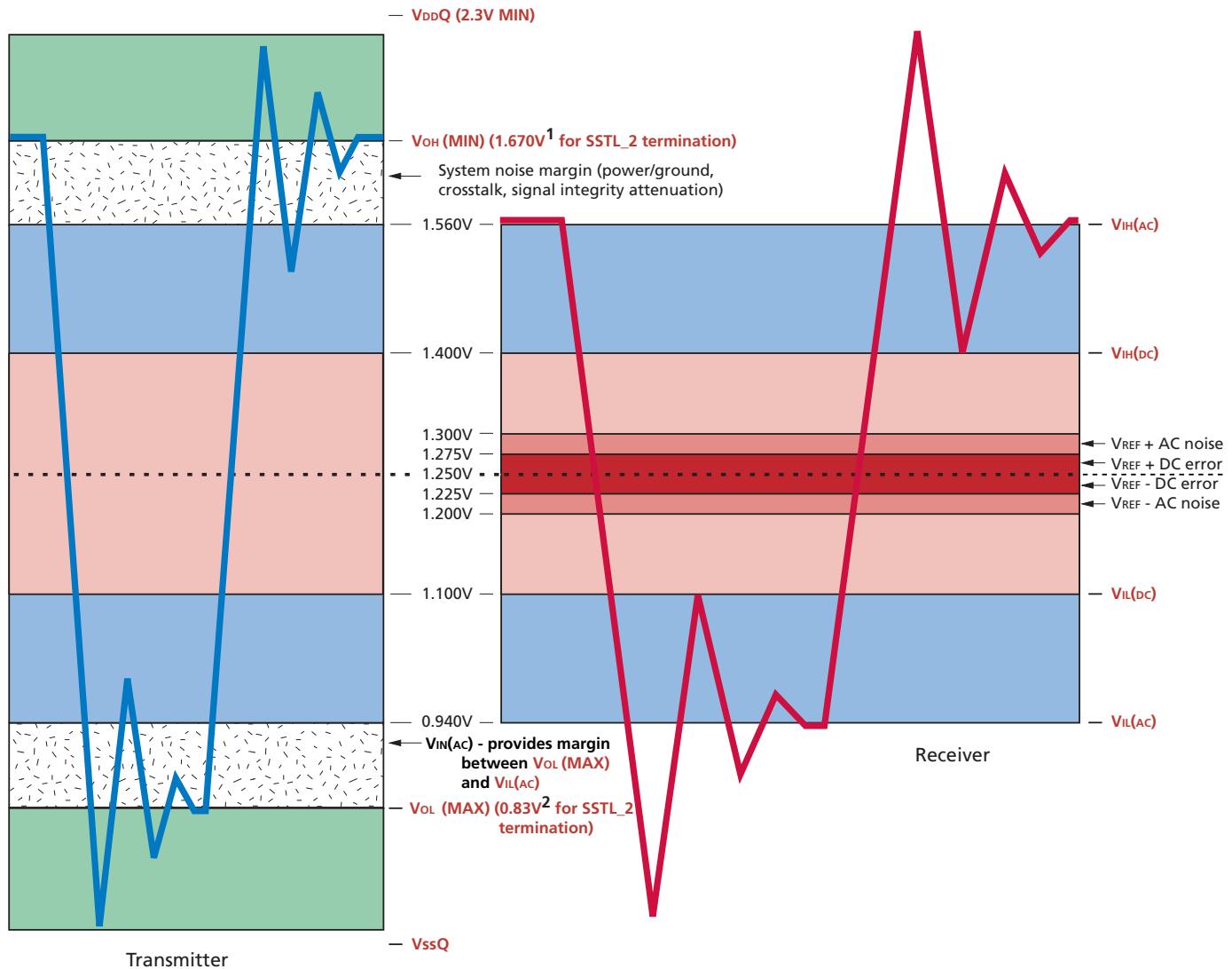
| Parameter/Condition  | Symbol   | Min                   | Max                   | Units   | Notes       |        |
|--|--|-----------------------|-----------------------|---------|-------------|--------|
| Supply voltage   | $V_{DD}$   | 2.3                   | 2.7                   | V       | 37, 42      |        |
| I/O supply voltage   | $V_{DDQ}$  | 2.3                   | 2.7                   | V       | 37, 42, 45  |        |
| I/O reference voltage  | $V_{REF}$  | $0.49 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V       | 7, 45       |        |
| I/O termination voltage (system)   | $V_{TT}$   | $V_{REF} - 0.04$      | $V_{REF} + 0.04$      | V       | 8, 45       |        |
| Input high (logic 1) voltage   | $V_{IH(DC)}$   | $V_{REF} + 0.15$      | $V_{DD} + 0.3$        | V       | 29          |        |
| Input low (logic 0) voltage  | $V_{IL(DC)}$   | -0.3                  | $V_{REF} - 0.15$      | V       | 29          |        |
| Input leakage current:<br>Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 1.35V$<br>(All other pins not under test = 0V) | $I_I$  | -2                    | 2                     | $\mu A$ |             |        |
| Output leakage current:<br>(DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )  | $I_{OZ}$   | -5                    | 5                     | $\mu A$ |             |        |
| Full-drive option output levels (x4, x8, x16):   | High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ ) | $I_{OH}$              | -16.8                 | -       | mA          | 38, 40 |
|  | Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )            | $I_{OL}$              | 16.8                  | -       | mA          |        |
| Reduced-drive option output levels:  | High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ ) | $I_{OHR}$             | -9                    | -       | mA          | 39, 40 |
|  | Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )            | $I_{OLR}$             | 9                     | -       | mA          |        |
| Ambient operating temperatures   | Commercial   | $T_A$                 | 0                     | 70      | $^{\circ}C$ |        |
|  | Industrial   | $T_A$                 | -40                   | 85      | $^{\circ}C$ |        |

**Table 14: AC Input Operating Conditions**

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;

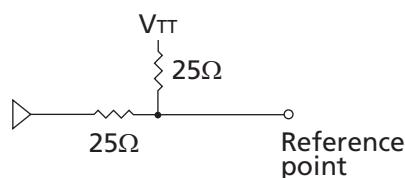
 $0^{\circ}C \leq T_A \leq 70^{\circ}C$ ;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  ( $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  for -5B)

| Parameter/Condition          | Symbol        | Min                   | Max                   | Units | Notes      |
|------------------------------|---------------|-----------------------|-----------------------|-------|------------|
| Input high (logic 1) voltage | $V_{IH(AC)}$  | $V_{REF} + 0.310$     | -                     | V     | 15, 29, 41 |
| Input low (logic 0) voltage  | $V_{IL(AC)}$  | -                     | $V_{REF} - 0.310$     | V     | 15, 29, 41 |
| I/O reference voltage        | $V_{REF(AC)}$ | $0.49 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V     | 7          |

**Figure 11: Input Voltage Waveform**


Notes:

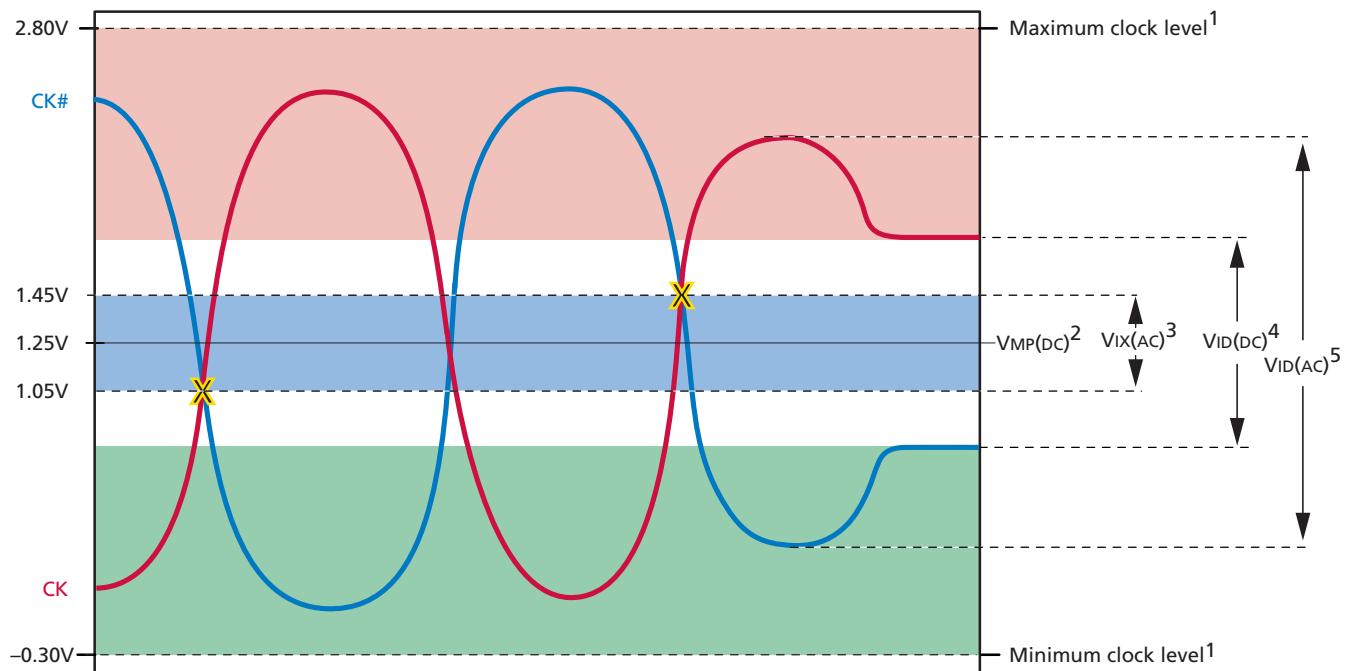
1.  $V_{OH\text{,min}}$  with test load is 1.927V.
2.  $V_{OL\text{,max}}$  with test load is 0.373V.
3. Numbers in diagram reflect nominal values utilizing circuit below for all devices other than -5B.



**Table 15: Clock Input Operating Conditions**

Notes: 1–5, 16, 17, and 31 apply to the entire table; Notes appear on page 37;  
 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  ( $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  for -5B)

| Parameter/Condition                            | Symbol       | Min                        | Max                        | Units | Notes |
|--|--------------|----------------------------|----------------------------|-------|-------|
| Clock input mid-point voltage: CK and CK#      | $V_{MP(DC)}$ | 1.15                       | 1.35                       | V     | 7, 10 |
| Clock input voltage level: CK and CK#          | $V_{IN(DC)}$ | -0.3                       | $V_{DDQ} + 0.3$            | V     | 7     |
| Clock input differential voltage: CK and CK#   | $V_{ID(DC)}$ | 0.36                       | $V_{DDQ} + 0.6$            | V     | 7, 9  |
| Clock input differential voltage: CK and CK#   | $V_{ID(AC)}$ | 0.7                        | $V_{DDQ} + 0.6$            | V     | 9     |
| Clock input crossing point voltage: CK and CK# | $V_{IX(AC)}$ | $0.5 \times V_{DDQ} - 0.2$ | $0.5 \times V_{DDQ} + 0.2$ | V     | 10    |

**Figure 12: SSTL\_2 Clock Input**


- Notes:
1. CK or CK# may not be more positive than  $V_{DDQ} + 0.3V$  or more negative than  $V_{SS} - 0.3V$ .
  2. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of  $V_{DDQ}$ .
  3. CK and CK# must cross in this region.
  4. CK and CK# must meet at least  $V_{ID(DC),min}$  when static and is centered around  $V_{MP(DC)}$ .
  5. CK and CK# must have a minimum 700mV peak-to-peak swing.
  6. For AC operation, all DC clock requirements must also be satisfied.
  7. Numbers in diagram reflect nominal values for all devices other than -5B.

**Table 16: Capacitance (x4, x8 TSOP)**

Note: 14 applies to the entire table; Notes appear on page 37

| Parameter  | Symbol           | Min | Max  | Units | Notes |
|--|------------------|-----|------|-------|-------|
| Delta input/output capacitance: DQ[3:0] (x4), DQ[7:0] (x8) | DC <sub>IO</sub> | –   | 0.50 | pF    | 25    |
| Delta input capacitance: Command and address               | DC <sub>I1</sub> | –   | 0.50 | pF    | 30    |
| Delta input capacitance: CK, CK#                           | DC <sub>I2</sub> | –   | 0.25 | pF    | 30    |
| Input/output capacitance: DQ, DQS, DM                      | C <sub>IO</sub>  | 4.0 | 5.0  | pF    |       |
| Input capacitance: Command and address                     | C <sub>I1</sub>  | 2.0 | 3.0  | pF    |       |
| Input capacitance: CK, CK#                                 | C <sub>I2</sub>  | 2.0 | 3.0  | pF    |       |
| Input capacitance: CKE                                     | C <sub>I3</sub>  | 2.0 | 3.0  | pF    |       |

**Table 17: Capacitance (x4, x8 FBGA)**

Note: 14 applies to the entire table; Notes appear on page 37

| Parameter                                    | Symbol           | Min | Max  | Units | Notes |
|--|------------------|-----|------|-------|-------|
| Delta input/output capacitance: DQ, DQS, DM  | DC <sub>IO</sub> | –   | 0.50 | pF    | 25    |
| Delta input capacitance: Command and address | DC <sub>I1</sub> | –   | 0.50 | pF    | 30    |
| Delta input capacitance: CK, CK#             | DC <sub>I2</sub> | –   | 0.25 | pF    | 30    |
| Input/output capacitance: DQ, DQS, DM        | C <sub>IO</sub>  | 3.5 | 4.5  | pF    |       |
| Input capacitance: Command and address       | C <sub>I1</sub>  | 1.5 | 2.5  | pF    |       |
| Input capacitance: CK, CK#                   | C <sub>I2</sub>  | 1.5 | 2.5  | pF    |       |
| Input capacitance: CKE                       | C <sub>I3</sub>  | 1.5 | 2.5  | pF    |       |

**Table 18: Capacitance (x16 TSOP)**

Note: 14 applies to the entire table; Notes appear on page 37

| Parameter   | Symbol            | Min | Max  | Units | Notes |
|---|-------------------|-----|------|-------|-------|
| Delta input/output capacitance: DQ[7:0], LDQS, LDM  | DC <sub>IOL</sub> | –   | 0.50 | pF    | 25    |
| Delta input/output capacitance: DQ[15:8], UDQS, UDM | DC <sub>IOU</sub> | –   | 0.50 | pF    | 25    |
| Delta input capacitance: Command and address        | DC <sub>I1</sub>  | –   | 0.50 | pF    | 30    |
| Delta input capacitance: CK, CK#                    | DC <sub>I2</sub>  | –   | 0.25 | pF    | 30    |
| Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM  | C <sub>IO</sub>   | 4.0 | 5.0  | pF    |       |
| Input capacitance: Command and address              | C <sub>I1</sub>   | 2.0 | 3.0  | pF    |       |
| Input capacitance: CK, CK#                          | C <sub>I2</sub>   | 2.0 | 3.0  | pF    |       |
| Input capacitance: CKE                              | C <sub>I3</sub>   | 2.0 | 3.0  | pF    |       |

**Table 19: Capacitance (x16 FBGA)**

Note: 14 applies to the entire table; Notes appear on page 37

| Parameter   | Symbol            | Min | Max  | Units | Notes |
|---|-------------------|-----|------|-------|-------|
| Delta input/output capacitance: DQ[7:0], LDQS, LDM  | DC <sub>IOL</sub> | –   | 0.50 | pF    | 25    |
| Delta input/output capacitance: DQ[15:8], UDQS, UDM | DC <sub>IOU</sub> | –   | 0.50 | pF    | 25    |
| Delta input capacitance: Command and address        | DC <sub>I1</sub>  | –   | 0.50 | pF    | 30    |
| Delta input capacitance: CK, CK#                    | DC <sub>I2</sub>  | –   | 0.25 | pF    | 30    |
| Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM  | C <sub>IO</sub>   | 3.5 | 4.5  | pF    |       |
| Input capacitance: Command and address              | C <sub>I1</sub>   | 1.5 | 2.5  | pF    |       |
| Input capacitance: CK, CK#                          | C <sub>I2</sub>   | 1.5 | 2.5  | pF    |       |
| Input capacitance: CKE                              | C <sub>I3</sub>   | 1.5 | 2.5  | pF    |       |

**Table 20: Electrical Characteristics and Recommended AC Operating Conditions (-5B)**

Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$

| AC Characteristics   |               | -5B                |        | Units         | Notes  |
|--|---------------|--------------------|--------|---------------|--------|
| Parameter  | Symbol        | Min                | Max    |               |        |
| Access window of DQ from CK/CK#  | $t_{AC}$      | -0.70              | 0.70   | ns            |        |
| CK high-level width  | $t_{CH}$      | 0.45               | 0.55   | $t_{CK}$      | 31     |
| Clock cycle time   | $t_{CK}(3)$   | 5                  | 7.5    | ns            | 52     |
|  | $t_{CK}(2.5)$ | 6                  | 13     | ns            | 46, 52 |
|  | $t_{CK}(2)$   | 7.5                | 13     | ns            | 46, 52 |
| CK low-level width   | $t_{CL}$      | 0.45               | 0.55   | $t_{CK}$      | 31     |
| DQ and DM input hold time relative to DQS                                | $t_{DH}$      | 0.40               | –      | ns            | 27, 32 |
| DQ and DM input pulse width (for each input)                             | $t_{DIPW}$    | 1.75               | –      | ns            | 32     |
| Access window of DQS from CK/CK#   | $t_{DQSCK}$   | -0.60              | 0.60   | ns            |        |
| DQS input high pulse width   | $t_{DQSH}$    | 0.35               | –      | $t_{CK}$      |        |
| DQS input low pulse width  | $t_{DQL}$     | 0.35               | –      | $t_{CK}$      |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access                 | $t_{DQSQ}$    | –                  | 0.40   | ns            | 26, 27 |
| WRITE command to first DQS latching transition                           | $t_{DQSS}$    | 0.72               | 1.28   | $t_{CK}$      |        |
| DQ and DM input setup time relative to DQS                               | $t_{DS}$      | 0.40               | –      | ns            | 27, 32 |
| DQS falling edge from CK rising – hold time                              | $t_{DSH}$     | 0.2                | –      | $t_{CK}$      |        |
| DQS falling edge to CK rising – setup time                               | $t_{DSS}$     | 0.2                | –      | $t_{CK}$      |        |
| Half-clock period  | $t_{HP}$      | $t_{CH}, t_{CL}$   | –      | ns            | 35     |
| Data-out High-Z window from CK/CK#                                       | $t_{HZ}$      | –                  | 0.70   | ns            | 19, 43 |
| Address and control input hold time (slew rate $\geq 0.5\text{ V/ns}$ )  | $t_{IH_F}$    | 0.60               | –      | ns            | 15     |
| Address and control input pulse width (for each input)                   | $t_{IPW}$     | 2.2                | –      | ns            |        |
| Address and control input setup time (slew rate $\geq 0.5\text{ V/ns}$ ) | $t_{IS_F}$    | 0.60               | –      | ns            | 15     |
| Data-out Low-Z window from CK/CK#  | $t_{LZ}$      | -0.70              | –      | ns            | 19, 43 |
| LOAD MODE REGISTER command cycle time                                    | $t_{MRD}$     | 10                 | –      | ns            |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access                 | $t_{QH}$      | $t_{HP} - t_{QHS}$ | –      | ns            | 26, 27 |
| Data hold skew factor  | $t_{QHS}$     | –                  | 0.50   | ns            |        |
| ACTIVE-to-READ with auto precharge command                               | $t_{RAP}$     | 15                 | –      | ns            |        |
| ACTIVE-to-PRECHARGE command  | $t_{RAS}$     | 40                 | 70,000 | ns            | 36     |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period                             | $t_{RC}$      | 55                 | –      | ns            | 55     |
| ACTIVE-to-READ or WRITE delay  | $t_{RCD}$     | 15                 | –      | ns            |        |
| REFRESH-to-REFRESH command interval                                      | $t_{RFC}$     | –                  | 70.3   | $\mu\text{s}$ | 24     |
| Average periodic refresh interval  | $t_{REFI}$    | –                  | 7.8    | $\mu\text{s}$ | 24     |
| AUTO REFRESH command period  | $t_{RFC}$     | 70                 | –      | ns            | 50     |
| PRECHARGE command period   | $t_{RP}$      | 15                 | –      | ns            |        |
| DQS read preamble  | $t_{RPRE}$    | 0.9                | 1.1    | $t_{CK}$      | 44     |
| DQS read postamble   | $t_{RPST}$    | 0.4                | 0.6    | $t_{CK}$      | 44     |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command                     | $t_{RRD}$     | 10                 | –      | ns            |        |
| Terminating voltage delay to $V_{DD}$                                    | $t_{VTD}$     | 0                  | –      | ns            |        |
| DQS write preamble   | $t_{WPRE}$    | 0.25               | –      | $t_{CK}$      |        |
| DQS write preamble setup time  | $t_{WPRES}$   | 0                  | –      | ns            | 21, 22 |
| DQS write postamble  | $t_{WPST}$    | 0.4                | 0.6    | $t_{CK}$      | 20     |
| Write recovery time  | $t_{WR}$      | 15                 | –      | ns            |        |
| Internal WRITE-to-READ command delay                                     | $t_{WTR}$     | 2                  | –      | $t_{CK}$      |        |

**Table 20: Electrical Characteristics and Recommended AC Operating Conditions (-5B) (continued)**

Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.6\text{V} \pm 0.1\text{V}$ ,  $V_{\text{DD}} = 2.6\text{V} \pm 0.1\text{V}$

| AC Characteristics                    |                   | -5B                               |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 70                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ |     | ns              | 26    |

**Table 21: Electrical Characteristics and Recommended AC Operating Conditions (-6)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                                       |             | -6 (FBGA)          |        | Units         | Notes  |
|--|-------------|--------------------|--------|---------------|--------|
| Parameter  | Symbol      | Min                | Max    |               |        |
| Access window of DQ from CK/CK#                          | $t_{AC}$    | -0.70              | 0.70   | ns            |        |
| CK high-level width                                      | $t_{CH}$    | 0.45               | 0.55   | $t_{CK}$      | 31     |
| Clock cycle time   | CL = 2.5    | $t_{CK}(2.5)$      | 6      | ns            | 46, 52 |
|  | CL = 2      | $t_{CK}(2)$        | 7.5    | ns            | 46, 52 |
| CK low-level width                                       | $t_{CL}$    | 0.45               | 0.55   | $t_{CK}$      | 31     |
| DQ and DM input hold time relative to DQS                | $t_{DH}$    | 0.45               | –      | ns            | 27, 32 |
| DQ and DM input pulse width (for each input)             | $t_{DIPW}$  | 1.75               | –      | ns            | 32     |
| Access window of DQS from CK/CK#                         | $t_{DQSCK}$ | -0.6               | 0.6    | ns            |        |
| DQS input high pulse width                               | $t_{DQSH}$  | 0.35               | –      | $t_{CK}$      |        |
| DQS input low pulse width                                | $t_{DQL}$   | 0.35               | –      | $t_{CK}$      |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | $t_{DQSQ}$  | –                  | 0.4    | ns            | 26, 27 |
| WRITE command to first DQS latching transition           | $t_{DQSS}$  | 0.75               | 1.25   | $t_{CK}$      |        |
| DQ and DM input setup time relative to DQS               | $t_{DS}$    | 0.45               | –      | ns            | 27, 32 |
| DQS falling edge from CK rising - hold time              | $t_{DSH}$   | 0.2                | –      | $t_{CK}$      |        |
| DQS falling edge to CK rising - setup time               | $t_{DSS}$   | 0.2                | –      | $t_{CK}$      |        |
| Half-clock period  | $t_{HP}$    | $t_{CH}, t_{CL}$   | –      | ns            | 35     |
| Data-out High-Z window from CK/CK#                       | $t_{HZ}$    | –                  | 0.7    | ns            | 19, 43 |
| Address and control input hold time (fast slew rate)     | $t_{IH_F}$  | 0.75               | –      | ns            |        |
| Address and control input hold time (slow slew rate)     | $t_{IH_S}$  | 0.8                | –      | ns            | 15     |
| Address and control input pulse width (for each input)   | $t_{IPW}$   | 2.2                | –      | ns            |        |
| Address and control input setup time (fast slew rate)    | $t_{IS_F}$  | 0.75               | –      | ns            |        |
| Address and control input setup time (slow slew rate)    | $t_{IS_S}$  | 0.8                | –      | ns            | 15     |
| Data-out Low-Z window from CK/CK#                        | $t_{LZ}$    | -0.7               | –      | ns            | 19, 43 |
| LOAD MODE REGISTER command cycle time                    | $t_{MRD}$   | 12                 | –      | ns            |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{QH}$    | $t_{HP} - t_{QHS}$ | –      | ns            | 26, 27 |
| Data hold skew factor                                    | $t_{QHS}$   | –                  | 0.50   | ns            |        |
| ACTIVE-to-READ with auto precharge command               | $t_{RAP}$   | 15                 | –      | ns            |        |
| ACTIVE-to-PRECHARGE command                              | $t_{RAS}$   | 42                 | 70,000 | ns            | 36, 54 |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period             | $t_{RC}$    | 60                 | –      | ns            | 55     |
| ACTIVE-to-READ or WRITE delay                            | $t_{RCD}$   | 15                 | –      | ns            |        |
| REFRESH-to-REFRESH command interval                      | $t_{REFC}$  | –                  | 70.3   | $\mu\text{s}$ | 24     |
| Average periodic refresh interval                        | $t_{REFI}$  | –                  | 7.8    | $\mu\text{s}$ | 24     |
| AUTO REFRESH command period                              | $t_{RFC}$   | 72                 | –      | ns            | 50     |
| PRECHARGE command period                                 | $t_{RP}$    | 15                 | –      | ns            |        |
| DQS read preamble  | $t_{RPRE}$  | 0.9                | 1.1    | $t_{CK}$      | 44     |
| DQS read postamble                                       | $t_{RPST}$  | 0.4                | 0.6    | $t_{CK}$      | 44     |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command     | $t_{RRD}$   | 12                 | –      | ns            |        |
| Terminating voltage delay to $V_{SS}$                    | $t_{VTD}$   | 0                  | –      | ns            |        |
| DQS write preamble                                       | $t_{WPRE}$  | 0.25               | –      | $t_{CK}$      |        |
| DQS write preamble setup time                            | $t_{WPRES}$ | 0                  | –      | ns            | 21, 22 |
| DQS write postamble                                      | $t_{WPST}$  | 0.4                | 0.6    | $t_{CK}$      | 20     |
| Write recovery time                                      | $t_{WR}$    | 15                 | –      | ns            |        |

**Table 21: Electrical Characteristics and Recommended AC Operating Conditions (-6) (continued)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                    |                   | -6 (FBGA)                         |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Internal WRITE-to-READ command delay  | $t_{\text{WTR}}$  | 1                                 | –   | $t_{\text{CK}}$ |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 75                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ | –   | ns              | 26    |

**Table 22: Electrical Characteristics and Recommended AC Operating Conditions (-6T)**

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                                       |               | -6T (TSOP)         |        | Units         | Notes  |
|--|---------------|--------------------|--------|---------------|--------|
| Parameter  | Symbol        | Min                | Max    |               |        |
| Access window of DQ from CK/CK#                          | $t_{AC}$      | -0.70              | 0.70   | ns            |        |
| CK high-level width                                      | $t_{CH}$      | 0.45               | 0.55   | $t_{CK}$      | 31     |
| Clock cycle time   | $t_{CK}(2.5)$ | 6                  | 13     | ns            | 46, 52 |
|  | $t_{CK}(2)$   | 7.5                | 13     | ns            | 46, 52 |
| CK low-level width                                       | $t_{CL}$      | 0.45               | 0.55   | $t_{CK}$      | 31     |
| DQ and DM input hold time relative to DQS                | $t_{DH}$      | 0.45               | –      | ns            | 27, 32 |
| DQ and DM input pulse width (for each input)             | $t_{DIPW}$    | 1.75               | –      | ns            | 32     |
| Access window of DQS from CK/CK#                         | $t_{DQSCK}$   | -0.6               | 0.6    | ns            |        |
| DQS input high pulse width                               | $t_{DQSH}$    | 0.35               | –      | $t_{CK}$      |        |
| DQS input low pulse width                                | $t_{DQL}$     | 0.35               | –      | $t_{CK}$      |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | $t_{DQSQ}$    | –                  | 0.45   | ns            | 26, 27 |
| WRITE command to first DQS latching transition           | $t_{DQSS}$    | 0.75               | 1.25   | $t_{CK}$      |        |
| DQ and DM input setup time relative to DQS               | $t_{DS}$      | 0.45               | –      | ns            | 27, 32 |
| DQS falling edge from CK rising - hold time              | $t_{DSH}$     | 0.2                | –      | $t_{CK}$      |        |
| DQS falling edge to CK rising - setup time               | $t_{DSS}$     | 0.2                | –      | $t_{CK}$      |        |
| Half-clock period  | $t_{HP}$      | $t_{CH}, t_{CL}$   | –      | ns            | 35     |
| Data-out High-Z window from CK/CK#                       | $t_{HZ}$      | –                  | 0.7    | ns            | 19, 43 |
| Address and control input hold time (fast slew rate)     | $t_{IH_F}$    | 0.75               | –      | ns            |        |
| Address and control input hold time (slow slew rate)     | $t_{IH_S}$    | 0.8                | –      | ns            | 15     |
| Address and control input pulse width (for each input)   | $t_{IPW}$     | 2.2                | –      | ns            |        |
| Address and control input setup time (fast slew rate)    | $t_{IS_F}$    | 0.75               | –      | ns            |        |
| Address and control input setup time (slow slew rate)    | $t_{IS_S}$    | 0.8                | –      | ns            | 15     |
| Data-out Low-Z window from CK/CK#                        | $t_{LZ}$      | -0.7               | –      | ns            | 19, 43 |
| LOAD MODE REGISTER command cycle time                    | $t_{MRD}$     | 12                 | –      | ns            |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{QH}$      | $t_{HP} - t_{QHS}$ | –      | ns            | 26, 27 |
| Data hold skew factor                                    | $t_{QHS}$     | –                  | 0.55   | ns            |        |
| ACTIVE-to-READ with auto precharge command               | $t_{RAP}$     | 15                 | –      | ns            |        |
| ACTIVE-to-PRECHARGE command                              | $t_{RAS}$     | 42                 | 70,000 | ns            | 36, 54 |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period             | $t_{RC}$      | 60                 | –      | ns            | 55     |
| ACTIVE-to-READ or WRITE delay                            | $t_{RCD}$     | 15                 | –      | ns            |        |
| REFRESH-to-REFRESH command interval                      | $t_{REFC}$    | –                  | 70.3   | $\mu\text{s}$ | 24     |
| Average periodic refresh interval                        | $t_{REFI}$    | –                  | 7.8    | $\mu\text{s}$ | 24     |
| AUTO REFRESH command period                              | $t_{RFC}$     | 72                 | –      | ns            | 50     |
| PRECHARGE command period                                 | $t_{RP}$      | 15                 | –      | ns            |        |
| DQS read preamble  | $t_{RPRE}$    | 0.9                | 1.1    | $t_{CK}$      | 44     |
| DQS read postamble                                       | $t_{RPST}$    | 0.4                | 0.6    | $t_{CK}$      | 44     |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command     | $t_{RRD}$     | 12                 | –      | ns            |        |
| Terminating voltage delay to $V_{SS}$                    | $t_{VTD}$     | 0                  | –      | ns            |        |
| DQS write preamble                                       | $t_{WPRE}$    | 0.25               | –      | $t_{CK}$      |        |
| DQS write preamble setup time                            | $t_{WPRES}$   | 0                  | –      | ns            | 21, 22 |
| DQS write postamble                                      | $t_{WPST}$    | 0.4                | 0.6    | $t_{CK}$      | 20     |

**Table 22: Electrical Characteristics and Recommended AC Operating Conditions (-6T) (continued)**

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                    |                   | -6T (TSOP)                        |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Write recovery time                   | $t_{\text{WR}}$   | 15                                | –   | ns              |       |
| Internal WRITE-to-READ command delay  | $t_{\text{WTR}}$  | 1                                 | –   | $t_{\text{CK}}$ |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 75                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ |     | ns              | 26    |

**Table 23: Electrical Characteristics and Recommended AC Operating Conditions (-75E)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                                       |                      | -75E                             |         | Units           | Notes  |
|--|----------------------|----------------------------------|---------|-----------------|--------|
| Parameter  | Symbol               | Min                              | Max     |                 |        |
| Access window of DQ from CK/CK#                          | $t_{\text{AC}}$      | -0.75                            | 0.75    | ns              |        |
| CK high-level width                                      | $t_{\text{CH}}$      | 0.45                             | 0.55    | $t_{\text{CK}}$ | 31     |
| Clock cycle time   | $t_{\text{CK}}(2.5)$ | 7.5                              | 13      | ns              | 46, 52 |
|  | $t_{\text{CK}}(2)$   | 7.5                              | 13      | ns              | 46, 52 |
| CK low-level width                                       | $t_{\text{CL}}$      | 0.45                             | 0.55    | $t_{\text{CK}}$ | 31     |
| DQ and DM input hold time relative to DQS                | $t_{\text{DH}}$      | 0.5                              | –       | ns              | 27, 32 |
| DQ and DM input pulse width (for each input)             | $t_{\text{DIPW}}$    | 1.75                             | –       | ns              | 32     |
| Access window of DQS from CK/CK#                         | $t_{\text{DQSCK}}$   | -0.75                            | 0.75    | ns              |        |
| DQS input high pulse width                               | $t_{\text{DQSH}}$    | 0.35                             | –       | $t_{\text{CK}}$ |        |
| DQS input low pulse width                                | $t_{\text{DQL}}$     | 0.35                             | –       | $t_{\text{CK}}$ |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | $t_{\text{DQSQ}}$    | –                                | 0.5     | ns              | 26, 27 |
| WRITE command to first DQS latching transition           | $t_{\text{DQSS}}$    | 0.75                             | 1.25    | $t_{\text{CK}}$ |        |
| DQ and DM input setup time relative to DQS               | $t_{\text{DS}}$      | 0.5                              | –       | ns              | 27, 32 |
| DQS falling edge from CK rising - hold time              | $t_{\text{DSH}}$     | 0.2                              | –       | $t_{\text{CK}}$ |        |
| DQS falling edge to CK rising - setup time               | $t_{\text{DSS}}$     | 0.2                              | –       | $t_{\text{CK}}$ |        |
| Half-clock period  | $t_{\text{HP}}$      | $t_{\text{CH}}, t_{\text{CL}}$   | –       | ns              | 35     |
| Data-out High-Z window from CK/CK#                       | $t_{\text{HZ}}$      | –                                | 0.75    | ns              | 19, 43 |
| Address and control input hold time (fast slew rate)     | $t_{\text{IH}_F}$    | 0.90                             | –       | ns              |        |
| Address and control input hold time (slow slew rate)     | $t_{\text{IH}_S}$    | 1                                | –       | ns              | 15     |
| Address and control input pulse width (for each input)   | $t_{\text{IPW}}$     | 2.2                              | –       | ns              |        |
| Address and control input setup time (fast slew rate)    | $t_{\text{IS}_F}$    | 0.90                             | –       | ns              |        |
| Address and control input setup time (slow slew rate)    | $t_{\text{IS}_S}$    | 1                                | –       | ns              | 15     |
| Data-out Low-Z window from CK/CK#                        | $t_{\text{LZ}}$      | -0.75                            | –       | ns              | 19, 43 |
| LOAD MODE REGISTER command cycle time                    | $t_{\text{MRD}}$     | 15                               | –       | ns              |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{\text{QH}}$      | $t_{\text{HP}} - t_{\text{QHS}}$ | –       | ns              | 26, 27 |
| Data hold skew factor                                    | $t_{\text{QHS}}$     | –                                | 0.75    | ns              |        |
| ACTIVE-to-READ with auto precharge command               | $t_{\text{RAP}}$     | 15                               | –       | ns              |        |
| ACTIVE-to-PRECHARGE command                              | $t_{\text{RAS}}$     | 40                               | 120,000 | ns              | 36, 54 |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period             | $t_{\text{RC}}$      | 60                               | –       | ns              | 55     |
| ACTIVE-to-READ or WRITE delay                            | $t_{\text{RCD}}$     | 15                               | –       | ns              |        |
| REFRESH-to-REFRESH command interval                      | $t_{\text{REFC}}$    | –                                | 70.3    | $\mu\text{s}$   | 24     |
| Average periodic refresh interval                        | $t_{\text{REFI}}$    | –                                | 7.8     | $\mu\text{s}$   | 24     |
| AUTO REFRESH command period                              | $t_{\text{RFC}}$     | 75                               | –       | ns              | 50     |
| PRECHARGE command period                                 | $t_{\text{RP}}$      | 15                               | –       | ns              |        |
| DQS read preamble  | $t_{\text{RPRE}}$    | 0.9                              | 1.1     | $t_{\text{CK}}$ | 44     |
| DQS read postamble                                       | $t_{\text{RPST}}$    | 0.4                              | 0.6     | $t_{\text{CK}}$ | 44     |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command     | $t_{\text{RRD}}$     | 15                               | –       | ns              |        |
| Terminating voltage delay to $V_{\text{SS}}$             | $t_{\text{VTD}}$     | 0                                | –       | ns              |        |
| DQS write preamble                                       | $t_{\text{WPRE}}$    | 0.25                             | –       | $t_{\text{CK}}$ |        |
| DQS write preamble setup time                            | $t_{\text{WPRES}}$   | 0                                | –       | ns              | 21, 22 |
| DQS write postamble                                      | $t_{\text{WPST}}$    | 0.4                              | 0.6     | $t_{\text{CK}}$ | 20     |

**Table 23: Electrical Characteristics and Recommended AC Operating Conditions (-75E) (continued)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                    |                   | -75E                              |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Write recovery time                   | $t_{\text{WR}}$   | 15                                | –   | ns              |       |
| Internal WRITE-to-READ command delay  | $t_{\text{WTR}}$  | 1                                 | –   | $t_{\text{CK}}$ |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 75                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ |     | ns              | 26    |

**Table 24: Electrical Characteristics and Recommended AC Operating Conditions (-75Z)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$

| AC Characteristics                                       |               | -75Z               |         | Units         | Notes  |
|--|---------------|--------------------|---------|---------------|--------|
| Parameter  | Symbol        | Min                | Max     |               |        |
| Access window of DQ from CK/CK#                          | $t_{AC}$      | -0.75              | 0.75    | ns            |        |
| CK high-level width                                      | $t_{CH}$      | 0.45               | 0.55    | $t_{CK}$      | 31     |
| Clock cycle time   | $t_{CK}(2.5)$ | 7.5                | 13      | ns            | 46     |
|  | $t_{CK}(2)$   | 7.5                | 13      | ns            | 46     |
| CK low-level width                                       | $t_{CL}$      | 0.45               | 0.55    | $t_{CK}$      | 31     |
| DQ and DM input hold time relative to DQS                | $t_{DH}$      | 0.5                | –       | ns            | 27, 32 |
| DQ and DM input pulse width (for each input)             | $t_{DIPW}$    | 1.75               | –       | ns            | 32     |
| Access window of DQS from CK/CK#                         | $t_{DQSCK}$   | -0.75              | 0.75    | ns            |        |
| DQS input high pulse width                               | $t_{DQSH}$    | 0.35               | –       | $t_{CK}$      |        |
| DQS input low pulse width                                | $t_{DQL}$     | 0.35               | –       | $t_{CK}$      |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | $t_{DQSQ}$    | –                  | 0.5     | ns            | 26, 27 |
| WRITE command-to-first DQS latching transition           | $t_{DQSS}$    | 0.75               | 1.25    | $t_{CK}$      |        |
| DQ and DM input setup time relative to DQS               | $t_{DS}$      | 0.5                | –       | ns            | 27, 32 |
| DQS falling edge from CK rising – hold time              | $t_{DSH}$     | 0.2                | –       | $t_{CK}$      |        |
| DQS falling edge to CK rising – setup time               | $t_{DSS}$     | 0.2                | –       | $t_{CK}$      |        |
| Half-clock period  | $t_{HP}$      | $t_{CH}, t_{CL}$   | –       | ns            | 35     |
| Data-out High-Z window from CK/CK#                       | $t_{HZ}$      | –                  | 0.75    | ns            | 19, 43 |
| Address and control input hold time (fast slew rate)     | $t_{IH_F}$    | 0.90               | –       | ns            |        |
| Address and control input hold time (slow slew rate)     | $t_{IH_S}$    | 1                  | –       | ns            | 15     |
| Address and control input pulse width (for each input)   | $t_{IPW}$     | 2.2                | –       | ns            |        |
| Address and control input setup time (fast slew rate)    | $t_{IS_F}$    | 0.90               | –       | ns            |        |
| Address and control input setup time (slow slew rate)    | $t_{IS_S}$    | 1                  | –       | ns            | 15     |
| Data-out Low-Z window from CK/CK#                        | $t_{LZ}$      | -0.75              | –       | ns            | 19, 43 |
| LOAD MODE REGISTER command cycle time                    | $t_{MRD}$     | 15                 | –       | ns            |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{QH}$      | $t_{HP} - t_{QHS}$ | –       | ns            | 26, 27 |
| Data hold skew factor                                    | $t_{QHS}$     | –                  | 0.75    | ns            |        |
| ACTIVE-to-READ with auto precharge command               | $t_{RAP}$     | 20                 | –       | ns            |        |
| ACTIVE-to-PRECHARGE command                              | $t_{RAS}$     | 40                 | 120,000 | ns            | 36     |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period             | $t_{RC}$      | 65                 | –       | ns            | 55     |
| ACTIVE-to-READ or WRITE delay                            | $t_{RCD}$     | 20                 | –       | ns            |        |
| REFRESH-to-REFRESH command interval                      | $t_{REFC}$    | –                  | 70.3    | $\mu\text{s}$ | 24     |
| Average periodic refresh interval                        | $t_{REFI}$    | –                  | 7.8     | $\mu\text{s}$ | 24     |
| AUTO REFRESH command period                              | $t_{RFC}$     | 75                 | –       | ns            | 50     |
| PRECHARGE command period                                 | $t_{RP}$      | 20                 | –       | ns            |        |
| DQS read preamble  | $t_{RPRE}$    | 0.9                | 1.1     | $t_{CK}$      | 44     |
| DQS read postamble                                       | $t_{RPST}$    | 0.4                | 0.6     | $t_{CK}$      | 44     |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command     | $t_{RRD}$     | 15                 | –       | ns            |        |
| Terminating voltage delay to $V_{DD}$                    | $t_{VTD}$     | 0                  | –       | ns            |        |
| DQS write preamble                                       | $t_{WPRE}$    | 0.25               | –       | $t_{CK}$      |        |
| DQS write preamble setup time                            | $t_{WPRES}$   | 0                  | –       | ns            | 21, 22 |
| DQS write postamble                                      | $t_{WPST}$    | 0.4                | 0.6     | $t_{CK}$      | 20     |
| Write recovery time                                      | $t_{WR}$      | 15                 | –       | ns            |        |

**Table 24: Electrical Characteristics and Recommended AC Operating Conditions (-75Z) (continued)**

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                    |                   | -75Z                              |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Internal WRITE-to-READ command delay  | $t_{\text{WTR}}$  | 1                                 | –   | $t_{\text{CK}}$ |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 75                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ | –   | ns              | 26    |

**Table 25: Electrical Characteristics and Recommended AC Operating Conditions (-75)**

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;

 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ 

| AC Characteristics                                       |               | -75                |         | Units         | Notes  |
|--|---------------|--------------------|---------|---------------|--------|
| Parameter  | Symbol        | Min                | Max     |               |        |
| Access window of DQ from CK/CK#                          | $t_{AC}$      | -0.75              | 0.75    | ns            |        |
| CK high-level width                                      | $t_{CH}$      | 0.45               | 0.55    | $t_{CK}$      | 31     |
| Clock cycle time   | $t_{CK}(2.5)$ | 7.5                | 13      | ns            | 46     |
|  | $t_{CK}(2)$   | 10                 | 13      | ns            | 46     |
| CK low-level width                                       | $t_{CL}$      | 0.45               | 0.55    | $t_{CK}$      | 31     |
| DQ and DM input hold time relative to DQS                | $t_{DH}$      | 0.5                | –       | ns            | 27, 32 |
| DQ and DM input pulse width (for each input)             | $t_{DIPW}$    | 1.75               | –       | ns            | 32     |
| Access window of DQS from CK/CK#                         | $t_{DQSCK}$   | -0.75              | 0.75    | ns            |        |
| DQS input high pulse width                               | $t_{DQSH}$    | 0.35               | –       | $t_{CK}$      |        |
| DQS input low pulse width                                | $t_{DQL}$     | 0.35               | –       | $t_{CK}$      |        |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | $t_{DQSQ}$    | –                  | 0.5     | ns            | 26, 27 |
| WRITE command-to-first DQS latching transition           | $t_{DQSS}$    | 0.75               | 1.25    | $t_{CK}$      |        |
| DQ and DM input setup time relative to DQS               | $t_{DS}$      | 0.5                | –       | ns            | 27, 32 |
| DQS falling edge from CK rising – hold time              | $t_{DSH}$     | 0.2                | –       | $t_{CK}$      |        |
| DQS falling edge to CK rising – setup time               | $t_{DSS}$     | 0.2                | –       | $t_{CK}$      |        |
| Half-clock period  | $t_{HP}$      | $t_{CH}, t_{CL}$   | –       | ns            | 35     |
| Data-out High-Z window from CK/CK#                       | $t_{HZ}$      | –                  | 0.75    | ns            | 19, 43 |
| Address and control input hold time (fast slew rate)     | $t_{IH_F}$    | 0.90               | –       | ns            |        |
| Address and control input hold time (slow slew rate)     | $t_{IH_S}$    | 1                  | –       | ns            | 15     |
| Address and control input pulse width (for each input)   | $t_{IPW}$     | 2.2                | –       | ns            |        |
| Address and control input setup time (fast slew rate)    | $t_{IS_F}$    | 0.90               | –       | ns            |        |
| Address and control input setup time (slow slew rate)    | $t_{IS_S}$    | 1                  | –       | ns            | 15     |
| Data-out Low-Z window from CK/CK#                        | $t_{LZ}$      | -0.75              | –       | ns            | 19, 43 |
| LOAD MODE REGISTER command cycle time                    | $t_{MRD}$     | 15                 | –       | ns            |        |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{QH}$      | $t_{HP} - t_{QHS}$ | –       | ns            | 26, 27 |
| Data hold skew factor                                    | $t_{QHS}$     | –                  | 0.75    | ns            |        |
| ACTIVE-to-READ with auto precharge command               | $t_{RAP}$     | 20                 | –       | ns            |        |
| ACTIVE-to-PRECHARGE command                              | $t_{RAS}$     | 40                 | 120,000 | ns            | 36     |
| ACTIVE-to-ACTIVE/AUTO REFRESH command period             | $t_{RC}$      | 65                 | –       | ns            | 55     |
| ACTIVE-to-READ or WRITE delay                            | $t_{RCD}$     | 20                 | –       | ns            |        |
| REFRESH-to-REFRESH command interval                      | $t_{REFC}$    | –                  | 70.3    | $\mu\text{s}$ | 24     |
| Average periodic refresh interval                        | $t_{REFI}$    | –                  | 7.8     | $\mu\text{s}$ | 24     |
| AUTO REFRESH command period                              | $t_{RFC}$     | 75                 | –       | ns            | 50     |
| PRECHARGE command period                                 | $t_{RP}$      | 20                 | –       | ns            |        |
| DQS read preamble  | $t_{RPRE}$    | 0.9                | 1.1     | $t_{CK}$      | 44     |
| DQS read postamble                                       | $t_{RPST}$    | 0.4                | 0.6     | $t_{CK}$      | 44     |
| ACTIVE bank a to ACTIVE bank b command                   | $t_{RRD}$     | 15                 | –       | ns            |        |
| Terminating voltage delay to $V_{DD}$                    | $t_{VTD}$     | 0                  | –       | ns            |        |
| DQS write preamble                                       | $t_{WPRE}$    | 0.25               | –       | $t_{CK}$      |        |
| DQS write preamble setup time                            | $t_{WPRES}$   | 0                  | –       | ns            | 21, 22 |
| DQS write postamble                                      | $t_{WPST}$    | 0.4                | 0.6     | $t_{CK}$      | 20     |
| Write recovery time                                      | $t_{WR}$      | 15                 | –       | ns            |        |

**Table 25: Electrical Characteristics and Recommended AC Operating Conditions (-75) (continued)**

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| AC Characteristics                    |                   | -75                               |     | Units           | Notes |
|---------------------------------------|-------------------|-----------------------------------|-----|-----------------|-------|
| Parameter                             | Symbol            | Min                               | Max |                 |       |
| Internal WRITE-to-READ command delay  | $t_{\text{WTR}}$  | 1                                 | –   | $t_{\text{CK}}$ |       |
| Exit SELF REFRESH-to-non-READ command | $t_{\text{XSNR}}$ | 75                                | –   | ns              |       |
| Exit SELF REFRESH-to-READ command     | $t_{\text{XSRD}}$ | 200                               | –   | $t_{\text{CK}}$ |       |
| Data valid output window              | n/a               | $t_{\text{QH}} - t_{\text{DQSQ}}$ | –   | ns              | 26    |

**Table 26: Input Slew Rate Derating Values for Addresses and Commands**

Note: 15 applies to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| Speed     | Slew Rate  | $t_{\text{IS}}$ | $t_{\text{IH}}$ | Units |
|-----------|------------|-----------------|-----------------|-------|
| -75Z/-75E | 0.500 V/ns | 1.00            | 1               | ns    |
| -75Z/-75E | 0.400 V/ns | 1.05            | 1               | ns    |
| -75Z/-75E | 0.300 V/ns | 1.10            | 1               | ns    |

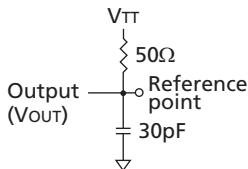
**Table 27: Input Slew Rate Derating Values for DQ, DQS, and DM**

Note: 32 applies to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{\text{DD}} = 2.5\text{V} \pm 0.2\text{V}$

| Speed     | Slew Rate  | $t_{\text{DS}}$ | $t_{\text{DH}}$ | Units |
|-----------|------------|-----------------|-----------------|-------|
| -75Z/-75E | 0.500 V/ns | 0.50            | 0.50            | ns    |
| -75Z/-75E | 0.400 V/ns | 0.55            | 0.55            | ns    |
| -75Z/-75E | 0.300 V/ns | 0.60            | 0.60            | ns    |

## Notes

1. All voltages referenced to  $V_{SS}$ .
2. Tests for AC timing,  $I_{DD}$ , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the device operation are guaranteed for the full voltage range specified.
3. Outputs (except for  $I_{DD}$  measurements) measured with equivalent load:

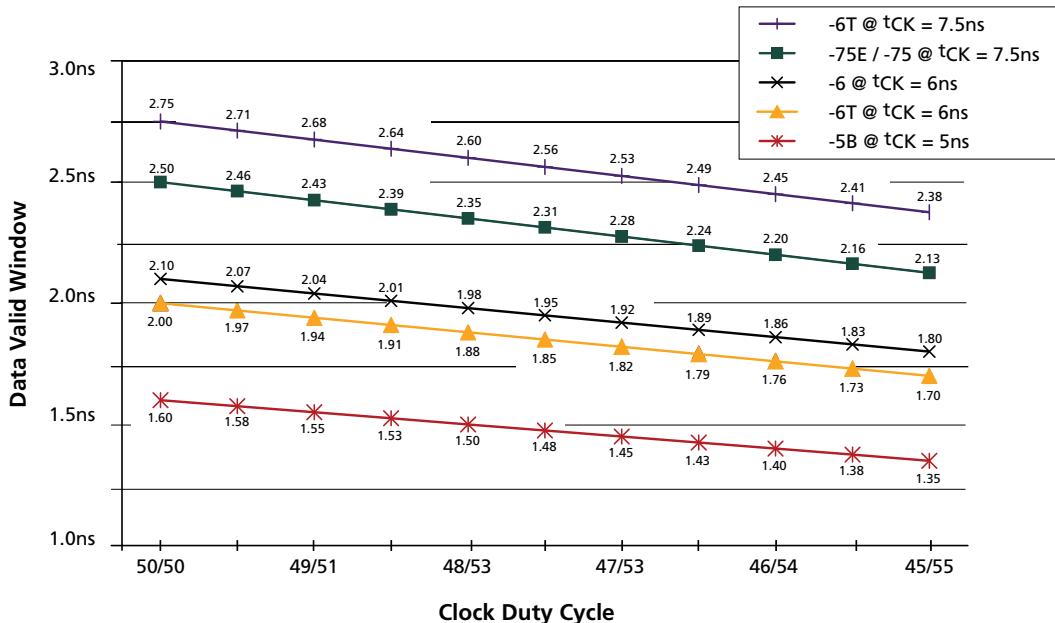


4. AC timing and  $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 1.5V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1 V/ns in the range between  $V_{IL(AC)}$  and  $V_{IH(AC)}$ .
5. The AC and DC input level specifications are as defined in the SSTL\_2 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. All speed grades are not offered on all densities. Refer to page 1 for availability.
7.  $V_{REF}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on  $V_{REF}$  may not exceed  $\pm 2\%$  of the DC value. Thus, from  $V_{DDQ}/2$ ,  $V_{REF}$  is allowed  $\pm 25\text{mV}$  for DC error and an additional  $\pm 25\text{mV}$  for AC noise. This measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.
8.  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, it is expected to be set equal to  $V_{REF}$  and it must track variations in the DC level of  $V_{REF}$ .
9.  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of  $V_{IX}$  and  $V_{MP}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and must track variations in the DC level of the same.
11.  $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle times at CL = 3 for -5B; CL = 2.5, -6/-6T/-75; and CL = 2, -75E/-75Z speeds with the outputs open.
12. Enables on-chip refresh and address counters.
13.  $I_{DD}$  specifications are tested after the device is properly initialized and is averaged at the defined cycle rate.
14. This parameter is sampled.  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{REF} = V_{SS}$ ,  $f = 100\text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
15. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated:  $t_{IS}$  has an additional 50ps per each 100 mV/ns reduction in slew rate from the 500 mV/ns.  $t_{IH}$  has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain. For -5B, -6, and -6T, slew rates must be greater than or equal to 0.5 V/ns.

16. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is  $V_{REF}$ .
17. Inputs are not recognized as valid until  $V_{REF}$  stabilizes. Once initialized, including self refresh mode,  $V_{REF}$  must be powered within specified range. Exception: during the period before  $V_{REF}$  stabilizes,  $CKE < 0.3 \times V_{DD}$  is recognized as LOW.
18. The output timing reference level, as measured at the timing reference point (indicated in Note 3), is  $V_{TT}$ .
19.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (High-Z) or begins driving (Low-Z).
20. The intent of the “Don’t Care” state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above  $V_{IH(DC)min}$ ) then it must not transition LOW (below  $V_{IH(DC)}$  prior to  $t_{DQSH} [MIN]$ ).
21. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
22. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on  $t_{DQSS}$ .
23. MIN ( $t_{RC}$  or  $t_{RFC}$ ) for  $I_{DD}$  measurements is the smallest multiple of  $t_{CK}$  that meets the minimum absolute value for the respective parameter.  $t_{RAS} (\text{MAX})$  for  $I_{DD}$  measurements is the largest multiple of  $t_{CK}$  that meets the maximum absolute value for  $t_{RAS}$ .
24. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 $\mu$ s; burst refreshing or posting by the DRAM controller greater than 8 REFRESH cycles is not allowed.
25. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
26. The data valid window is derived by achieving other specifications:  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, because functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided in Figure 13 on page 39 for duty cycles ranging between 50/50 and 45/55.
27. Referenced to each output group: x4 = DQS with DQ[3:0]; x8 = DQS with DQ[7:0]; x16 = LDQS with DQ[7:0] and UDQS with DQ[15:8].
28. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during the REFRESH command period ( $t_{RFC} [\text{MIN}]$ ), else CKE is LOW (that is, during standby).
29. To maintain a valid level, the transitioning edge of the input must:
  - 29a. Sustain a constant slew rate from the current AC level through to the target AC level,  $V_{IL(AC)}$  or  $V_{IH(AC)}$ .
  - 29b. Reach at least the target AC level.
  - 29c. After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL(DC)}$  or  $V_{IH(DC)}$ .

30. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
31. CK and CK# input slew rate must be  $\geq 1$  V/ns ( $\geq 2$  V/ns if measured differentially).

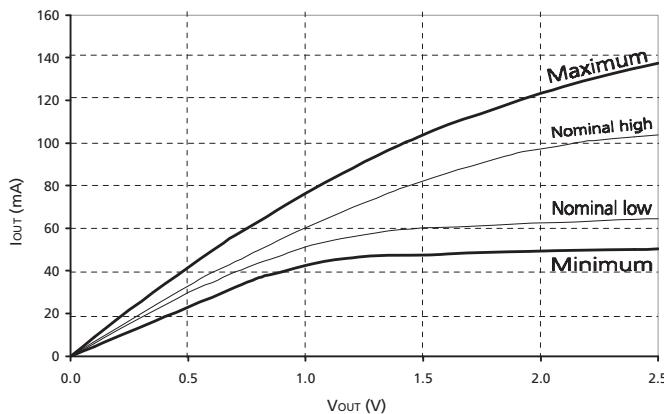
**Figure 13: Derating Data Valid Window ( $t_{QH} - t_{DQSQ}$ )**



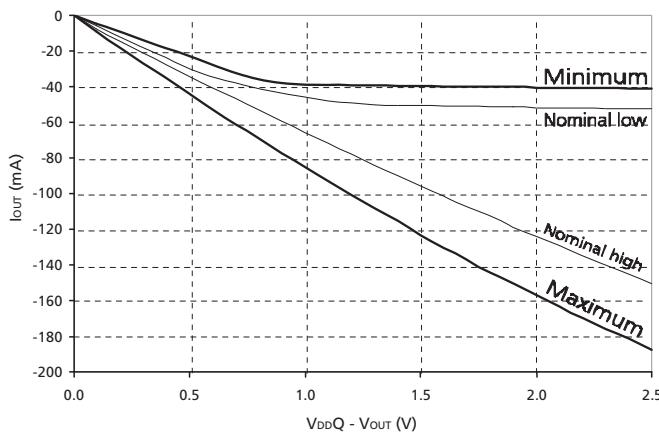
32. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each 100 mV/ns reduction in slew rate. For -5B, -6, and -6T speed grades, the slew rate must be  $\geq 0.5$  V/ns. If the slew rate exceeds 4 V/ns, functionality is uncertain.
33.  $V_{DD}$  must not vary more than 4% if CKE is not active while any bank is active.
34. The clock is allowed up to  $\pm 150$ ps of jitter. Each timing parameter is allowed to vary by the same amount.
35.  $t_{HP}$  (MIN) is the lesser of  $t_{CL}$  (MIN) and  $t_{CH}$  (MIN) actually applied to the device CK and CK# inputs, collectively, during bank active.
36. READs and WRITEs with auto precharge are not allowed to be issued until  $t_{RAS}$  (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
37. Any positive glitch must be less than 1/3 of the clock cycle and not more than 400mV or 2.9V (300mV or 2.9V maximum for -5B), whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V (2.4V for -5B), whichever is more positive. The average cannot be below the 2.5V (2.6V for -5B) minimum.
38. Normal output drive curves:
  - 38a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 14 on page 40.
  - 38b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 14 on page 40.

- 38c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 15 on page 40.
- 38d. The driver pull-up current variation within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 15 on page 40.
- 38e. The full ratio variation of MAX to MIN pull-up and pull-down current should be between 0.71 and 1.4 for drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.
- 38f. The full ratio variation of the nominal pull-up to pull-down current should be unity  $\pm 10\%$  for device drain-to-source voltages from 0.1V to 1.0V.

**Figure 14: Full Drive Pull-Down Characteristics**



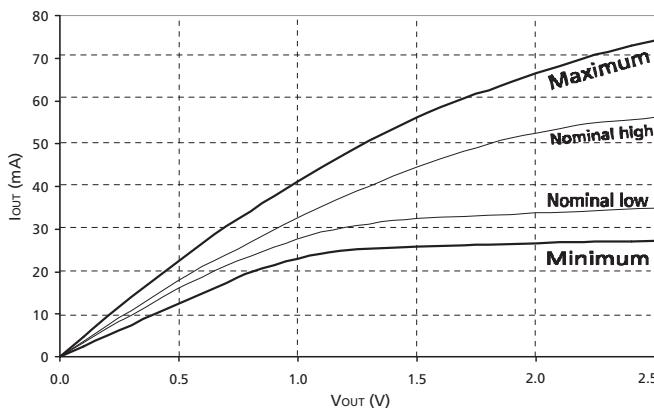
**Figure 15: Full Drive Pull-Up Characteristics**



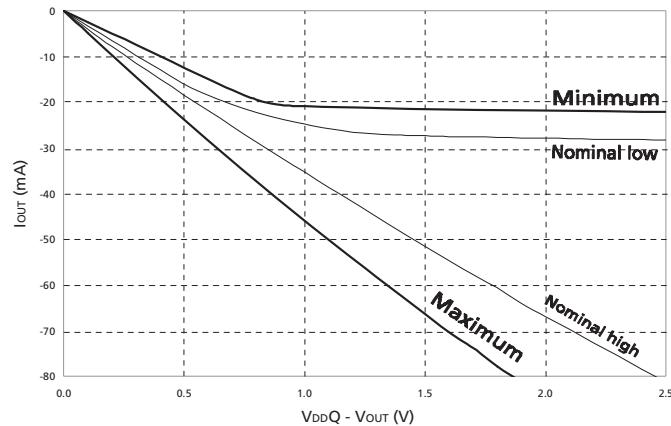
- 39. Reduced output drive curves:
- 39a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 16 on page 41.
- 39b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 16 on page 41.
- 39c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 17.

- 39d. The driver pull-up current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 17 on page 41.
- 39e. The full ratio variation of the MAX-to-MIN pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.
- 39f. The full ratio variation of the nominal pull-up to pull-down current should be unity  $\pm 10\%$ , for device drain-to-source voltages from 0.1V to 1.0V.

**Figure 16: Reduced Drive Pull-Down Characteristics**



**Figure 17: Reduced Drive Pull-Up Characteristics**



- 40. The voltage levels used are derived from a minimum  $V_{DD}$  level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
- 41.  $V_{IH}$  overshoot:  $V_{IH,max} = V_{DDQ} + 1.5V$  for a pulse width  $\leq 3ns$ , and the pulse width can not be greater than 1/3 of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL,min} = -1.5V$  for a pulse width  $\leq 3ns$ , and the pulse width can not be greater than 1/3 of the cycle rate.
- 42.  $V_{DD}$  and  $V_{DDQ}$  must track each other.
- 43.  $t_{HZ}^{MAX}$  will prevail over  $t_{DQSCK}^{MAX} + t_{RPST}^{MAX}$  condition.  $t_{LZ}^{MIN}$  will prevail over  $t_{DQSCK}^{MIN} + t_{RPRE}^{MAX}$  condition.

44.  $t_{RPST}$  end point and  $t_{RPRE}$  begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ( $t_{RPST}$ ) or begins driving ( $t_{RPRE}$ ).
45. During initialization,  $V_{DDQ}$ ,  $V_{TT}$ , and  $V_{REF}$  must be equal to or less than  $V_{DD} + 0.3V$ . Alternatively,  $V_{TT}$  may be 1.35V maximum during power-up, even if  $V_{DD}/V_{DDQ}$  are 0V, provided a minimum of  $42\Omega$  of series resistance is used between the  $V_{TT}$  supply and the input pin.
46. The current Micron part operates below 83 MHz (slowest specified JEDEC operating frequency). As such, future die may not reflect this option.
47. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
48. Random address is changing; 50% of data is changing at every transfer.
49. Random address is changing; 100% of data is changing at every transfer.
50. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{RFC}$  has been satisfied.
51.  $I_{DD2N}$  specifies the DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.  $I_{DD2Q}$  is similar to  $I_{DD2F}$  except  $I_{DD2Q}$  specifies the address and control inputs to remain stable. Although  $I_{DD2F}$ ,  $I_{DD2N}$ , and  $I_{DD2Q}$  are similar,  $I_{DD2F}$  is “worst case.”
52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset followed by 200 clock cycles before any READ command.
53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM generated from any source other than that of the DRAM itself may not exceed the DC voltage range of  $2.6V \pm 100mV$ .
54. The -6/-6T speed grades will operate with  $t_{RAS}(\text{MIN}) = 40ns$  and  $t_{RAS}(\text{MAX}) = 120,000ns$  at any slower frequency.
55. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

**Table 28: Normal Output Drive Characteristics**

Characteristics are specified under best, worst, and nominal process variation/conditions

| Voltage (V) | Pull-Down Current (mA) |              |      |       | Pull-Up Current (mA) |              |       |        |
|-------------|------------------------|--------------|------|-------|----------------------|--------------|-------|--------|
|             | Nominal Low            | Nominal High | Min  | Max   | Nominal Low          | Nominal High | Min   | Max    |
| 0.1         | 6.0                    | 6.8          | 4.6  | 9.6   | -6.1                 | -7.6         | -4.6  | -10.0  |
| 0.2         | 12.2                   | 13.5         | 9.2  | 18.2  | -12.2                | -14.5        | -9.2  | -20.0  |
| 0.3         | 18.1                   | 20.1         | 13.8 | 26.0  | -18.1                | -21.2        | -13.8 | -29.8  |
| 0.4         | 24.1                   | 26.6         | 18.4 | 33.9  | -24.0                | -27.7        | -18.4 | -38.8  |
| 0.5         | 29.8                   | 33.0         | 23.0 | 41.8  | -29.8                | -34.1        | -23.0 | -46.8  |
| 0.6         | 34.6                   | 39.1         | 27.7 | 49.4  | -34.3                | -40.5        | -27.7 | -54.4  |
| 0.7         | 39.4                   | 44.2         | 32.2 | 56.8  | -38.1                | -46.9        | -32.2 | -61.8  |
| 0.8         | 43.7                   | 49.8         | 36.8 | 63.2  | -41.1                | -53.1        | -36.0 | -69.5  |
| 0.9         | 47.5                   | 55.2         | 39.6 | 69.9  | -43.8                | -59.4        | -38.2 | -77.3  |
| 1.0         | 51.3                   | 60.3         | 42.6 | 76.3  | -46.0                | -65.5        | -38.7 | -85.2  |
| 1.1         | 54.1                   | 65.2         | 44.8 | 82.5  | -47.8                | -71.6        | -39.0 | -93.0  |
| 1.2         | 56.2                   | 69.9         | 46.2 | 88.3  | -49.2                | -77.6        | -39.2 | -100.6 |
| 1.3         | 57.9                   | 74.2         | 47.1 | 93.8  | -50.0                | -83.6        | -39.4 | -108.1 |
| 1.4         | 59.3                   | 78.4         | 47.4 | 99.1  | -50.5                | -89.7        | -39.6 | -115.5 |
| 1.5         | 60.1                   | 82.3         | 47.7 | 103.8 | -50.7                | -95.5        | -39.9 | -123.0 |
| 1.6         | 60.5                   | 85.9         | 48.0 | 108.4 | -51.0                | -101.3       | -40.1 | -130.4 |
| 1.7         | 61.0                   | 89.1         | 48.4 | 112.1 | -51.1                | -107.1       | -40.2 | -136.7 |
| 1.8         | 61.5                   | 92.2         | 48.9 | 115.9 | -51.3                | -112.4       | -40.3 | -144.2 |
| 1.9         | 62.0                   | 95.3         | 49.1 | 119.6 | -51.5                | -118.7       | -40.4 | -150.5 |
| 2.0         | 62.5                   | 97.2         | 49.4 | 123.3 | -51.6                | -124.0       | -40.5 | -156.9 |
| 2.1         | 62.8                   | 99.1         | 49.6 | 126.5 | -51.8                | -129.3       | -40.6 | -163.2 |
| 2.2         | 63.3                   | 100.9        | 49.8 | 129.5 | -52.0                | -134.6       | -40.7 | -169.6 |
| 2.3         | 63.8                   | 101.9        | 49.9 | 132.4 | -52.2                | -139.9       | -40.8 | -176.0 |
| 2.4         | 64.1                   | 102.8        | 50.0 | 135.0 | -52.3                | -145.2       | -40.9 | -181.3 |
| 2.5         | 64.6                   | 103.8        | 50.2 | 137.3 | -52.5                | -150.5       | -41.0 | -187.6 |
| 2.6         | 64.8                   | 104.6        | 50.4 | 139.2 | -52.7                | -155.3       | -41.1 | -192.9 |
| 2.7         | 65.0                   | 105.4        | 50.5 | 140.8 | -52.8                | -160.1       | -41.2 | -198.2 |

**Table 29: Reduced Output Drive Characteristics**

Characteristics are specified under best, worst, and nominal process variation/conditions

| Voltage (V) | Pull-Down Current (mA) |              |      |      | Pull-Up Current (mA) |              |       |       |
|-------------|------------------------|--------------|------|------|----------------------|--------------|-------|-------|
|             | Nominal Low            | Nominal High | Min  | Max  | Nominal Low          | Nominal High | Min   | Max   |
| 0.1         | 3.4                    | 3.8          | 2.6  | 5.0  | -3.5                 | -4.3         | -2.6  | -5.0  |
| 0.2         | 6.9                    | 7.6          | 5.2  | 9.9  | -6.9                 | -7.8         | -5.2  | -9.9  |
| 0.3         | 10.3                   | 11.4         | 7.8  | 14.6 | -10.3                | -12.0        | -7.8  | -14.6 |
| 0.4         | 13.6                   | 15.1         | 10.4 | 19.2 | -13.6                | -15.7        | -10.4 | -19.2 |
| 0.5         | 16.9                   | 18.7         | 13.0 | 23.6 | -16.9                | -19.3        | -13.0 | -23.6 |
| 0.6         | 19.9                   | 22.1         | 15.7 | 28.0 | -19.4                | -22.9        | -15.7 | -28.0 |
| 0.7         | 22.3                   | 25.0         | 18.2 | 32.2 | -21.5                | -26.5        | -18.2 | -32.2 |
| 0.8         | 24.7                   | 28.2         | 20.8 | 35.8 | -23.3                | -30.1        | -20.4 | -35.8 |
| 0.9         | 26.9                   | 31.3         | 22.4 | 39.5 | -24.8                | -33.6        | -21.6 | -39.5 |
| 1.0         | 29.0                   | 34.1         | 24.1 | 43.2 | -26.0                | -37.1        | -21.9 | -43.2 |
| 1.1         | 30.6                   | 36.9         | 25.4 | 46.7 | -27.1                | -40.3        | -22.1 | -46.7 |
| 1.2         | 31.8                   | 39.5         | 26.2 | 50.0 | -27.8                | -43.1        | -22.2 | -50.0 |
| 1.3         | 32.8                   | 42.0         | 26.6 | 53.1 | -28.3                | -45.8        | -22.3 | -53.1 |
| 1.4         | 33.5                   | 44.4         | 26.8 | 56.1 | -28.6                | -48.4        | -22.4 | -56.1 |
| 1.5         | 34.0                   | 46.6         | 27.0 | 58.7 | -28.7                | -50.7        | -22.6 | -58.7 |
| 1.6         | 34.3                   | 48.6         | 27.2 | 61.4 | -28.9                | -52.9        | -22.7 | -61.4 |
| 1.7         | 34.5                   | 50.5         | 27.4 | 63.5 | -28.9                | -55.0        | -22.7 | -63.5 |
| 1.8         | 34.8                   | 52.2         | 27.7 | 65.6 | -29.0                | -56.8        | -22.8 | -65.6 |
| 1.9         | 35.1                   | 53.9         | 27.8 | 67.7 | -29.2                | -58.7        | -22.9 | -67.7 |
| 2.0         | 35.4                   | 55.0         | 28.0 | 69.8 | -29.2                | -60.0        | -22.9 | -69.8 |
| 2.1         | 35.6                   | 56.1         | 28.1 | 71.6 | -29.3                | -61.2        | -23.0 | -71.6 |
| 2.2         | 35.8                   | 57.1         | 28.2 | 73.3 | -29.5                | -62.4        | -23.0 | -73.3 |
| 2.3         | 36.1                   | 57.7         | 28.3 | 74.9 | -29.5                | -63.1        | -23.1 | -74.9 |
| 2.4         | 36.3                   | 58.2         | 28.3 | 76.4 | -29.6                | -63.8        | -23.2 | -76.4 |
| 2.5         | 36.5                   | 58.7         | 28.4 | 77.7 | -29.7                | -64.4        | -23.2 | -77.7 |
| 2.6         | 36.7                   | 59.2         | 28.5 | 78.8 | -29.8                | -65.1        | -23.3 | -78.8 |
| 2.7         | 36.8                   | 59.6         | 28.6 | 79.7 | -29.9                | -65.8        | -23.3 | -79.7 |

## Commands

Tables 30 and 31 provide a quick reference of available commands. Two additional Truth Tables—Table 32 on page 46 and Table 33 on page 47—provide current state/next state information.

**Table 30: Truth Table 1 – Commands**

CKE is HIGH for all commands shown except SELF REFRESH; All states and sequences not shown are illegal or reserved

| Function  | CS# | RAS# | CAS# | WE# | Address  | Notes |
|---|-----|------|------|-----|----------|-------|
| DESELECT  | H   | X    | X    | X   | X        | 1     |
| NO OPERATION (NOP)  | L   | H    | H    | H   | X        | 1     |
| ACTIVE (select bank and activate row)                     | L   | L    | H    | H   | Bank/row | 2     |
| READ (select bank and column and start READ burst)        | L   | H    | L    | H   | Bank/col | 3     |
| WRITE (select bank and column and start WRITE burst)      | L   | H    | L    | L   | Bank/col | 3     |
| BURST TERMINATE   | L   | H    | H    | L   | X        | 4     |
| PRECHARGE (deactivate row in bank or banks)               | L   | L    | H    | L   | Code     | 5     |
| AUTO REFRESH or SELF REFRESH<br>(enter self refresh mode) | L   | L    | L    | H   | X        | 6, 7  |
| LOAD MODE REGISTER  | L   | L    | L    | L   | Op-code  | 8     |

- Notes:
1. DESELECT and NOP are functionally interchangeable.
  2. BA[1:0] provide bank address and A[n:0] (128Mb: n = 11; 256Mb and 512Mb: n = 12; 1Gb: n = 13) provide row address.
  3. BA[1:0] provide bank address; A[i:0] provide column address, (where Ai is the most significant column address bit for a given density and configuration, see Table 2 on page 2) A10 HIGH enables the auto precharge feature (non persistent), and A10 LOW disables the auto precharge feature.
  4. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
  5. A10 LOW: BA[1:0] determine which bank is precharged. A10 HIGH: all banks are precharged and BA[1:0] are “Don’t Care.”
  6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing while in self refresh mode, all inputs and I/Os are “Don’t Care” except for CKE.
  8. BA[1:0] select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA[1:0] are reserved). A[n:0] provide the op-code to be written to the selected mode register.

**Table 31: Truth Table 2 – DM Operation**

Used to mask write data, provided coincident with the corresponding data

| Name (Function) | DM | DQ    |
|-----------------|----|-------|
| Write enable    | L  | Valid |
| Write inhibit   | H  | X     |

**Table 32: Truth Table 3 – Current State Bank  $n$  – Command to Bank  $n$** 

Notes: 1–6 apply to the entire table; Notes appear below

| <b>Current State</b>               | <b>CS#</b> | <b>RAS#</b> | <b>CAS#</b> | <b>WE#</b> | <b>Command/Action</b>                             | <b>Notes</b> |
|------------------------------------|------------|-------------|-------------|------------|---|--------------|
| Any                                | H          | X           | X           | X          | DESELECT (NOP/continue previous operation)        |              |
|                                    | L          | H           | H           | H          | NO OPERATION (NOP/continue previous operation)    |              |
| Idle                               | L          | L           | H           | H          | ACTIVE (select and activate row)                  |              |
|                                    | L          | L           | L           | H          | AUTO REFRESH                                      | 7            |
|                                    | L          | L           | L           | L          | LOAD MODE REGISTER                                | 7            |
| Row active                         | L          | H           | L           | H          | READ (select column and start READ burst)         | 10           |
|                                    | L          | H           | L           | L          | WRITE (select column and start WRITE burst)       | 10           |
|                                    | L          | L           | H           | L          | PRECHARGE (deactivate row in bank or banks)       | 8            |
| Read<br>(auto precharge disabled)  | L          | H           | L           | H          | READ (select column and start new READ burst)     | 10           |
|                                    | L          | H           | L           | L          | WRITE (select column and start new WRITE burst)   | 10, 12       |
|                                    | L          | L           | H           | L          | PRECHARGE (truncate READ burst, start PRECHARGE)  | 8            |
|                                    | L          | H           | H           | L          | BURST TERMINATE                                   | 9            |
| Write<br>(auto precharge disabled) | L          | H           | L           | H          | READ (select column and start READ burst)         | 10, 11       |
|                                    | L          | H           | L           | L          | WRITE (select column and start new WRITE burst)   | 10           |
|                                    | L          | L           | H           | L          | PRECHARGE (truncate WRITE burst, start PRECHARGE) | 8, 11        |

- Notes:
1. This table applies when  $\text{CKE}_{n-1}$  was HIGH and  $\text{CKE}_n$  is HIGH (see Table 35 on page 49) and after  $t_{XSNR}$  has been met (if the previous state was self refresh).
  2. This table is bank-specific, except where noted (that is, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
  3. Current state definitions:
    - Idle: The bank has been precharged, and  $t_{RP}$  has been met.
    - Row active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/addresses and no register accesses are in progress.
    - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
  4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 32 and according to Table 33 on page 47.
    - Precharging: Starts with registration of a PRECHARGE command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, the bank will be in the idle state.
    - Row activating: Starts with registration of an ACTIVE command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the bank will be in the “row active” state.
    - Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.
    - Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.
  5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

- Refreshing: Starts with registration of an AUTO REFRESH command and ends when  $t_{RFC}$  is met. After  $t_{RFC}$  is met, the DDR SDRAM will be in the all banks idle state.
  - Accessing mode register: Starts with registration of an LMR command and ends when  $t_{MRD}$  has been met. After  $t_{MRD}$  is met, the DDR SDRAM will be in the all banks idle state.
  - Precharging all: Starts with registration of a PRECHARGE ALL command and ends when  $t_{RP}$  is met. After  $t_{RP}$  is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
  7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
  8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
  9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
  10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
  11. Requires appropriate DM masking.
  12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

**Table 33: Truth Table 4 – Current State Bank  $n$  – Command to Bank  $m$** 

Notes: 1–6 apply to the entire table; Notes appear on page 47

| <b>Current State</b>                   | <b>CS#</b> | <b>RAS#</b> | <b>CAS#</b> | <b>WE#</b> | <b>Command/Action</b>                           | <b>Notes</b> |
|--|------------|-------------|-------------|------------|---|--------------|
| Any                                    | H          | X           | X           | X          | DESELECT (NOP/continue previous operation)      |              |
|  | L          | H           | H           | H          | NO OPERATION (NOP/continue previous operation)  |              |
| Idle                                   | X          | X           | X           | X          | Any command otherwise allowed to bank $m$       |              |
| Row activating, active, or precharging | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |
|  | L          | H           | L           | H          | READ (select column and start READ burst)       | 7            |
|  | L          | H           | L           | L          | WRITE (select column and start WRITE burst)     | 7            |
|  | L          | L           | H           | L          | PRECHARGE                                       |              |
|  | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |
| Read (auto precharge disabled)         | L          | H           | L           | H          | READ (select column and start new READ burst)   | 7            |
|  | L          | H           | L           | L          | WRITE (select column and start WRITE burst)     | 7, 9         |
|  | L          | L           | H           | L          | PRECHARGE                                       |              |
|  | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |
| Write (auto precharge disabled)        | L          | H           | L           | H          | READ (select column and start new READ burst)   | 7, 8         |
|  | L          | H           | L           | L          | WRITE (select column and start new WRITE burst) | 7            |
|  | L          | L           | H           | L          | PRECHARGE                                       |              |
|  | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |
| Read (with auto-precharge)             | L          | H           | L           | H          | READ (select column and start new READ burst)   | 7            |
|  | L          | H           | L           | L          | WRITE (select column and start WRITE burst)     | 7, 9         |
|  | L          | L           | H           | L          | PRECHARGE                                       |              |
|  | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |
| Write (with auto-precharge)            | L          | H           | L           | H          | READ (select column and start new READ burst)   | 7            |
|  | L          | H           | L           | L          | WRITE (select column and start new WRITE burst) | 7            |
|  | L          | L           | H           | L          | PRECHARGE                                       |              |
|  | L          | L           | H           | H          | ACTIVE (select and activate row)                |              |

Notes: 1. This table applies when  $CKE_{n-1}$  was HIGH and  $CKE_n$  is HIGH (see Table 35 on page 49) and after  $t_{XSNR}$  has been met (if the previous state was self refresh).

2. This table describes alternate bank operation, except where noted (that is, the current state is for bank  $n$ , and the commands shown are those allowed to be issued to bank  $m$ , assuming that bank  $m$  is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
  - Idle: The bank has been precharged, and  $t_{RP}$  has been met.
  - Row active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress.
  - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
  - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
  - Read with auto precharge enabled: See note 3a below.
  - Write with auto precharge enabled: See note 3a below.
    - a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when  $t_{WR}$  ends, with  $t_{WR}$  measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or  $t_{RP}$ ) begins. This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (for example, contention between read data and write data must be avoided).
    - b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized in Table 34.

**Table 34: Command Delays**
 $CL_{RU} = CL$  rounded up to the next integer

| From Command              | To Command                         | Minimum Delay with Concurrent Auto Precharge |
|---------------------------|------------------------------------|--|
| WRITE with auto precharge | READ or READ with auto precharge   | $[1 + (BL/2)] \times t_{CK} + t_{WTR}$       |
|                           | WRITE or WRITE with auto precharge | $(BL/2) \times t_{CK}$                       |
|                           | PRECHARGE                          | $1 t_{CK}$                                   |
|                           | ACTIVE                             | $1 t_{CK}$                                   |
| READ with auto precharge  | READ or READ with auto precharge   | $(BL/2) \times t_{CK}$                       |
|                           | WRITE or WRITE with auto precharge | $[CL_{RU} + (BL/2)] \times t_{CK}$           |
|                           | PRECHARGE                          | $1 t_{CK}$                                   |
|                           | ACTIVE                             | $1 t_{CK}$                                   |

4. AUTO REFRESH and LMR commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the "Command/Action" column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

**Table 35: Truth Table 5 – CKE**

Notes 1–6 apply to the entire table; Notes appear below

| <b>CKE<sub>n-1</sub></b> | <b>CKE<sub>n</sub></b> | <b>Current State</b> | <b>Command<sub>n</sub></b> | <b>Action<sub>n</sub></b>  | <b>Notes</b> |
|--------------------------|------------------------|----------------------|----------------------------|----------------------------|--------------|
| L                        | L                      | Power-down           | X                          | Maintain power-down        |              |
|                          |                        | Self refresh         | X                          | Maintain self refresh      |              |
| L                        | H                      | Power-down           | DESELECT or NOP            | Exit power-down            |              |
|                          |                        | Self refresh         | DESELECT or NOP            | Exit self refresh          | 7            |
| H                        | L                      | All banks idle       | DESELECT or NOP            | Precharge power-down entry |              |
|                          |                        | Bank(s) active       | DESELECT or NOP            | Active power-down entry    |              |
|                          |                        | All banks idle       | AUTO REFRESH               | Self refresh entry         |              |
| H                        | H                      |                      | See Table 30 on page 45    |                            |              |

- Notes:
1. CKE<sub>n</sub> is the logic state of CKE at clock edge *n*; CKE<sub>n-1</sub> was the state of CKE at the previous clock edge.
  2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
  3. COMMAND<sub>n</sub> is the command registered at clock edge *n*, and ACTION<sub>n</sub> is a result of COMMAND<sub>n</sub>.
  4. All states and sequences not shown are illegal or reserved.
  5. CKE must not drop LOW during a column access. For a READ, this means CKE must stay HIGH until after the read postamble time (*t*<sub>RPST</sub>); for a WRITE, CKE must stay HIGH until the write recovery time (*t*<sub>WR</sub>) has been met.
  6. Once initialized, including during self refresh mode, V<sub>REF</sub> must be powered within the specified range.
  7. Upon exit of the self refresh mode, the DLL is automatically enabled. A minimum of 200 clock cycles is needed before applying a READ command for the DLL to lock. DESELECT or NOP commands should be issued on any clock edges occurring during the *t*<sub>XSNR</sub> period.

## DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

## NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

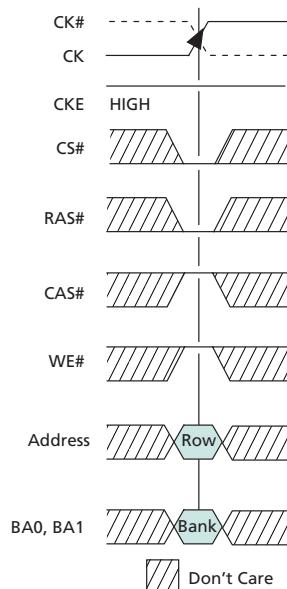
## LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A0–An (see "REGISTER DEFINITION" on page 57). The LMR command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until *t*<sub>MRD</sub> is met.

## ACTIVE (ACT)

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or a write, as shown in Figure 18. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[n:0] selects the row.

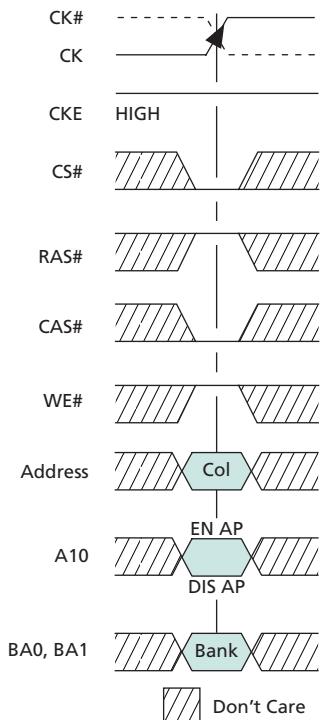
**Figure 18: Activating a Specific Row in a Specific Bank**



## READ

The READ command is used to initiate a burst read access to an active row, as shown in Figure 19 on page 51. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[i:0] (where Ai is the most significant column address bit for a given density and configuration, see Table 2 on page 2) selects the starting column location.

**Figure 19: READ Command**

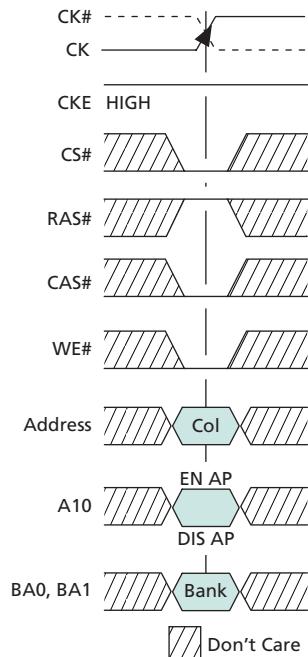


Note: EN AP = enable auto precharge; DIS AP = disable auto precharge.

## WRITE

The WRITE command is used to initiate a burst write access to an active row as shown in Figure 20. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[*i*:0] (where  $A_i$  is the most significant column address bit for a given density and configuration, see Table 2 on page 2) selects the starting column location.

**Figure 20: WRITE Command**

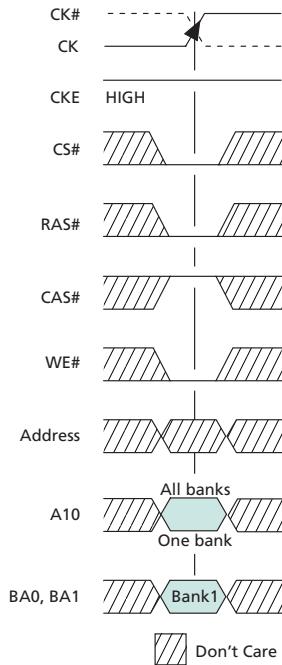


Note: EN AP = enable auto precharge; and DIS AP = disable auto precharge.

## PRECHARGE (PRE)

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks as shown in Figure 21. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single bank is precharged or whether all banks are precharged.

**Figure 21: PRECHARGE Command**



Notes: 1. If A10 is HIGH, bank address becomes "Don't Care."

## BURST TERMINATE (BST)

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 54. The open page from which the READ burst was terminated remains open.

## AUTO REFRESH (AR)

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

## SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW).

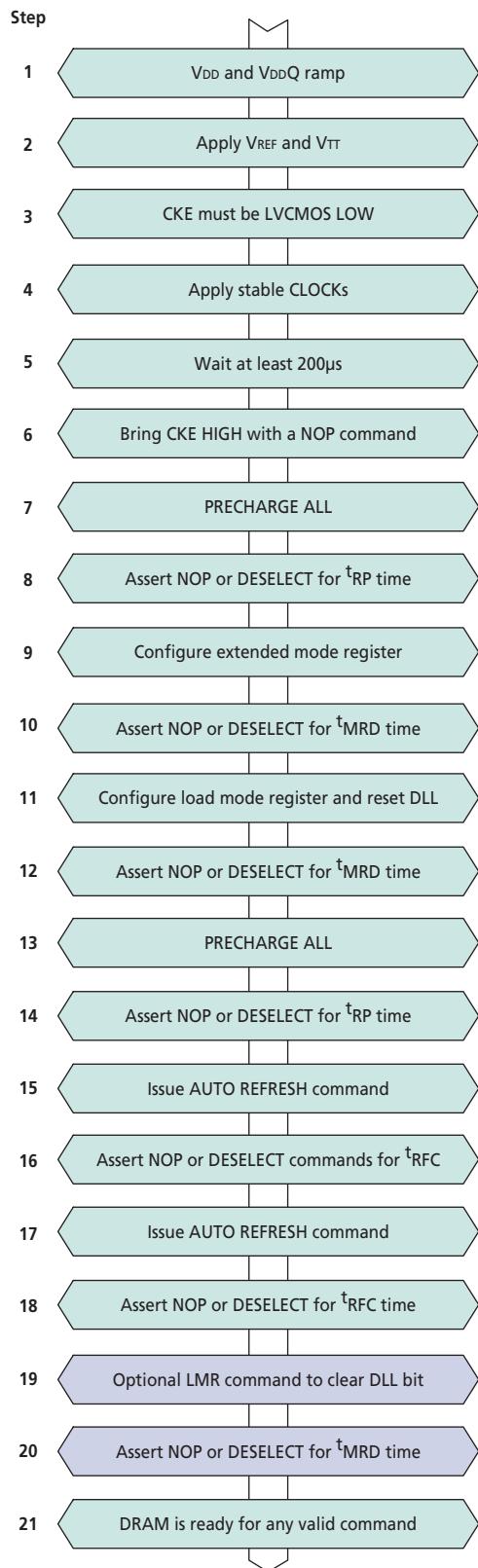
## Operations

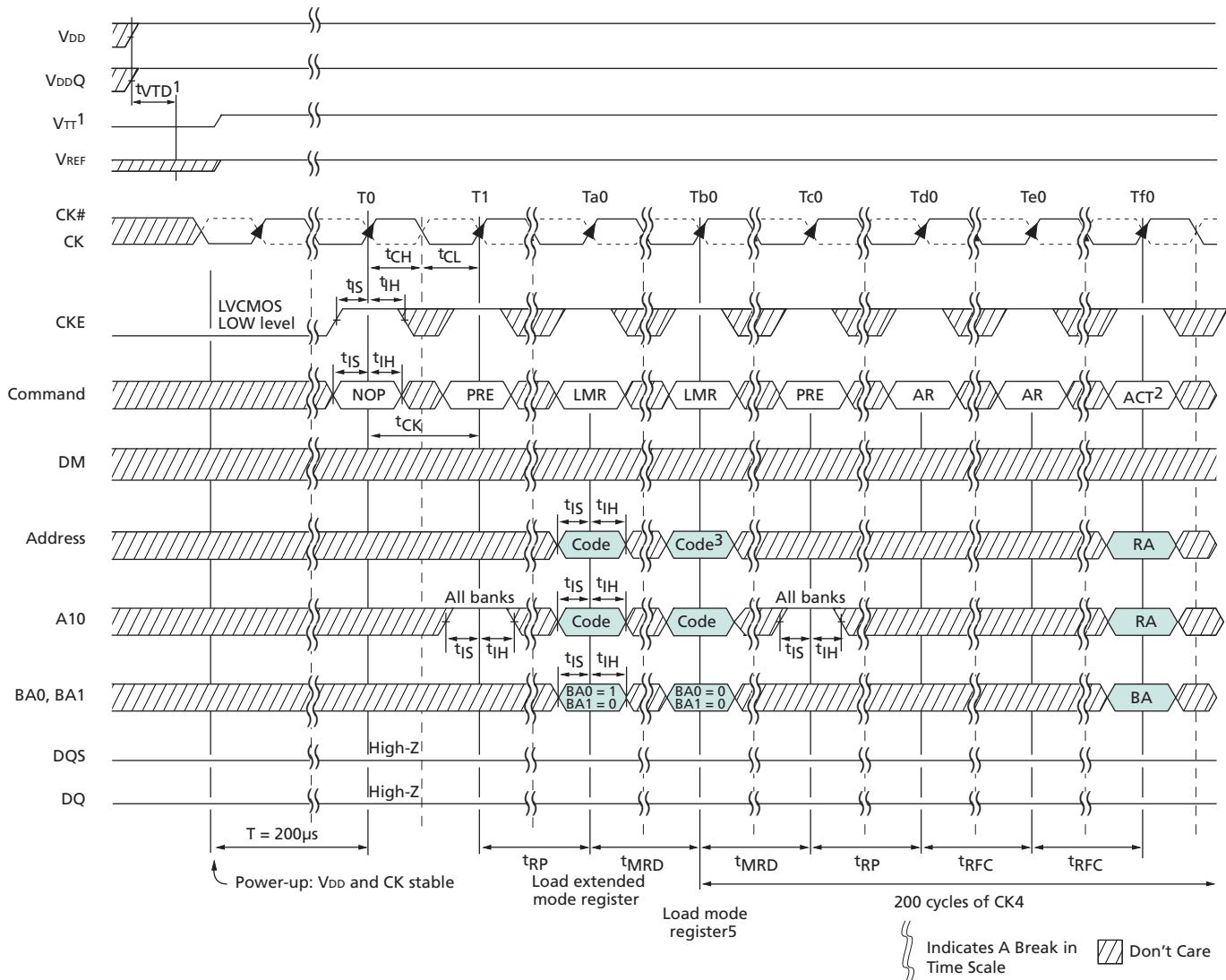
### INITIALIZATION

Prior to normal operation, DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures, other than those specified, may result in undefined operation.

To ensure device operation, the DRAM must be initialized as described in the following steps:

1. Simultaneously apply power to  $V_{DD}$  and  $V_{DDQ}$ .
2. Apply  $V_{REF}$  and then  $V_{TT}$  power.  $V_{TT}$  must be applied after  $V_{DDQ}$  to avoid device latch-up, which may cause permanent damage to the device. Except for CKE, inputs are not recognized as valid until after  $V_{REF}$  is applied.
3. Assert and hold CKE at a LVC MOS logic LOW. Maintaining an LVC MOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access).
4. Provide stable clock signals.
5. Wait at least 200 $\mu$ s.
6. Bring CKE HIGH, and provide at least one NOP or DESELECT command. At this point, the CKE input changes from a LVC MOS input to a SSTL\_2 input only and will remain a SSTL\_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least  $t_{RP}$  time; during this time NOPs or DESELECT commands must be given.
9. Using the LMR command, program the extended mode register ( $E0 = 0$  to enable the DLL and  $E1 = 0$  for normal drive; or  $E1 = 1$  for reduced drive and  $E2-En$  must be set to 0 [where  $n$  = most significant bit]).
10. Wait at least  $t_{MRD}$  time; only NOPs or DESELECT commands are allowed.
11. Using the LMR command, program the mode register to set operating parameters and to reset the DLL. At least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least  $t_{MRD}$  time; only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least  $t_{RP}$  time; only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command. This may be moved prior to step 13.
16. Wait at least  $t_{RFC}$  time; only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command. This may be moved prior to step 13.
18. Wait at least  $t_{RFC}$  time; only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires an LMR command to clear the DLL bit (set  $M8 = 0$ ). If an LMR command is issued, the same operating parameters should be utilized as in step 11.
20. Wait at least  $t_{MRD}$  time; only NOPs or DESELECT commands are supported.
21. At this point the DRAM is ready for any valid command. At least 200 clock cycles with CKE HIGH are required between step 11 (DLL RESET) and any READ command.

**Figure 22: INITIALIZATION Flow Diagram**


**Figure 23: INITIALIZATION Timing Diagram**


- Notes:**
1. V<sub>TT</sub> is not applied directly to the device; however, t<sub>VTD</sub> ≥ 0 to avoid device latch-up. V<sub>DDQ</sub>, V<sub>TT</sub>, and V<sub>REF</sub> ≤ V<sub>DD</sub> + 0.3V. Alternatively, V<sub>TT</sub> may be 1.35V maximum during power-up, even if V<sub>DD</sub>/V<sub>DDQ</sub> are 0V, provided a minimum of 42Ω of series resistance is used between the V<sub>TT</sub> supply and the input pin. Once initialized, V<sub>REF</sub> must always be powered within the specified range.
  2. Although not required by the Micron device, JEDEC specifies issuing another LMR command (A8 = 0) prior to activating any bank. If another LMR command is issued, the same, previously issued operating parameters must be used.
  3. The two AUTO REFRESH commands at Td0 and Te0 may be applied following the LMR command at Ta0.
  4. t<sub>MRD</sub> is required before any command can be applied (during MRD time only NOPs or DESELECTs are allowed), and 200 cycles of CK are required before a READ command can be issued.
  5. While programming the operating parameters, reset the DLL with A8 = 1.

## REGISTER DEFINITION

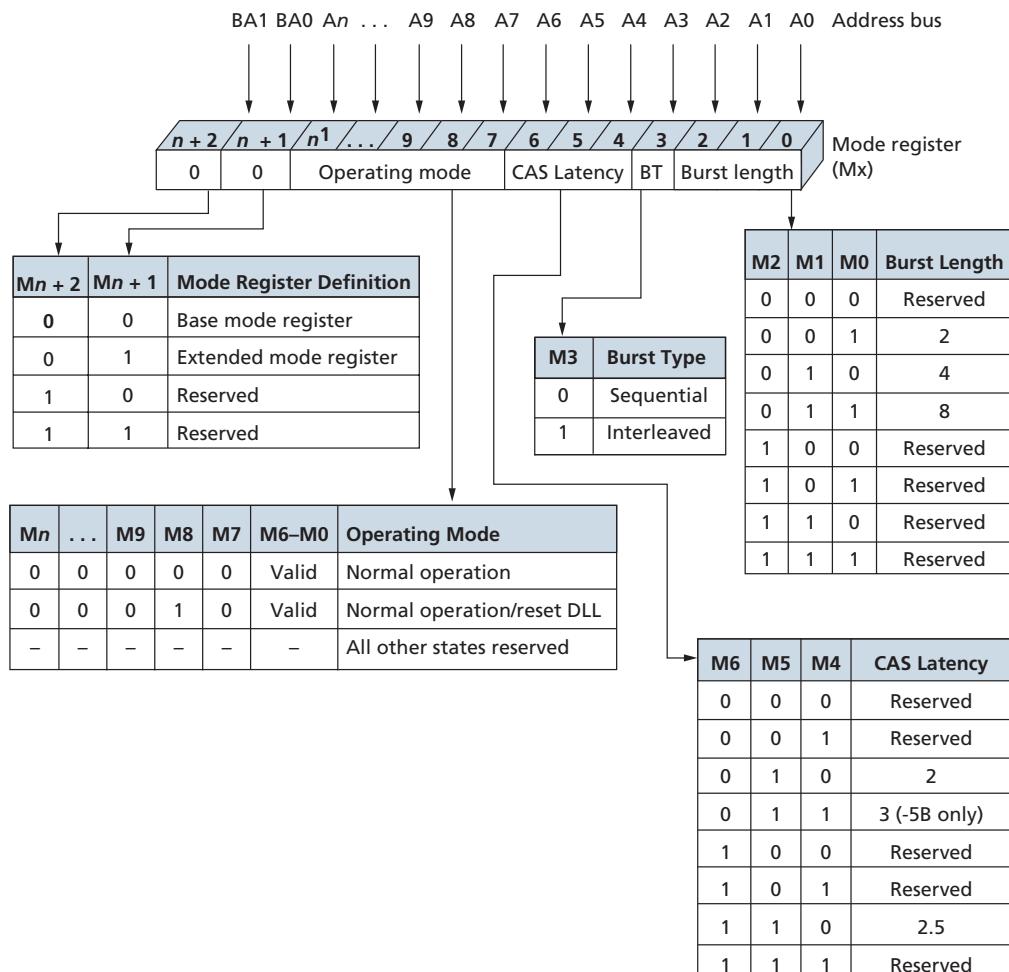
### Mode Register

The mode register is used to define the specific DDR SDRAM mode of operation. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 24. The mode register is programmed via the LMR command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or until the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A[2:0] specify the burst length, A3 specifies the type of burst (sequential or interleaved), A[6:4] specify the CAS latency, and A[n:7] specify the operating mode.

**Figure 24: Mode Register Definition**



Notes: 1. *n* is the most significant row address bit from Table 2 on page 2.

### Burst Length (BL)

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable for both READ and WRITE bursts, as shown in Figure 24 on page 57. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL = 2, BL = 4, or BL = 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block—meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[i:1] when BL = 2, by A[i:2] when BL = 4, and by A[i:3] when BL = 8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. For example: for BL = 8, A[i:3] select the eight-data-element block; A[2:0] select the first access within the block.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 36.

**Table 36: Burst Definition**

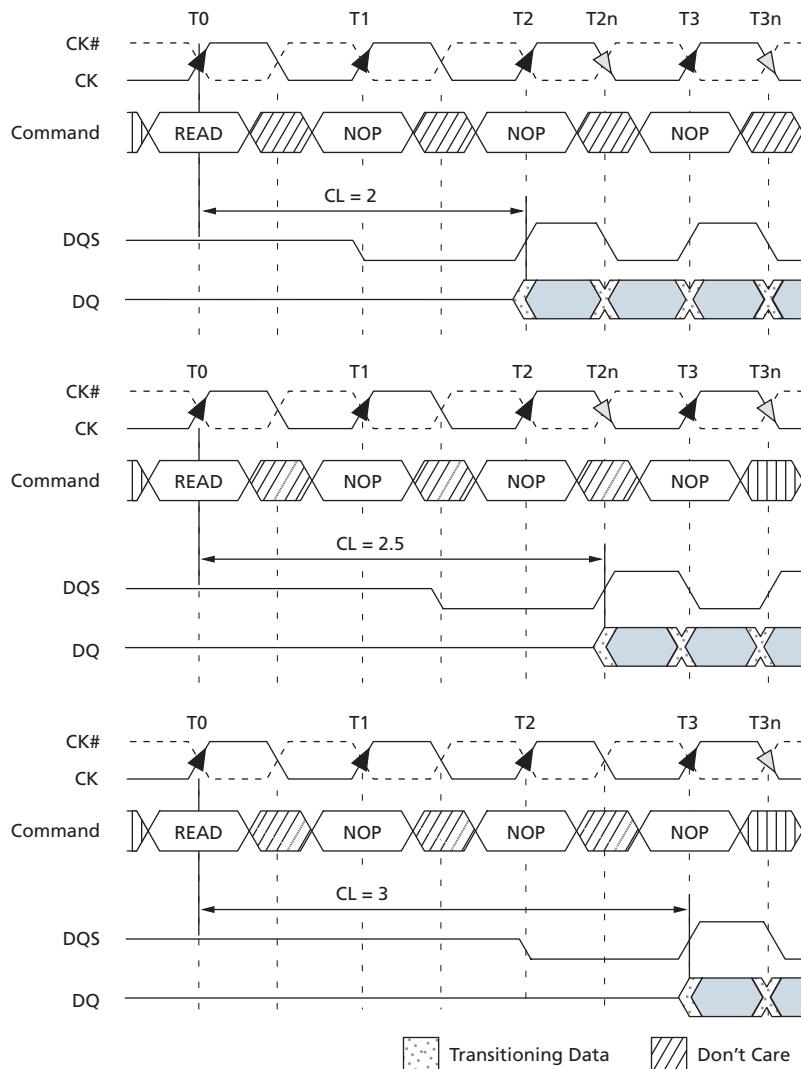
| Burst Length | Starting Column Address       | Order of Accesses Within a Burst |                    |  |
|--------------|-------------------------------|----------------------------------|--------------------|--|
|              |                               | Type = Sequential                | Type = Interleaved |  |
| 2            | – – <b>A0</b>                 | –                                | –                  |  |
|              | – – 0                         | 0-1                              | 0-1                |  |
|              | – – 1                         | 1-0                              | 1-0                |  |
| 4            | – <b>A1</b> <b>A0</b>         | –                                | –                  |  |
|              | – 0 0                         | 0-1-2-3                          | 0-1-2-3            |  |
|              | – 0 1                         | 1-2-3-0                          | 1-0-3-2            |  |
|              | – 1 0                         | 2-3-0-1                          | 2-3-0-1            |  |
|              | – 1 1                         | 3-0-1-2                          | 3-2-1-0            |  |
| 8            | <b>A2</b> <b>A1</b> <b>A0</b> | –                                | –                  |  |
|              | 0 0 0                         | 0-1-2-3-4-5-6-7                  | 0-1-2-3-4-5-6-7    |  |
|              | 0 0 1                         | 1-2-3-4-5-6-7-0                  | 1-0-3-2-5-4-7-6    |  |
|              | 0 1 0                         | 2-3-4-5-6-7-0-1                  | 2-3-0-1-6-7-4-5    |  |
|              | 0 1 1                         | 3-4-5-6-7-0-1-2                  | 3-2-1-0-7-6-5-4    |  |
|              | 1 0 0                         | 4-5-6-7-0-1-2-3                  | 4-5-6-7-0-1-2-3    |  |
|              | 1 0 1                         | 5-6-7-0-1-2-3-4                  | 5-4-7-6-1-0-3-2    |  |
|              | 1 1 0                         | 6-7-0-1-2-3-4-5                  | 6-7-4-5-2-3-0-1    |  |
|              | 1 1 1                         | 7-0-1-2-3-4-5-6                  | 7-6-5-4-3-2-1-0    |  |

### CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, 2.5, or 3 (-5B only) clocks, as shown in Figure 25. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available nominally coincident with clock edge  $n + m$ . Table 37 on page 60 indicates the operating frequencies at which each CL setting can be used.

**Figure 25: CAS Latency**



Note: BL = 4 in the cases shown; shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .

**Table 37: CAS Latency**

| Speed  | Allowable Operating Clock Frequency (MHz) |              |               |
|--------|---|--------------|---------------|
|        | CL = 2                                    | CL = 2.5     | CL = 3        |
| -5B    | 75 ≤ f ≤ 133                              | 75 ≤ f ≤ 167 | 133 ≤ f ≤ 200 |
| -6/-6T | 75 ≤ f ≤ 133                              | 75 ≤ f ≤ 167 | —             |
| -75E   | 75 ≤ f ≤ 133                              | 75 ≤ f ≤ 133 | —             |
| -75Z   | 75 ≤ f ≤ 133                              | 75 ≤ f ≤ 133 | —             |
| -75    | 75 ≤ f ≤ 100                              | 75 ≤ f ≤ 133 | —             |

### **Operating Mode**

The normal operating mode is selected by issuing an LMR command with bits A7–An each set to zero and bits A[6:0] set to the desired values. A DLL reset is initiated by issuing an LMR command with bits A7 and A[n:9] each set to zero, bit A8 set to one, and bits A[6:0] set to the desired values. Although not required by the Micron device, JEDEC specifications recommend that an LMR command resetting the DLL should always be followed by an LMR command selecting normal operating mode.

All other combinations of values for A[n:7] are reserved for future use and/or test modes. Test modes and reserved states should not be used, as unknown operation or incompatibility with future versions may result.

### **Extended Mode Register**

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 26 on page 61. The extended mode register is programmed via the LMR command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or until the device loses power. The enabling of the DLL should always be followed by an LMR command to the mode register (BA0/BA1 = 0) to reset the DLL. The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either requirement could result in an unspecified operation.

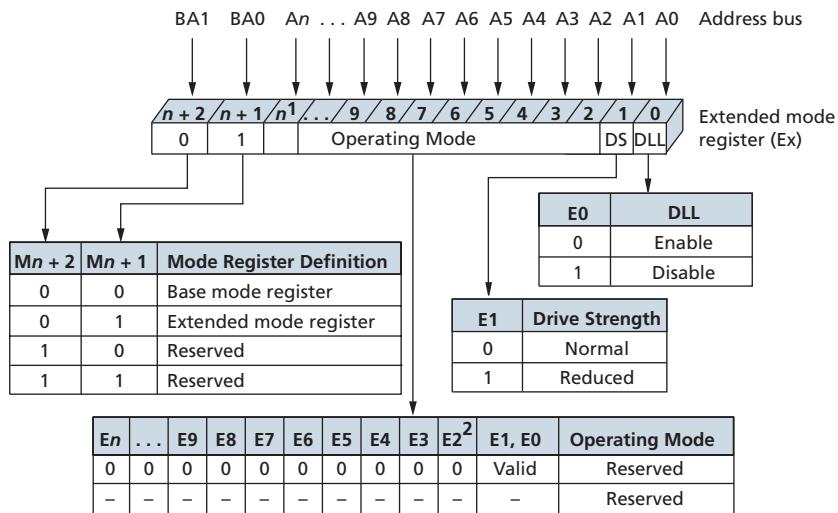
### **Output Drive Strength**

The normal drive strength for all outputs is specified to be SSTL\_2, Class II. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQ and DQS pins from SSTL\_2, Class II drive strength to a reduced drive strength, which is approximately 54% of the SSTL\_2, Class II drive strength.

### **DLL Enable/Disable**

When the part is running without the DLL enabled, device functionality may be altered. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (when the device exits self refresh mode, the DLL is enabled automatically). Anytime the DLL is enabled, 200 clock cycles with CKE HIGH must occur before a READ command can be issued.

**Figure 26: Extended Mode Register Definition**



Notes:

1.  $n$  is the most significant row address bit from Table 2 on page 2.
2. The QFC# option is not supported.

## ACTIVE

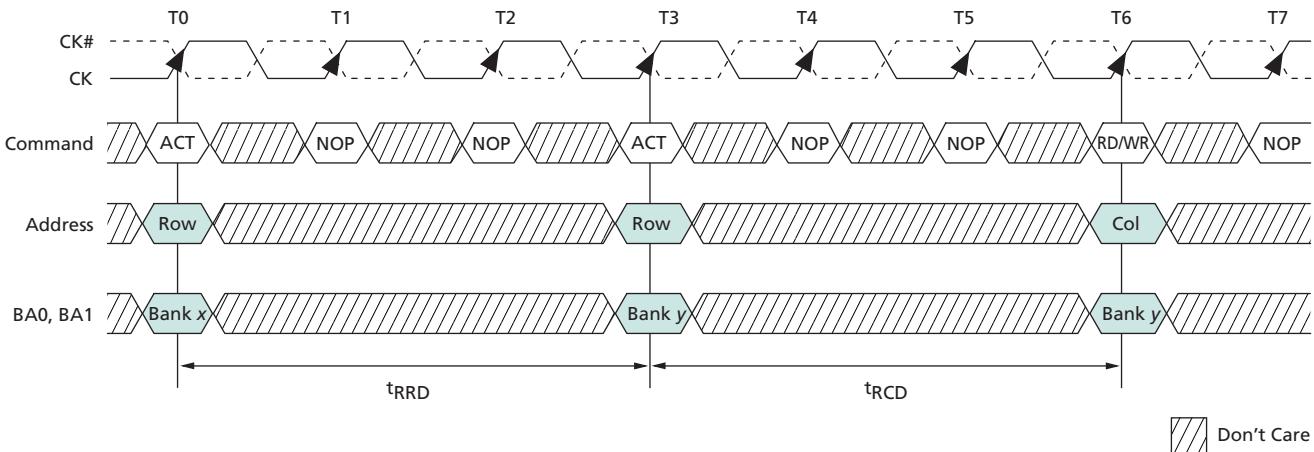
After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the  $t_{RCD}$  specification.  $t_{RCD}$  (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a  $t_{RCD}$  specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 27 on page 62, which covers any case where  $2 < t_{RCD}$  (MIN) /  $t_{CK} \leq 3$  (Figure 27 also shows the same case for  $t_{RRD}$ ; the same procedure is used to convert other specification limits from time units to clock cycles).

A row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by  $t_{RC}$ .

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by  $t_{RRD}$ .

**Figure 27: Example: Meeting  $t_{RCD}$  ( $t_{RRD}$ ) MIN When  $2 < t_{RCD}$  ( $t_{RRD}$ ) MIN/ $t_{CK}$   $\leq 3$**



## READ

During the READ command, the value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

**Note:** For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 28 on page 64 shows the general timing for each possible CL setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

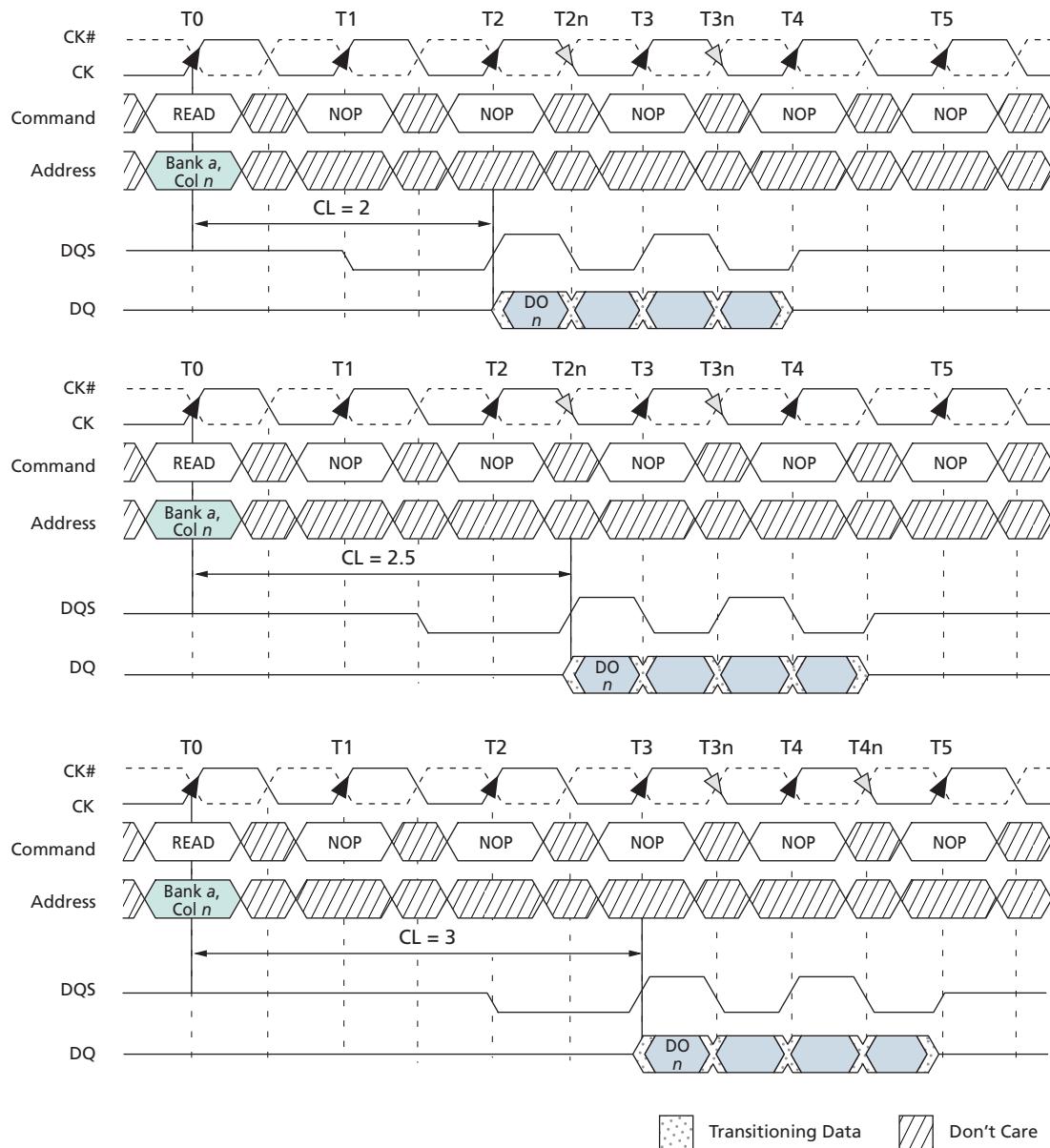
Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. Detailed explanations of  $t_{DQSQ}$  (valid data-out skew),  $t_{QH}$  (data-out window hold), and the valid data window are depicted in Figure 36 on page 72 and Figure 37 on page 73. Detailed explanations of  $t_{DQSCK}$  (DQS transition skew to CK) and  $t_{AC}$  (data-out transition skew to CK) are depicted in Figure 38 on page 74.

Data from any READ burst may be concatenated or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued  $x$  cycles after the first READ command, where  $x$  equals the number of desired data element pairs (pairs are required by the  $2n$ -prefetch architecture). This is shown in Figure 29 on page 65. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is illustrated in Figure 30 on page 66. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 31 on page 67.

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 32 on page 68. The BURST TERMINATE latency is equal to the CL, that is, the BURST TERMINATE command should be issued  $x$  cycles after the READ command where  $x$  equals the number of desired data element pairs (pairs are required by the  $2n$ -prefetch architecture).

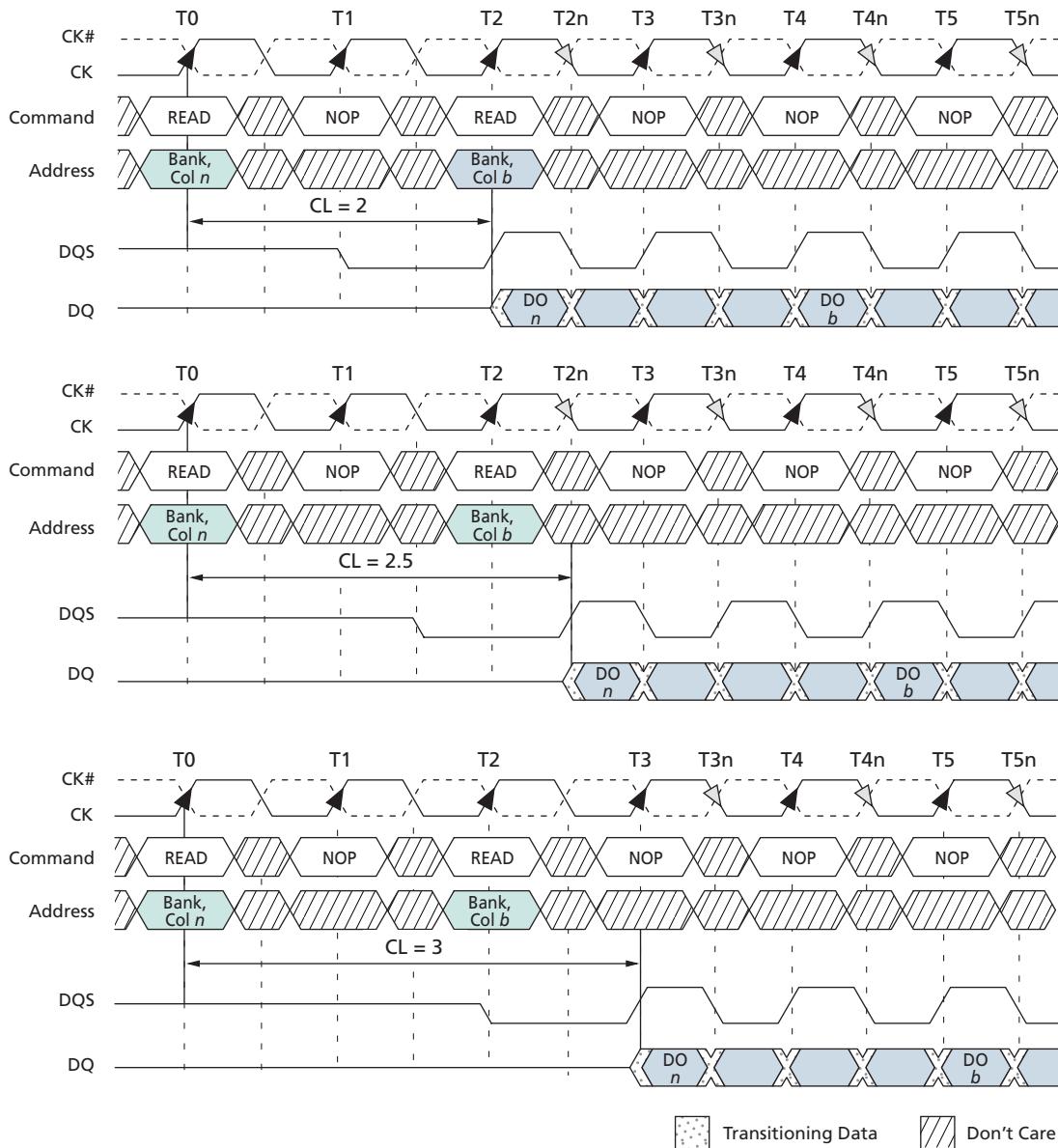
Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 33 on page 69. The  $t_{DQSS}$  (NOM) case is shown; the  $t_{DQSS}$  (MAX) case has a longer bus idle time. ( $t_{DQSS}$  [MIN] and  $t_{DQSS}$  [MAX] are defined in the section on WRITEs.) A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated.

The PRECHARGE command should be issued  $x$  cycles after the READ command, where  $x$  equals the number of desired data element pairs (pairs are required by the  $2n$ -prefetch architecture). This is shown in Figure 34 on page 70. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until both  $t_{RAS}$  and  $t_{RP}$  have been met. Part of the row precharge time is hidden during the access of the last data elements.

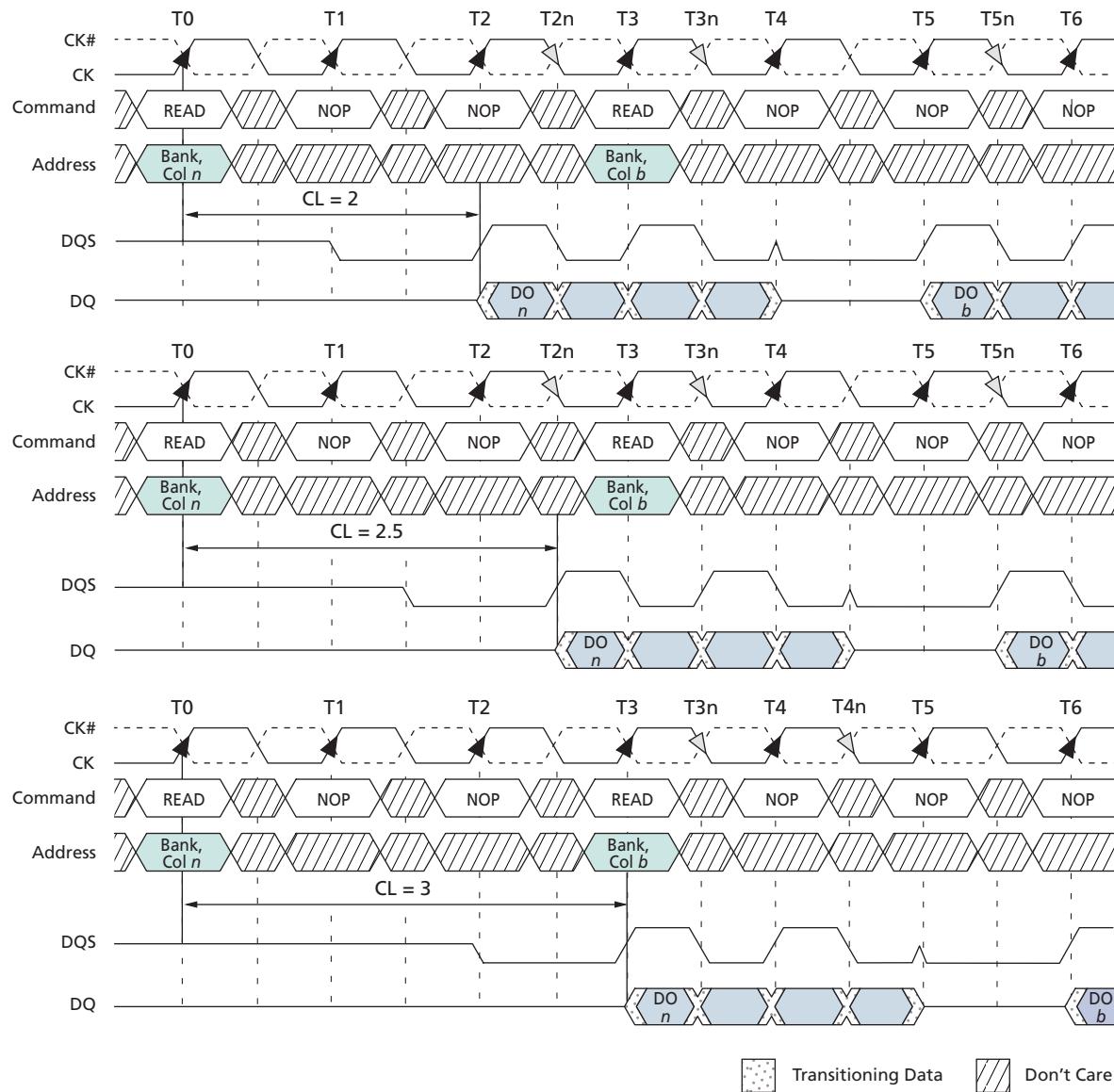
**Figure 28: READ Burst**


- Notes:**
1. DO<sub>n</sub> = data-out from column n.
  2. BL = 4.
  3. Three subsequent elements of data-out appear in the programmed order following DO<sub>n</sub>.
  4. Shown with nominal t<sub>AC</sub>, t<sub>DQSCK</sub>, and t<sub>DQSQ</sub>.

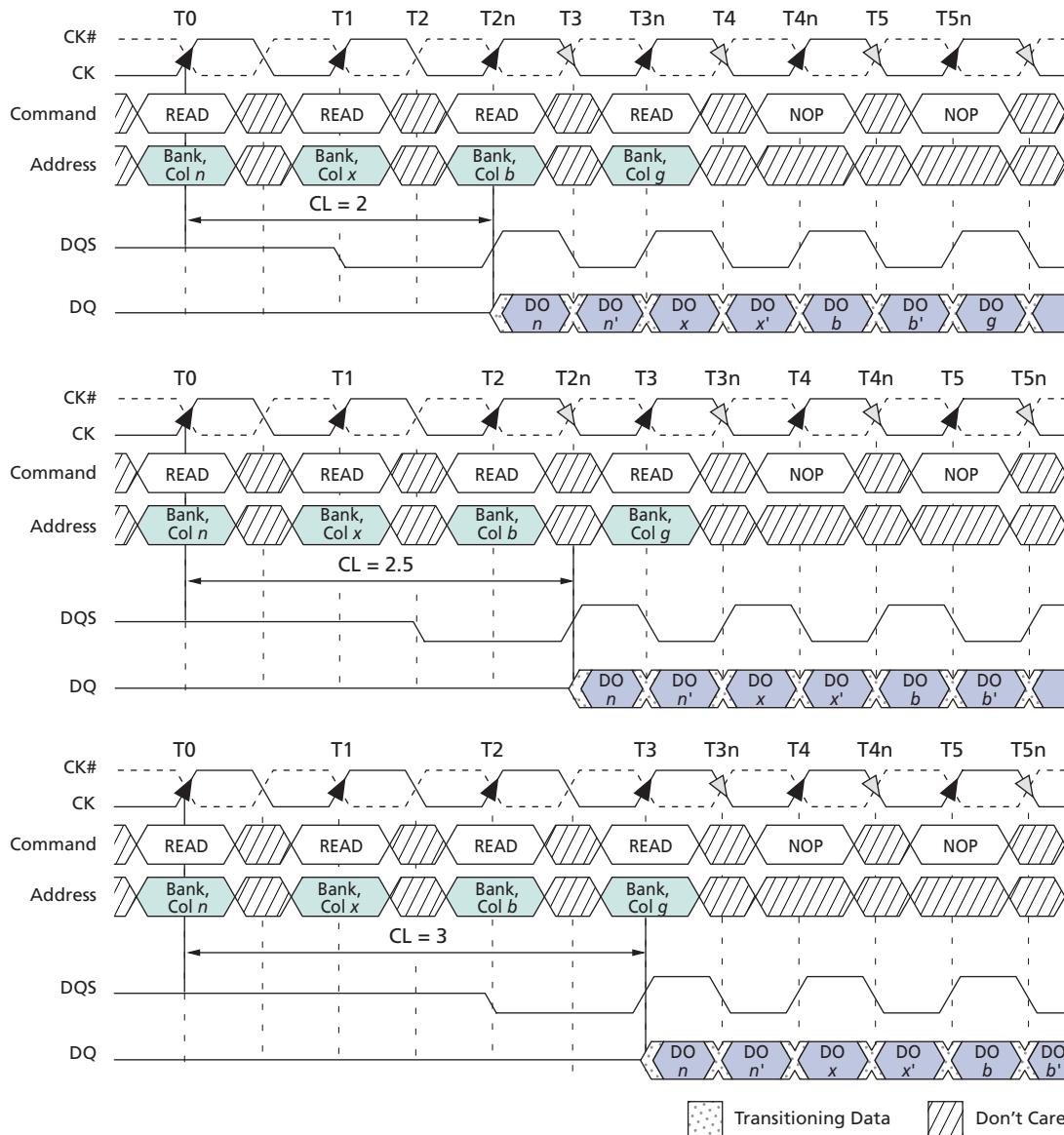
**Figure 29: Consecutive READ Bursts**



- Notes:
1. DO<sub>n</sub> (or b) = data-out from column n (or column b).
  2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
  3. Three subsequent elements of data-out appear in the programmed order following DO<sub>n</sub>.
  4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO<sub>b</sub>.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .
  6. Example applies only when READ commands are issued to same device.

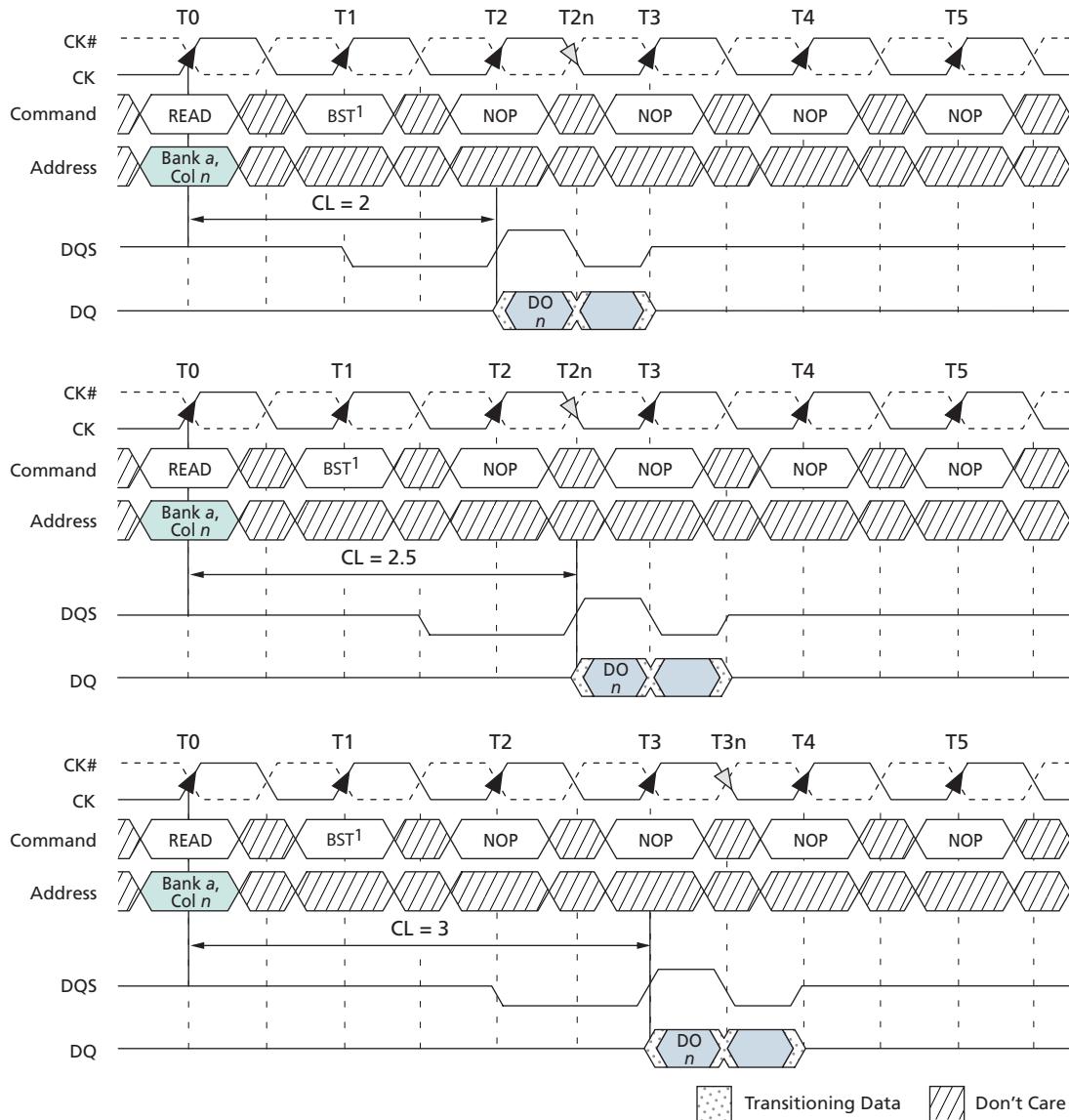
**Figure 30: Nonconsecutive READ Bursts**


- Notes:**
1. DO n (or b) = data-out from column n (or column b).
  2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
  3. Three subsequent elements of data-out appear in the programmed order following DO n.
  4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO b.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .

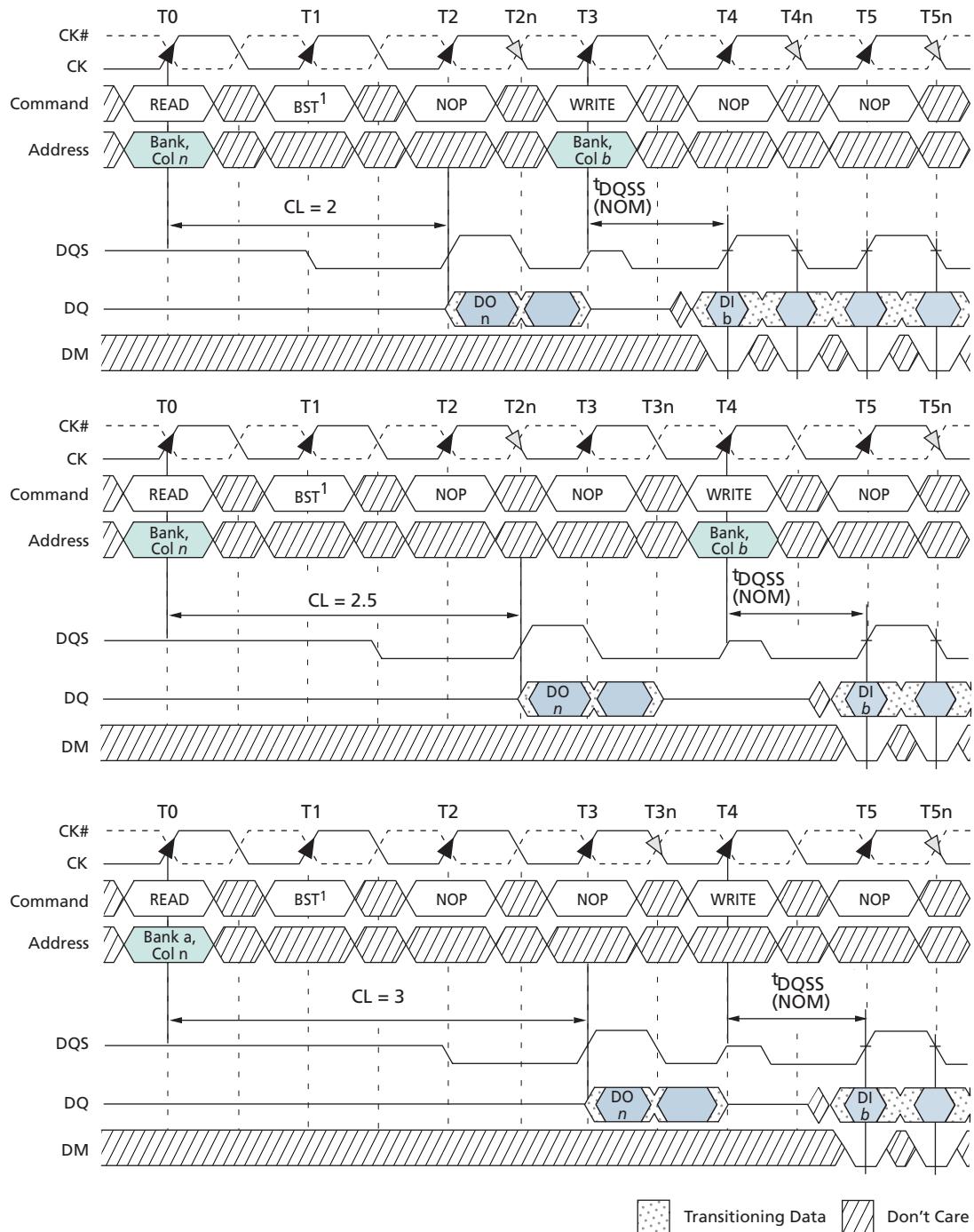
**Figure 31: Random READ Accesses**


- Notes:
1. DO n (or x or b or g) = data-out from column n (or column x or column b or column g).
  2. BL = 2, BL = 4, or BL = 8 (if BL = 4 or BL = 8, the following burst interrupts the previous).
  3. n', x', b', or g' indicate the next data-out following DO n, DO x, DO b, or DO g, respectively.
  4. READs are to an active row in any bank.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .

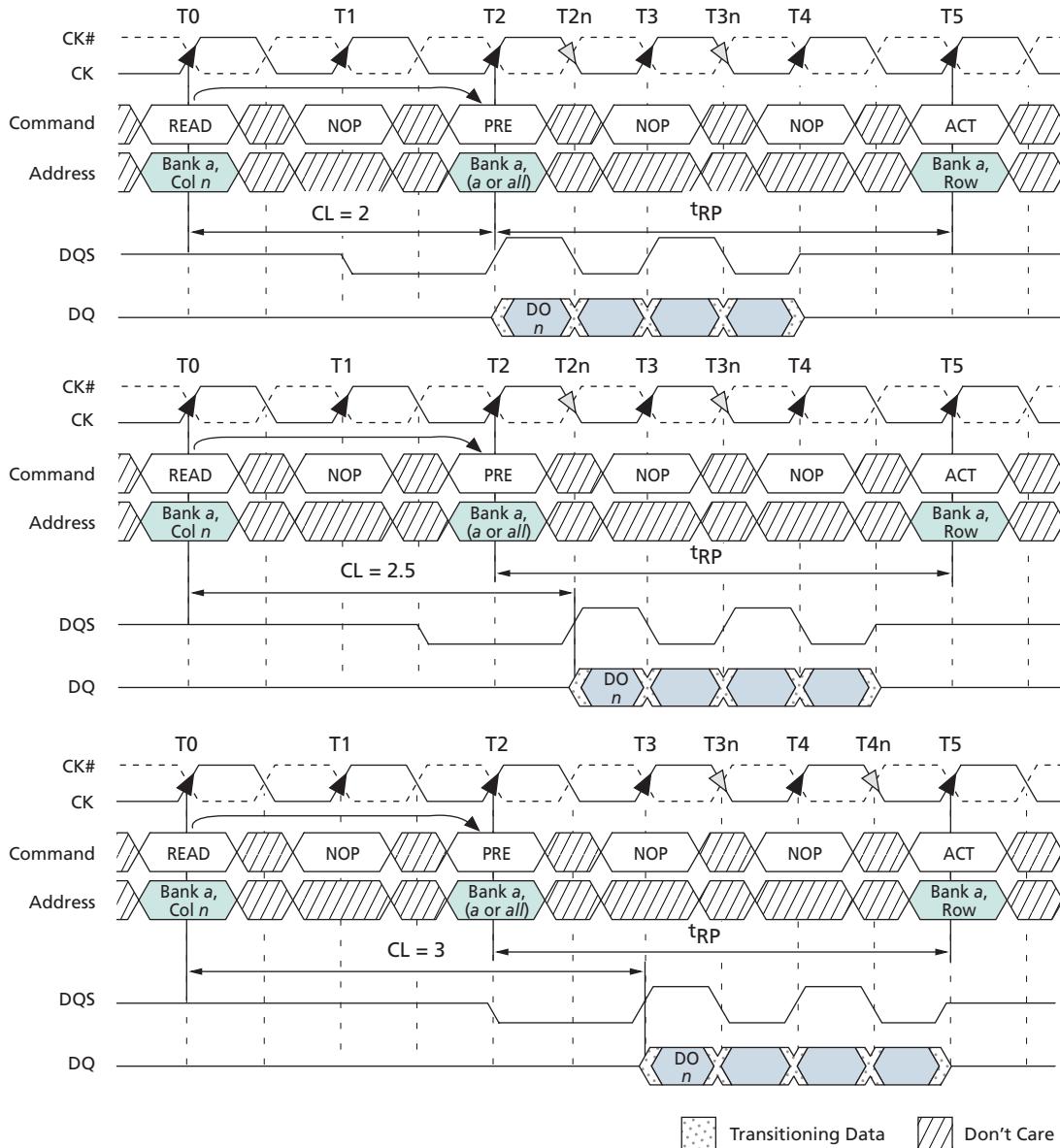
**Figure 32: Terminating a READ Burst**



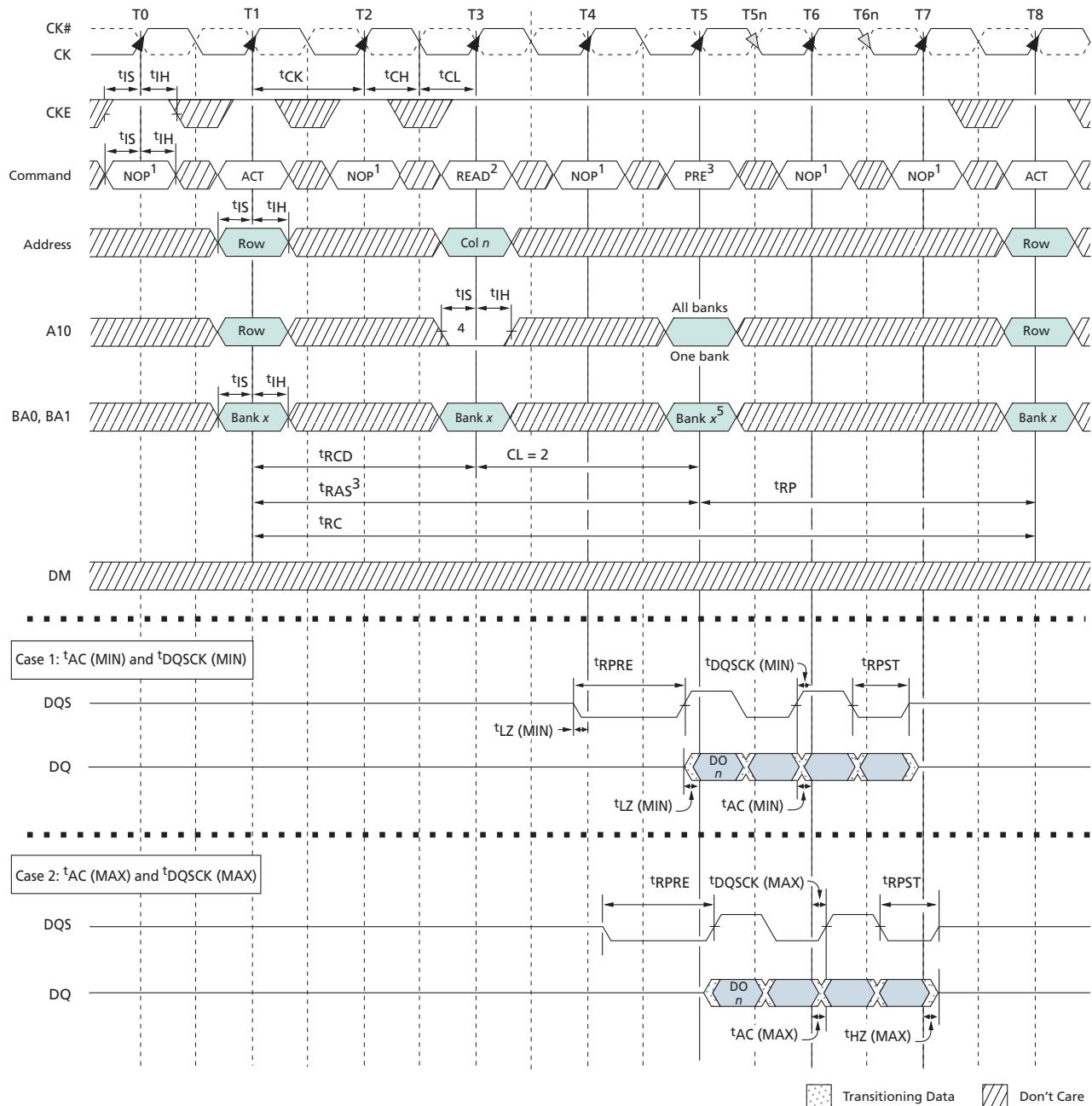
- Notes:
1. Page remains open.
  2. DO  $n$  = data-out from column  $n$ .
  3. BL = 4.
  4. Subsequent element of data-out appears in the programmed order following DO  $n$ .
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .

**Figure 33: READ-to-WRITE**


- Notes:
1. Page remains open.
  2. DO<sub>n</sub> = data-out from column *n*; DI<sub>b</sub> = data-in from column *b*.
  3. BL = 4 (applies for bursts of 8 as well; if BL = 2, the BURST command shown can be NOP).
  4. One subsequent element of data-out appears in the programmed order following DO<sub>n</sub>.
  5. Data-in elements are applied following DI<sub>b</sub> in the programmed order.
  6. Shown with nominal t<sub>AC</sub>, t<sub>DQSCK</sub>, and t<sub>DQSQ</sub>.

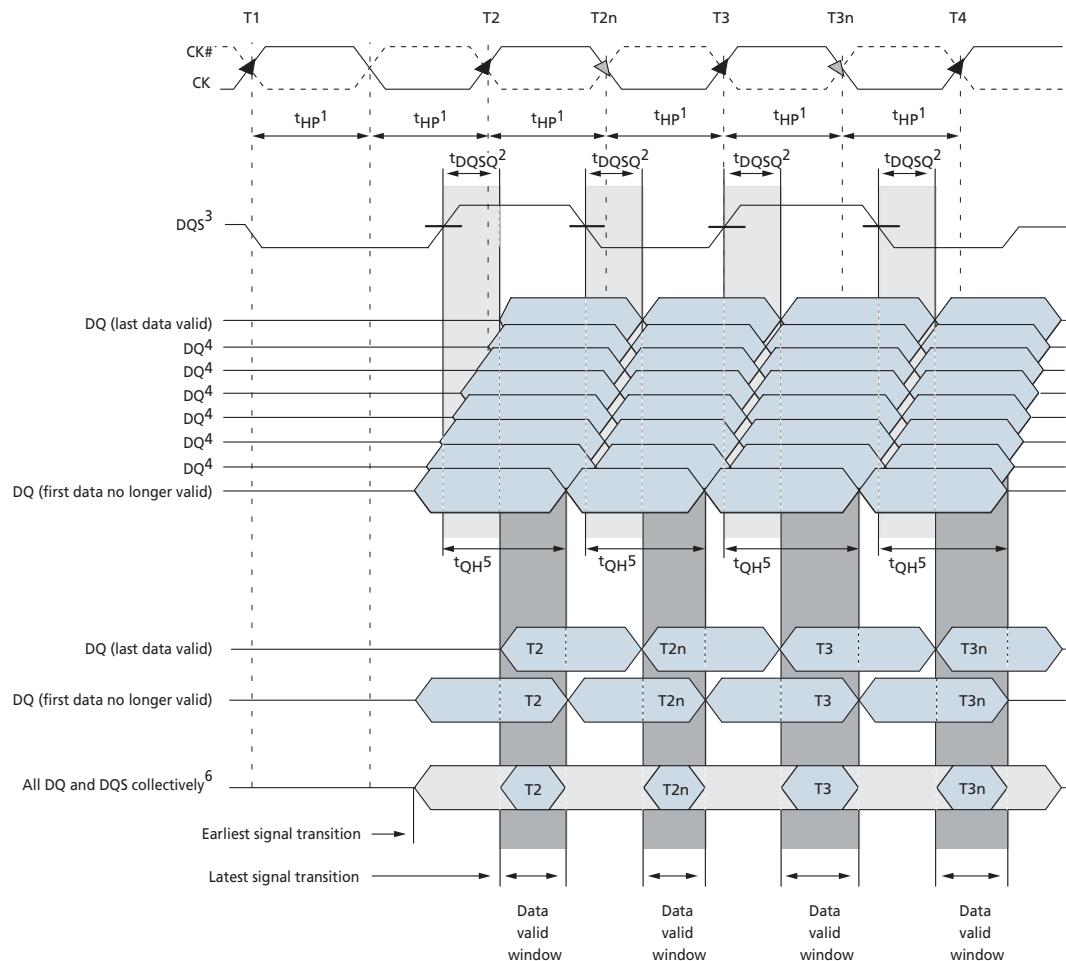
**Figure 34: READ-to-PRECHARGE**


- Notes:
1. Provided  $t_{RAS} (\text{MIN})$  is met, a READ command with auto precharge enabled would cause a precharge to be performed at  $x$  number of clock cycles after the READ command, where  $x = BL/2$ .
  2. DO  $n$  = data-out from column  $n$ .
  3. BL = 4 or an interrupted burst of 8.
  4. Three subsequent elements of data-out appear in the programmed order following DO  $n$ .
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .
  6. READ-to-PRECHARGE equals two clocks, which allows two data pairs of data-out; it is also assumed that  $t_{RAS} (\text{MIN})$  is met.
  7. An ACTIVE command to the same bank is only allowed if  $t_{RC} (\text{MIN})$  is met.

**Figure 35: Bank READ – Without Auto Precharge**


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4.
  3. The PRECHARGE command can only be applied at T5 if  $t_{RAS}$  (MIN) is met.
  4. Disable auto precharge.
  5. "Don't Care" if A10 is HIGH at T5.
  6. DO *n* (or *b*) = data-out from column *n* (or column *b*); subsequent elements are provided in the programmed order.
  7. Refer to Figure 36 on page 72, Figure 37 on page 73, and Figure 38 on page 74 for detailed DQS and DQ timing.

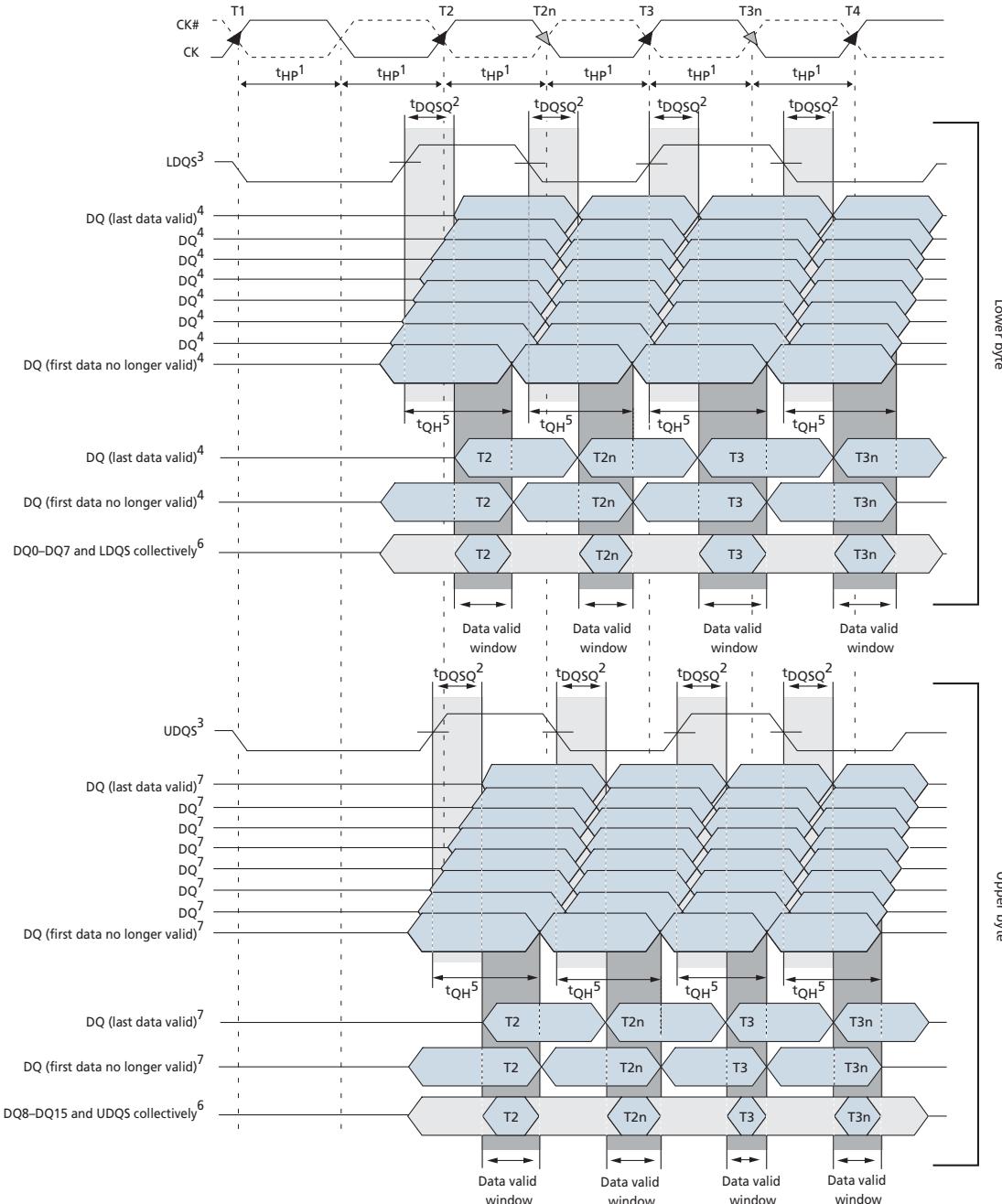
**Figure 36: x4, x8 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**



Notes:

1.  $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transition collectively when a bank is active.
2.  $t_{DQSQ}$  is derived at each DQS clock edge, is not cumulative over time, begins with DQS transition, and ends with the last valid DQ transition.
3. DQ transitioning after DQS transition define the  $t_{DQSQ}$  window. DQS transitions at T2 and T2n are an "early DQS"; at T3, a "nominal DQS"; and at T3n, a "late DQS".
4. For a x4, only two DQ apply.
5.  $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
6. The data valid window is derived for each DQS transitions and is defined as  $t_{QH} - t_{DQSQ}$ .

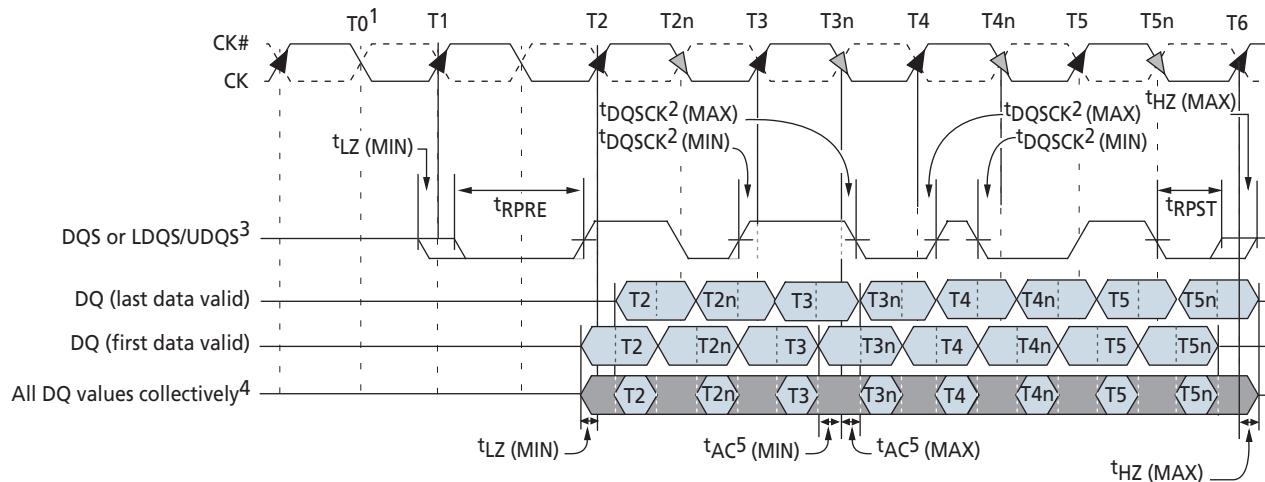
**Figure 37: x16 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**



Notes:

1.  $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transition collectively when a bank is active.
2.  $t_{DQSQ}$  is derived at each DQS clock edge, is not cumulative over time, begins with DQS transition, and ends with the last valid DQ transition.
3. DQ transitioning after DQS transition define the  $t_{DQSQ}$  window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
5.  $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
6. The data valid window is derived for each DQS transition and is  $t_{QH} - t_{DQSQ}$ .
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

**Figure 38: Data Output Timing –  $t_{AC}$  and  $t_{DQSCK}$**



- Notes:
1. READ command with CL = 2 issued at T0.
  2.  $t_{DQSCK}$  is the DQS output window relative to CK and is the “long term” component of the DQS skew.
  3. DQ transitioning after DQS transition define the  $t_{DQSQ}$  window.
  4. All DQ must transition by  $t_{DQSQ}$  after DQS transitions, regardless of  $t_{AC}$ .
  5.  $t_{AC}$  is the DQ output window relative to CK and is the “long term” component of DQ skew.
  6.  $t_{LZ}$  (MIN) and  $t_{AC}$  (MIN) are the first valid signal transitions.
  7.  $t_{HZ}$  (MAX) and  $t_{AC}$  (MAX) are the latest valid signal transitions.

## WRITE

During a WRITE command, the value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst (after  $t_{WR}$  time); if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

**Note:** For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS ( $t_{DQSS}$ ) is specified with a relatively wide range (from 75% to 125% of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (that is,  $t_{DQSS}$  [MIN] and  $t_{DQSS}$  [MAX]) might not be intuitive; they have also been included. Figure 39 on page 76 shows the nominal case and the extremes of  $t_{DQSS}$  for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued  $x$  cycles after the first WRITE command, where  $x$  equals the number of desired data element pairs (pairs are required by the  $2n$ -prefetch architecture).

Figure 40 on page 77 shows concatenated bursts of 4. An example of nonconsecutive WRITES is shown in Figure 41 on page 78. Full-speed random write accesses within a page or pages can be performed as shown in Figure 42 on page 78.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst,  $t_{WTR}$  should be met, as shown in Figure 43 on page 79.

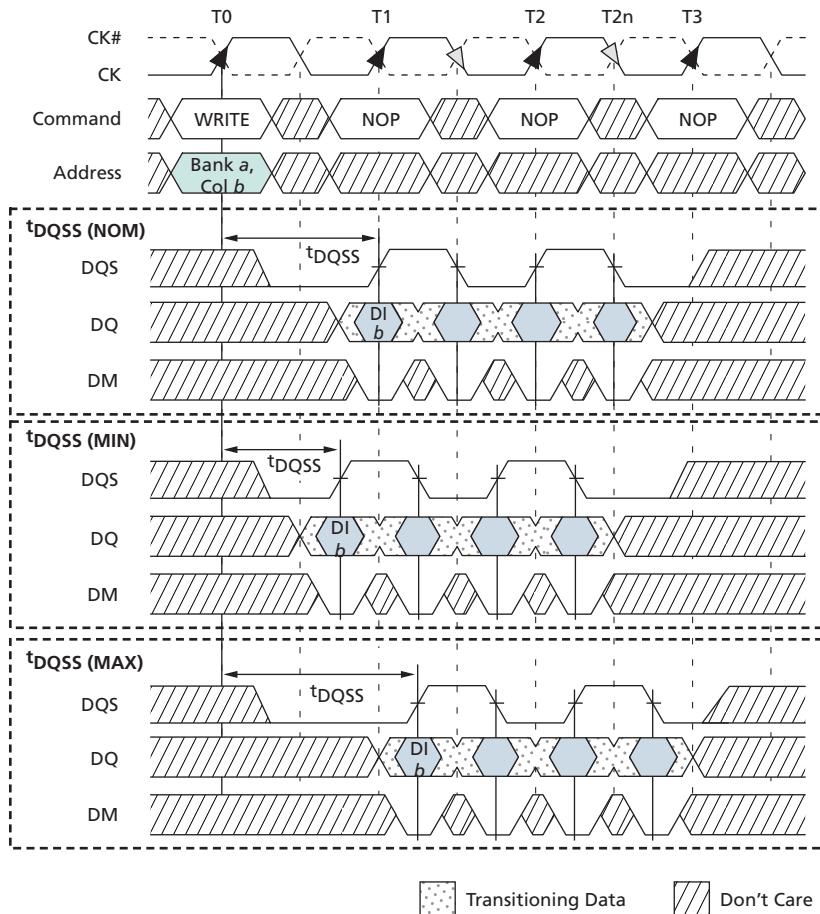
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 44 on page 80.

Note that only the data-in pairs that are registered prior to the  $t_{WTR}$  period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 45 on page 81.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst,  $t_{WR}$  should be met, as shown in Figure 46 on page 82.

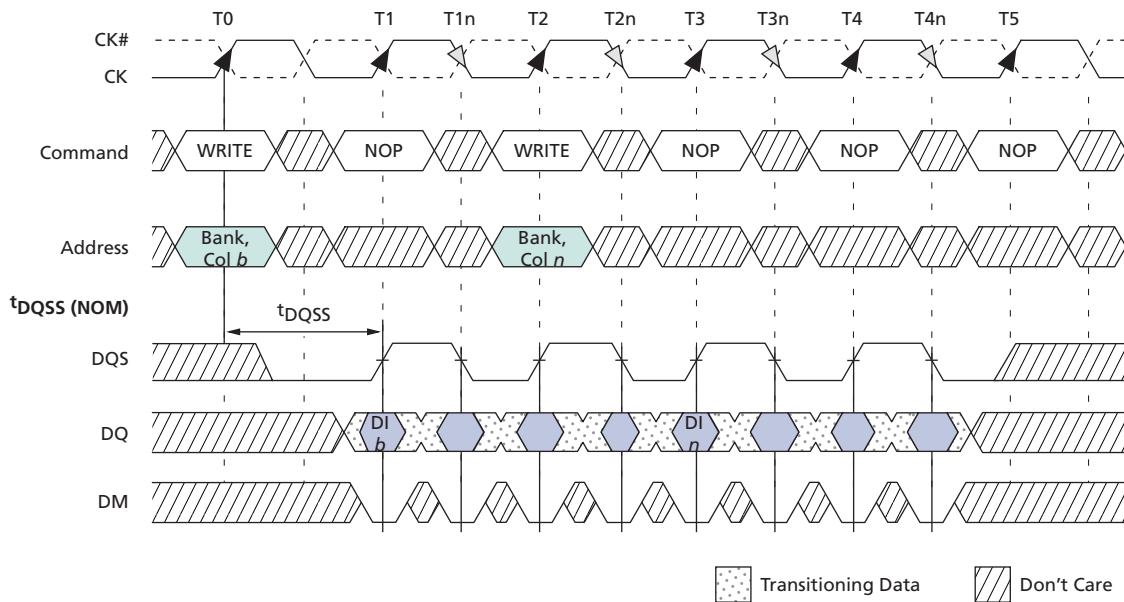
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 47 on page 83 and Figure 48 on page 84. Only the data-in pairs registered prior to the  $t_{WR}$  period are written to the internal array; any subsequent data-in should be masked with DM, as shown in Figures 47 and 48. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met.

**Figure 39: WRITE Burst**



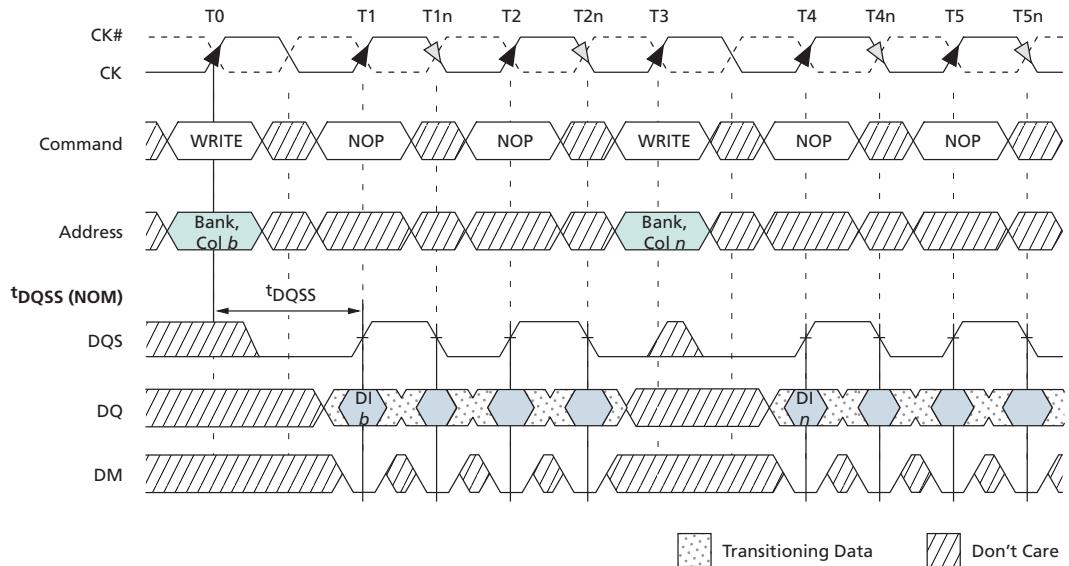
- Notes:
1. DI *b* = data-in for column *b*.
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. An uninterrupted burst of 4 is shown.
  4. A10 is LOW with the WRITE command (auto precharge is disabled).

**Figure 40: Consecutive WRITE-to-WRITE**



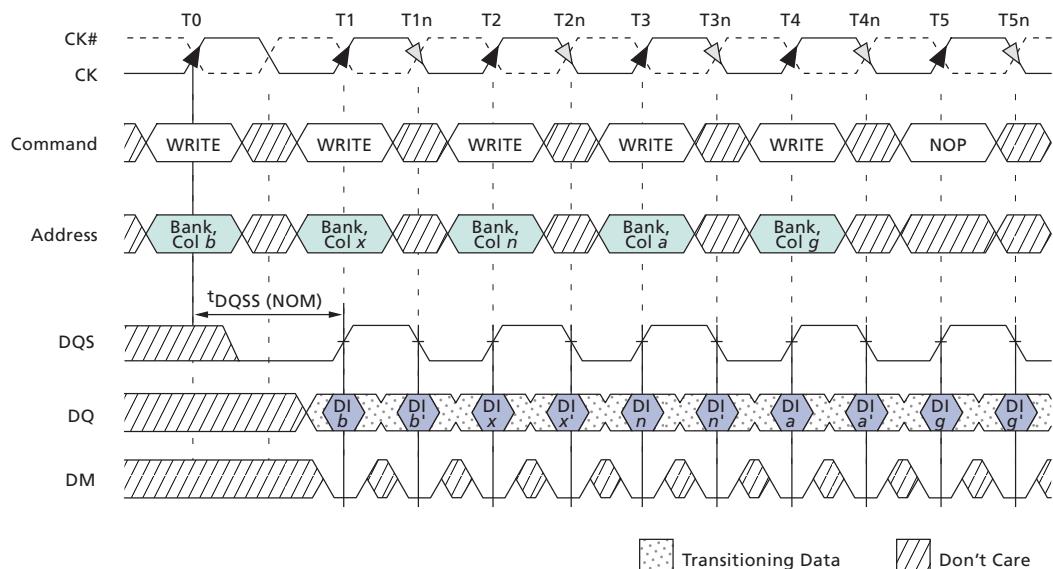
- Notes:
1. DI *b* (or *n*) = data-in from column *b* (or column *n*).
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
  4. An uninterrupted burst of 4 is shown.
  5. Each WRITE command may be to any bank.

**Figure 41: Nonconsecutive WRITE-to-WRITE**



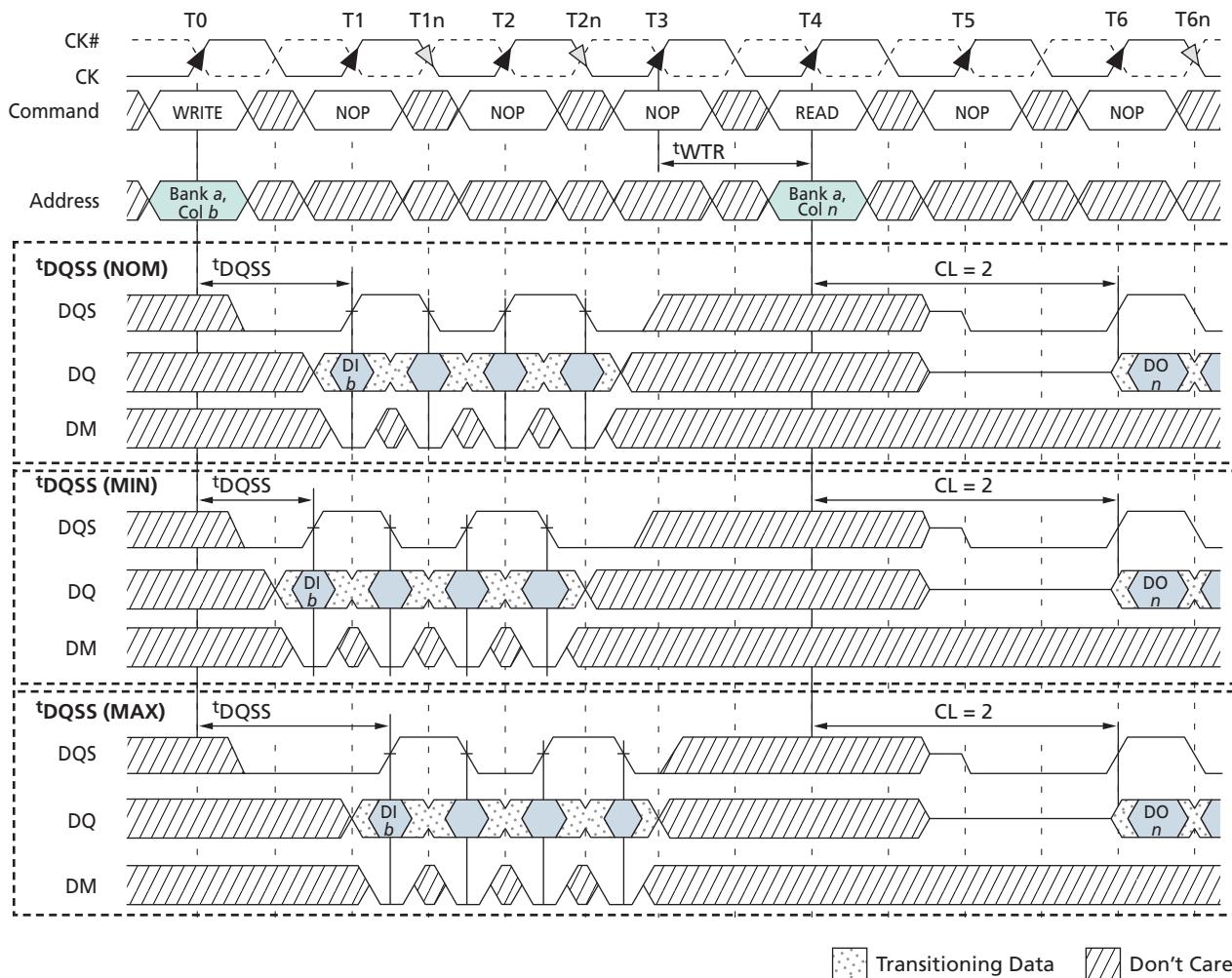
- Notes:
1. DI *b* (or *n*) = data-in from column *b* (or column *n*).
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
  4. An uninterrupted burst of 4 is shown.
  5. Each WRITE command may be to any bank.

**Figure 42: Random WRITE Cycles**

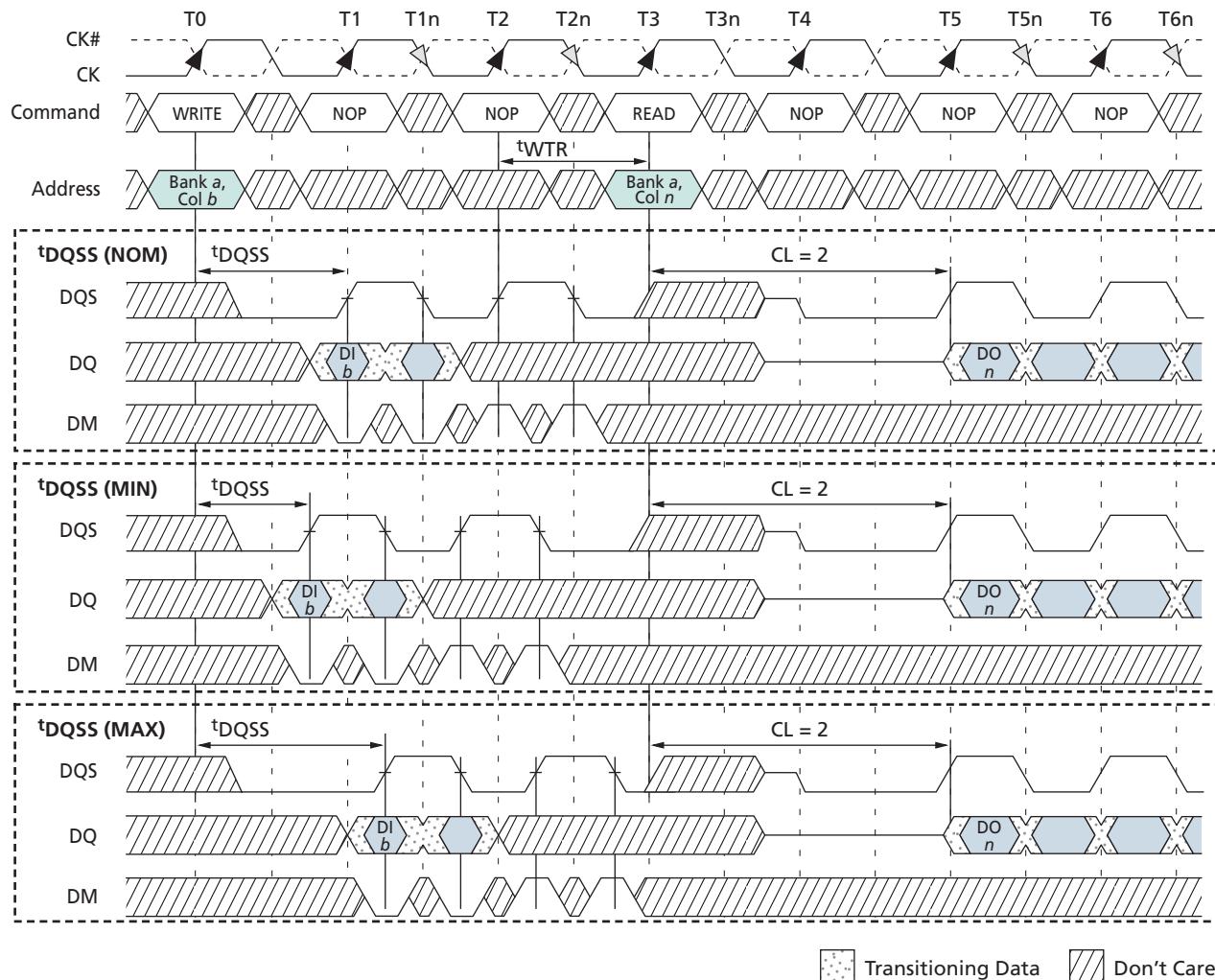


- Notes:
1. DI *b* (or *x* or *n* or *a* or *g*) = data-in from column *b* (or column *x*, or column *n*, or column *a*, or column *g*).
  2. *b'*, *x'*, *n'*, *a'* or *g'* indicate the next data-in following DO *b*, DO *x*, DO *n*, DO *a*, or DO *g*, respectively.
  3. Programmed BL = 2, BL = 4, or BL = 8 in cases shown.
  4. Each WRITE command may be to any bank.

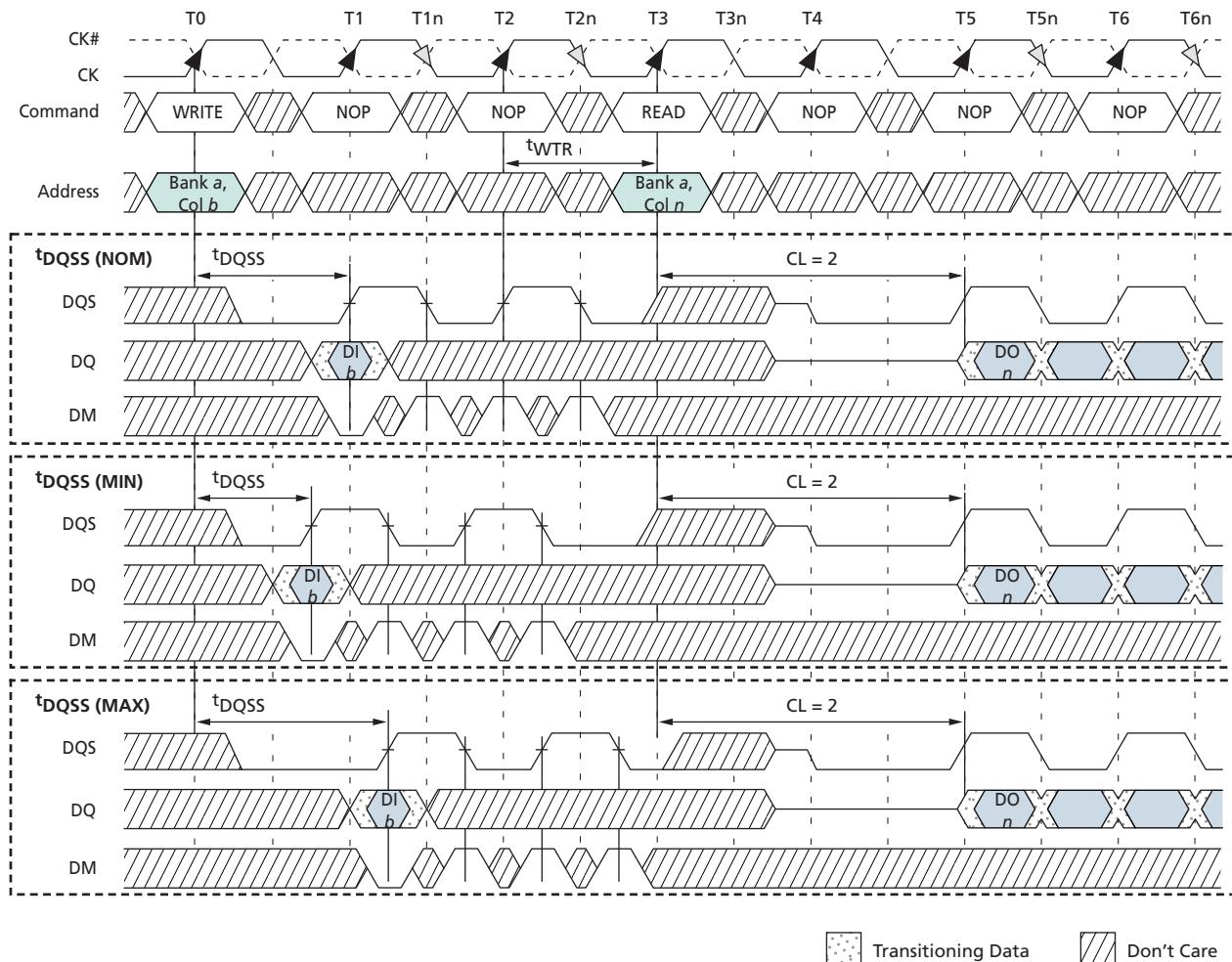
**Figure 43: WRITE-to-READ – Uninterrupting**



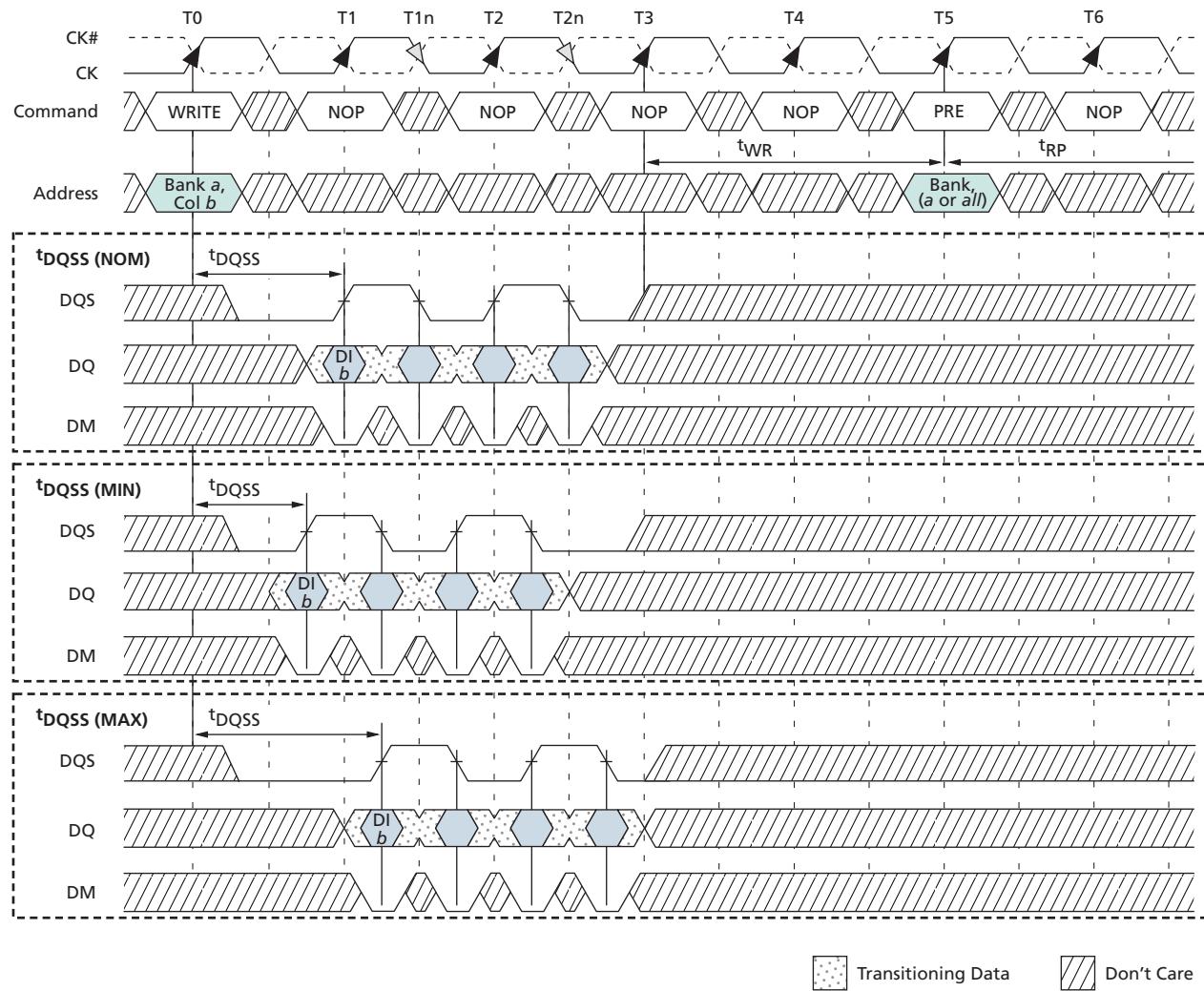
- Notes:
1. DI  $b$  = data-in for column  $b$ ; DO  $n$  = data-out for column  $n$ .
  2. Three subsequent elements of data-in are applied in the programmed order following DI  $b$ .
  3. An uninterrupted burst of 4 is shown.
  4.  $t_{WTR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case  $t_{WTR}$  is not required, and the READ command could be applied earlier.
  6. A10 is LOW with the WRITE command (auto precharge is disabled).

**Figure 44: WRITE-to-READ – Interrupting**


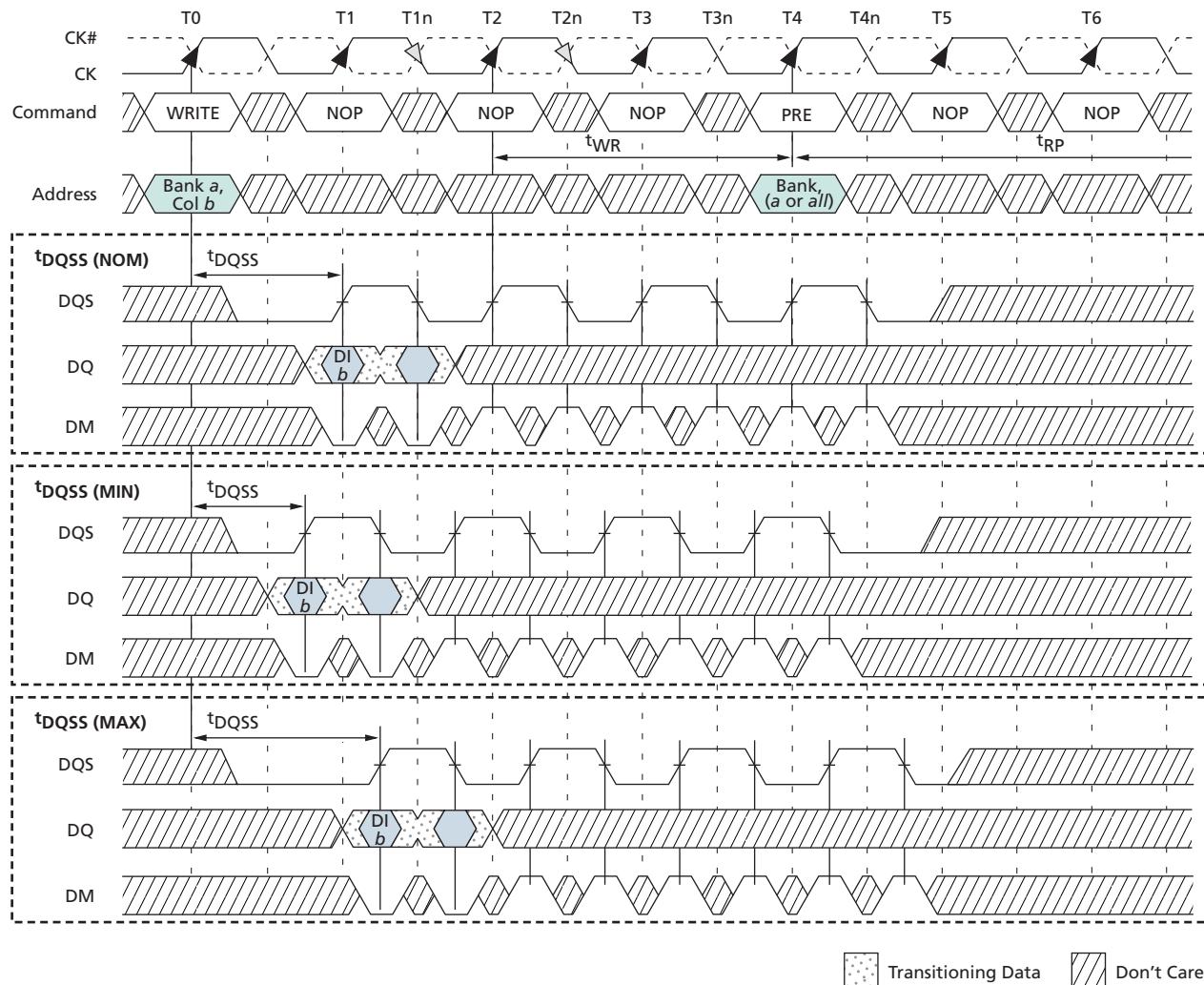
- Notes:
1. DI  $b$  = data-in for column  $b$ ; DO  $n$  = data-out for column  $n$ .
  2. An interrupted burst of 4 is shown; two data elements are written.
  3. One subsequent element of data-in is applied in the programmed order following DI  $b$ .
  4.  $t_{WTR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. A10 is LOW with the WRITE command (auto precharge is disabled).
  6. DQS is required at T2 and T2n (nominal case) to register DM.
  7. If the burst of 8 is used, DM and DQS are required at T3 and T3n because the READ command will not mask these two data elements.

**Figure 45: WRITE-to-READ – Odd Number of Data, Interrupting**


- Notes:
1. DI *b* = data-in for column *b*; DO *n* = data-out for column *n*.
  2. An interrupted burst of 4 is shown; one data element is written.
  3.  $t_{WTR}$  is referenced from the first positive CK edge after the last desired data-in pair (not the last two data elements).
  4. A10 is LOW with the WRITE command (auto precharge is disabled).
  5. DQS is required at T1n, T2, and T2n (nominal case) to register DM.
  6. If the burst of 8 is used, DM and DQS are required at T3-T3n because the READ command will not mask these data elements.

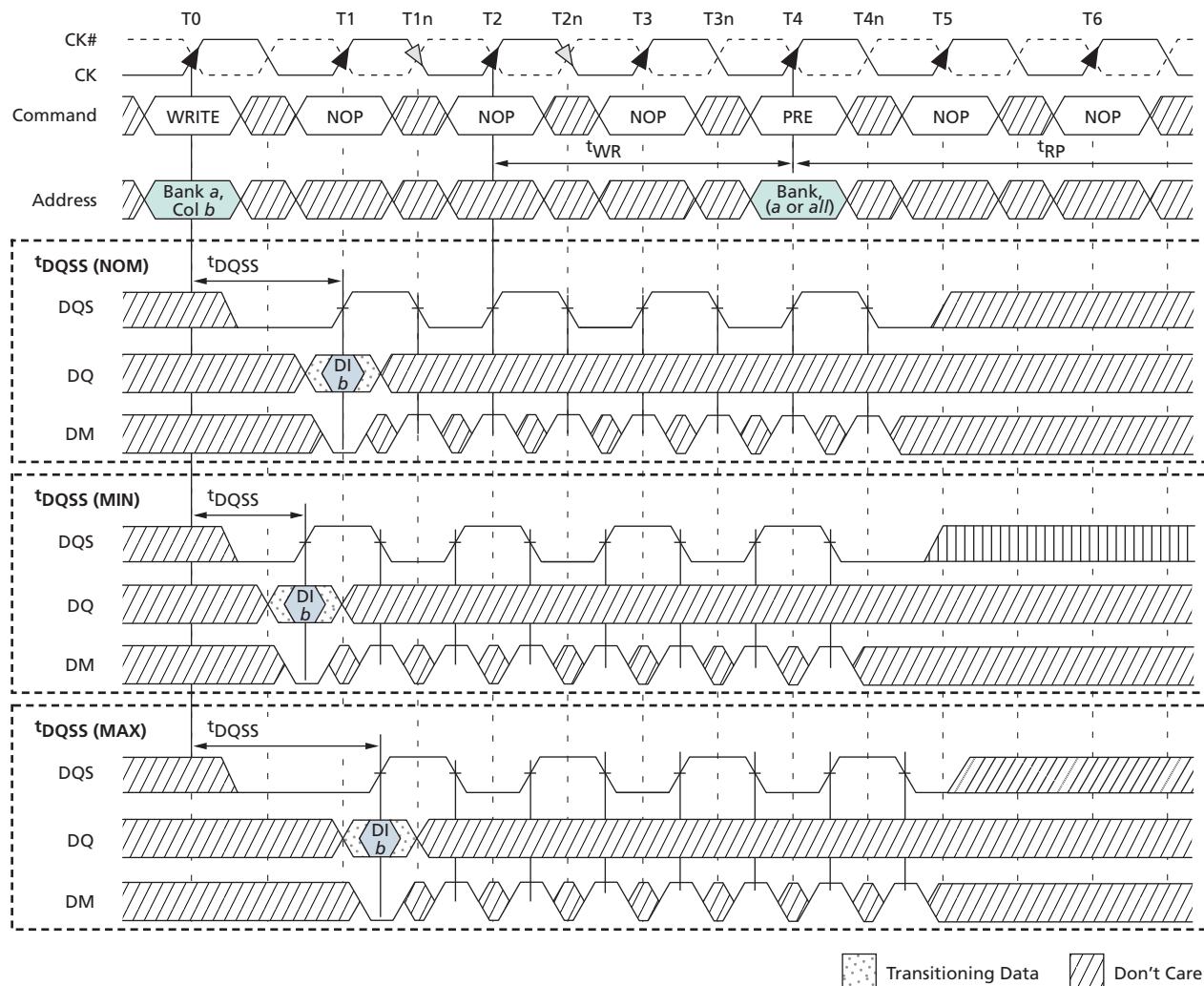
**Figure 46: WRITE-to-PRECHARGE – Uninterrupting**


- Notes:**
1. DI *b* = data-in for column *b*.
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. An uninterrupted burst of 4 is shown.
  4.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case  $t_{WR}$  is not required, and the PRECHARGE command could be applied earlier.
  6. A10 is LOW with the WRITE command (auto precharge is disabled).

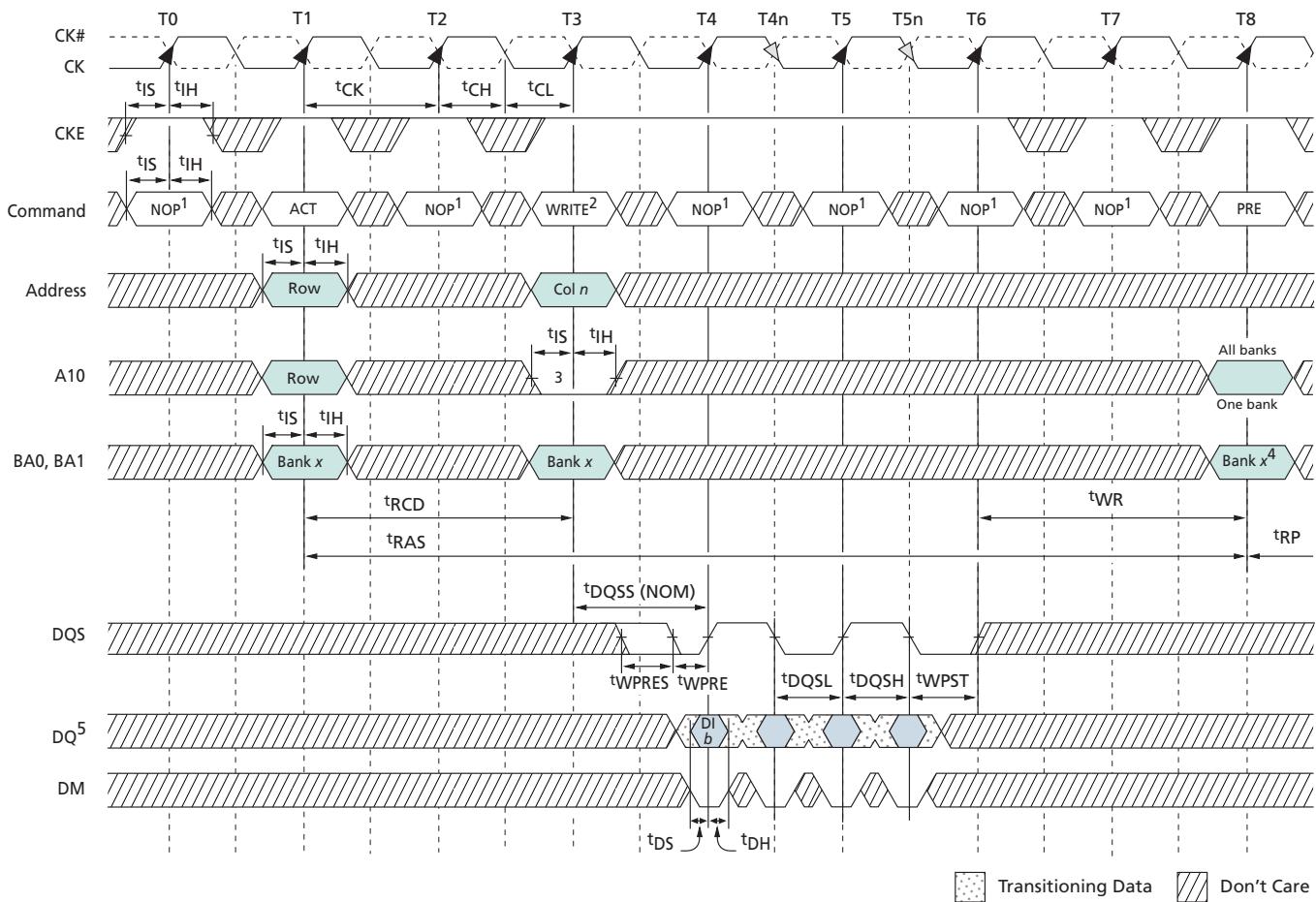
**Figure 47: WRITE-to-PRECHARGE – Interrupting**


- Notes:**
1. DI *b* = data-in for column *b*.
  2. Subsequent element of data-in is applied in the programmed order following DI *b*.
  3. An interrupted burst of 8 is shown; two data elements are written.
  4.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. A10 is LOW with the WRITE command (auto precharge is disabled).
  6. DQS is required at T4 and T4n (nominal case) to register DM.
  7. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

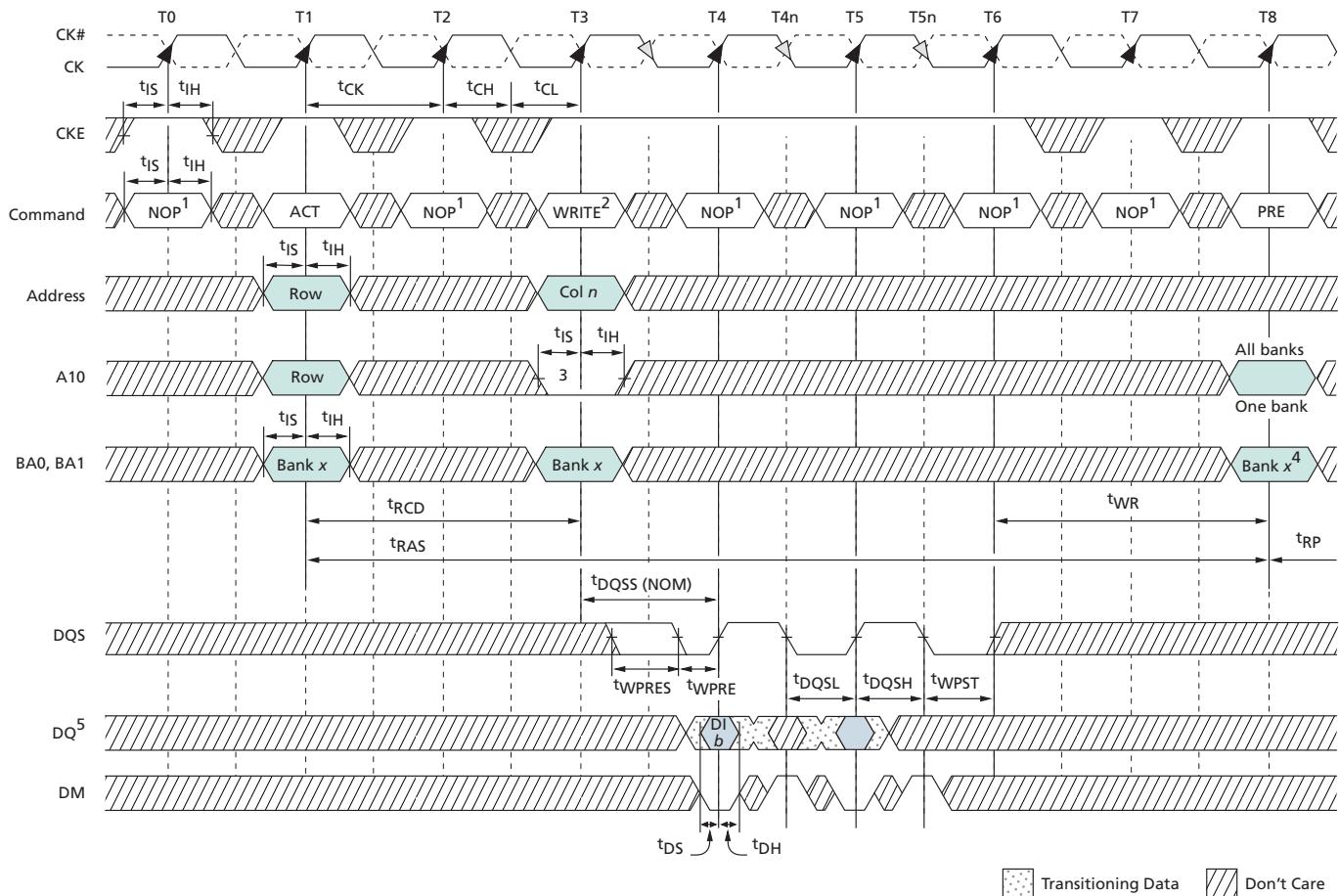
**Figure 48: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting**



- Notes:
1. DI *b* = data-in for column *b*.
  2. An interrupted burst of 8 is shown; one data element is written.
  3.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  4. A10 is LOW with the WRITE command (auto precharge is disabled).
  5. DQS is required at T4 and T4n (nominal case) to register DM.
  6. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

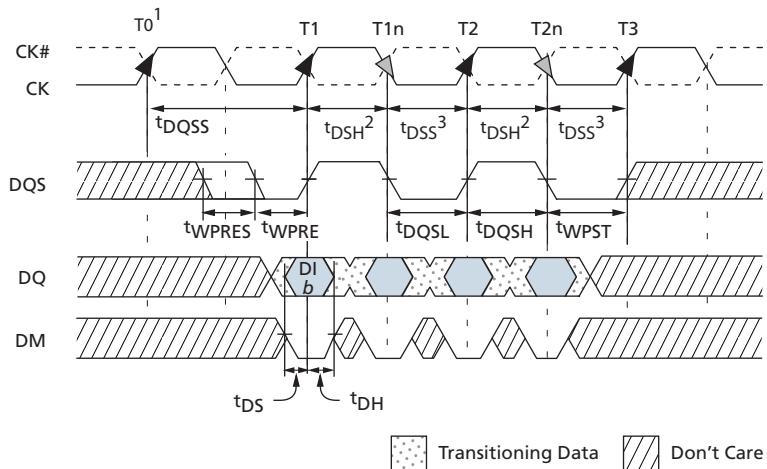
**Figure 49: Bank WRITE – Without Auto Precharge**


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T8.
  5. DI *b* = data-in from column *b*; subsequent elements are provided in the programmed order.
  6. See Figure 51 on page 87 for detailed DQ timing.

**Figure 50: WRITE – DM Operation**


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T8.
  5. DI b = data-in from column b; subsequent elements are provided in the programmed order.
  6. See Figure 51 on page 87 for detailed DQ timing.

**Figure 51: Data Input Timing**



- Notes:**
1. WRITE command issued at  $T_0^1$ .
  2.  $t_{DSH}$  (MIN) generally occurs during  $t_{DQSS}$  (MIN).
  3.  $t_{DSS}$  (MIN) generally occurs during  $t_{DQSS}$  (MAX).
  4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
  5. DI  $b$  = data-in from column  $b$ .

## PRECHARGE

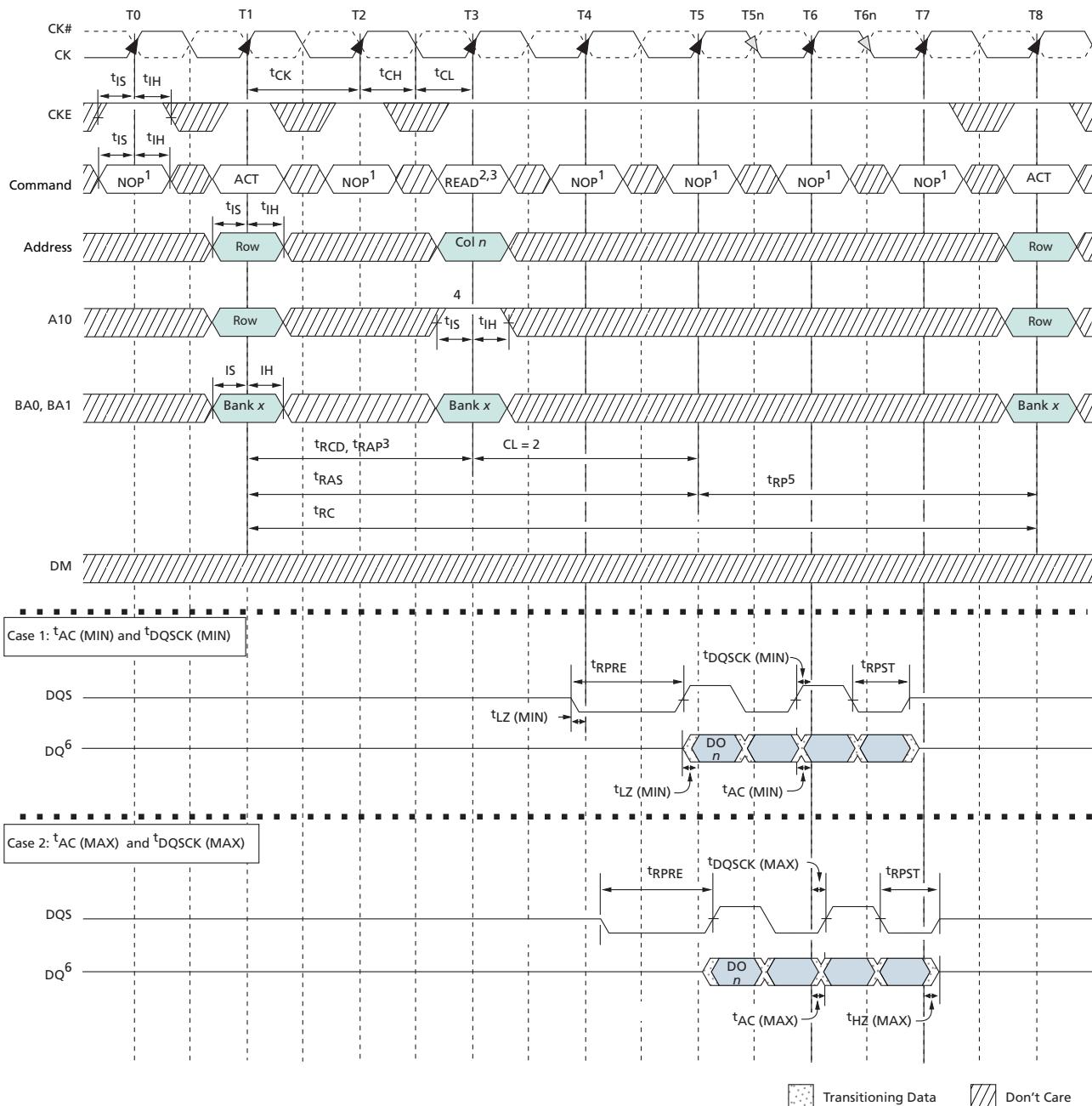
The bank(s) will be available for a subsequent row access a specified time ( $t_{RP}$ ) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. With concurrent auto precharge, a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

## Auto Precharge

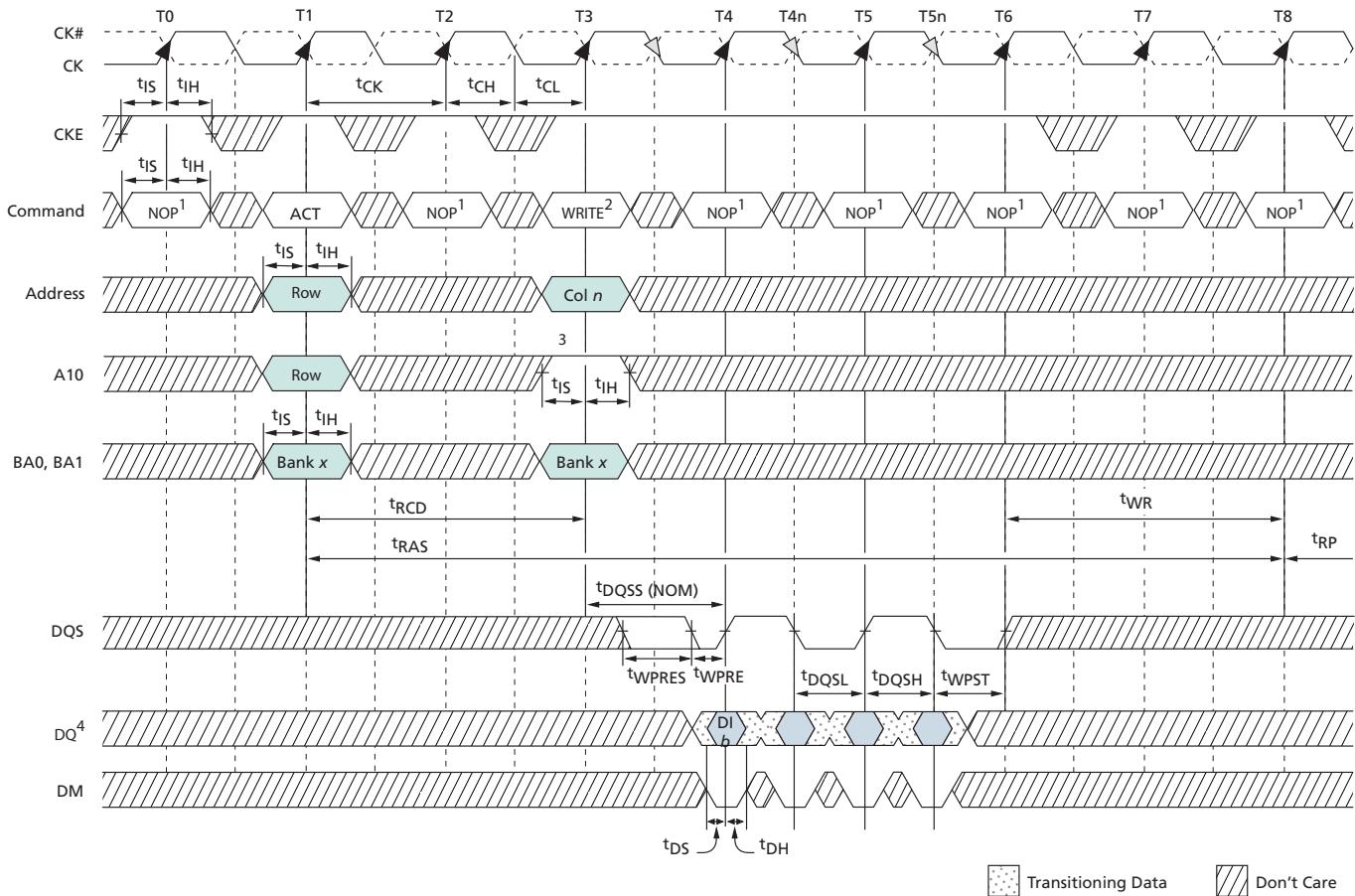
Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating  $t_{RAS}$  (MIN), as described for each burst type in “Operations” on page 54. The user must not issue another command to the same bank until the precharge time ( $t_{RP}$ ) is completed.

**Figure 52: Bank READ – with Auto Precharge**



- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4.
  3. The READ command can only be applied at T3 if  $t_{RAP}$  is satisfied at T3.
  4. Enable auto precharge.
  5.  $t_{RP}$  starts only after  $t_{RAS}$  has been satisfied.
  6. DO  $n$  = data-out from column  $n$ ; subsequent elements are provided in the programmed order.
  7. Refer to Figure 36 on page 72, Figure 37 on page 73, and Figure 38 on page 74 for detailed DQS and DQ timing.

**Figure 53: Bank WRITE – with Auto Precharge**


- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  2. BL = 4.
  3. Enable auto precharge.
  4. DI  $n$  = data-out from column  $n$ ; subsequent elements are provided in the programmed order.
  5. See Figure 51 on page 87 for detailed DQ timing.

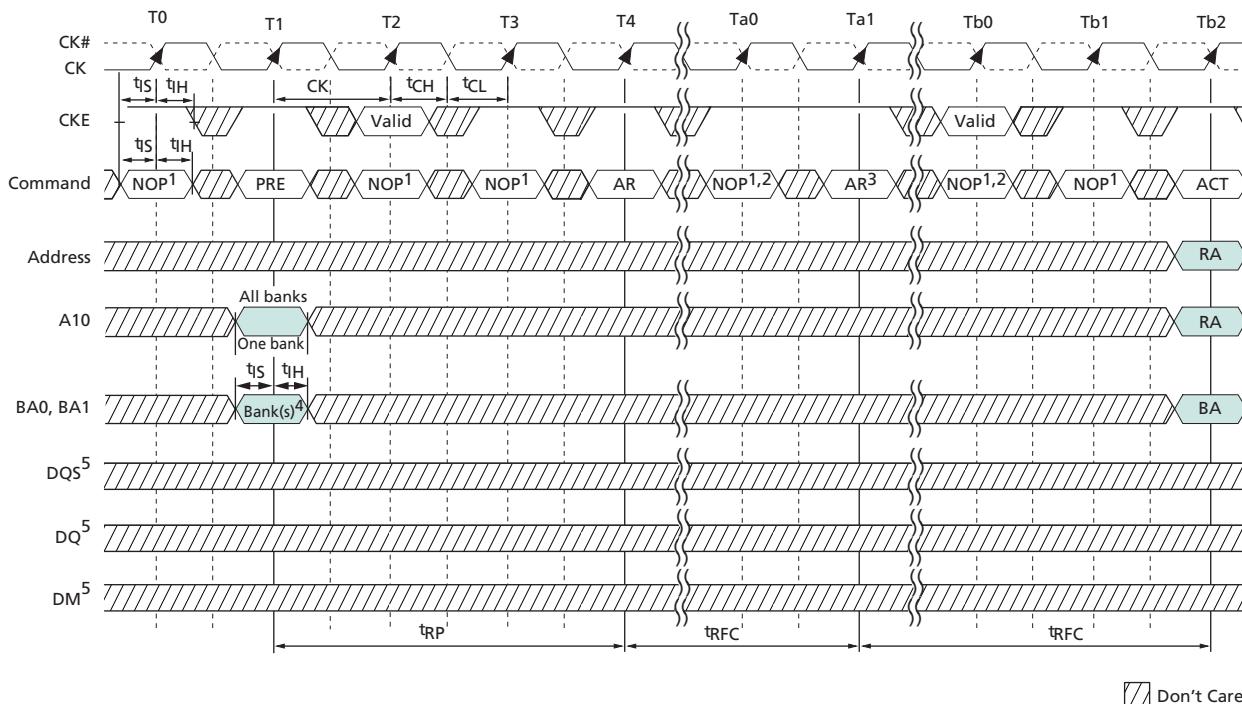
## AUTO REFRESH

During auto refresh, the addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average interval of  $t_{REFI} (\text{MAX})$ .

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is  $9 \times t_{REFI} (= t_{REFC})$ . JEDEC specifications only support  $8 \times t_{REFI}$ ; Micron specifications exceed the JEDEC requirement by one clock. This maximum absolute interval is to allow future support for DLL updates, internal to the DDR SDRAM, to be restricted to AUTO REFRESH cycles, without allowing excessive drift in  $t_{AC}$  between updates.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends  $t_{RFC}$  later.

**Figure 54: Auto Refresh Mode**



- Notes:**
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock-positive transitions.
  2. NOP or COMMAND INHIBIT are the only commands allowed until after  $t_{RFC}$  time; CKE must be active during clock-positive transitions.
  3. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.
  4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (that is, must precharge all active banks).
  5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for the operations shown.

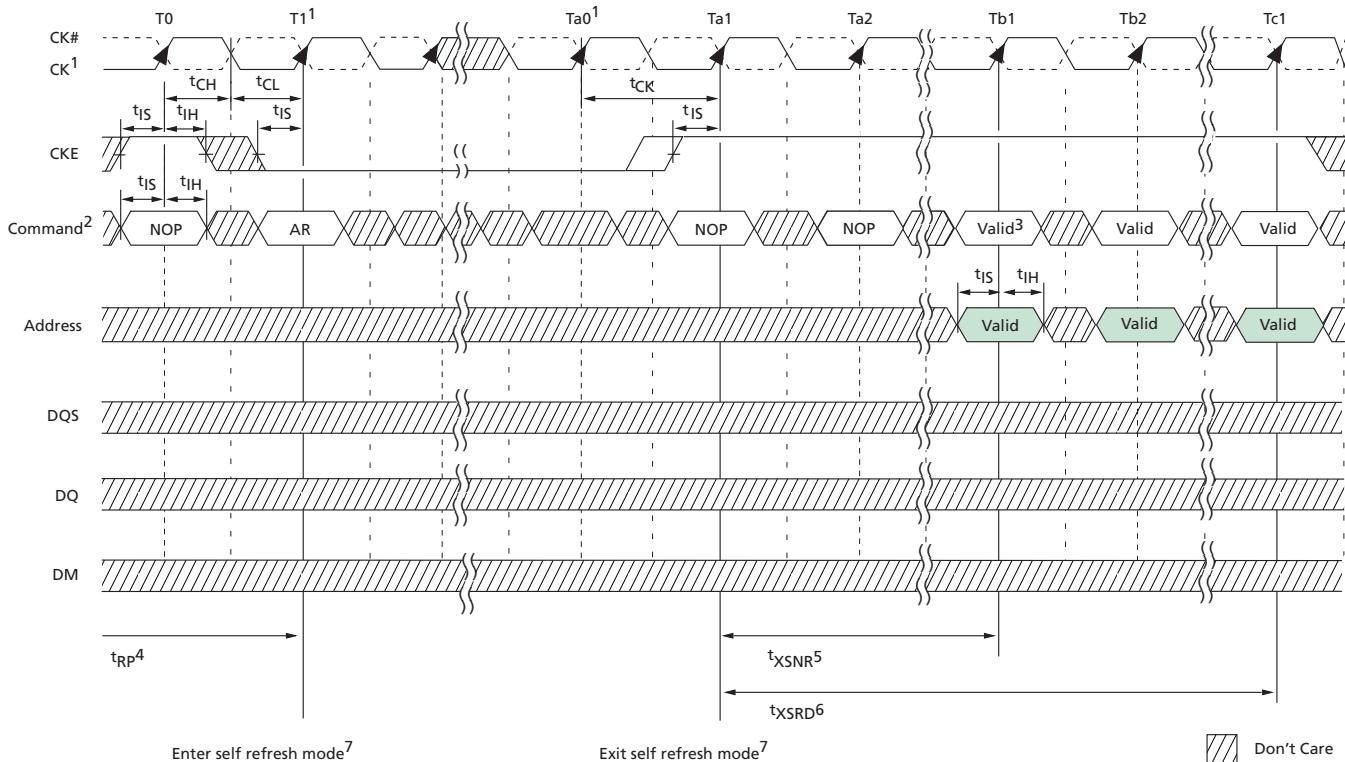
## SELF REFRESH

When in the self refresh mode, the DDR SDRAM retains data without external clocking. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH (a DLL reset and 200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH.  $V_{REF}$  voltage is also required for the full duration of SELF REFRESH.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for  $t_{XSNR}$  because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for  $t_{XSRD}$  time, then a DLL RESET (via

the extended mode register) and NOPs for 200 additional clock cycles before applying a READ. Any command other than a READ can be performed  $t_{XSNR}^{(MIN)}$  after the DLL reset. NOP or DESELECT commands must be issued during the  $t_{XSNR}^{(MIN)}$  time.

**Figure 55: Self Refresh Mode**



- Notes:**
1. Clock must be stable until after the SELF REFRESH command has been registered. A change in clock frequency is allowed before  $Ta0$ , provided it is within the specified  $t_{CK}$  limits. Regardless, the clock must be stable before exiting self refresh mode—that is, the clock must be cycling within specifications by  $Ta0$ .
  2. NOPs are interchangeable with DESELECT commands.
  3. AUTO REFRESH is not required at this point but is highly recommended.
  4. Device must be in the all banks idle state prior to entering self refresh mode.
  5.  $t_{XSNR}$  is required before any non-READ command can be applied; that is only NOP or DESELECT commands are allowed until  $Tb1$ .
  6.  $t_{XSRD}$  (200 cycles of a valid clock with  $CKE = HIGH$ ) is required before any READ command can be applied.
  7. As a general rule, any time self refresh mode is exited, the DRAM may not re-enter the self refresh mode until all rows have been refreshed via the AUTO REFRESH command at the distributed refresh rate,  $t_{REFI}$ , or faster. However, the self refresh mode may be re-entered anytime after exiting if each of the following conditions is met:
    - a. The DRAM had been in the self refresh mode for a minimum of 200ms prior to exiting.
    - b.  $t_{XSNR}$  and  $t_{XSRD}$  are not violated.
    - c. At least two AUTO REFRESH commands are performed during each  $t_{REFI}$  interval while the DRAM remains out of self refresh mode.
  8. If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.
  9. Once the device is initialized,  $V_{REF}$  must always be powered within specified range.

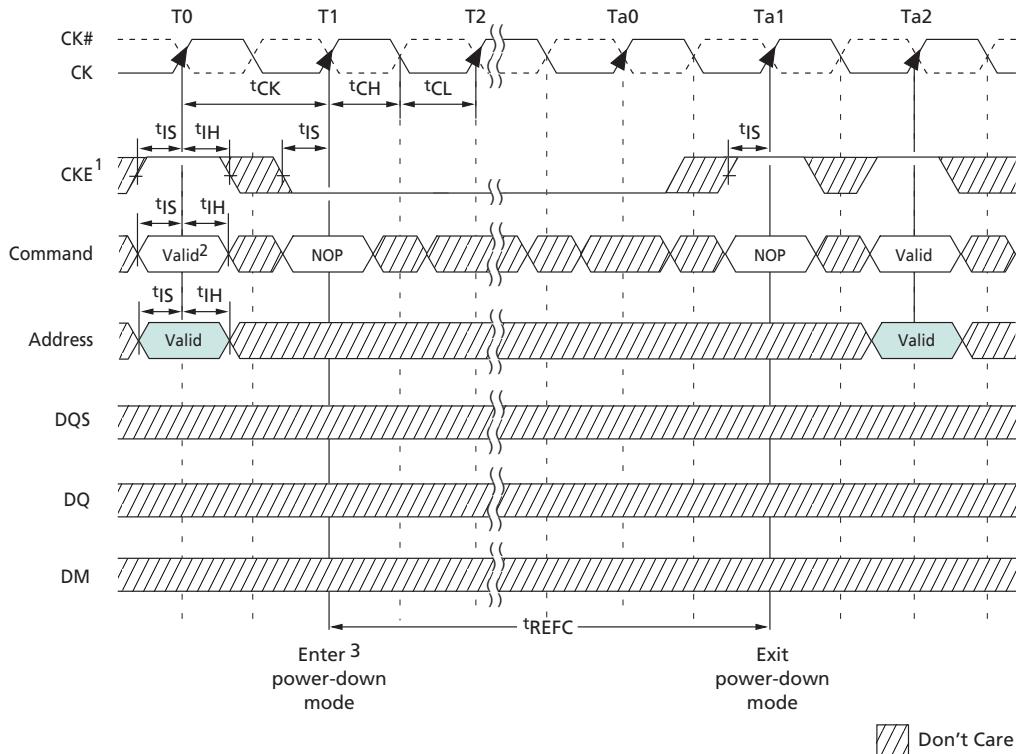
## Power-down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress, from the issuing of a READ or WRITE command, until completion of the access. Thus a clock suspend is not supported. For READs, an access completion is defined when the read postamble is satisfied; for WRITEs, when the write recovery time ( $t_{WR}$ ) is satisfied.

Power-down, as shown in Figure 56 on page 93, is entered when CKE is registered LOW and all criteria in Table 35 on page 49 are met. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when a row is active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. For maximum power savings, the DLL is frozen during precharge power-down mode. Exiting power-down requires the device to be at the same voltage and frequency as when it entered power-down. However, power-down duration is limited by the refresh requirements of the device ( $t_{REFC}$ ).

While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

**Figure 56: Power-Down Mode**



- Notes:
- Once initialized,  $V_{REF}$  must always be powered within the specified range.
  - If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
  - No column accesses are allowed to be in progress at the time power-down is entered.

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[www.micron.com/productsupport](http://www.micron.com/productsupport) Customer Comment Line: 800-932-4992

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SN5476, SN54LS76A  
SN7476, SN74LS76A  
**DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR**  
SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

### description

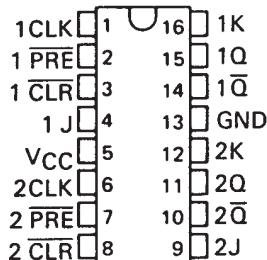
The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7476 and the SN74LS76A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN5476, SN54LS76A . . . J PACKAGE**  
**SN7476 . . . N PACKAGE**  
**SN74LS76A . . . D OR N PACKAGE**

(TOP VIEW)



**'76**  
**FUNCTION TABLE**

| INPUTS |     |     |   |   | OUTPUTS        |                |
|--------|-----|-----|---|---|----------------|----------------|
| PRE    | CLR | CLK | J | K | Q              | $\bar{Q}$      |
| L      | H   | X   | X | X | H              | L              |
| H      | L   | X   | X | X | L              | H              |
| L      | L   | X   | X | X | H <sup>†</sup> | H <sup>†</sup> |
| H      | H   | ↓   | L | L | Q <sub>0</sub> | $\bar{Q}_0$    |
| H      | H   | ↓   | H | L | H              | L              |
| H      | H   | ↓   | L | H | L              | H              |
| H      | H   | ↓   | H | H | TOGGLE         |                |

**'LS76A**  
**FUNCTION TABLE**

| INPUTS |     |     |   |   | OUTPUTS        |                |
|--------|-----|-----|---|---|----------------|----------------|
| PRE    | CLR | CLK | J | K | Q              | $\bar{Q}$      |
| L      | H   | X   | X | X | H              | L              |
| H      | L   | X   | X | X | L              | H              |
| L      | L   | X   | X | X | H <sup>†</sup> | H <sup>†</sup> |
| H      | H   | ↓   | L | L | Q <sub>0</sub> | $\bar{Q}_0$    |
| H      | H   | ↓   | H | L | H              | L              |
| H      | H   | ↓   | L | H | L              | H              |
| H      | H   | ↓   | H | H | TOGGLE         |                |
| H      | H   | H   | X | X | Q <sub>0</sub> | $\bar{Q}_0$    |

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5476, SN54LS76A

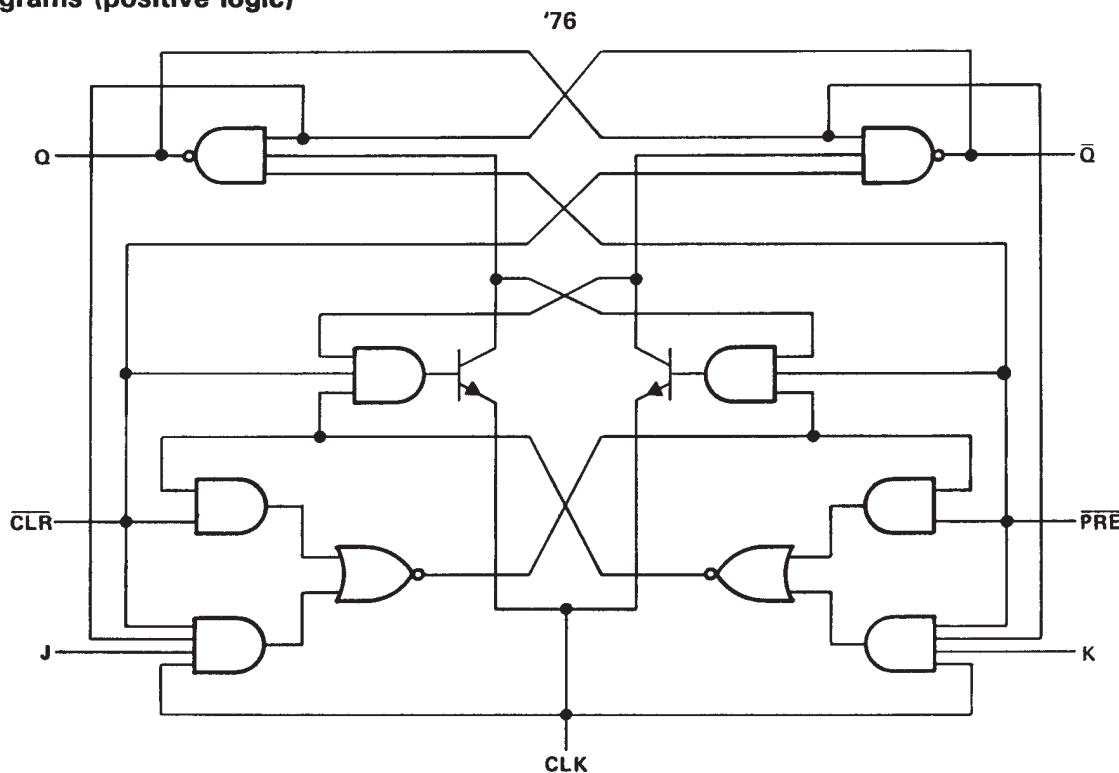
SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

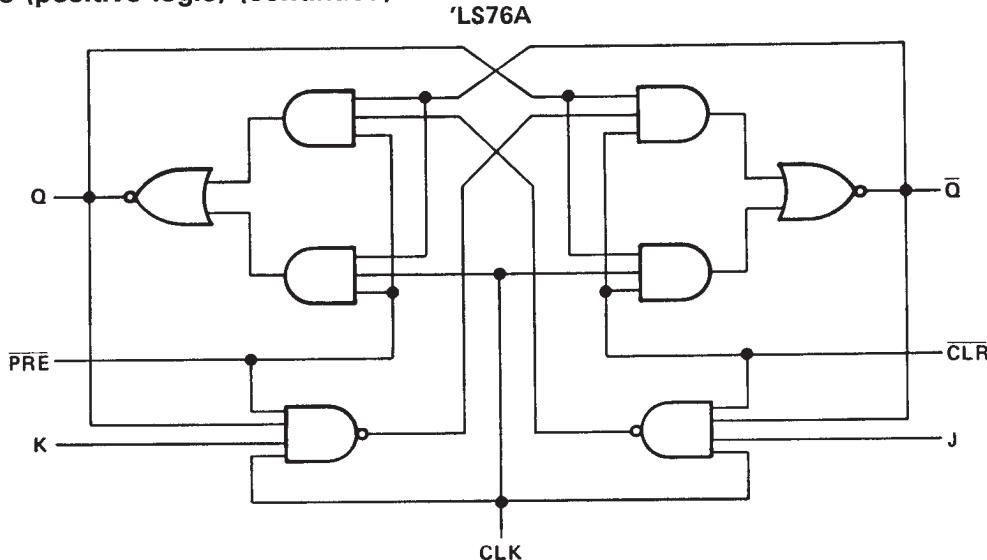
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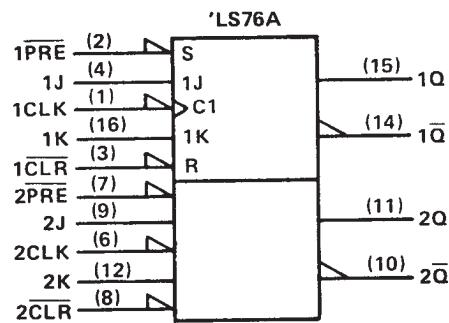
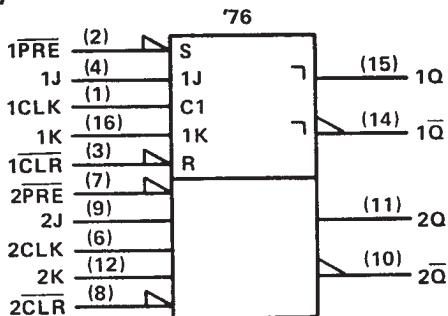
### logic diagrams (positive logic)



logic diagrams (positive logic) (continued)

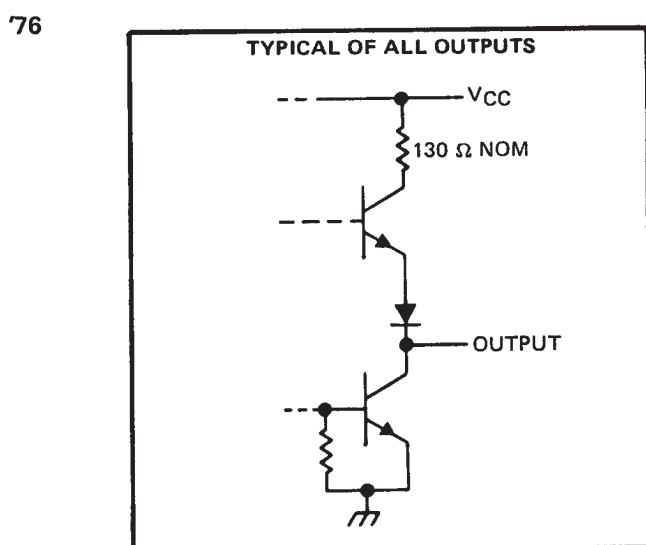
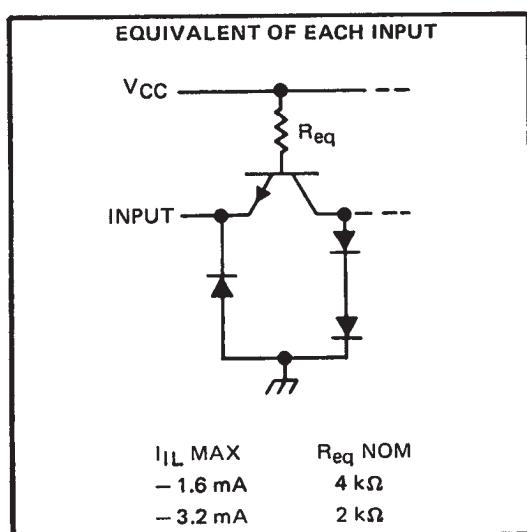


logic symbols<sup>†</sup>



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN5476, SN54LS76A

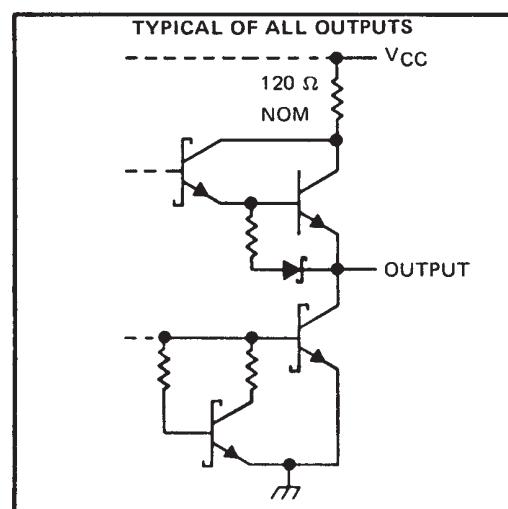
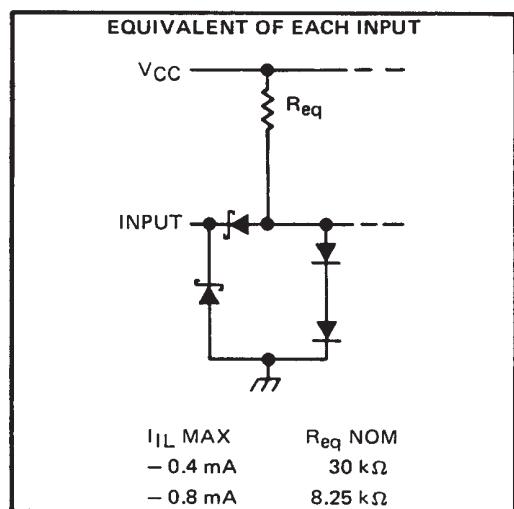
SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 - DECEMBER 1983 - REVISED MARCH 1988

### schematics of inputs and outputs (continued)

'LS76A



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub> (see Note 1) . . . . . | 7 V            |
| Input voltage: '76 . . . . .                           | 5.5 V          |
| 'LS76A . . . . .                                       | 7 V            |
| Operating free-air temperature range: SN54' . . . . .  | -55°C to 125°C |
| SN74' . . . . .  | 0°C to 70°C    |
| Storage temperature range . . . . .                    | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN5476, SN54LS76A  
SN7476, SN74LS76A  
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR  
SDS121 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

|                 |                                  | SN5476         |     |      | SN7476 |     |      | UNIT |
|-----------------|----------------------------------|----------------|-----|------|--------|-----|------|------|
|                 |                                  | MIN            | NOM | MAX  | MIN    | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                   | 4.5            | 5   | 5.5  | 4.75   | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage         | 2              |     |      | 2      |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage          |                |     | 0.8  |        |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current        |                |     | -0.4 |        |     | -0.4 | mA   |
| I <sub>OL</sub> | Low-level output current         |                |     | 16   |        |     | 16   | mA   |
| t <sub>w</sub>  | Pulse duration                   | CLK high       | 20  |      | 20     |     |      | ns   |
|                 |                                  | CLK low        | 47  |      | 47     |     |      |      |
|                 |                                  | PRE or CLR low | 25  |      | 25     |     |      |      |
| t <sub>su</sub> | Input setup time before CLK ↑    |                | 0   |      | 0      |     |      | ns   |
| t <sub>h</sub>  | Input hold time-data after CLK ↓ |                | 0   |      | 0      |     |      | ns   |
| T <sub>A</sub>  | Operating free-air temperature   | -55            |     | 125  | 0      |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                    | TEST CONDITIONS <sup>†</sup>   | SN5476 |                  |      | SN7476 |                  |      | UNIT |
|------------------------------|--|--------|------------------|------|--------|------------------|------|------|
|                              |  | MIN    | TYP <sup>‡</sup> | MAX  | MIN    | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IK</sub>              | V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA   |        |                  | -1.5 |        |                  | -1.5 | V    |
| V <sub>OH</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA | 2.4    | 3.4              |      | 2.4    | 3.4              |      | V    |
| V <sub>OL</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA   |        | 0.2              | 0.4  |        | 0.2              | 0.4  | V    |
| I <sub>I</sub>               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V  |        |                  | 1    |        |                  | 1    | mA   |
| I <sub>IH</sub>              | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V  |        | 40               |      |        | 40               |      | μA   |
|                              |  |        | 80               |      |        | 80               |      |      |
| I <sub>IIL</sub>             | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V  |        | -1.6             |      |        | -1.6             |      | mA   |
|                              |  |        | -3.2             |      |        | -3.2             |      |      |
| I <sub>OS</sub> <sup>§</sup> | V <sub>CC</sub> = MAX  | -20    | -57              | -18  | -57    |                  |      | mA   |
| I <sub>CC</sub> <sup>#</sup> | V <sub>CC</sub> = MAX, See Note 2  | 10     | 20               |      | 10     | 20               |      | mA   |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time.

<sup>¶</sup> Clear is tested with preset high and preset is tested with clear high.

<sup>#</sup> Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

| PARAMETER        | FROM (INPUT)                                       | TO (OUTPUT)    | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |  |
|------------------|--|----------------|--|-----|-----|-----|------|--|
| f <sub>max</sub> |  |                | R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF | 15  | 20  |     | MHz  |  |
| t <sub>PLH</sub> | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\bar{Q}$ |  | 16  | 25  |     | ns   |  |
| t <sub>PHL</sub> |  |                |  | 25  | 40  |     | ns   |  |
| t <sub>PLH</sub> | CLK  | Q or $\bar{Q}$ |  | 16  | 25  |     | ns   |  |
| t <sub>PHL</sub> |  |                |  | 25  | 40  |     | ns   |  |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5476, SN54LS76A

SN7476, SN74LS76A

## DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

### recommended operating conditions

|                    |                                |                  | SN54LS76A | SN74LS76A | UNIT |      |     |      |      |
|--------------------|--------------------------------|------------------|-----------|-----------|------|------|-----|------|------|
|                    |                                |                  | MIN       | NOM       | MAX  | MIN  | NOM | MAX  | UNIT |
| V <sub>CC</sub>    | Supply voltage                 |                  | 4.5       | 5         | 5.5  | 4.75 | 5   | 5.75 | V    |
| V <sub>IH</sub>    | High-level input voltage       |                  | 2         |           |      | 2    |     |      | V    |
| V <sub>IL</sub>    | Low-level input voltage        |                  |           |           | 0.7  |      |     | 0.8  | V    |
| I <sub>OH</sub>    | High-level output current      |                  |           |           | -0.4 |      |     | -0.4 | mA   |
| I <sub>OL</sub>    | Low-level output current       |                  |           |           | 4    |      |     | 8    | mA   |
| f <sub>clock</sub> | Clock frequency                |                  | 0         |           | 30   | 0    |     | 30   | MHz  |
| t <sub>w</sub>     | Pulse duration                 | CLK high         | 20        |           |      | 20   |     |      | ns   |
|                    |                                | PRE or CLR low   | 25        |           |      | 25   |     |      |      |
| t <sub>su</sub>    | Setup time before CLK↓         | data high or low | 20        |           |      | 20   |     |      | ns   |
|                    |                                | CLR inactive     | 20        |           |      | 20   |     |      |      |
|                    |                                | PRE inactive     | 25        |           |      | 25   |     |      |      |
| t <sub>h</sub>     | Hold time-data after CLK↓      |                  | 0         |           |      | 0    |     |      | ns   |
| T <sub>A</sub>     | Operating free-air temperature |                  | -55       |           | 125  | 0    |     | 70   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS†   | SN54LS76A                                     |      |      | SN74LS76A |      |      | UNIT |
|-------------------------|--|---|------|------|-----------|------|------|------|
|                         |  | MIN   | TYP‡ | MAX  | MIN       | TYP‡ | MAX  |      |
| V <sub>IK</sub>         | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA   |   |      | -1.5 |           |      | -1.5 | V    |
| V <sub>OH</sub>         | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA | 2.5   | 3.4  |      | 2.7       | 3.4  |      | V    |
| V <sub>OL</sub>         | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA    |   | 0.25 | 0.4  | 0.25      | 0.4  |      | V    |
|                         | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA    |   |      |      | 0.35      | 0.5  |      |      |
| I <sub>I</sub>          | J or K<br>CLR or PRE<br>CLK  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V   |      | 0.1  |           | 0.1  |      | mA   |
|                         |  |   |      | 0.3  |           | 0.3  |      |      |
|                         |  |   |      | 0.4  |           | 0.4  |      |      |
| I <sub>IH</sub>         | J or K<br>CLR or PRE<br>CLK  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |      | 20   |           | 20   |      | μA   |
|                         |  |   |      | 60   |           | 60   |      |      |
|                         |  |   |      | 80   |           | 80   |      |      |
| I <sub>IL</sub>         | J or K   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |      | -0.4 |           | -0.4 |      | mA   |
|                         | All other  |   |      | -0.8 |           | -0.8 |      |      |
| I <sub>OS\$</sub>       | V <sub>CC</sub> = MAX, See Note 4  |   | -20  | -100 | -20       | -100 |      | mA   |
| I <sub>CC</sub> (Total) | V <sub>CC</sub> = MAX, See Note 2  |   | 4    | 6    | 4         | 6    |      | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
|                  |                 |                |   | 30  | 45  |     | MHz  |
| f <sub>max</sub> |                 |                | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF |     |     |     |      |
| t <sub>PLH</sub> | PRE, CLR or CLK | Q or $\bar{Q}$ |   |     | 15  | 20  | ns   |
| t <sub>PHL</sub> |                 |                |   |     | 15  | 20  | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)         | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|---------------------------------|---|
| 5962-9557501QEA  | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QE<br>A<br>SNJ5476J | <span style="background-color: red; color: white;">Samples</span> |
| 5962-9557501QFA  | ACTIVE        | CFP          | W               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QF<br>A<br>SNJ5476W | <span style="background-color: red; color: white;">Samples</span> |
| 5962-9557501QFA  | ACTIVE        | CFP          | W               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QF<br>A<br>SNJ5476W | <span style="background-color: red; color: white;">Samples</span> |
| 7601301EA        | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7601301EA<br>SNJ54LS76AJ        | <span style="background-color: red; color: white;">Samples</span> |
| 7601301EA        | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7601301EA<br>SNJ54LS76AJ        | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/00204BEA | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>00204BEA            | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/00204BEA | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>00204BEA            | <span style="background-color: red; color: white;">Samples</span> |
| M38510/00204BEA  | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>00204BEA            | <span style="background-color: red; color: white;">Samples</span> |
| M38510/00204BEA  | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>00204BEA            | <span style="background-color: red; color: white;">Samples</span> |
| SN5476J          | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5476J                         | <span style="background-color: red; color: white;">Samples</span> |
| SN5476J          | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5476J                         | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS76AJ       | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS76AJ                      | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS76AJ       | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS76AJ                      | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5476J         | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QE<br>A<br>SNJ5476J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5476J         | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QE<br>A             | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)   | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|---------------------------|---|
|                  |               |              |                 |      |             |                      |                                      |                      |              | SNJ5476J                  |   |
| SNJ5476W         | ACTIVE        | CFP          | W               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QF A SNJ5476W | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5476W         | ACTIVE        | CFP          | W               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9557501QF A SNJ5476W | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS76AJ      | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7601301EA SNJ54LS76AJ     | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS76AJ      | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7601301EA SNJ54LS76AJ     | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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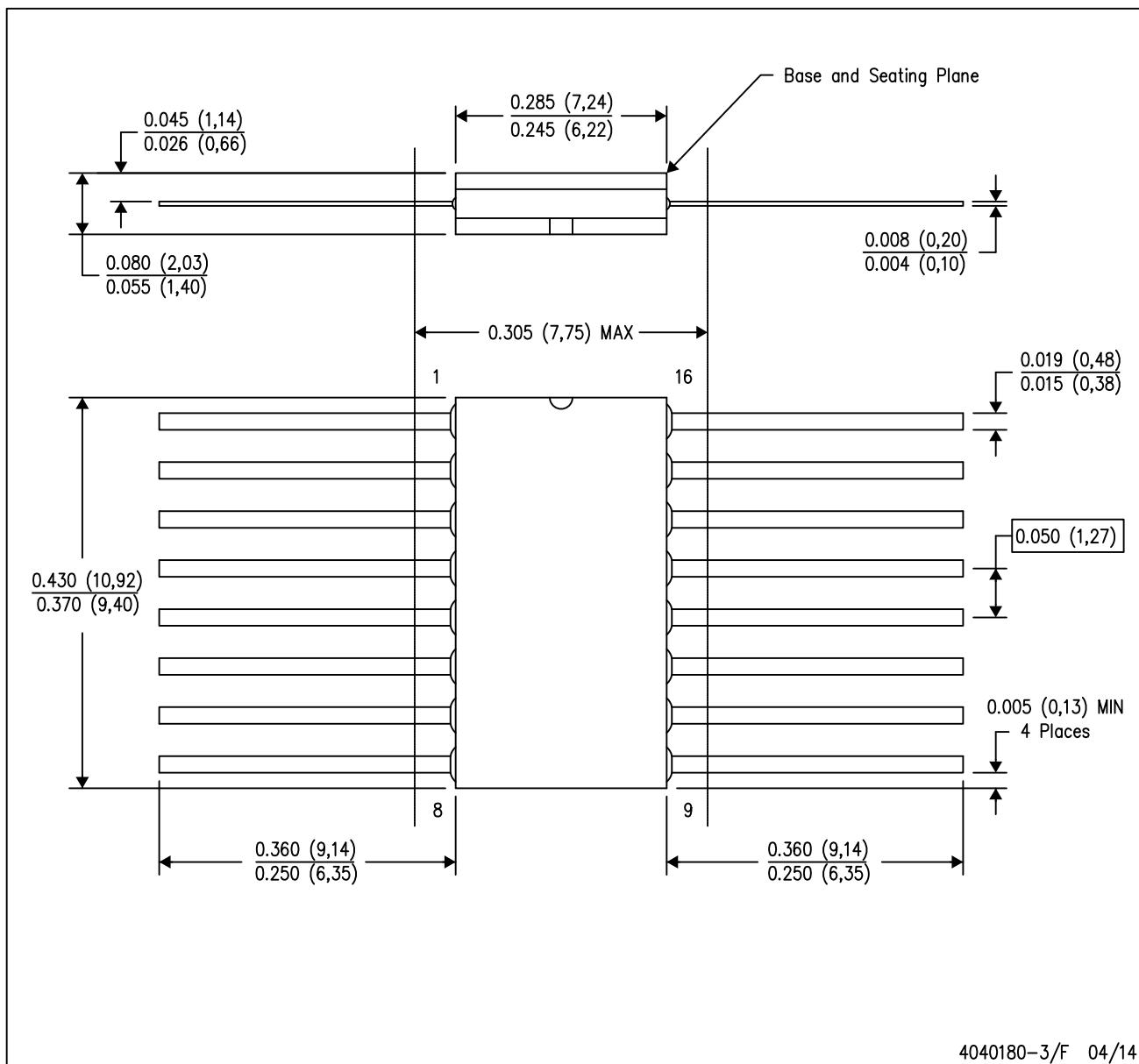
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## MECHANICAL DATA

W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



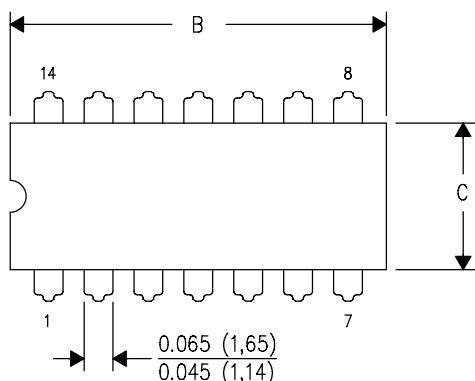
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

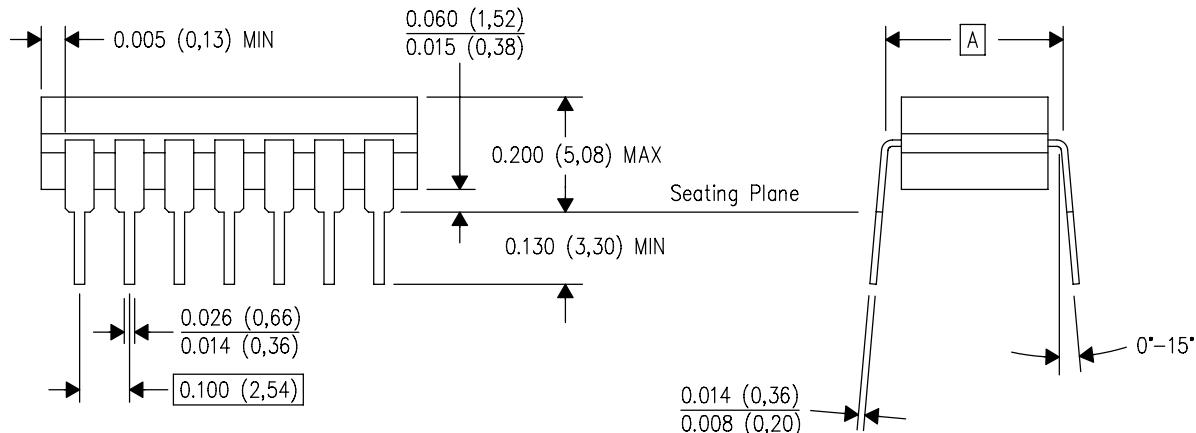
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **\nDIM | 14                     | 16                     | 18                     | 20                     |
|--------------|------------------------|------------------------|------------------------|------------------------|
| A            | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX        | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN        | —                      | —                      | —                      | —                      |
| C MAX        | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN        | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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**SN5430, SN54LS30, SN54S30  
SN7430, SN74LS30, SN74S30  
8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

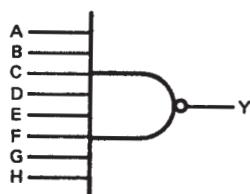
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7430, SN74LS30, and SN74S30 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

| INPUTS A THRU H      | OUTPUT Y |
|----------------------|----------|
| All inputs H         | L        |
| One or more inputs L | H        |

#### logic diagram

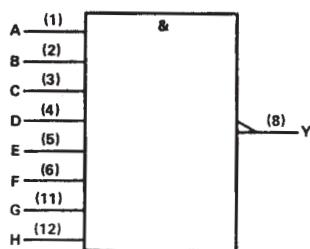


#### positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

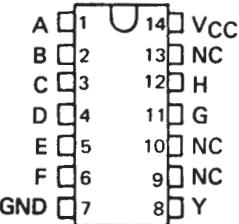
#### logic symbol†



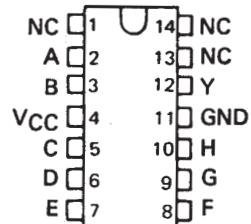
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

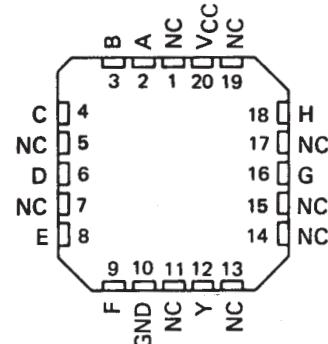
SN5430 . . . J PACKAGE  
SN54LS30, SN54S30 . . . J OR W PACKAGE  
SN7430 . . . N PACKAGE  
SN74LS30, SN74S30 . . . D OR N PACKAGE  
(TOP VIEW)



SN5430 . . . W PACKAGE  
(TOP VIEW)



SN54LS30, SN54S30 . . . FK PACKAGE  
(TOP VIEW)

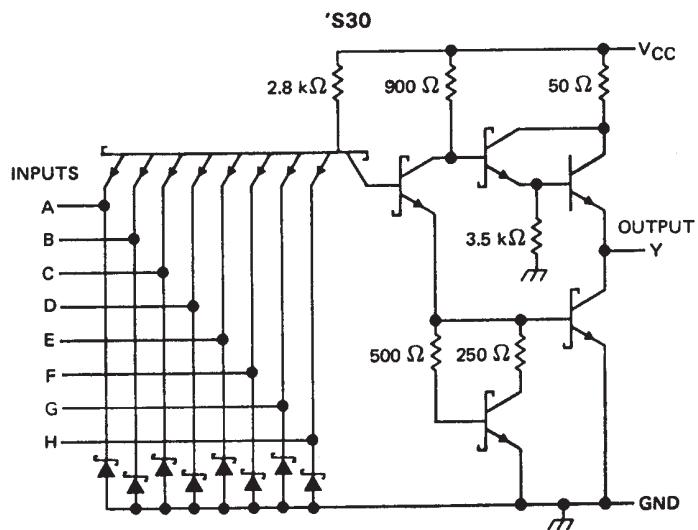
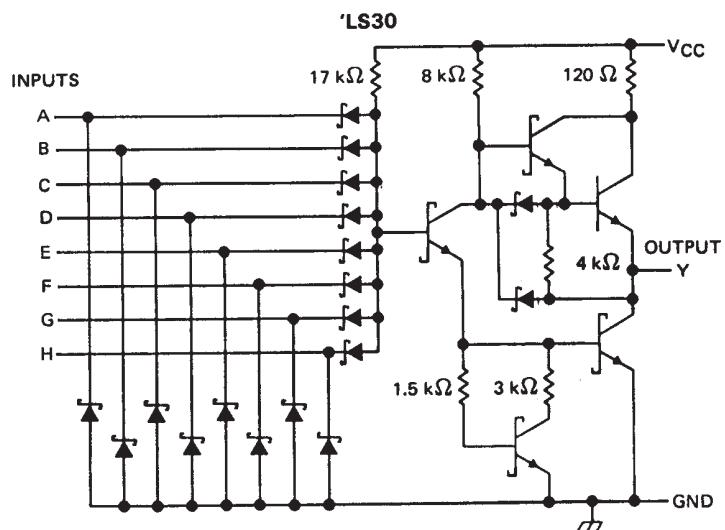
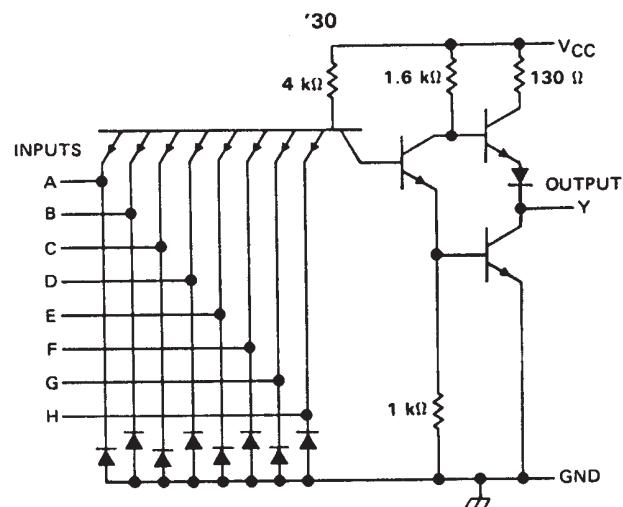


NC - No internal connection

**SN5430, SN54LS30, SN54S30  
SN7430, SN74LS30, SN74S30  
8-INPUT POSITIVE-NAND GATES**

SDLS099 - DECEMBER 1983 - REVISED MARCH 1988

**schematics (each gate)**



Resistor values shown are nominal.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5430, SN54LS30, SN54S30  
SN7430, SN74LS30, SN74S30  
8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|                 |                                | SN5430 |     |      | SN7430 |     |      | UNIT |
|-----------------|--------------------------------|--------|-----|------|--------|-----|------|------|
|                 |                                | MIN    | NOM | MAX  | MIN    | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5    | 5   | 5.5  | 4.75   | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       |        | 2   |      |        | 2   |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |        |     | 0.8  |        |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current      |        |     | -0.4 |        |     | -0.4 | mA   |
| I <sub>OL</sub> | Low-level output current       |        |     | 16   |        |     | 16   | mA   |
| T <sub>A</sub>  | Operating free-air temperature | -55    |     | 125  | 0      |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER          | TEST CONDITIONS †   | SN5430 |      |         | SN7430 |      |         | UNIT |
|--------------------|---|--------|------|---------|--------|------|---------|------|
|                    |   | MIN    | TYP‡ | MAX     | MIN    | TYP‡ | MAX     |      |
| V <sub>IK</sub>    | V <sub>CC</sub> = MIN, I <sub>I</sub> = - 12 mA                             |        |      | - 1.5   |        |      | - 1.5   | V    |
| V <sub>OH</sub>    | V <sub>CC</sub> = MIN, V <sub>IIL</sub> = 0.8 V, I <sub>OH</sub> = - 0.4 mA | 2.4    | 3.4  |         | 2.4    | 3.4  |         | V    |
| V <sub>OL</sub>    | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA       |        |      | 0.2 0.4 |        |      | 0.2 0.4 | V    |
| I <sub>I</sub>     | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                               |        |      | 1       |        |      | 1       | mA   |
| I <sub>IH</sub>    | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V                               |        |      | 40      |        |      | 40      | µA   |
| I <sub>IIL</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                               |        |      | - 1.6   |        |      | - 1.6   | mA   |
| I <sub>OSS</sub> § | V <sub>CC</sub> = MAX   | - 20   | - 55 | - 18    | - 55   |      |         | mA   |
| I <sub>CCH</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                                   |        | 1 2  |         | 1 2    |      |         | mA   |
| I <sub>CCL</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                               |        | 3 6  |         | 3 6    |      |         | mA   |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$  (see note 2)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|-----------|-----------------|----------------|---|-----|-----|-----|------|
| $t_{PLH}$ | Any             | Y              | $R_L = 400 \Omega$ ,<br>$C_L = 15 \text{ pF}$ | 13  | 22  | ns  |      |
| $t_{PHL}$ |                 |                |   | 8   | 15  | ns  |      |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



# **SN5430, SN54LS30, SN54S30 SN7430, SN74LS30, SN74S30 8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|                 |                                | SN54LS30 |     |      | SN74LS30 |     |      | UNIT |
|-----------------|--------------------------------|----------|-----|------|----------|-----|------|------|
|                 |                                | MIN      | NOM | MAX  | MIN      | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5      | 5   | 5.5  | 4.75     | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       |          | 2   |      |          | 2   |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |          |     | 0.7  |          |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current      |          |     | -0.4 |          |     | -0.4 | mA   |
| I <sub>OL</sub> | Low-level output current       |          |     | 4    |          |     | 8    | mA   |
| T <sub>A</sub>  | Operating free-air temperature | -55      |     | 125  | 0        |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER          | TEST CONDITIONS †   | SN54LS30 |       |       | SN74LS30 |       |       | UNIT |
|--------------------|---|----------|-------|-------|----------|-------|-------|------|
|                    |   | MIN      | TYP‡  | MAX   | MIN      | TYP‡  | MAX   |      |
| V <sub>IK</sub>    | V <sub>CC</sub> = MIN, I <sub>I</sub> = - 18 mA                           |          |       | - 1.5 |          |       | - 1.5 | V    |
| V <sub>OH</sub>    | V <sub>CC</sub> = MIN, V <sub>I</sub> L = MAX, I <sub>OH</sub> = - 0.4 mA | 2.5      | 3.4   |       | 2.7      | 3.4   |       | V    |
| V <sub>OL</sub>    | V <sub>CC</sub> = MIN, V <sub>I</sub> H = 2 V, I <sub>OL</sub> = 4 mA     |          | 0.25  | 0.4   |          |       | 0.4   | V    |
|                    | V <sub>CC</sub> = MIN, V <sub>I</sub> H = 2 V, I <sub>OL</sub> = 8 mA     |          |       |       |          | 0.25  | 0.5   |      |
| I <sub>I</sub>     | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                               |          |       | 0.1   |          |       | 0.1   | mA   |
| I <sub>I</sub> H   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                             |          |       | 20    |          |       | 20    | µA   |
| I <sub>I</sub> L   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                             |          |       | - 0.4 |          |       | - 0.4 | mA   |
| I <sub>OSS</sub> § | V <sub>CC</sub> = MAX   | - 20     | - 100 |       | - 20     | - 100 |       | mA   |
| I <sub>CCH</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                                 |          | 0.35  | 0.5   |          | 0.35  | 0.5   | mA   |
| I <sub>CCL</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                             |          | 0.6   | 1.1   |          | 0.6   | 1.1   | mA   |

**†** For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

6 Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics.  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$  (see note 2)

**NOTE 2:** Load circuits and voltage waveforms are shown in Section 1.



**SN5430, SN54LS30, SN54S30  
SN7430, SN74LS30, SN74S30  
8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|   | SN54S30 | SN74S30 |     |      | UNIT |      |
|---|---------|---------|-----|------|------|------|
|   |         | MIN     | NOM | MAX  |      |      |
| V <sub>CC</sub> Supply voltage                | 4.5     | 5       | 5.5 | 4.75 | 5    | 5.25 |
| V <sub>IH</sub> High-level input voltage      | 2       |         |     | 2    |      | V    |
| V <sub>IL</sub> Low-level input voltage       |         |         | 0.8 |      | 0.8  | V    |
| I <sub>OH</sub> High-level output current     |         |         | -1  |      | -1   | mA   |
| I <sub>OL</sub> Low-level output current      |         |         | 20  |      | 20   | mA   |
| T <sub>A</sub> Operating free-air temperature | -55     |         | 125 | 0    | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER        | TEST CONDITIONS †   | SN54S30 |      |      | SN74S30 |      |      | UNIT |
|------------------|---|---------|------|------|---------|------|------|------|
|                  |   | MIN     | TYP‡ | MAX  | MIN     | TYP‡ | MAX  |      |
| V <sub>IK</sub>  | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA                          |         |      | -1.2 |         |      | -1.2 | V    |
| V <sub>OH</sub>  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA | 2.5     | 3.4  |      | 2.7     | 3.4  |      | V    |
| V <sub>OL</sub>  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 20 mA   |         |      | 0.5  |         |      | 0.5  | V    |
| I <sub>I</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                           |         |      | 1    |         |      | 1    | mA   |
| I <sub>IH</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                           |         |      | 50   |         |      | 50   | µA   |
| I <sub>IL</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V                           |         |      | -2   |         |      | -2   | mA   |
| I <sub>OS§</sub> | V <sub>CC</sub> = MAX   | -40     |      | -100 | -40     |      | -100 | mA   |
| I <sub>CCH</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                               |         | 3    | 5    |         | 3    | 5    | mA   |
| I <sub>CCL</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                           |         | 5.5  | 10   |         | 5.5  | 10   | mA   |

**t** For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

**6** Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics.  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$  (see note 2)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT |
|-----------|-----------------|----------------|---|-----|-----|-----|------|
| $t_{PLH}$ | Any             | Y              | $R_L = 280 \Omega, C_L = 15 \text{ pF}$ |     | 4   | 6   | ns   |
| $t_{PHL}$ |                 |                |   |     | 4.5 | 7   | ns   |
| $t_{PLH}$ |                 | Y              | $R_L = 280 \Omega, C_L = 50 \text{ pF}$ |     | 5.5 |     | ns   |
| $t_{PHL}$ |                 |                |   |     | 6.5 |     | ns   |

**NOTE 2:** Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)          | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|----------------------------------|---|
| 5962-9679201QCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QC<br>A<br>SNJ54S30J | <span style="background-color: red; color: white;">Samples</span> |
| 5962-9679201QDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QD<br>A<br>SNJ54S30W | <span style="background-color: red; color: white;">Samples</span> |
| 5962-9679201QDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QD<br>A<br>SNJ54S30W | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009B2A             | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009B2A             | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BCA             | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BCA             | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BDA             | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/30009BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BDA             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009B2A             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009B2A             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BCA             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BCA             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BDA             | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30009BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30009BDA             | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN5430J          | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5430J                 | <span style="background-color: red; color: white;">Samples</span> |
| SN5430J          | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5430J                 | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS30J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS30J               | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS30J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS30J               | <span style="background-color: red; color: white;">Samples</span> |
| SN54S30J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S30J                | <span style="background-color: red; color: white;">Samples</span> |
| SN54S30J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S30J                | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS30                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS30                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS30                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS30                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS30N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS30N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS30N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS30N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS30                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS30NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS30                  | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5430J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5430J                | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5430J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5430J                | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5430W         | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5430W                | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)          | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|----------------------------------|---|
| SNJ5430W         | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5430W                         | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30FK      | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS30FK                      | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30FK      | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS30FK                      | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS30J                       | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS30J                       | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS30W                       | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS30W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS30W                       | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S30J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QC<br>A<br>SNJ54S30J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S30J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QC<br>A<br>SNJ54S30J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S30W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QD<br>A<br>SNJ54S30W | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S30W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9679201QD<br>A<br>SNJ54S30W | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS30, SN74LS30 :**

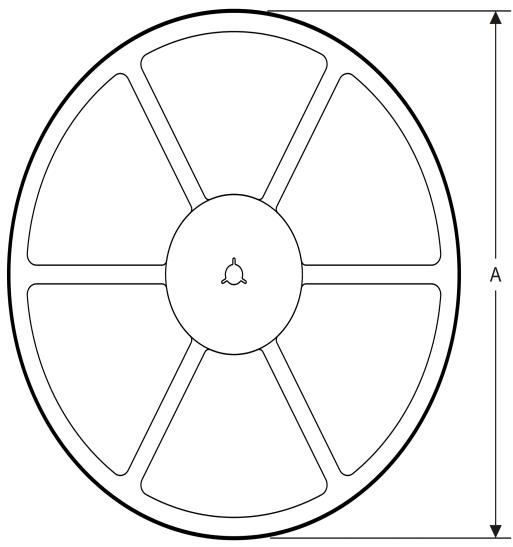
- Catalog: [SN74LS30](#)
- Military: [SN54LS30](#)

NOTE: Qualified Version Definitions:

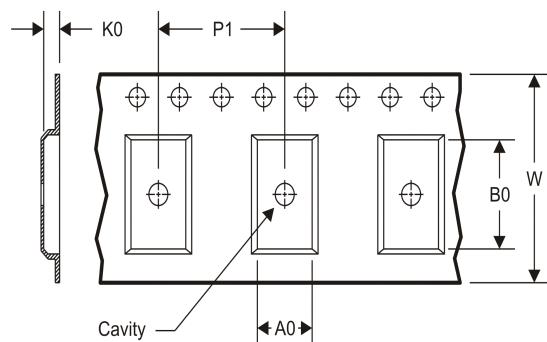
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

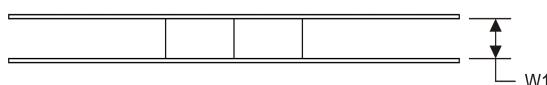
### REEL DIMENSIONS



### TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

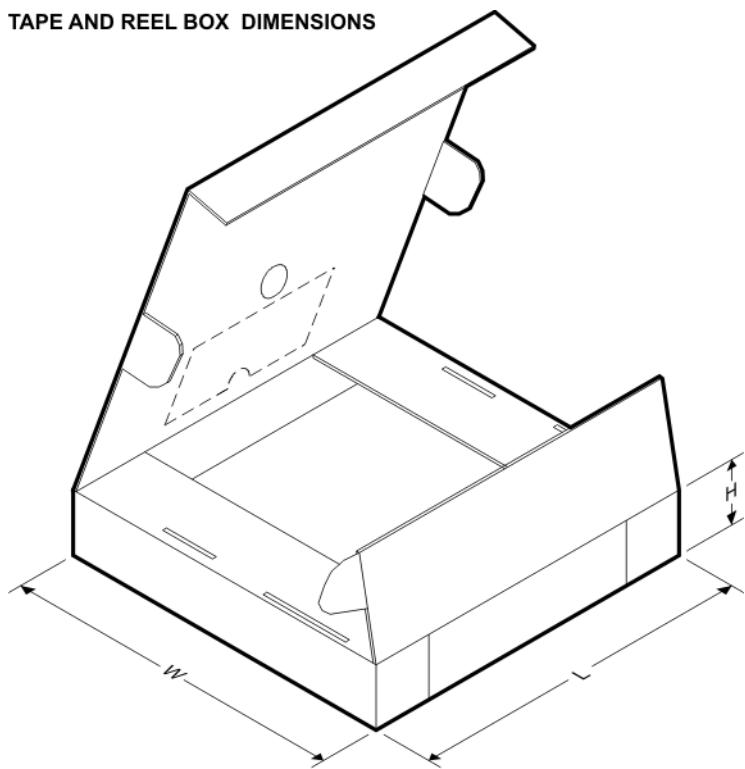


### TAPE AND REEL INFORMATION

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS30DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS30NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



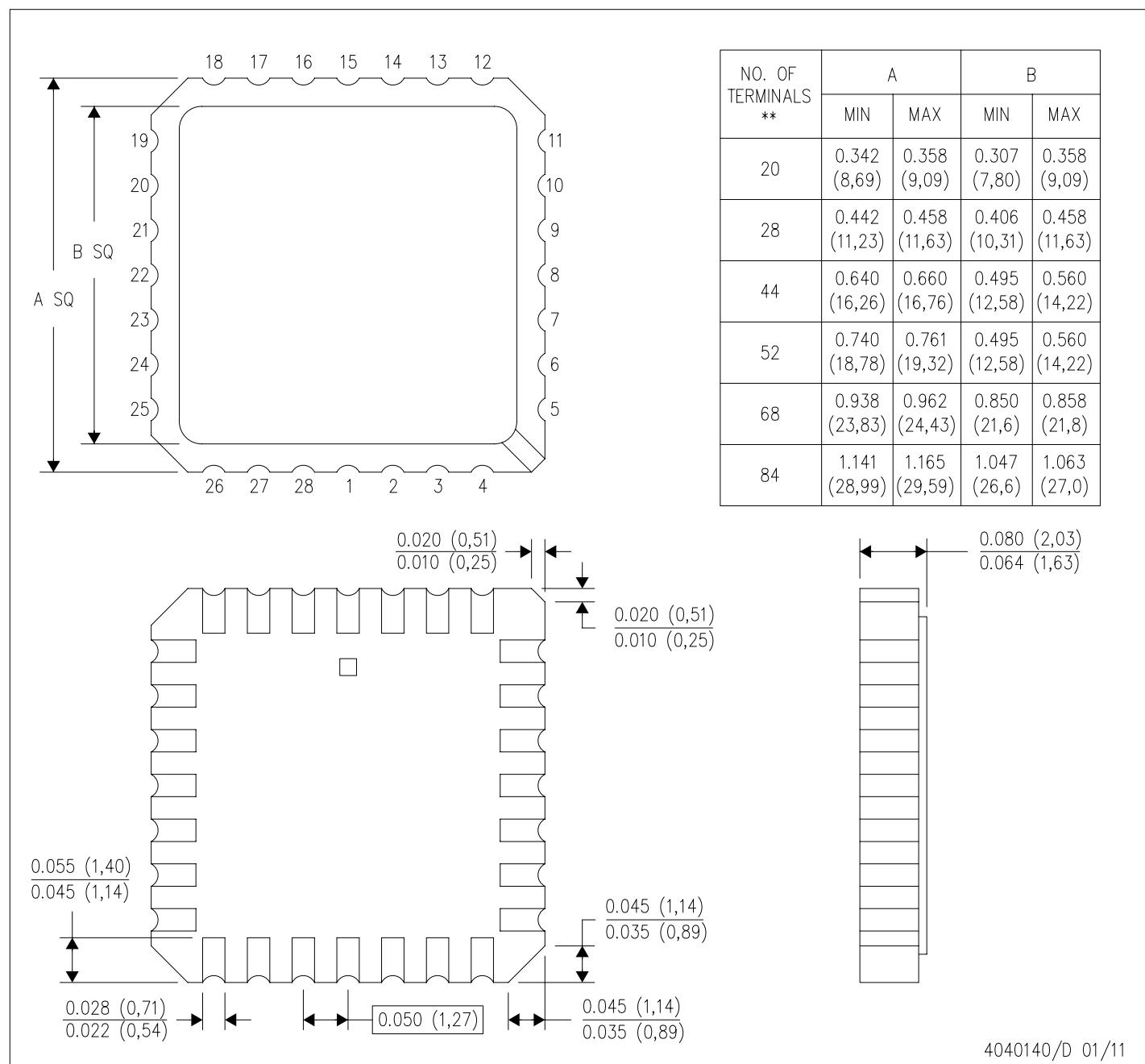
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS30DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LS30NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

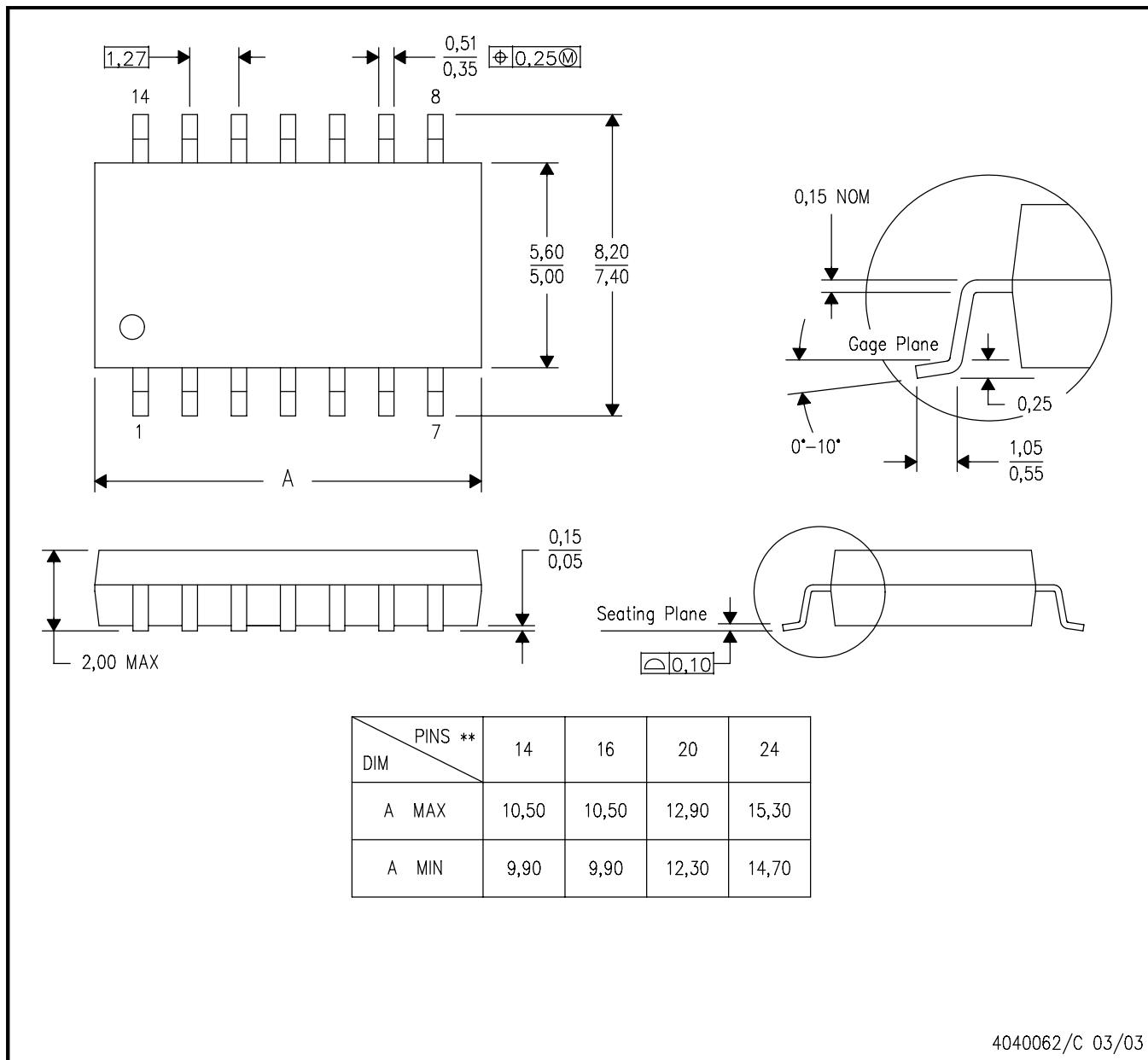
4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

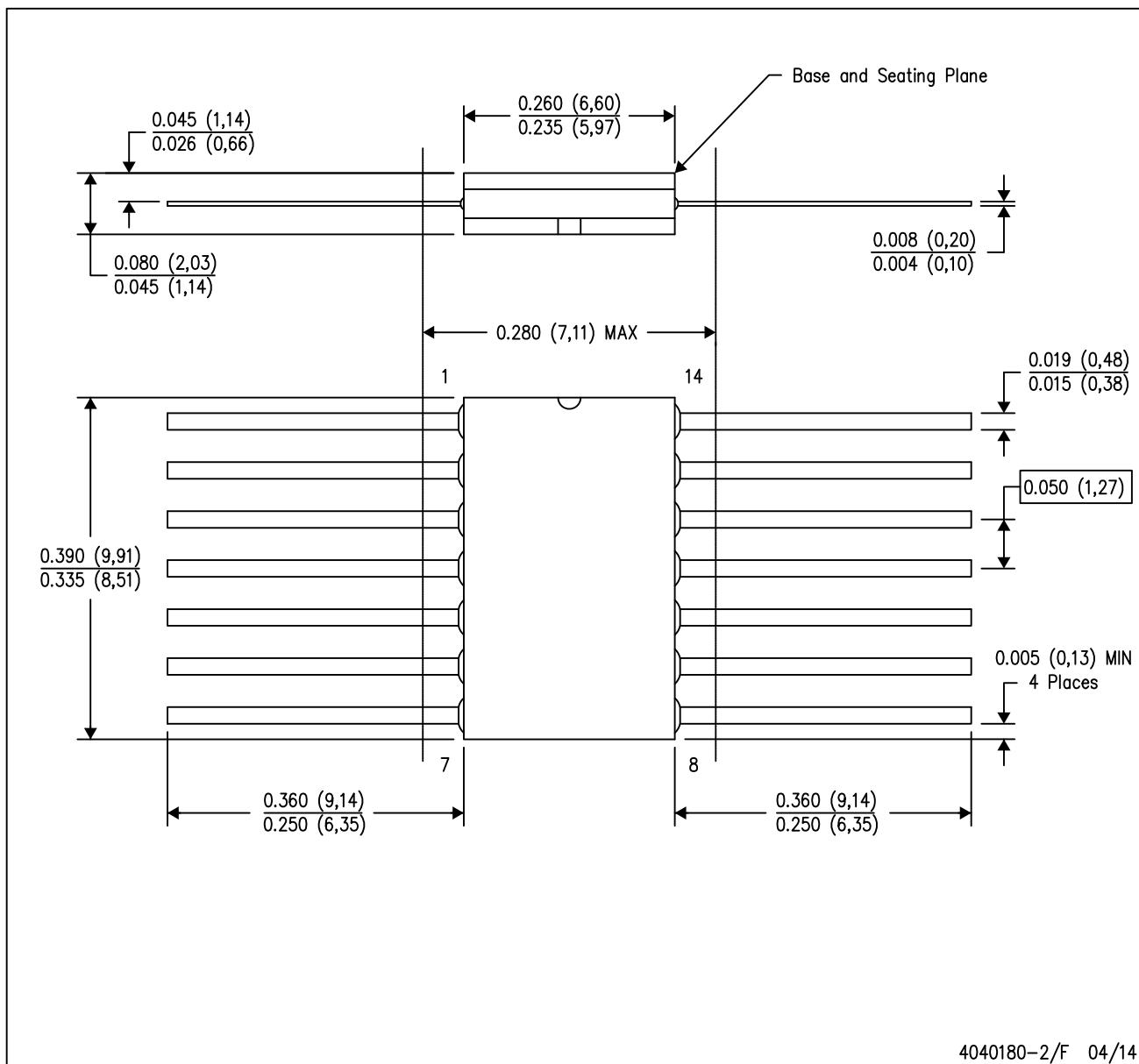


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

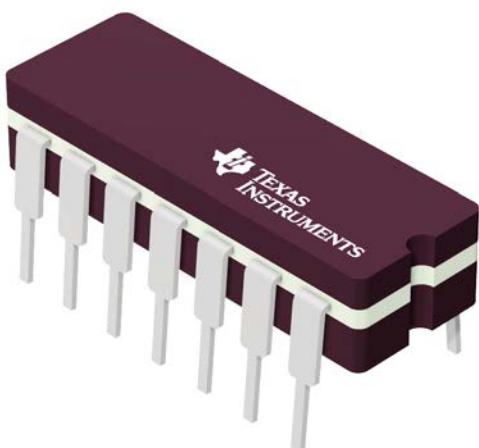
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

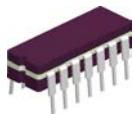
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

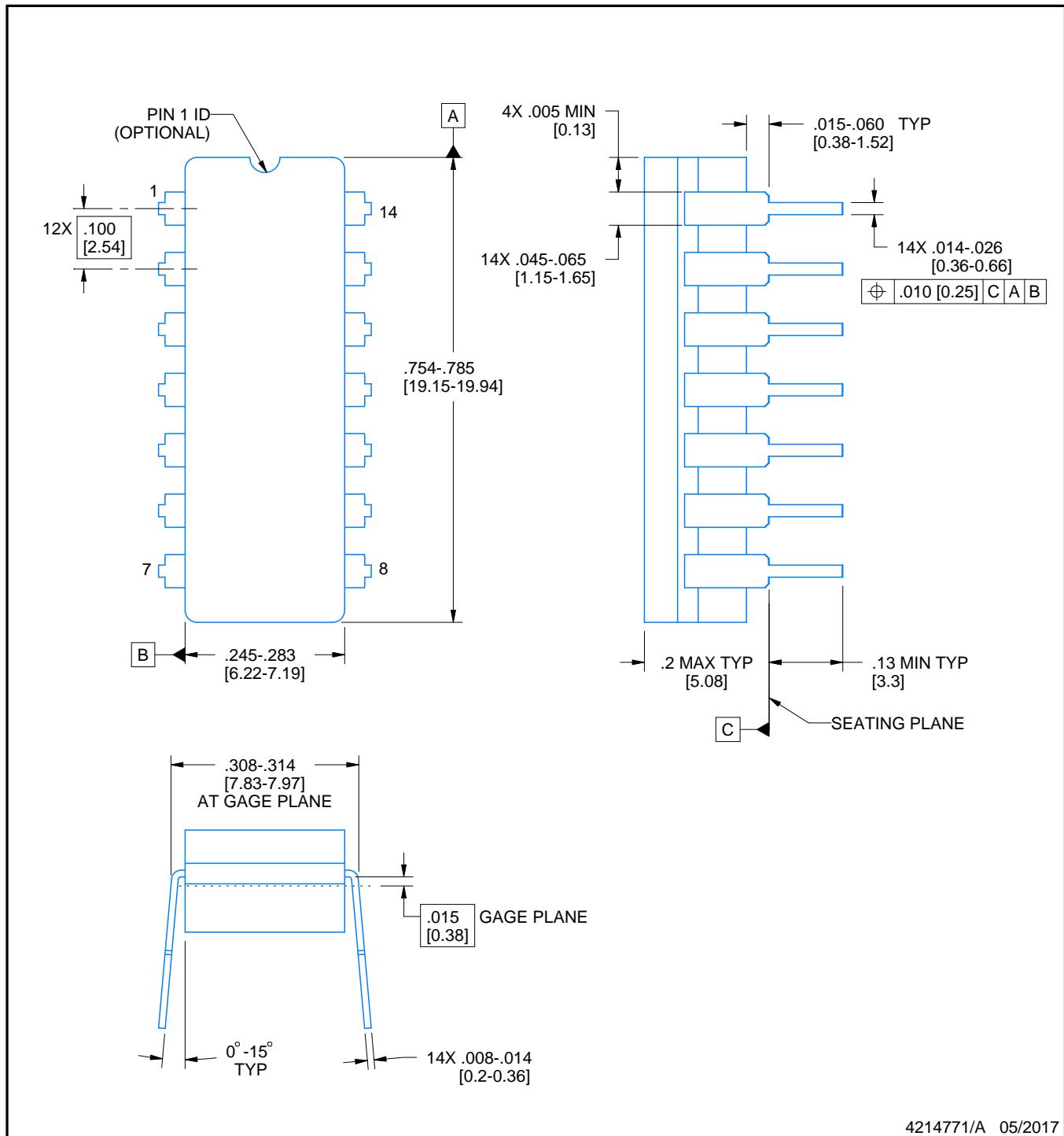
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

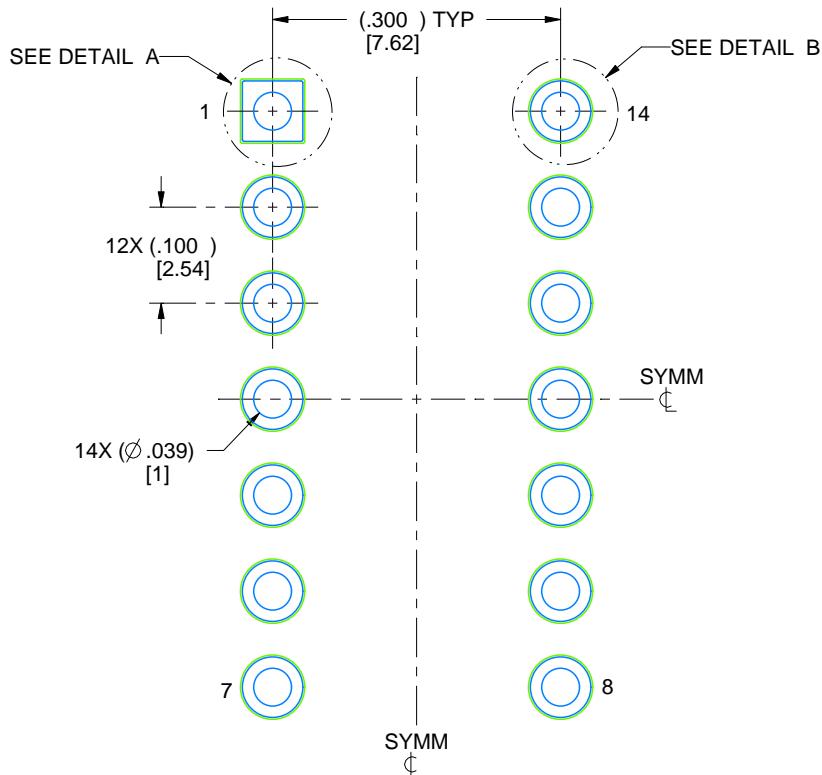
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

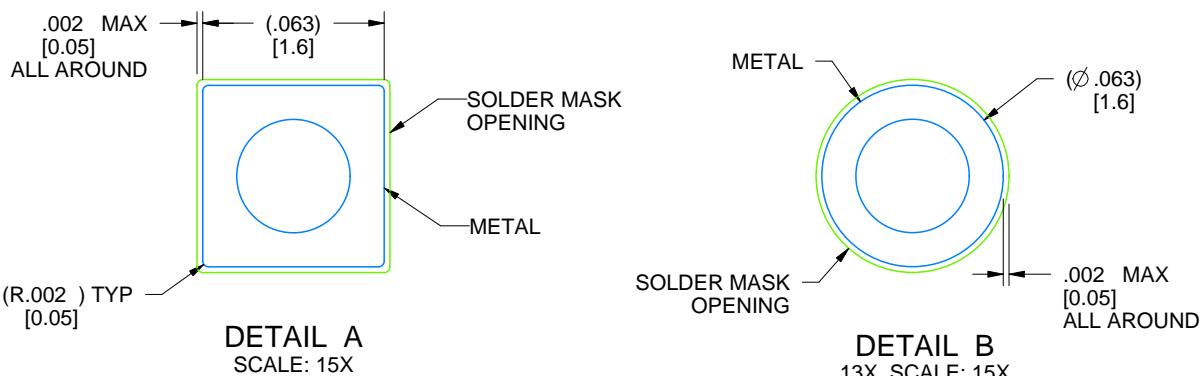
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



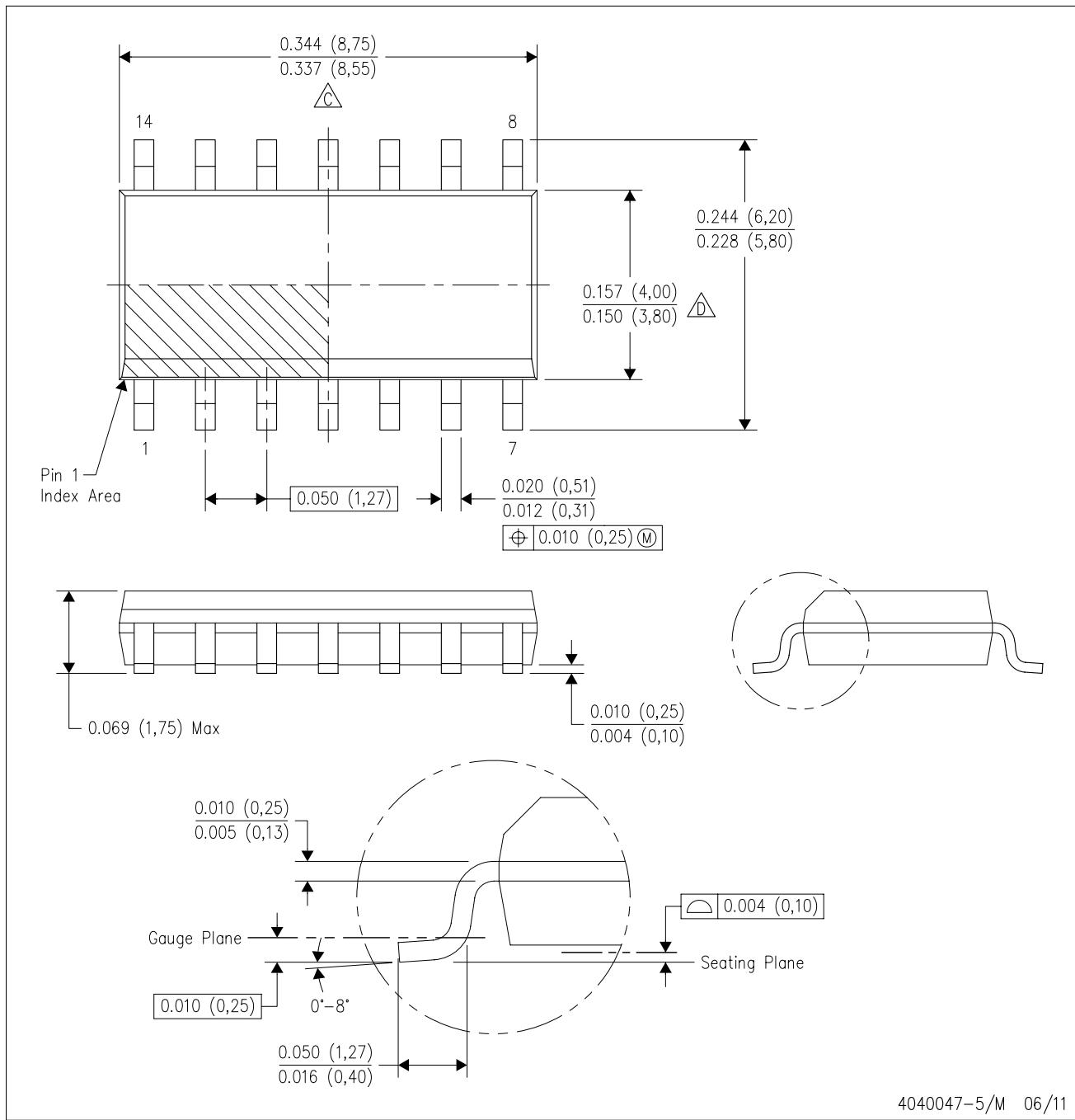
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

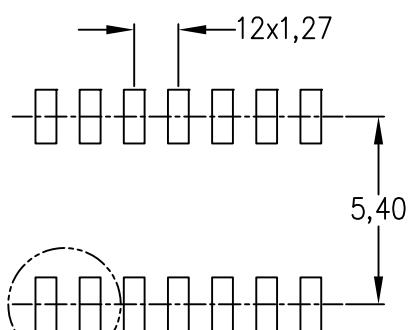
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

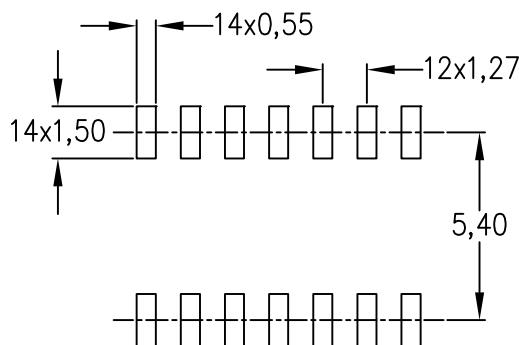
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

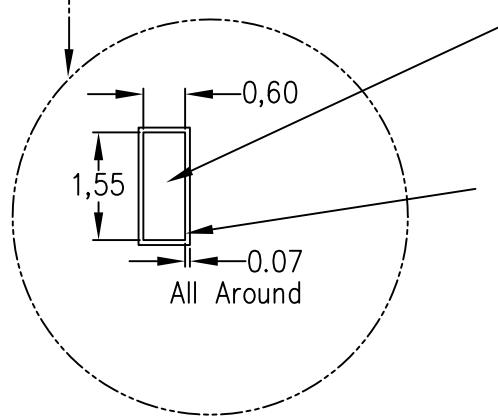
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

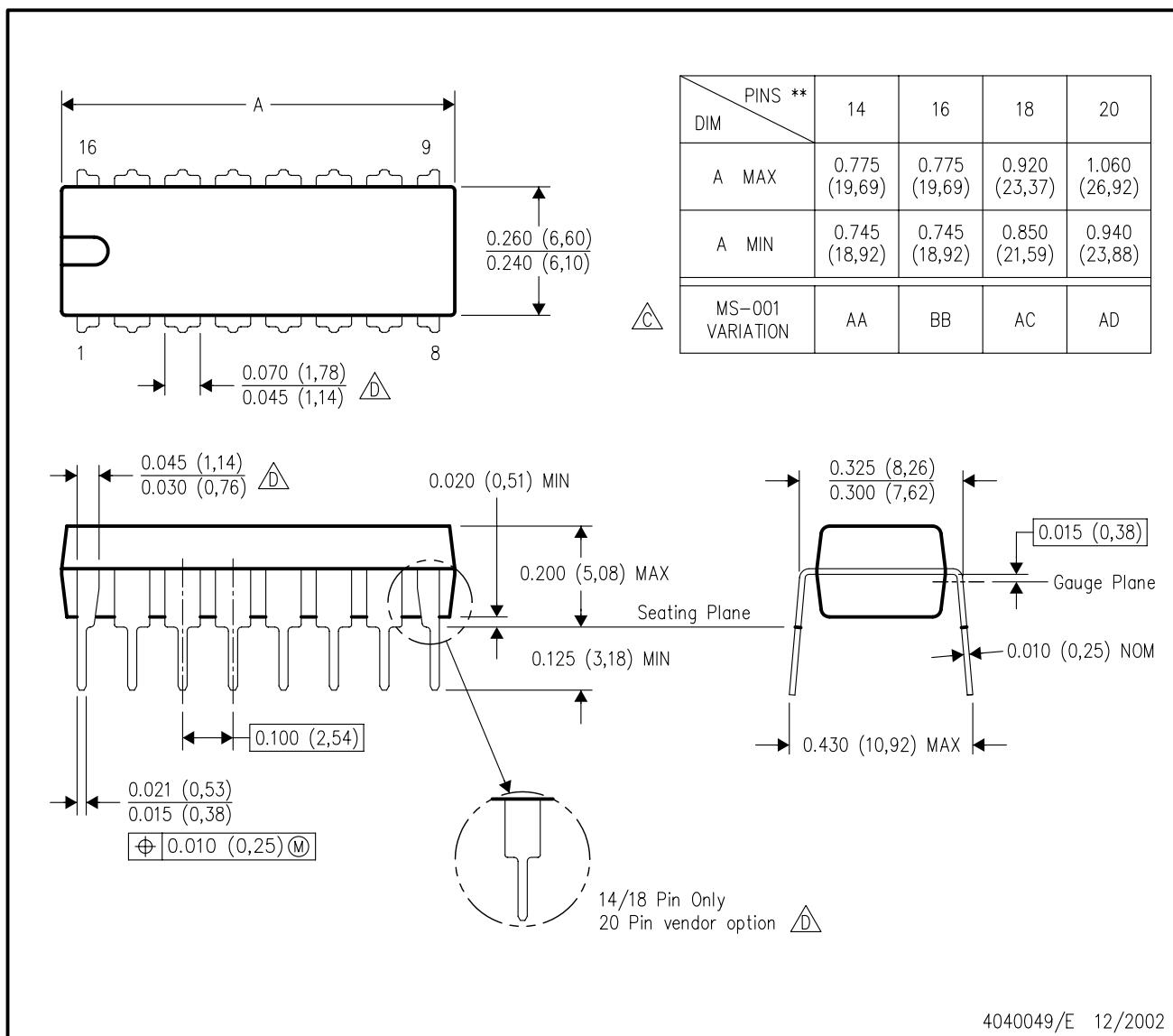
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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## QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

SDLS105 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

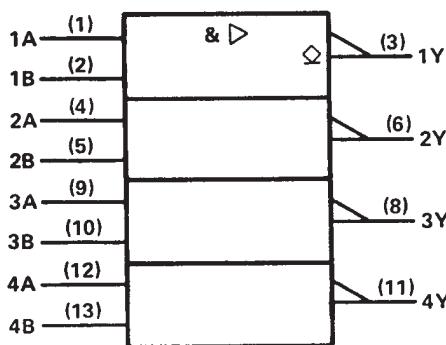
**description**

These devices contain four independent 2-input NAND buffer gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate high  $V_{OH}$  levels.

The SN5438, SN54LS38, and SN54S38 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7438, SN74LS38, and SN74S38 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | L      |
| L      | X | H      |
| X      | L | H      |

**logic symbol†**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

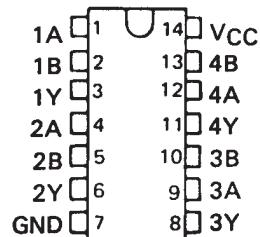
Pin numbers shown are for D, J, N, and W packages.

SN5438, SN54LS38, SN54S38 . . . J OR W PACKAGE

SN7438 . . . N PACKAGE

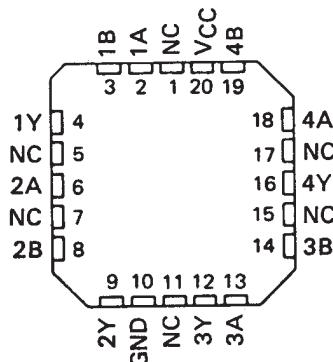
SN74LS38, SN74S38 . . . D OR N PACKAGE

(TOP VIEW)

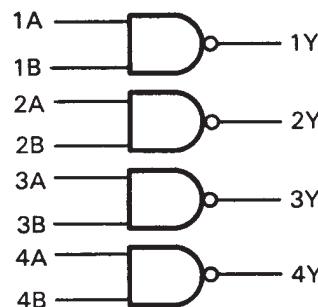


SN54LS38, SN54S38 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

**logic diagram****positive logic**

$$Y = \overline{A} \cdot \overline{B} \text{ or } Y = \overline{A} + \overline{B}$$

**SN5438, SN54LS38, SN54S38**

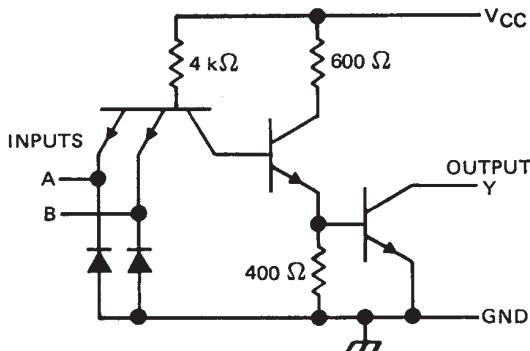
**SN7438, SN74LS38, SN74S38**

## **QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS**

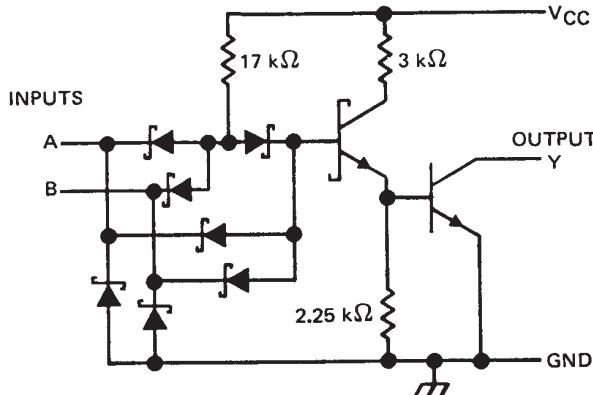
SDLS105 – DECEMBER 1983 – REVISED MARCH 1988

### **schematics (each gate)**

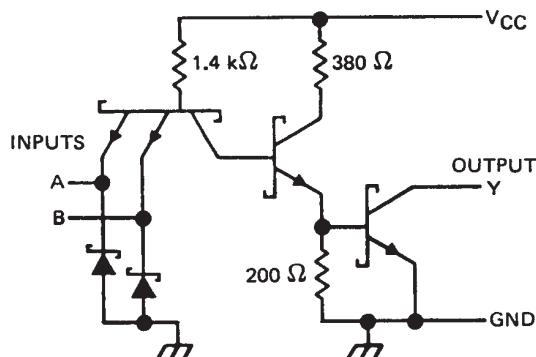
**'38**



**'LS38**



**'S38**



Resistor values shown are nominal.

### **absolute maximum ratings over operating free-air temperature (unless otherwise noted)**

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub> (see Note 1) ..... | 7 V            |
| Input voltage: '38 .....                           | 5.5 V          |
| LS38 .....   | 7 V            |
| Off-state output voltage .....                     | 7 V            |
| Operating free-air temperature range: SN54' .....  | -55°C to 125°C |
| SN74' .....  | 0°C to 70°C    |
| Storage temperature range .....                    | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

## QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

SDLS105 – DECEMBER 1983 – REVISED MARCH 1988

## recommended operating conditions

|   | SN5438 |     |     | SN7438 |     |      | UNIT |
|---|--------|-----|-----|--------|-----|------|------|
|   | MIN    | NOM | MAX | MIN    | NOM | MAX  |      |
| V <sub>CC</sub> Supply voltage                | 4.5    | 5   | 5.5 | 4.75   | 5   | 5.25 | V    |
| V <sub>IH</sub> High-level input voltage      | 2      |     |     | 2      |     |      | V    |
| V <sub>IL</sub> Low-level input voltage       |        |     |     | 0.8    |     |      | V    |
| V <sub>OH</sub> High-level output voltage     |        |     |     | 5.5    |     |      | V    |
| I <sub>OL</sub> Low-level output current      |        |     |     | 48     |     |      | mA   |
| T <sub>A</sub> Operating free-air temperature | –55    |     | 125 | 0      |     | 70   | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS <sup>†</sup>  | SN5438 |                  |      | SN7438 |                  |      | UNIT |
|------------------|---|--------|------------------|------|--------|------------------|------|------|
|                  |   | MIN    | TYP <sup>‡</sup> | MAX  | MIN    | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IK</sub>  | V <sub>CC</sub> = MIN, I <sub>I</sub> = –12 mA                          |        |                  | –1.5 |        |                  | –1.5 | V    |
| I <sub>OH</sub>  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V |        |                  |      |        |                  | 0.25 | mA   |
|                  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.7 V, V <sub>OH</sub> = 5.5 V |        |                  | 0.25 |        |                  |      |      |
| V <sub>OL</sub>  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA   |        |                  | 0.4  |        |                  | 0.4  | V    |
| I <sub>I</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                           |        |                  | 1    |        |                  | 1    | mA   |
| I <sub>IH</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V                           |        |                  | 40   |        |                  | 40   | μA   |
| I <sub>IL</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                           |        |                  | –1.6 |        |                  | –1.6 | mA   |
| I <sub>CCH</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                               |        | 5                | 8.5  |        | 5                | 8.5  | mA   |
| I <sub>CCL</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                           |        | 34               | 54   |        | 34               | 54   | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|--|-----|-----|-----|------|
| t <sub>PLH</sub> | A or B          | Y              | R <sub>L</sub> = 133 Ω, C <sub>L</sub> = 45 pF | 14  | 22  |     | ns   |
| t <sub>PHL</sub> |                 |                |  | 11  | 18  |     | ns   |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN5438, SN54LS38, SN54S38

SN7438, SN74LS38, SN74S38

## QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

SDLS105 – DECEMBER 1983 – REVISED MARCH 1988

### recommended operating conditions

|   | SN54LS38 | SN74LS38 |     |      | UNIT |      |
|---|----------|----------|-----|------|------|------|
|   |          | MIN      | NOM | MAX  |      |      |
| V <sub>CC</sub> Supply voltage                | 4.5      | 5        | 5.5 | 4.75 | 5    | 5.25 |
| V <sub>IH</sub> High-level input voltage      | 2        |          |     | 2    |      | V    |
| V <sub>IL</sub> Low-level input voltage       |          |          | 0.7 |      | 0.8  | V    |
| V <sub>OH</sub> High-level output voltage     |          |          | 5.5 |      | 5.5  | V    |
| I <sub>OL</sub> Low-level output current      |          |          | 12  |      | 24   | mA   |
| T <sub>A</sub> Operating free-air temperature | -55      |          | 125 | 0    | 70   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS†  | SN54LS38 |      |      | SN74LS38 |      |      | UNIT |
|------------------|---|----------|------|------|----------|------|------|------|
|                  |   | MIN      | TYP‡ | MAX  | MIN      | TYP‡ | MAX  |      |
| V <sub>IK</sub>  | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA                        |          |      | -1.5 |          |      | -1.5 | V    |
| I <sub>OH</sub>  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V |          |      | 0.25 |          |      | 0.25 | mA   |
| V <sub>OL</sub>  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 12 mA |          | 0.25 | 0.4  | 0.25     | 0.4  |      | V    |
|                  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 24 mA |          |      |      | 0.35     | 0.5  |      |      |
| I <sub>I</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                           |          |      | 0.1  |          |      | 0.1  | mA   |
| I <sub>IH</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                         |          |      | 20   |          |      | 20   | μA   |
| I <sub>IL</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                         |          |      | -0.4 |          |      | -0.4 | mA   |
| I <sub>CCH</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                             |          | 0.9  | 2    | 0.9      | 2    | mA   |      |
| I <sub>CCL</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                         |          | 6    | 12   | 6        | 12   | mA   |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|--|-----|-----|-----|------|
| t <sub>PLH</sub> | A or B          | Y              | R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF | 20  | 32  | ns  |      |
|                  |                 |                |  | 18  | 28  | ns  |      |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

SDS105 – DECEMBER 1983 – REVISED MARCH 1988

## recommended operating conditions

|                 |                                | SN54S38 |     |     | SN74S38 |     |      | UNIT |
|-----------------|--------------------------------|---------|-----|-----|---------|-----|------|------|
|                 |                                | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5     | 5   | 5.5 | 4.75    | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       |         | 2   |     | 2       |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |         |     | 0.8 |         | 0.8 |      | V    |
| V <sub>OH</sub> | High-level output voltage      |         |     | 5.5 |         | 5.5 |      | V    |
| I <sub>OL</sub> | Low-level output current       |         |     | 60  |         | 60  |      | mA   |
| T <sub>A</sub>  | Operating free-air temperature | -55     |     | 125 | 0       |     | 70   | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS <sup>†</sup>  | SN54S38 |                  |      | SN74S38 |                  |      | UNIT |
|------------------|---|---------|------------------|------|---------|------------------|------|------|
|                  |   | MIN     | TYP <sup>‡</sup> | MAX  | MIN     | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IK</sub>  | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA                          |         |                  | -1.2 |         |                  | -1.2 | V    |
| I <sub>OH</sub>  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V |         |                  |      |         | 0.25             |      | mA   |
|                  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.7 V, V <sub>OH</sub> = 5.5 V |         | 0.25             |      |         |                  |      |      |
| V <sub>OL</sub>  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 60 mA   |         | 0.5              |      |         | 0.5              |      | V    |
| I <sub>I</sub>   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                           |         |                  | 1    |         |                  | 1    | mA   |
| I <sub>IH</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V                           |         |                  | 0.1  |         |                  | 0.1  | mA   |
| I <sub>IL</sub>  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V                           |         |                  | -4   |         |                  | -4   | mA   |
| I <sub>CCH</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0                               | 20      | 36               |      | 20      | 36               |      | mA   |
| I <sub>CCL</sub> | V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V                           | 46      | 80               |      | 46      | 80               |      | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

| PARAMETER                   | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|----------------|--|-----|-----|-----|------|
| t <sub>PLH</sub>            | A or B          | Y              | R <sub>L</sub> = 93 Ω, C <sub>L</sub> = 50 pF  |     | 6.5 | 10  | ns   |
| t <sub>PHL</sub>            |                 |                |  |     | 6.5 | 10  | ns   |
| t <sub>P<sub>L</sub>H</sub> |                 |                | R <sub>L</sub> = 93 Ω, C <sub>L</sub> = 150 pF |     | 9   |     | ns   |
| t <sub>P<sub>H</sub>L</sub> |                 |                |  |     | 8.5 |     | ns   |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| JM38510/00303BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/00303BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30203B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30203B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30203BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/00303BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/00303BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/00303BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/00303BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30203B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30203B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30203BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30203BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN5438J          | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5438J                 | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN5438J          | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN5438J                 | <a href="#">Samples</a> |
| SN54LS38J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS38J               | <a href="#">Samples</a> |
| SN54LS38J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS38J               | <a href="#">Samples</a> |
| SN54S38J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S38J                | <a href="#">Samples</a> |
| SN54S38J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S38J                | <a href="#">Samples</a> |
| SN7438D          | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438D          | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438DE4        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438DE4        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438DR         | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438DR         | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 7438                    | <a href="#">Samples</a> |
| SN7438N          | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN7438N                 | <a href="#">Samples</a> |
| SN7438N          | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN7438N                 | <a href="#">Samples</a> |
| SN7438NSR        | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN7438                  | <a href="#">Samples</a> |
| SN7438NSR        | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN7438                  | <a href="#">Samples</a> |
| SN74LS38D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <a href="#">Samples</a> |
| SN74LS38D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <a href="#">Samples</a> |
| SN74LS38DBR      | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   |              | LS38                    | <a href="#">Samples</a> |
| SN74LS38DBR      | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   |              | LS38                    | <a href="#">Samples</a> |
| SN74LS38DG4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74LS38DG4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38DRE4     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38DRE4     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS38                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS38N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS38N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS38N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS38N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS38                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS38NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS38                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38D         | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S38                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38D         | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S38                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38DR        | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S38                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38DR        | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S38                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38N         | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74S38N                | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38N         | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74S38N                | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38NSR       | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74S38                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74S38NSR       | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74S38                   | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5438J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5438J                | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5438J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5438J                | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SNJ5438W         | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5438W                | <span style="background-color: red; color: white;">Samples</span> |
| SNJ5438W         | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ5438W                | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38FK      | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS38FK             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38FK      | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS38FK             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS38J              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS38J              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS38W              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS38W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS38W              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38FK       | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54S38FK              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38FK       | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54S38FK              | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S38J               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S38J               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S38W               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S38W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S38W               | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN5438, SN54LS38, SN54S38, SN7438, SN74LS38, SN74S38 :**

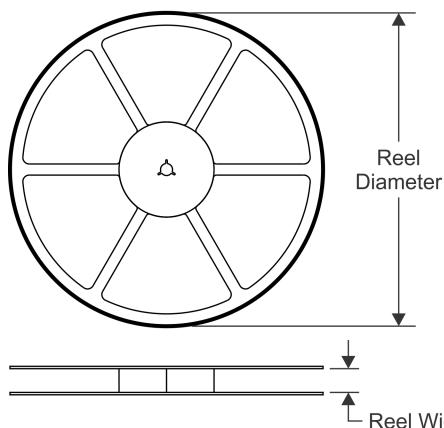
- Catalog: [SN7438](#), [SN74LS38](#), [SN74S38](#)
- Military: [SN5438](#), [SN54LS38](#), [SN54S38](#)

NOTE: Qualified Version Definitions:

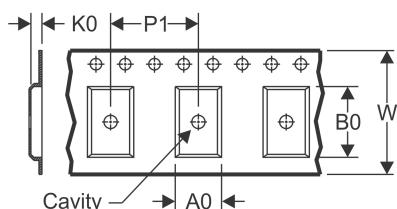
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

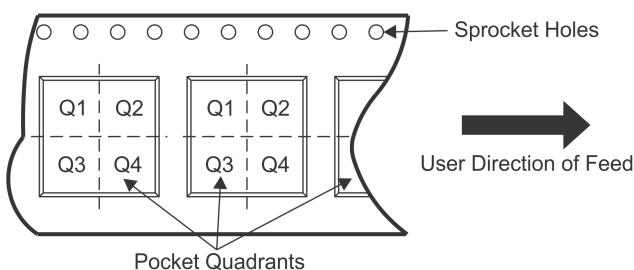


### TAPE DIMENSIONS



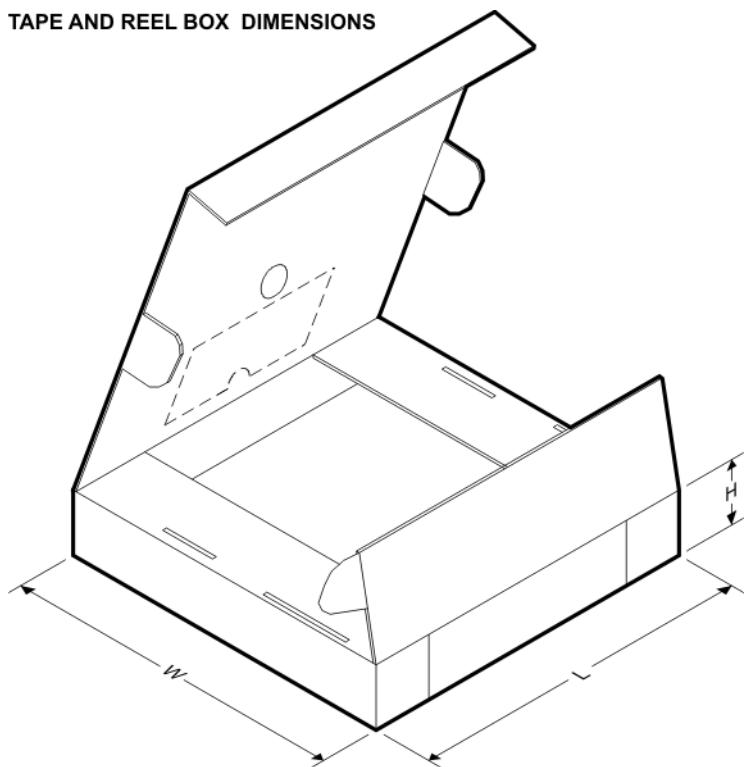
|       |   |
|-------|---|
| $A_0$ | Dimension designed to accommodate the component width     |
| $B_0$ | Dimension designed to accommodate the component length    |
| $K_0$ | Dimension designed to accommodate the component thickness |
| $W$   | Overall width of the carrier tape                         |
| $P_1$ | Pitch between successive cavity centers                   |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | $A_0$ (mm) | $B_0$ (mm) | $K_0$ (mm) | $P_1$ (mm) | $W$ (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|------------|------------|------------|------------|----------|---------------|
| SN7438DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5        | 9.0        | 2.1        | 8.0        | 16.0     | Q1            |
| SN7438NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2        | 10.5       | 2.5        | 12.0       | 16.0     | Q1            |
| SN74LS38DR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5        | 9.0        | 2.1        | 8.0        | 16.0     | Q1            |
| SN74S38DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5        | 9.0        | 2.1        | 8.0        | 16.0     | Q1            |
| SN74S38NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2        | 10.5       | 2.5        | 12.0       | 16.0     | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


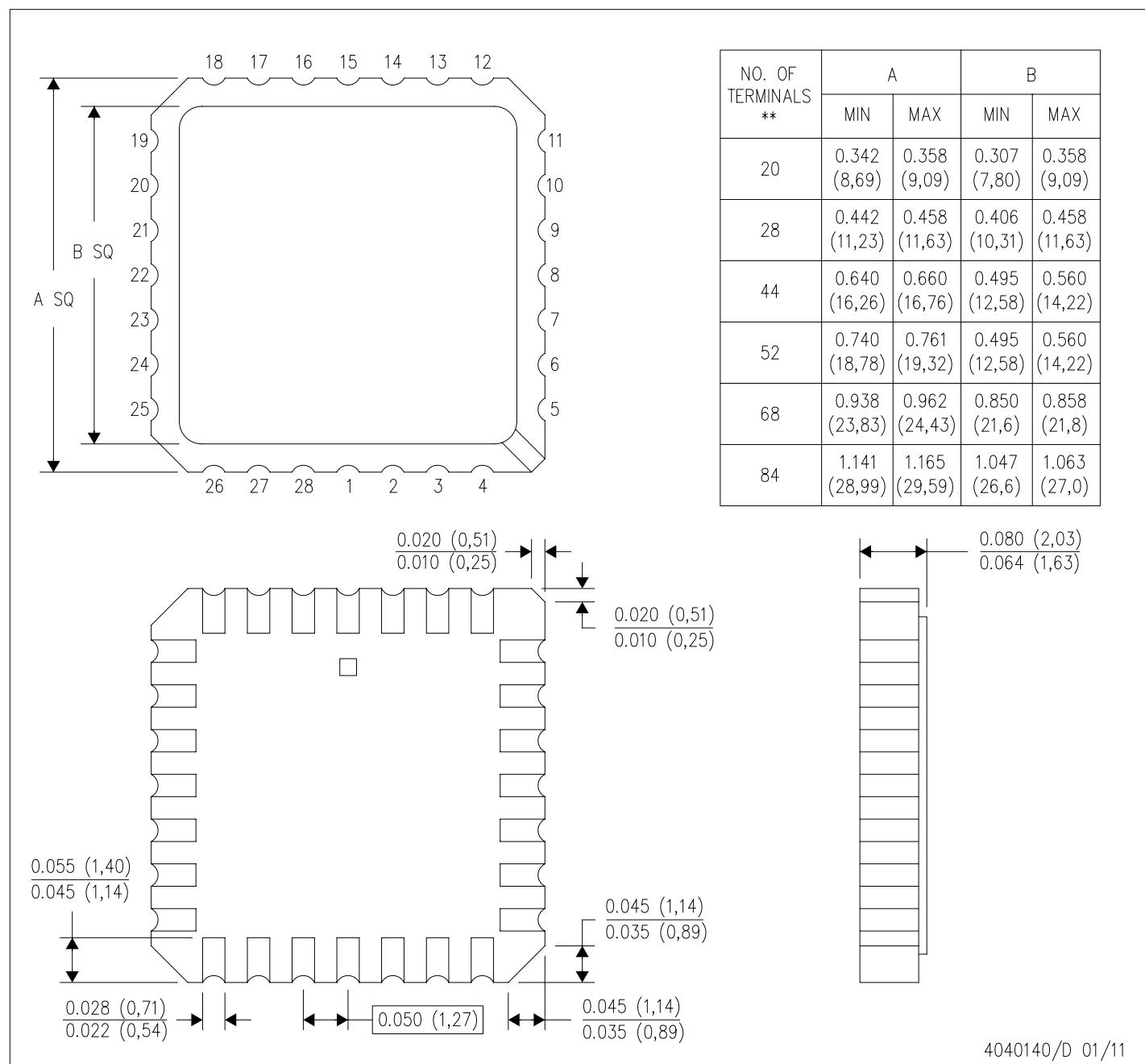
\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN7438DR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN7438NSR  | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LS38DR | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74S38DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74S38NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

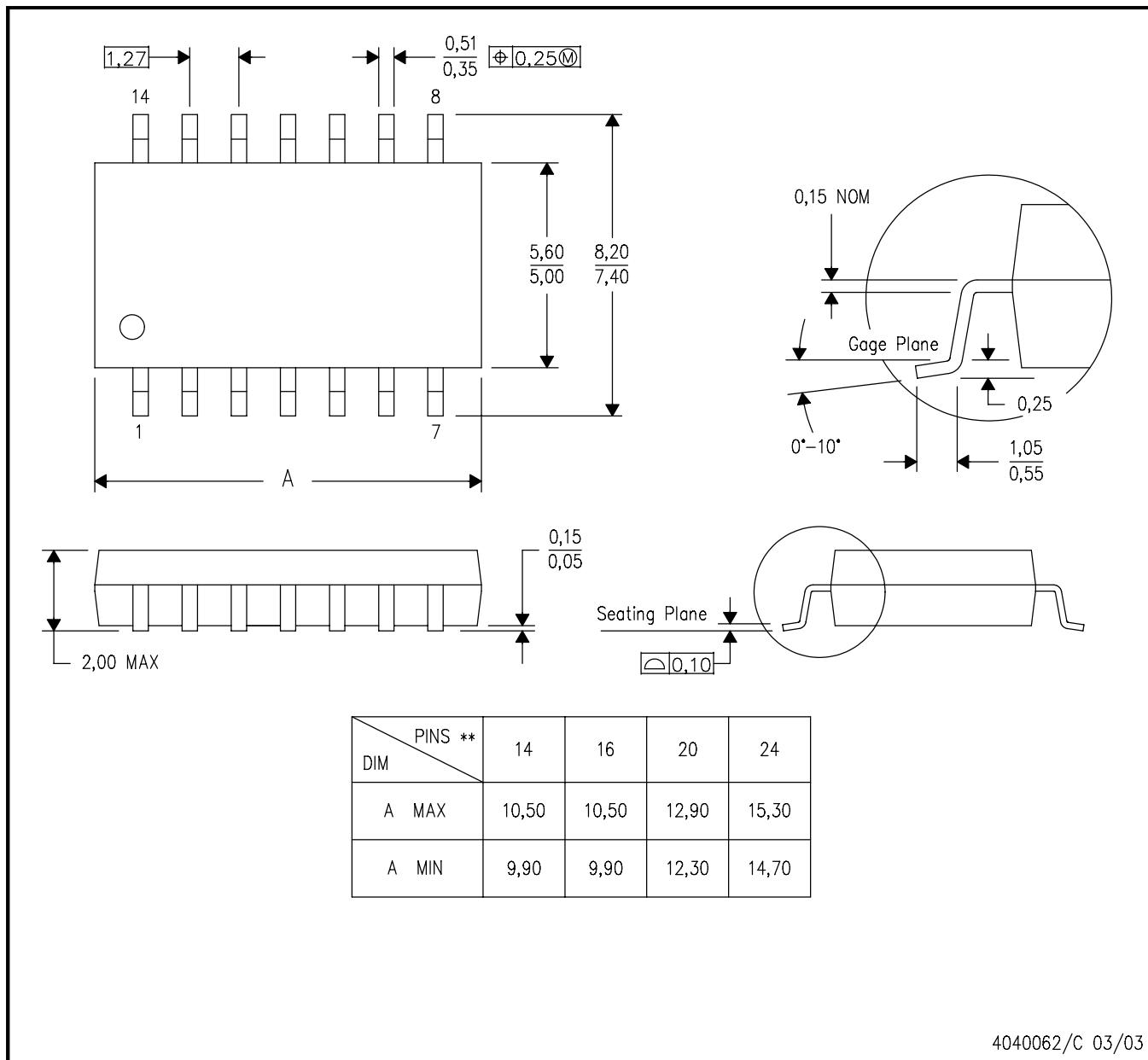
4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

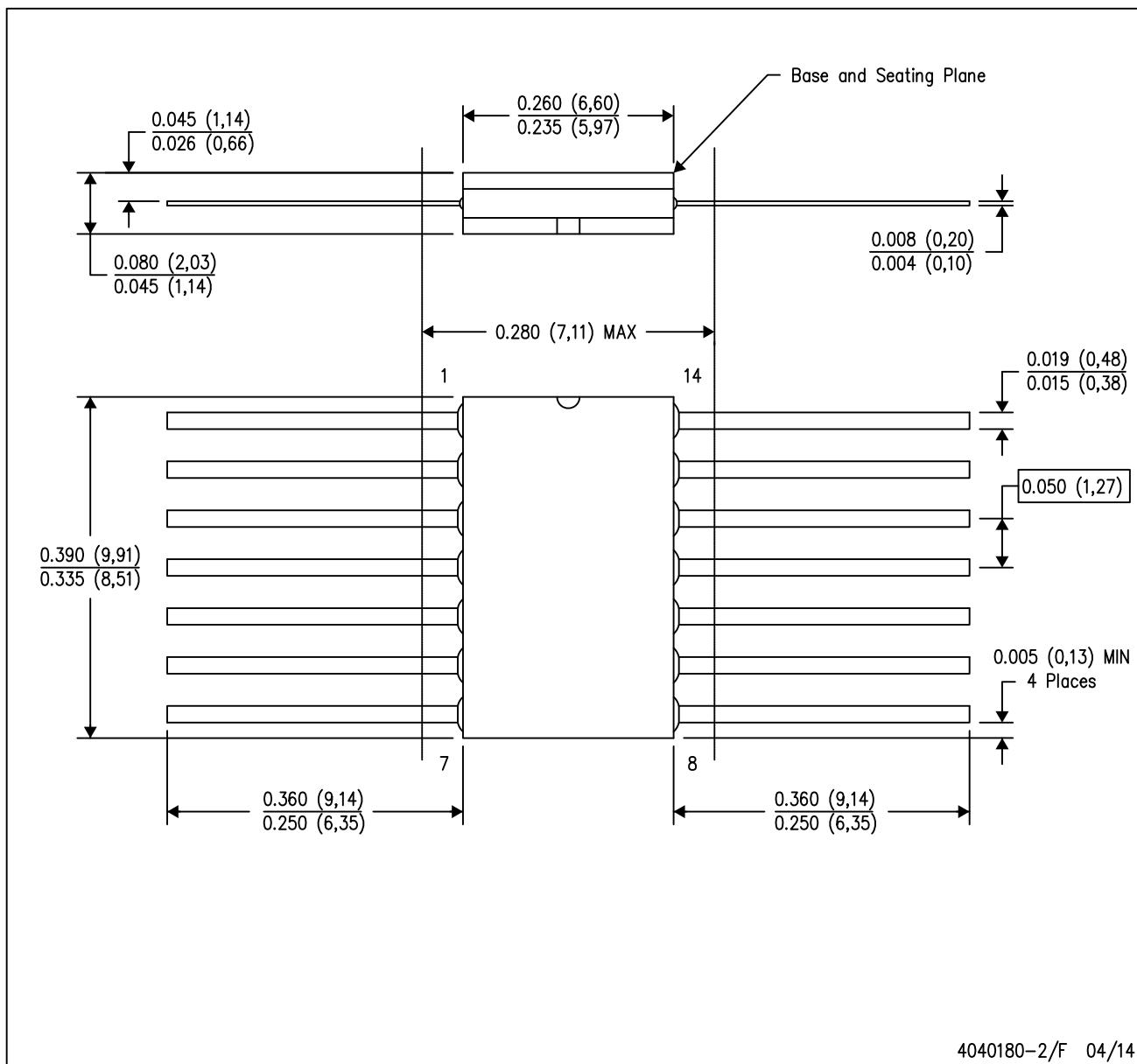


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



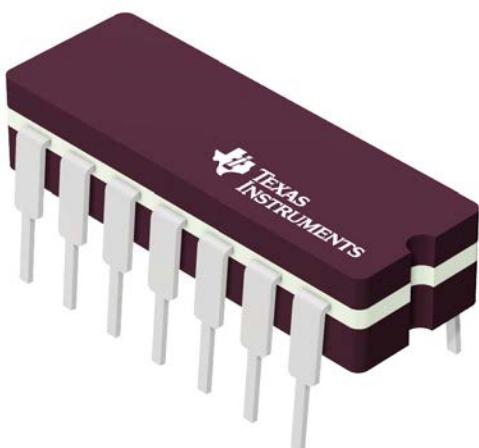
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

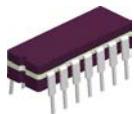
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

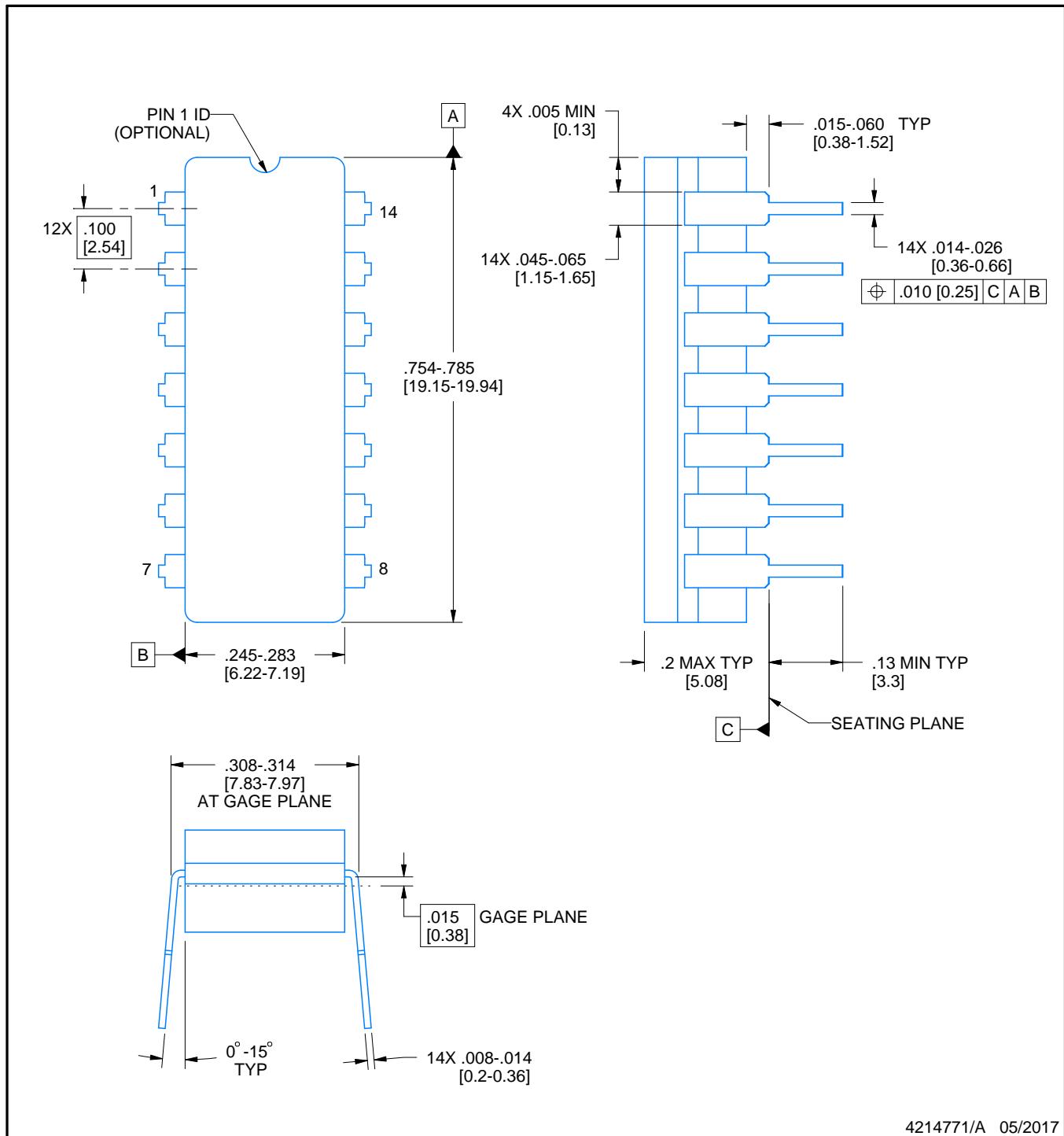
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

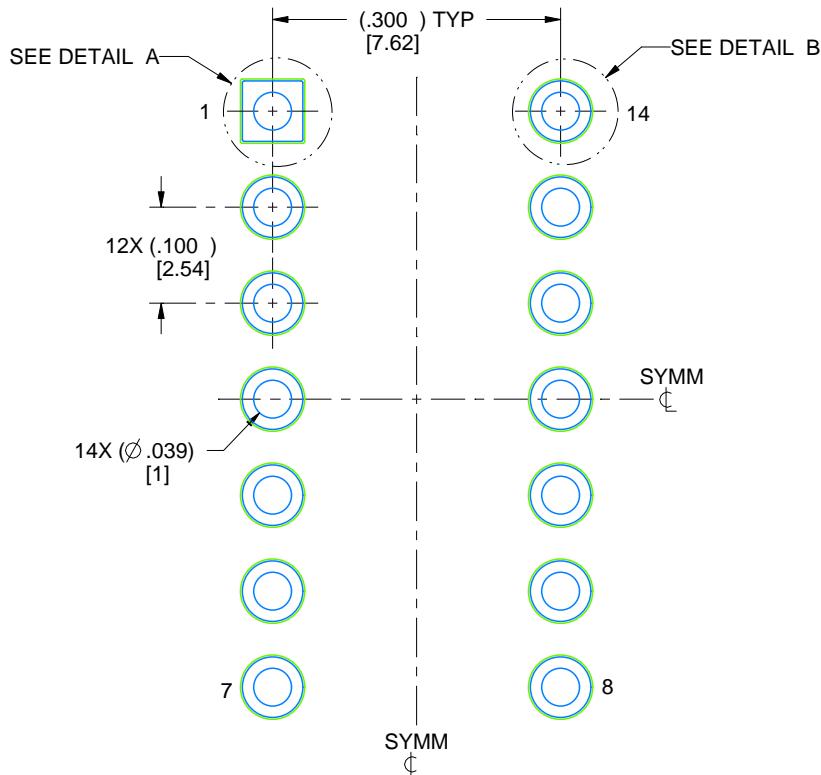
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

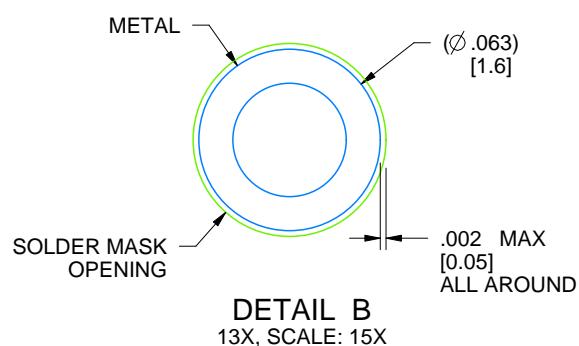
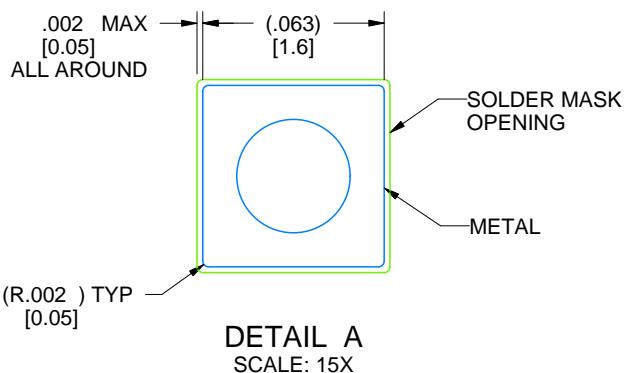
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



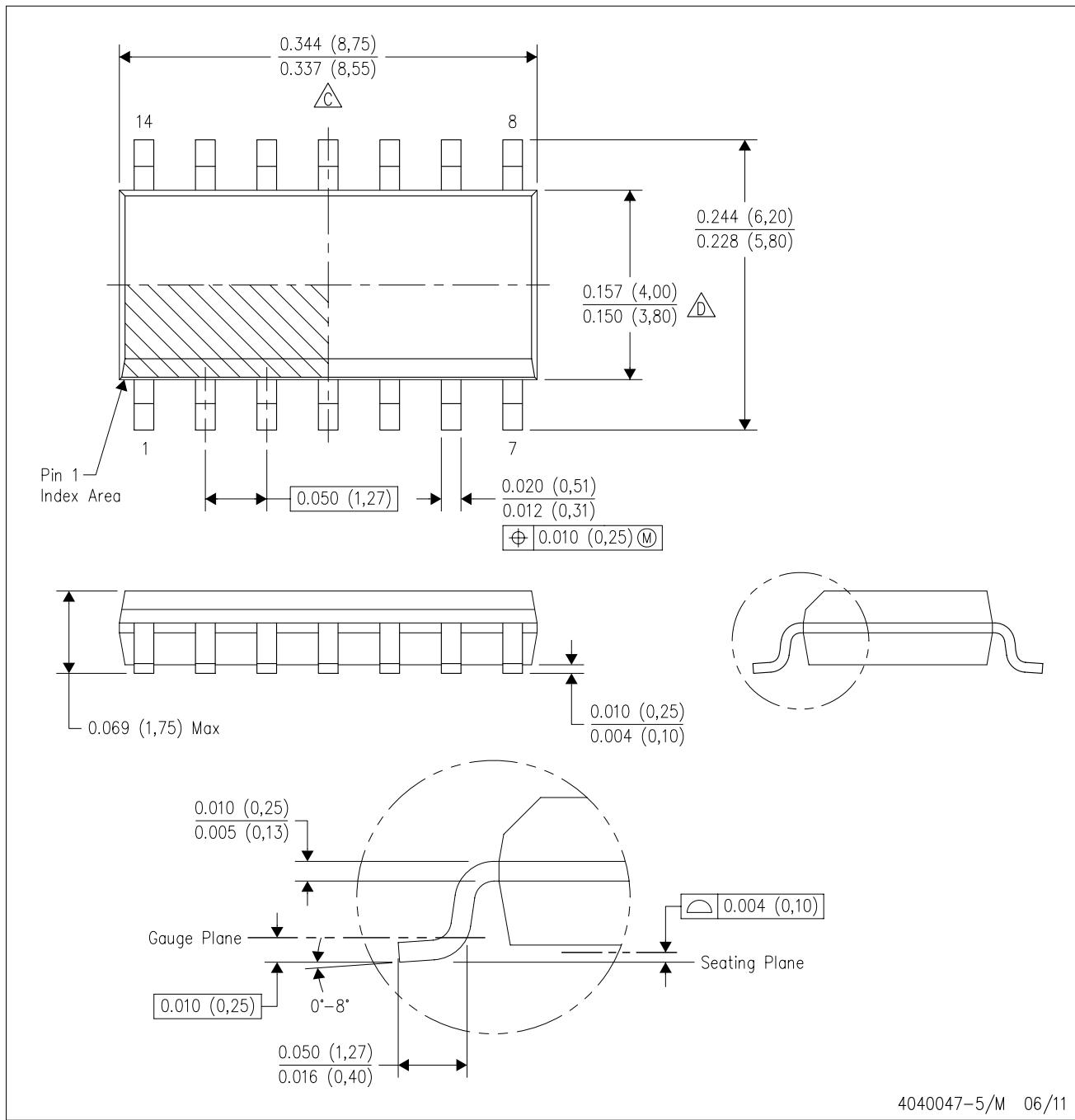
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

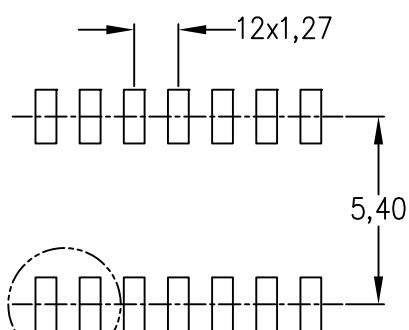
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

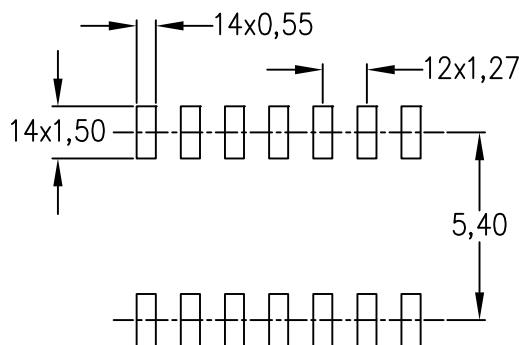
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

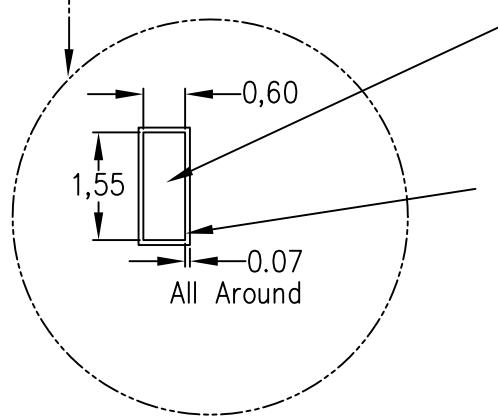
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

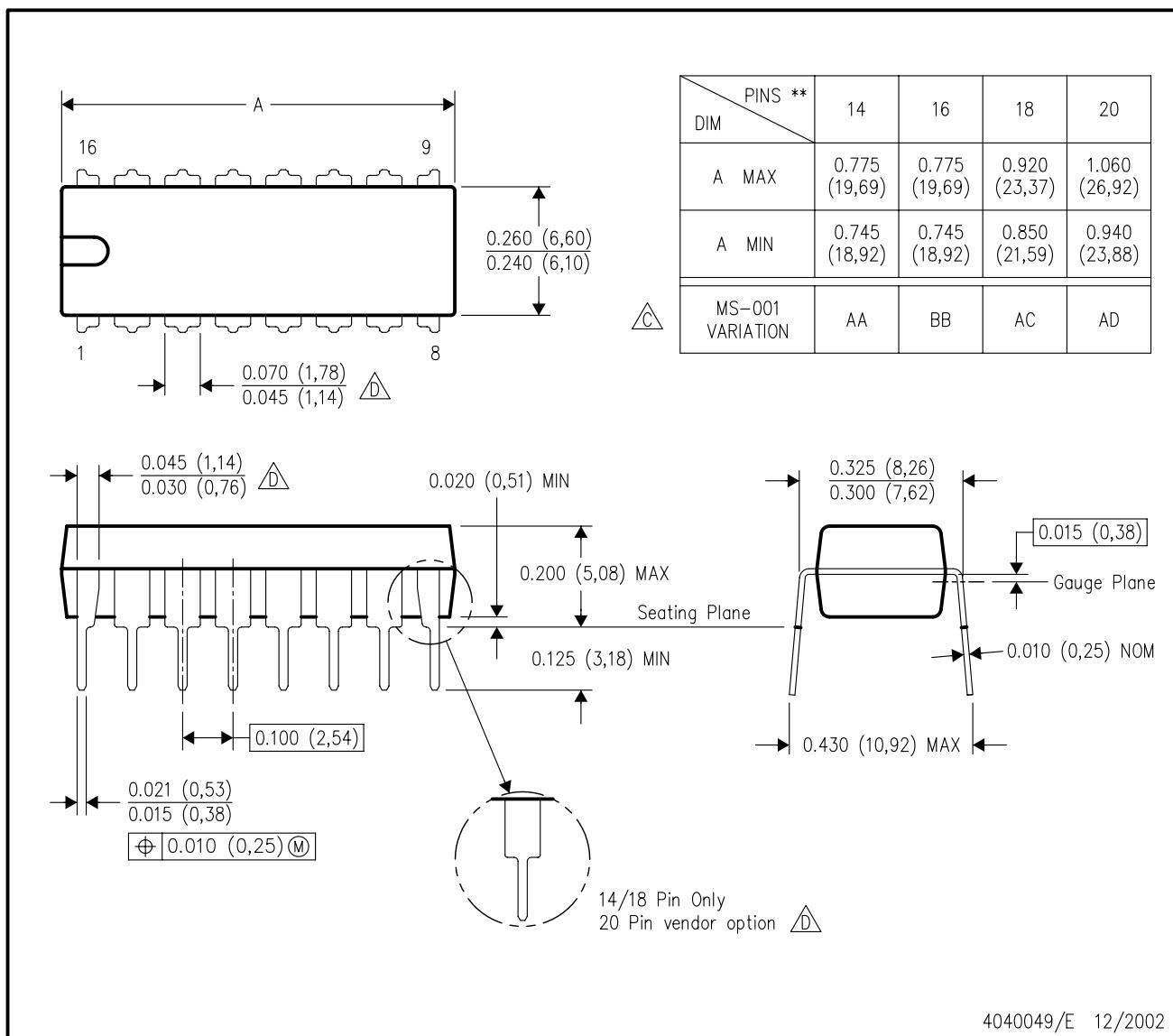
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

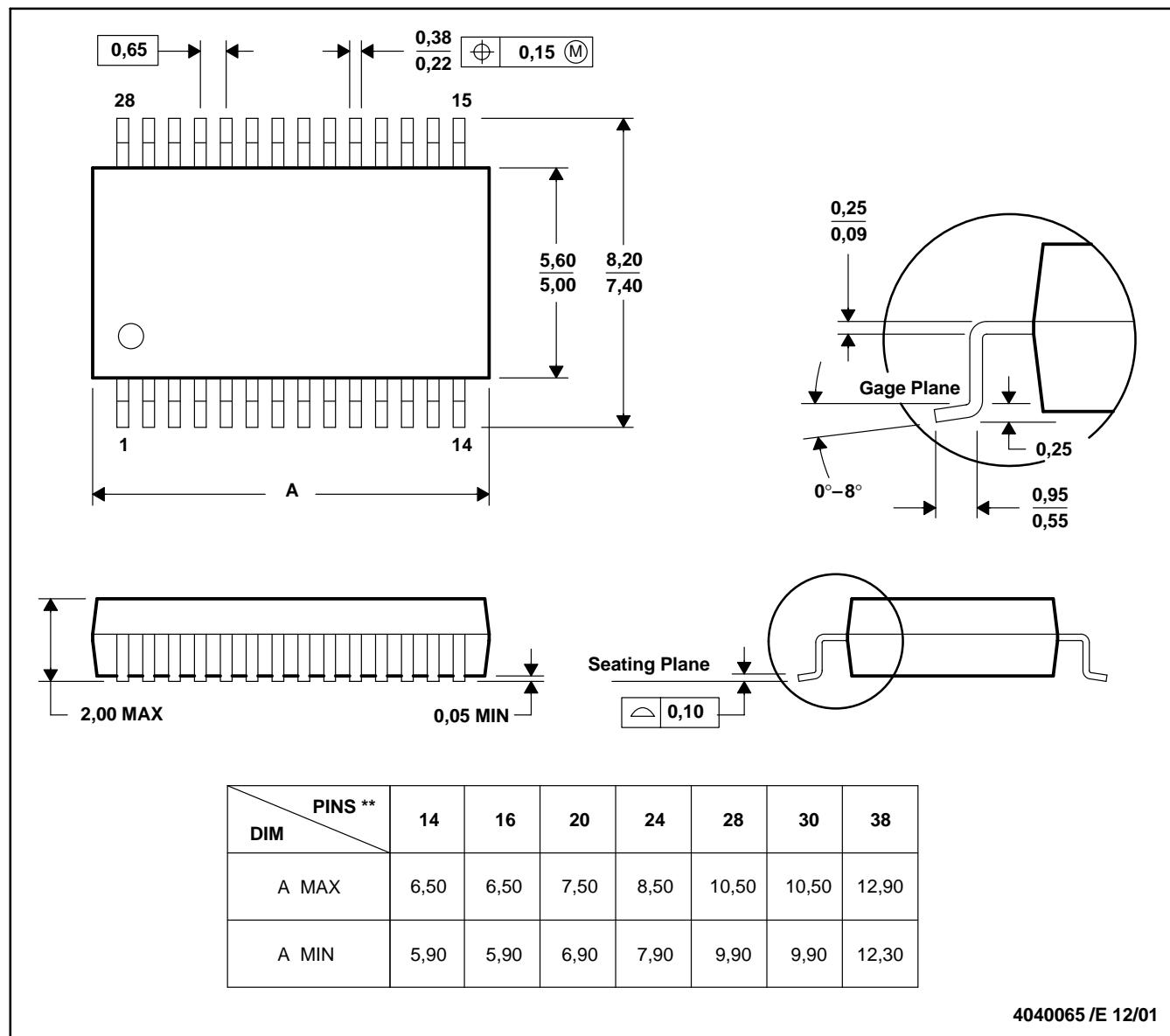
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

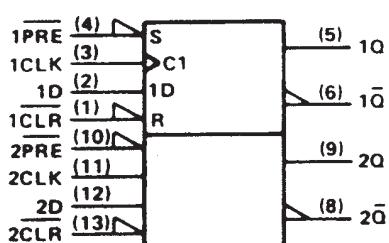
The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

| INPUTS |     |     |   | OUTPUTS        |                |
|--------|-----|-----|---|----------------|----------------|
| PRE    | CLR | CLK | D | Q              | $\bar{Q}$      |
| L      | H   | X   | X | H              | L              |
| H      | L   | X   | X | L              | H              |
| L      | L   | X   | X | H <sup>†</sup> | H <sup>†</sup> |
| H      | H   | ↑   | H | H              | L              |
| H      | H   | ↑   | L | L              | H              |
| H      | H   | L   | X | Q <sub>0</sub> | $\bar{Q}_0$    |

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

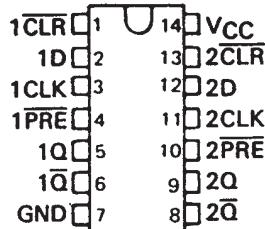
### logic symbol <sup>‡</sup>



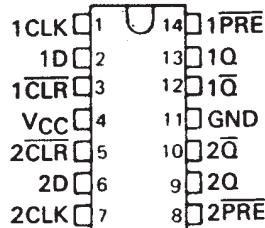
<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

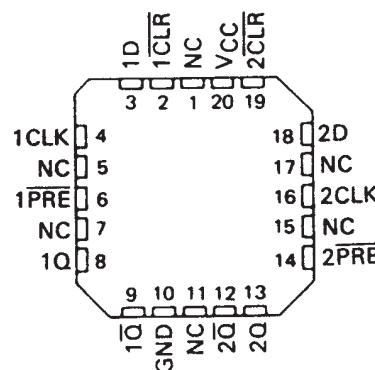
SN5474 . . . J PACKAGE  
 SN54LS74A, SN54S74 . . . J OR W PACKAGE  
 SN7474 . . . N PACKAGE  
 SN74LS74A, SN74S74 . . . D OR N PACKAGE  
 (TOP VIEW)



SN5474 . . . W PACKAGE  
 (TOP VIEW)

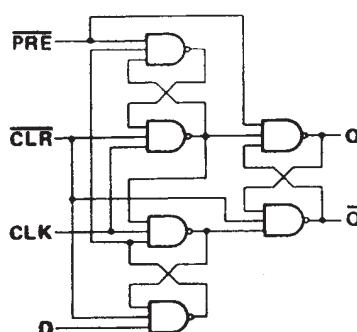


SN54LS74A, SN54S74 . . . FK PACKAGE  
 (TOP VIEW)



NC - No internal connection

### logic diagram (positive logic)



**SN5474, SN54LS74A, SN54S74**

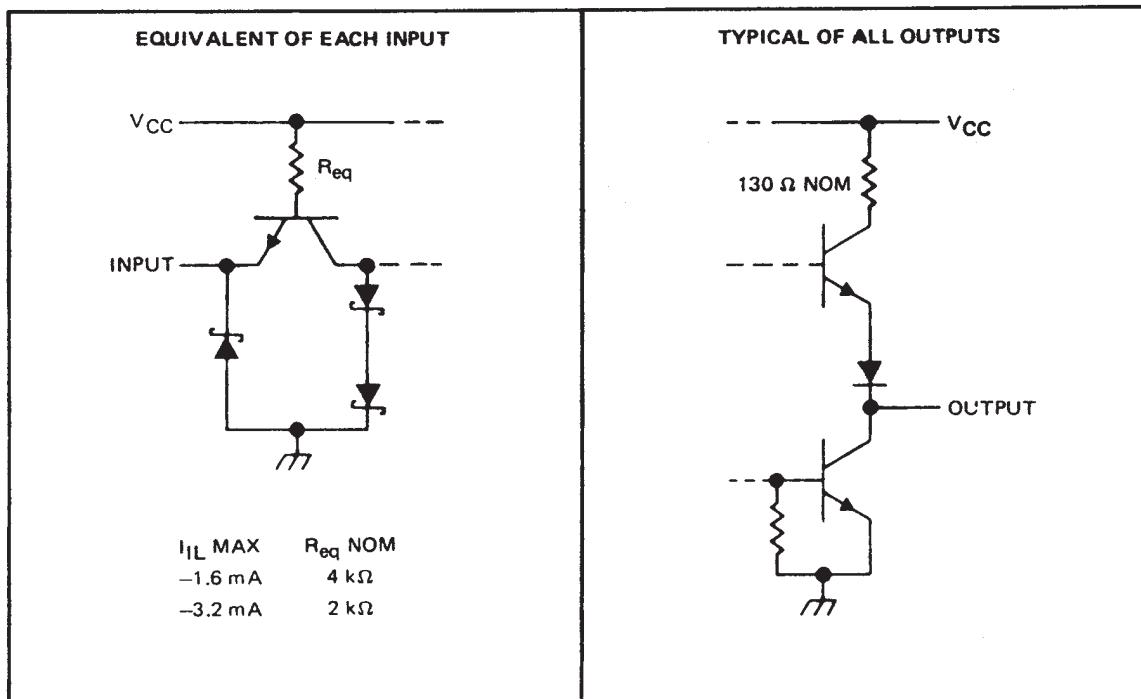
**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

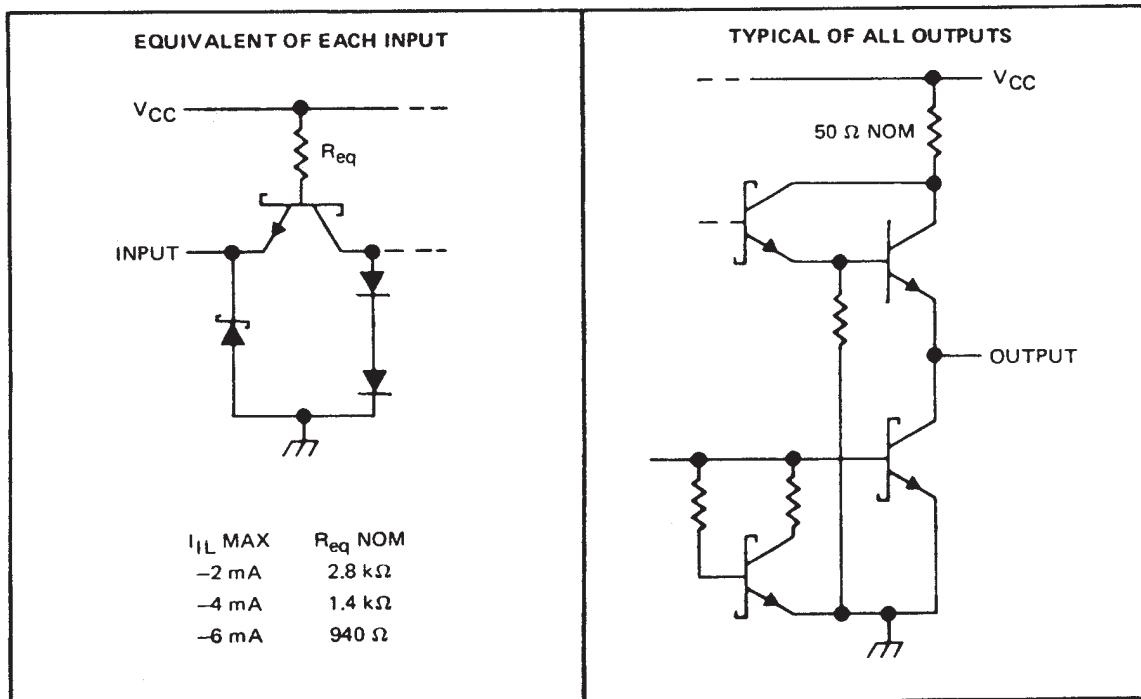
SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**schematics of inputs and outputs**

**74**



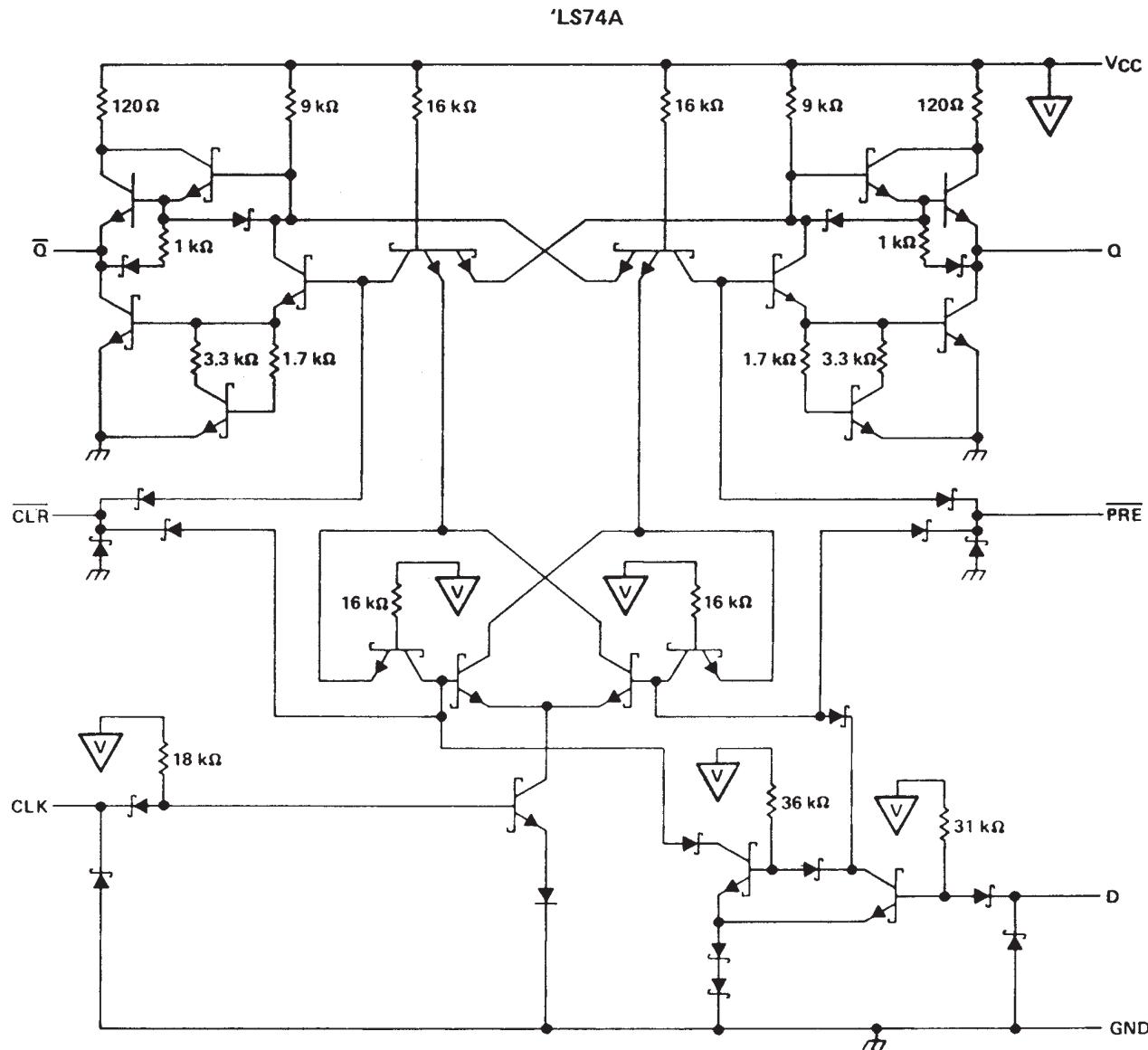
**'S74**



## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

## schematic



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub> (see Note 1) . . . . . | 7 V            |
| Input voltage: '74, 'S74 . . . . .                     | 5.5 V          |
| 'LS74A . . . . .                                       | 7 V            |
| Operating free-air temperature range: SN54' . . . . .  | -55°C to 125°C |
| SN74' . . . . .  | 0°C to 70°C    |
| Storage temperature range . . . . .                    | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**SN5474, SN54LS74A, SN54S74****SN7474, SN74LS74A, SN74S74****DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

**recommended operating conditions**

|                 |                                  |                | SN5474 |     |      | SN7474 |     |      | UNIT |
|-----------------|----------------------------------|----------------|--------|-----|------|--------|-----|------|------|
|                 |                                  |                | MIN    | NOM | MAX  | MIN    | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                   |                | 4.5    | 5   | 5.5  | 4.75   | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage         |                | 2      |     |      | 2      |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage          |                |        |     | 0.8  |        |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current        |                |        |     | -0.4 |        |     | -0.4 | mA   |
| I <sub>OL</sub> | Low-level output current         |                |        |     | 16   |        |     | 16   | mA   |
| t <sub>w</sub>  | Pulse duration                   | CLK high       | 30     |     |      | 30     |     |      | ns   |
|                 |                                  | CLK low        | 37     |     |      | 37     |     |      |      |
|                 |                                  | PRE or CLR low | 30     |     |      | 30     |     |      |      |
| t <sub>su</sub> | Input setup time before CLK t    |                | 20     |     |      | 20     |     |      | ns   |
| t <sub>h</sub>  | Input hold time-data after CLK t |                | 5      |     |      | 5      |     |      | ns   |
| T <sub>A</sub>  | Operating free-air temperature   |                | -55    |     | 125  | 0      |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                    | TEST CONDITIONS <sup>†</sup>  |   |  | SN5474 |                  |     | SN7474 |                  |     | UNIT |
|------------------------------|---|---|--|--------|------------------|-----|--------|------------------|-----|------|
|                              |   |   |  | MIN    | TYP <sup>‡</sup> | MAX | MIN    | TYP <sup>‡</sup> | MAX |      |
| V <sub>IK</sub>              | V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA  |   |  |        | -1.5             |     |        | -1.5             |     | V    |
| V <sub>OH</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,<br>I <sub>OH</sub> = -0.4 mA |   |  | 2.4    | 3.4              |     | 2.4    | 3.4              |     | V    |
| V <sub>OL</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,<br>I <sub>OL</sub> = 16 mA   |   |  | 0.2    | 0.4              |     | 0.2    | 0.4              |     | V    |
| I <sub>I</sub>               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V   |   |  |        |                  | 1   |        |                  | 1   | mA   |
| I <sub>IH</sub>              | D<br>CLR<br>All Other   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V |  |        | 40               |     |        | 40               |     | μA   |
|                              |   |   |  |        | 120              |     |        | 120              |     |      |
|                              |   |   |  |        | 80               |     |        | 80               |     |      |
| I <sub>IL</sub>              | D<br>PRE <sup>§</sup><br>CLR <sup>§</sup><br>CLK  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |  |        | -1.6             |     |        | -1.6             |     | mA   |
|                              |   |   |  |        | -1.6             |     |        | -1.6             |     |      |
|                              |   |   |  |        | -3.2             |     |        | -3.2             |     |      |
|                              |   |   |  |        | -3.2             |     |        | -3.2             |     |      |
| I <sub>OS</sub> <sup>¶</sup> | V <sub>CC</sub> = MAX   |   |  | -20    | -57              | -18 | -18    | -57              |     | mA   |
| I <sub>CC</sub> <sup>#</sup> | V <sub>CC</sub> = MAX, See Note 2   |   |  |        | 8.5              | 15  |        | 8.5              | 15  | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.<sup>§</sup>Clear is tested with preset high and preset is tested with clear high.<sup>¶</sup>Not more than one output should be shown at a time.<sup>#</sup>Average per flip-flop.NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

| PARAMETER        | FROM (INPUT) | TO (OUTPUT)    | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |  |
|------------------|--------------|----------------|--|-----|-----|-----|------|--|
| f <sub>max</sub> |              |                | R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF | 15  | 25  |     | MHz  |  |
| t <sub>PLH</sub> | PRE or CLR   | Q or $\bar{Q}$ |  |     | 25  |     | ns   |  |
| t <sub>PHL</sub> |              |                |  |     | 40  |     | ns   |  |
| t <sub>PLH</sub> | CLK          | Q or $\bar{Q}$ |  |     | 14  | 25  | ns   |  |
| t <sub>PHL</sub> |              |                |  |     | 20  | 40  | ns   |  |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDS119 - DECEMBER 1983 - REVISED MARCH 1988

## recommended operating conditions

|                    |                                |                 | SN54LS74A |     |      | SN74LS74A |      |      | UNIT |     |
|--------------------|--------------------------------|-----------------|-----------|-----|------|-----------|------|------|------|-----|
|                    | MIN                            | NOM             | MAX       | MIN | NOM  | MAX       |      |      |      |     |
| V <sub>CC</sub>    | Supply voltage                 |                 |           | 4.5 | 5    | 5.5       | 4.75 | 5    | 5.25 | V   |
| V <sub>IH</sub>    | High-level input voltage       |                 |           | 2   |      |           | 2    |      |      | V   |
| V <sub>IL</sub>    | Low-level input voltage        |                 |           |     | 0.7  |           |      | 0.8  |      | V   |
| I <sub>OH</sub>    | High-level output current      |                 |           |     | -0.4 |           |      | -0.4 |      | mA  |
| I <sub>OL</sub>    | Low-level output current       |                 |           |     | 4    |           |      | 8    |      | mA  |
| f <sub>clock</sub> | Clock frequency                |                 |           | 0   | 25   |           | 0    | 25   |      | MHz |
| t <sub>w</sub>     | Pulse duration                 | CLK high        |           | 25  |      |           | 25   |      |      | ns  |
|                    |                                | PRE or CLR low  |           | 25  |      |           | 25   |      |      |     |
| t <sub>su</sub>    | Setup time-before CLK↑         | High-level data |           | 20  |      |           | 20   |      |      | ns  |
|                    |                                | Low-level data  |           | 20  |      |           | 20   |      |      |     |
| t <sub>h</sub>     | Hold time-data after CLK↑      |                 |           | 5   |      |           | 5    |      |      | ns  |
| T <sub>A</sub>     | Operating free-air temperature |                 |           | -55 | 125  |           | 0    | 70   |      | °C  |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS <sup>†</sup> |                         |                        | SN54LS74A |                  |     | SN74LS74A |                  |     | UNIT |
|-------------------------|------------------------------|-------------------------|------------------------|-----------|------------------|-----|-----------|------------------|-----|------|
|                         |                              |                         |                        | MIN       | TYP <sup>‡</sup> | MAX | MIN       | TYP <sup>‡</sup> | MAX |      |
| V <sub>IK</sub>         | V <sub>CC</sub> = MIN,       | I <sub>I</sub> = -18 mA |                        |           | -1.5             |     |           | -1.5             |     | V    |
| V <sub>OH</sub>         | V <sub>CC</sub> = MIN,       | V <sub>IH</sub> = 2 V,  | V <sub>IL</sub> = MAX, | 2.5       | 3.4              |     | 2.7       | 3.4              |     | V    |
| V <sub>OL</sub>         | V <sub>CC</sub> = MIN,       | V <sub>IL</sub> = MAX,  | V <sub>IH</sub> = 2 V, |           | 0.25             | 0.4 | 0.25      | 0.4              |     | V    |
|                         | I <sub>OL</sub> = 4 mA       |                         |                        |           |                  |     | 0.35      | 0.5              |     |      |
| I <sub>I</sub>          | D or CLK                     | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 7 V   |           | 0.1              |     | 0.1       |                  |     | mA   |
|                         | CLR or PRE                   |                         |                        |           | 0.2              |     | 0.2       |                  |     |      |
| I <sub>IH</sub>         | D or CLK                     | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 2.7 V |           | 20               |     | 20        |                  |     | μA   |
|                         | CLR or PRE                   |                         |                        |           | 40               |     | 40        |                  |     |      |
| I <sub>IIL</sub>        | D or CLK                     | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 0.4 V |           | -0.4             |     | -0.4      |                  |     | mA   |
|                         | CLR or PRE                   |                         |                        |           | -0.8             |     | -0.8      |                  |     |      |
| I <sub>OS\$</sub>       | V <sub>CC</sub> = MAX,       | See Note 4              |                        | -20       | -100             |     | -20       | -100             |     | mA   |
| I <sub>CC</sub> (Total) | V <sub>CC</sub> = MAX,       | See Note 2              |                        | 4         | 8                |     | 4         | 8                |     | mA   |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
| f <sub>max</sub> |                 |                | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF | 25  | 33  |     | MHz  |
| t <sub>PLH</sub> | CLR, PRE or CLK | Q or $\bar{Q}$ |   | 13  | 25  |     | ns   |
| t <sub>PHL</sub> |                 |                |   | 25  | 40  |     | ns   |

Note 3: Load circuits and voltage waveforms are shown in Section 1.

**SN5474, SN54LS74A, SN54S74**

**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

|                 |                                    |                 | SN54S74 |     |     | SN74S74 |     |      | UNIT |
|-----------------|------------------------------------|-----------------|---------|-----|-----|---------|-----|------|------|
|                 |                                    |                 | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                     |                 | 4.5     | 5   | 5.5 | 4.75    | 5   | 6.25 | V    |
| V <sub>IH</sub> | High-level input voltage           |                 | 2       |     |     | 2       |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage            |                 |         |     | 0.8 |         |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current          |                 |         |     | -1  |         |     | -1   | mA   |
| I <sub>OL</sub> | Low-level output current           |                 |         |     | 20  |         |     | 20   | mA   |
| t <sub>w</sub>  | Pulse duration                     | CLK high        |         | 6   |     | 6       |     |      | ns   |
|                 |                                    | CLK low         |         | 7.3 |     | 7.3     |     |      |      |
|                 |                                    | CLR or PRE low  |         | 7   |     | 7       |     |      |      |
| t <sub>su</sub> | Setup time, before CLK ↑           | High-level data |         | 3   |     | 3       |     |      | ns   |
|                 |                                    | Low-level data  |         | 3   |     | 3       |     |      |      |
| t <sub>h</sub>  | Input hold time - data after CLK ↑ |                 |         | 2   |     | 2       |     |      | ns   |
| T <sub>A</sub>  | Operating free-air temperature     |                 | -55     |     | 125 | 0       |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                    | TEST CONDITIONS <sup>†</sup>  |   |     | SN54S74 |                  |     | SN74S74 |                  |     | UNIT |
|------------------------------|---|---|-----|---------|------------------|-----|---------|------------------|-----|------|
|                              | MIN   | TYP <sup>‡</sup>                              | MAX | MIN     | TYP <sup>‡</sup> | MAX | MIN     | TYP <sup>‡</sup> | MAX |      |
| V <sub>IK</sub>              | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA,   |   |     |         | -1.2             |     |         | -1.2             |     | V    |
| V <sub>OH</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,<br>I <sub>OH</sub> = -1 mA |   |     | 2.5     | 3.4              |     | 2.7     | 3.4              |     | V    |
| V <sub>OL</sub>              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V,<br>I <sub>OL</sub> = 20 mA |   |     |         | 0.5              |     |         | 0.5              |     | V    |
| I <sub>I</sub>               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V   |   |     |         | 1                |     |         | 1                |     | mA   |
| I <sub>IH</sub>              | D   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |     |         | 50               |     | 50      |                  |     | μA   |
|                              | CLR   |   | 150 |         | 150              |     |         |                  |     |      |
|                              | PRE or CLK  |   | 100 |         | 100              |     |         |                  |     |      |
| I <sub>IL</sub>              | D   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V |     |         | -2               |     | -2      |                  |     | mA   |
|                              | CLR <sup>§</sup>  |   | -6  |         | -6               |     |         |                  |     |      |
|                              | PRE <sup>§</sup>  |   | -4  |         | -4               |     |         |                  |     |      |
|                              | CLK   |   | -4  |         | -4               |     |         |                  |     |      |
| I <sub>OS</sub> <sup>§</sup> | V <sub>CC</sub> = MAX   |   |     | -40     | -100             | -40 | -100    |                  |     | mA   |
| I <sub>CC</sub> <sup>#</sup> | V <sub>CC</sub> = MAX, See Note 2   |   |     |         | 15               | 25  |         | 15               | 25  | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

<sup>¶</sup>Clear is tested with preset high and preset is tested with clear high.

<sup>#</sup>Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

| PARAMETER        | FROM<br>(INPUT)       | TO<br>(OUTPUT) | TEST CONDITIONS                                | MIN | TYP | MAX  | UNIT |
|------------------|-----------------------|----------------|--|-----|-----|------|------|
| f <sub>max</sub> |                       |                | R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF | 75  | 110 |      | MHz  |
| t <sub>PLH</sub> | PRE or CLR            | Q or $\bar{Q}$ |  |     | 4   | 6    | ns   |
| t <sub>PHL</sub> | PRE or CLR (CLK high) | $\bar{Q}$ or Q |  |     | 9   | 13.5 | ns   |
|                  | PRE or CLR (CLK low)  | Q or $\bar{Q}$ |  |     | 5   | 8    |      |
| t <sub>PLH</sub> | CLK                   | Q or $\bar{Q}$ |  |     | 6   | 9    | ns   |
| t <sub>PHL</sub> |                       |                |  |     | 6   | 9    | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| JM38510/07101BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/07101BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/07101BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30102B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30102B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102SCA | ACTIVE        | CDIP         | J               | 14   | 25          | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102SCA | ACTIVE        | CDIP         | J               | 14   | 25          | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102SDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30102SDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07101BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07101BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07101BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| M38510/07101BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07101BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30102B2A        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30102B2A        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102SCA  | ACTIVE        | CDIP         | J               | 14   | 25          | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102SCA  | ACTIVE        | CDIP         | J               | 14   | 25          | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102SDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30102SDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30102SDA        | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS74AJ       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS74AJ              | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS74AJ       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS74AJ              | <span style="background-color: red; color: white;">Samples</span> |
| SN54S74J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S74J                | <span style="background-color: red; color: white;">Samples</span> |
| SN54S74J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S74J                | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74AD       | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74AD       | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADBR     | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74LS74ADBR     | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADE4     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADE4     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADG4     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADG4     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADRG4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ADRG4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS74A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74AN       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS74AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74AN       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS74AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANE4     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS74AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANE4     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS74AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS74A                 | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS74A                 | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANSRG4   | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS74A                 | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS74ANSRG4   | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS74A                 | <span style="background-color: red; color: white;">Samples</span> |
| SN74S74D         | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S74                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S74D         | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | S74                     | <span style="background-color: red; color: white;">Samples</span> |
| SN74S74N         | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74S74N                | <span style="background-color: red; color: white;">Samples</span> |
| SN74S74N         | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74S74N                | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74S74NSR       | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74S74                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74S74NSR       | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74S74                   | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AFK     | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS &<br>Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS<br>74AFK        | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AFK     | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS &<br>Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS<br>74AFK        | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AJ      | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS74AJ             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AJ      | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS74AJ             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AW      | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS74AW             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS74AW      | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS74AW             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S74J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S74J               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S74J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S74J               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S74W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S74W               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S74W        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S74W               | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS74A, SN54LS74A-SP, SN54S74, SN74LS74A, SN74S74 :**

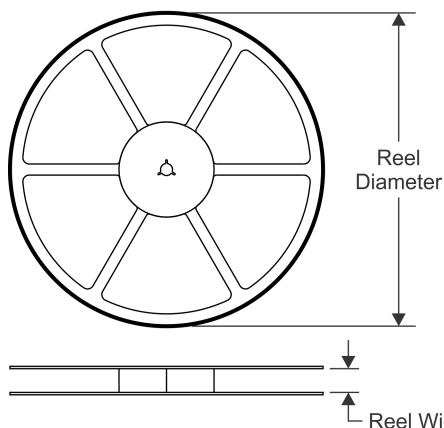
- Catalog: [SN74LS74A](#), [SN54LS74A](#), [SN74S74](#)
- Military: [SN54LS74A](#), [SN54S74](#)
- Space: [SN54LS74A-SP](#)

NOTE: Qualified Version Definitions:

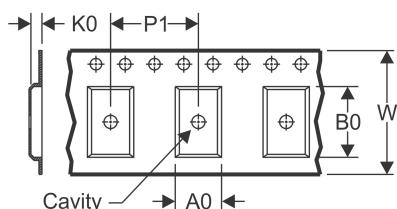
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

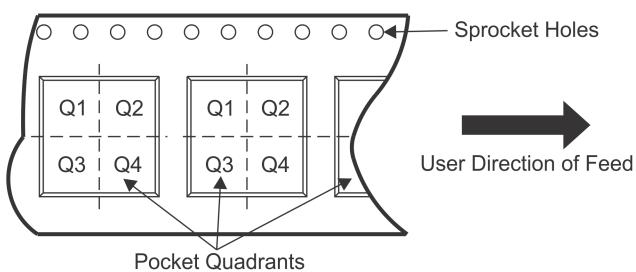


### TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

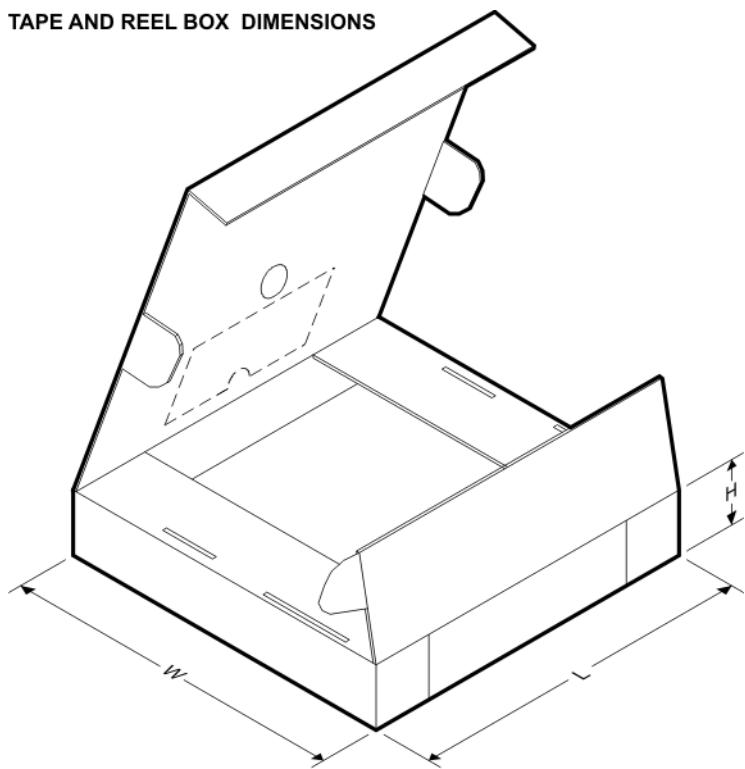
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS74ADR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74S74NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



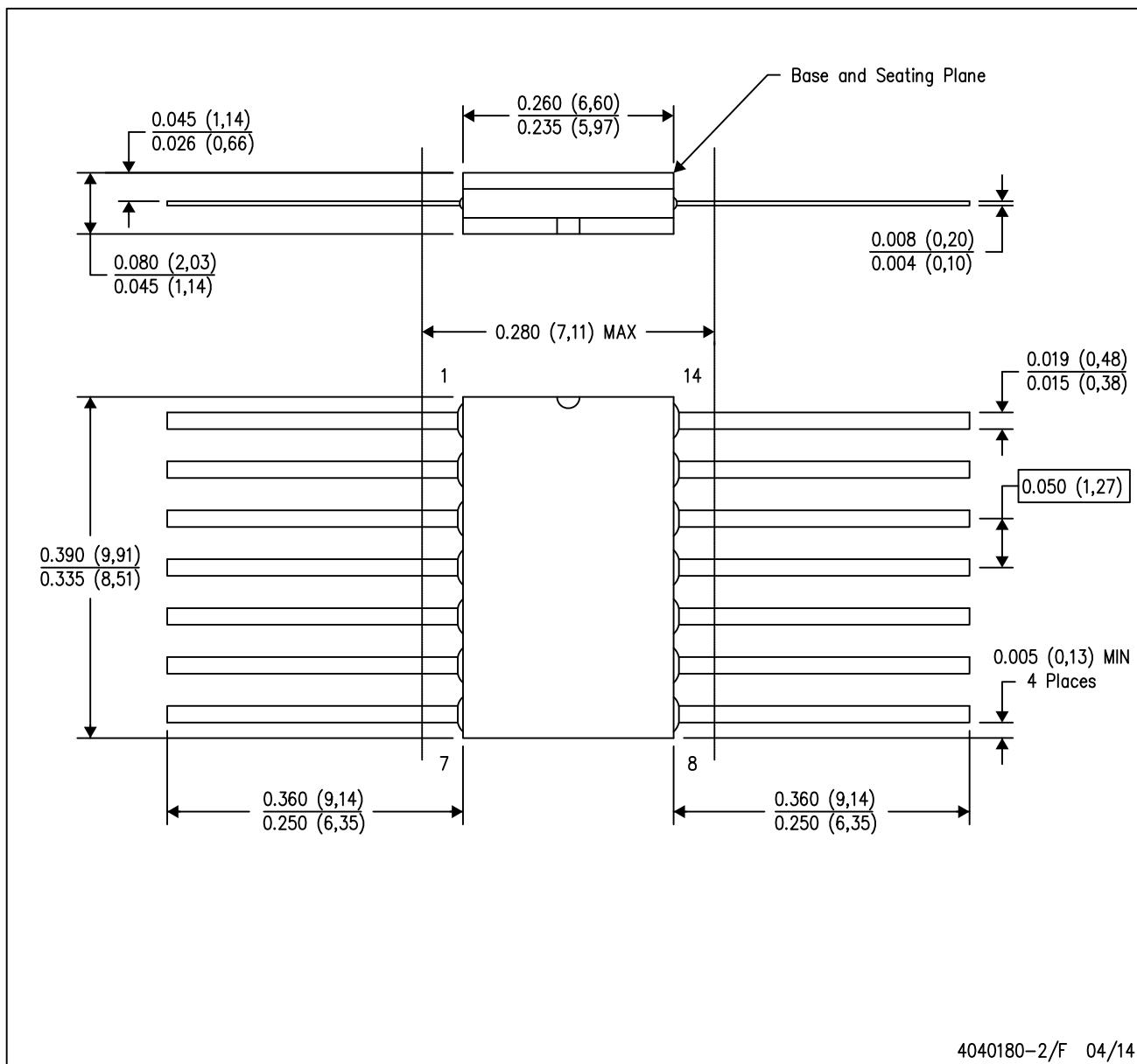
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS74ADR | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74S74NSR  | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

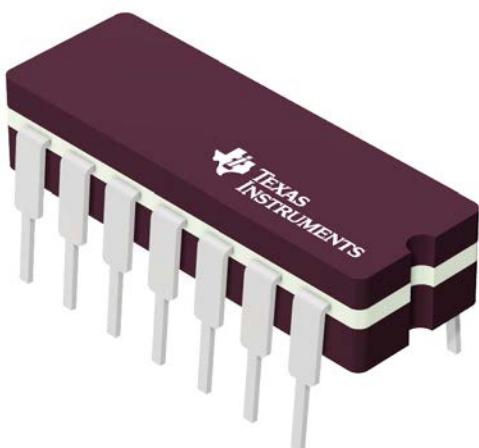
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

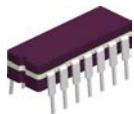
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

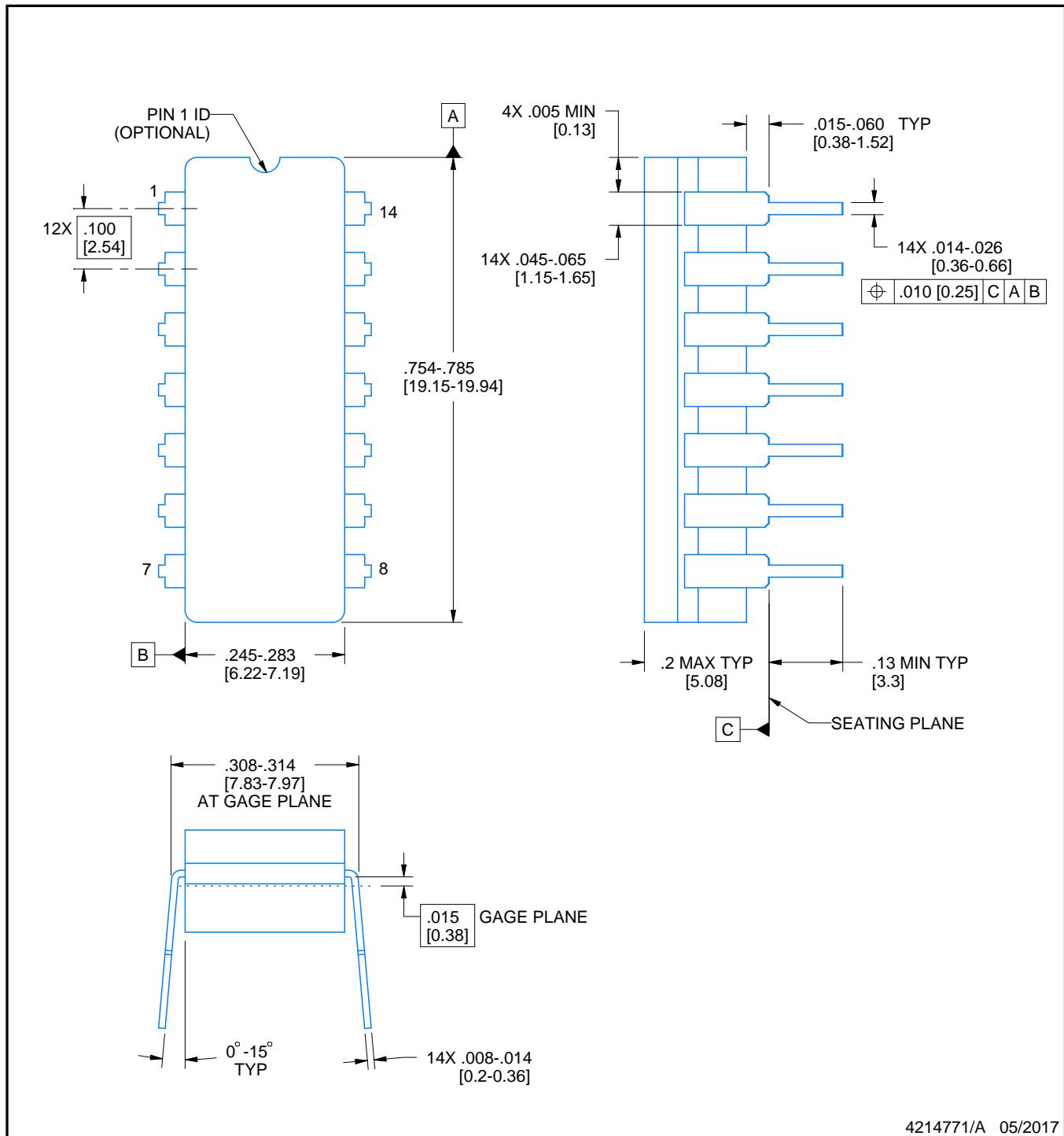
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

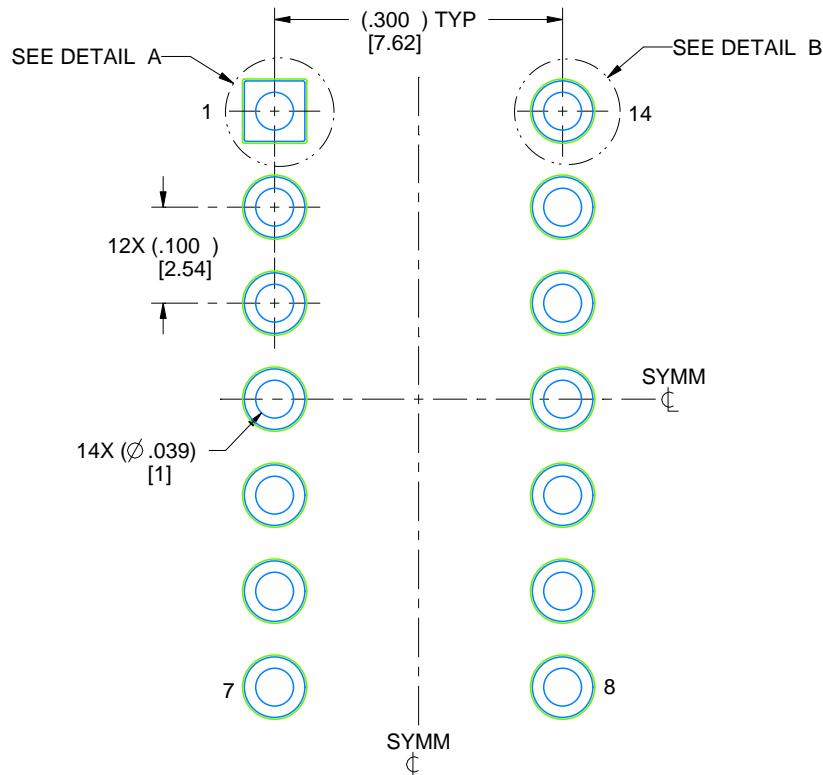
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

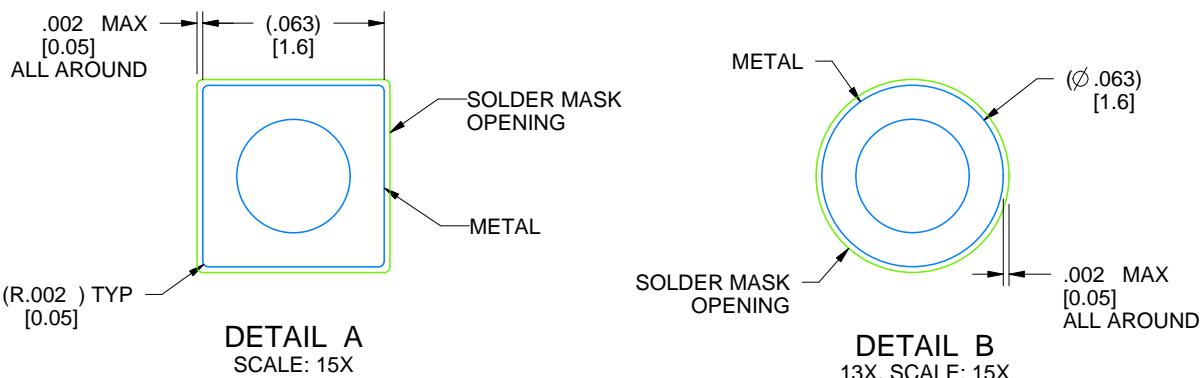
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



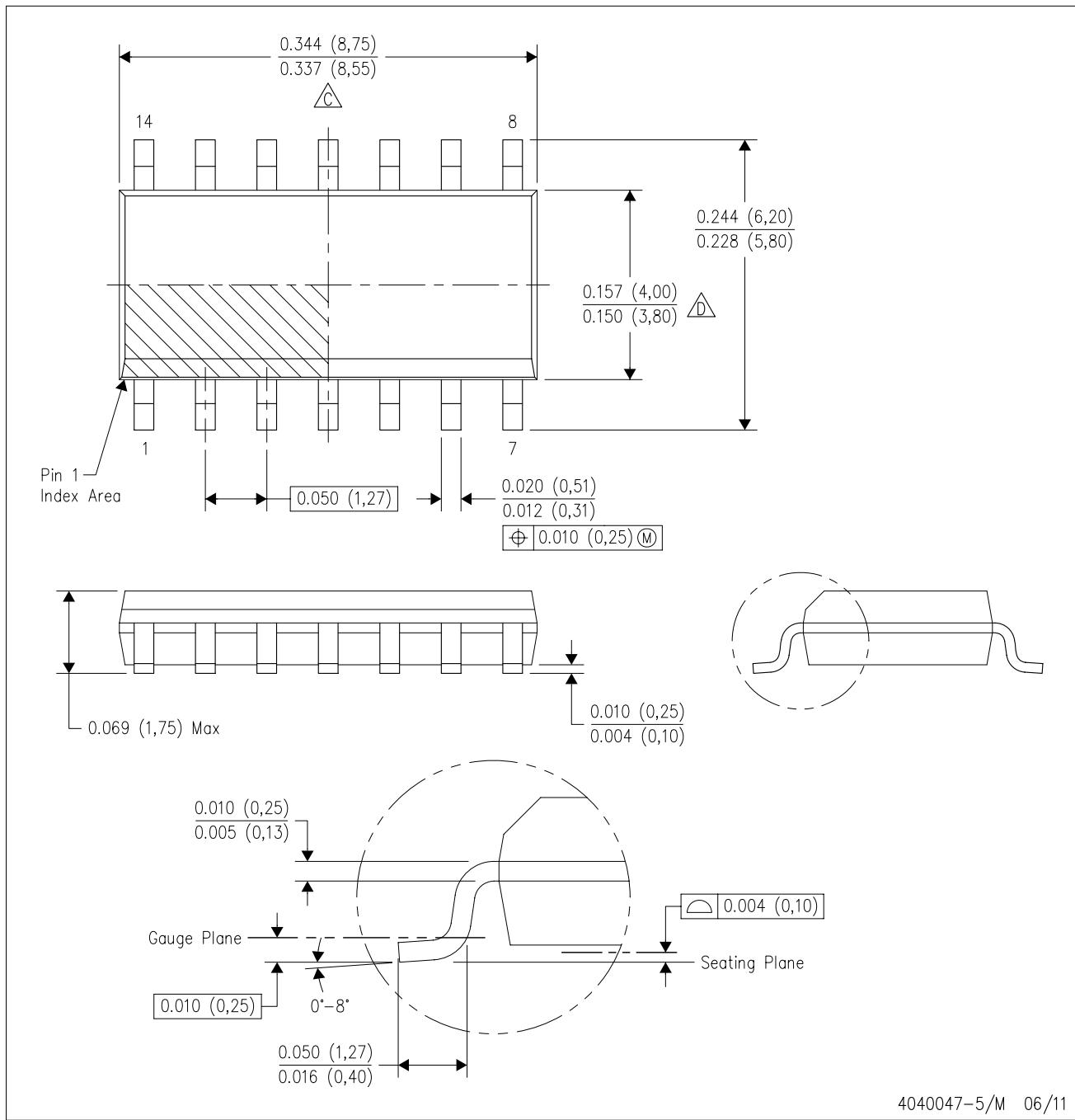
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

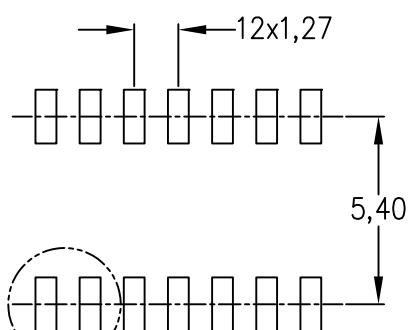
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

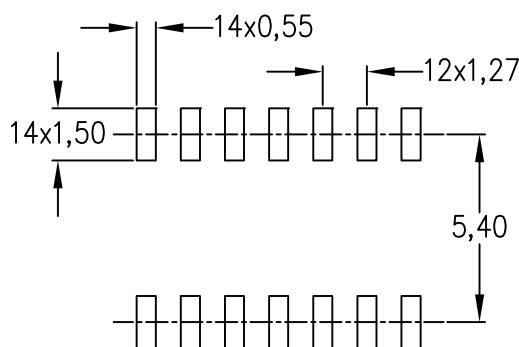
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

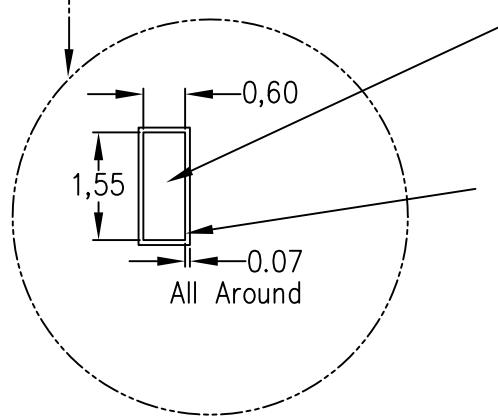
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

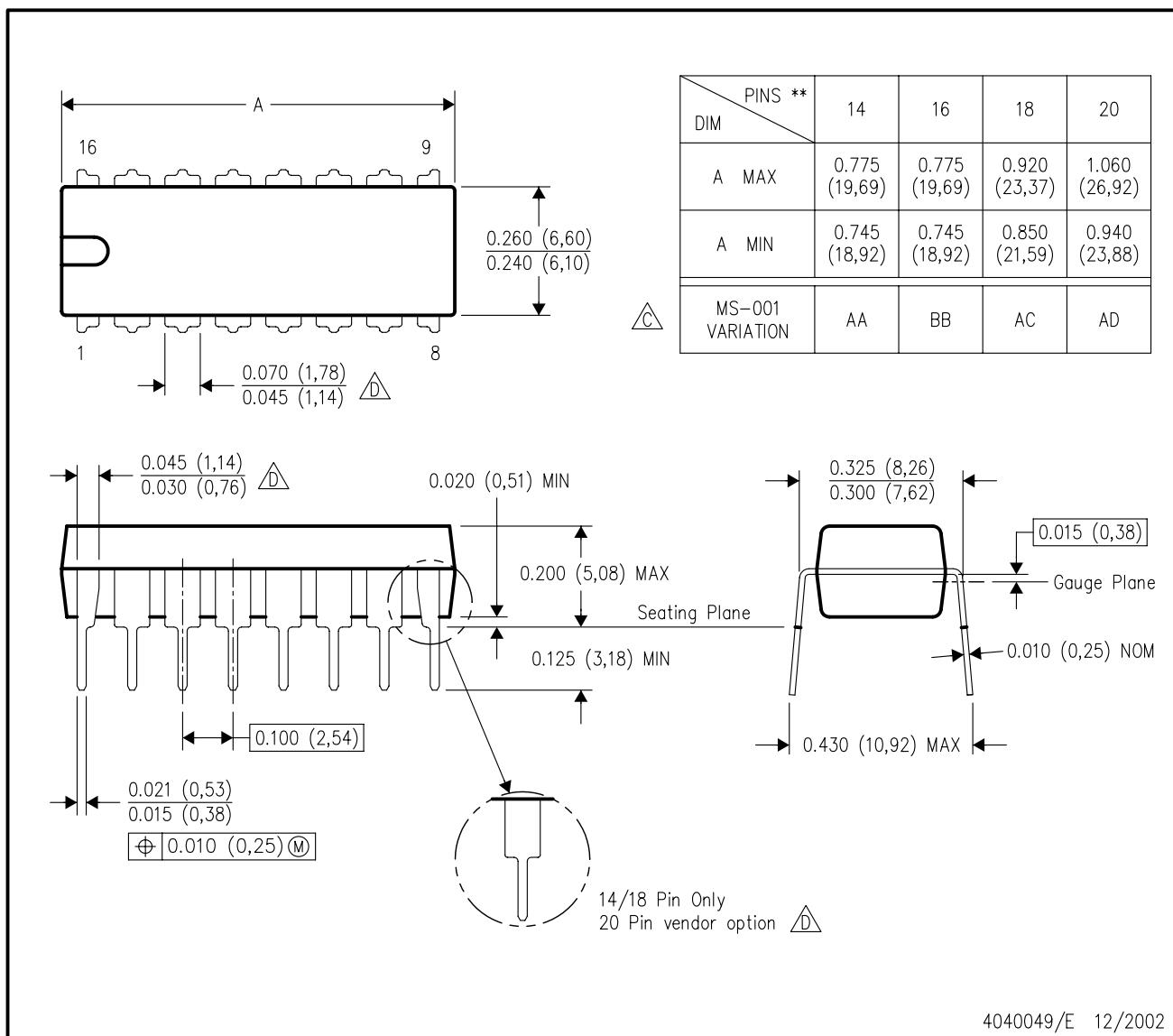
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

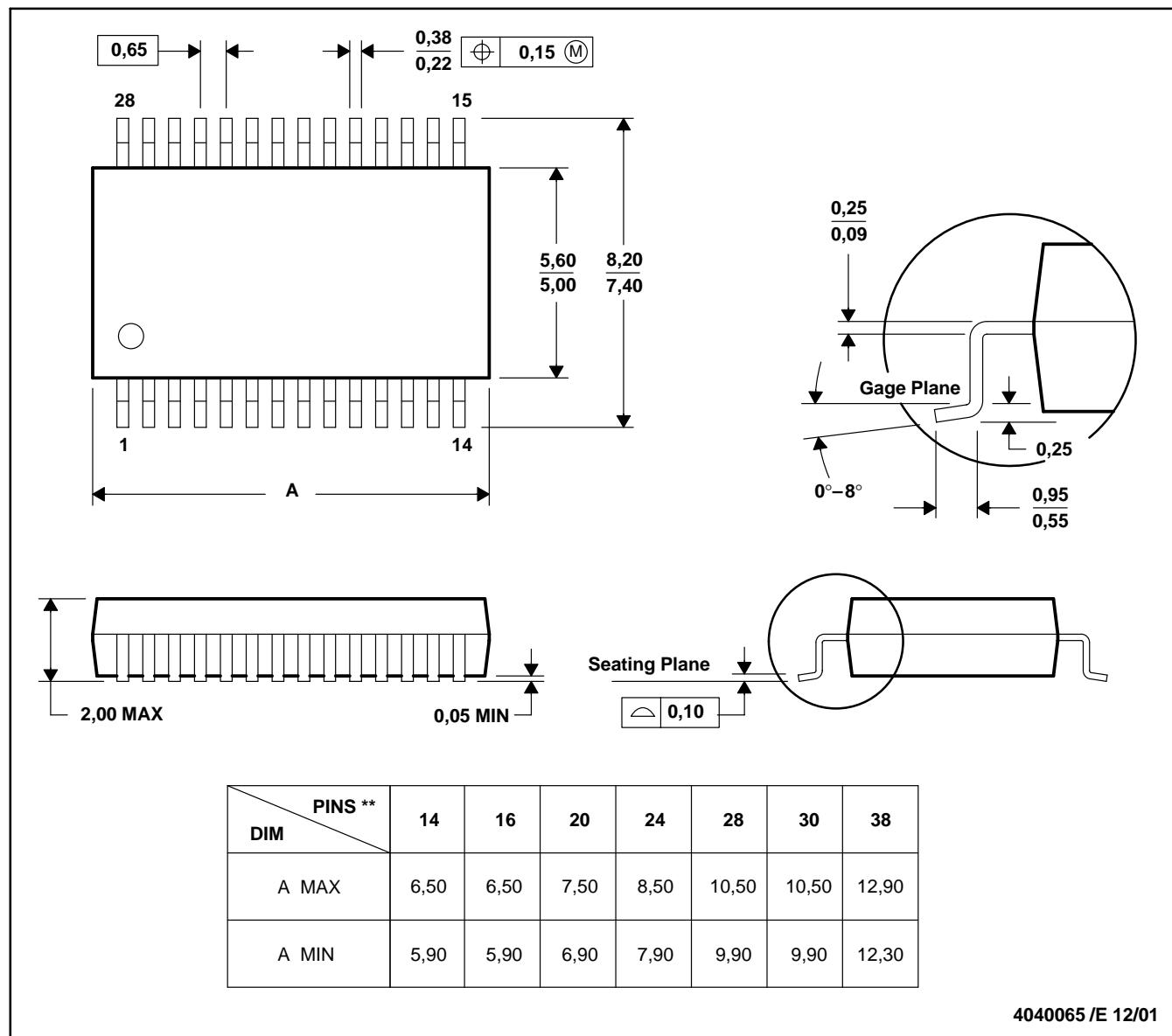
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

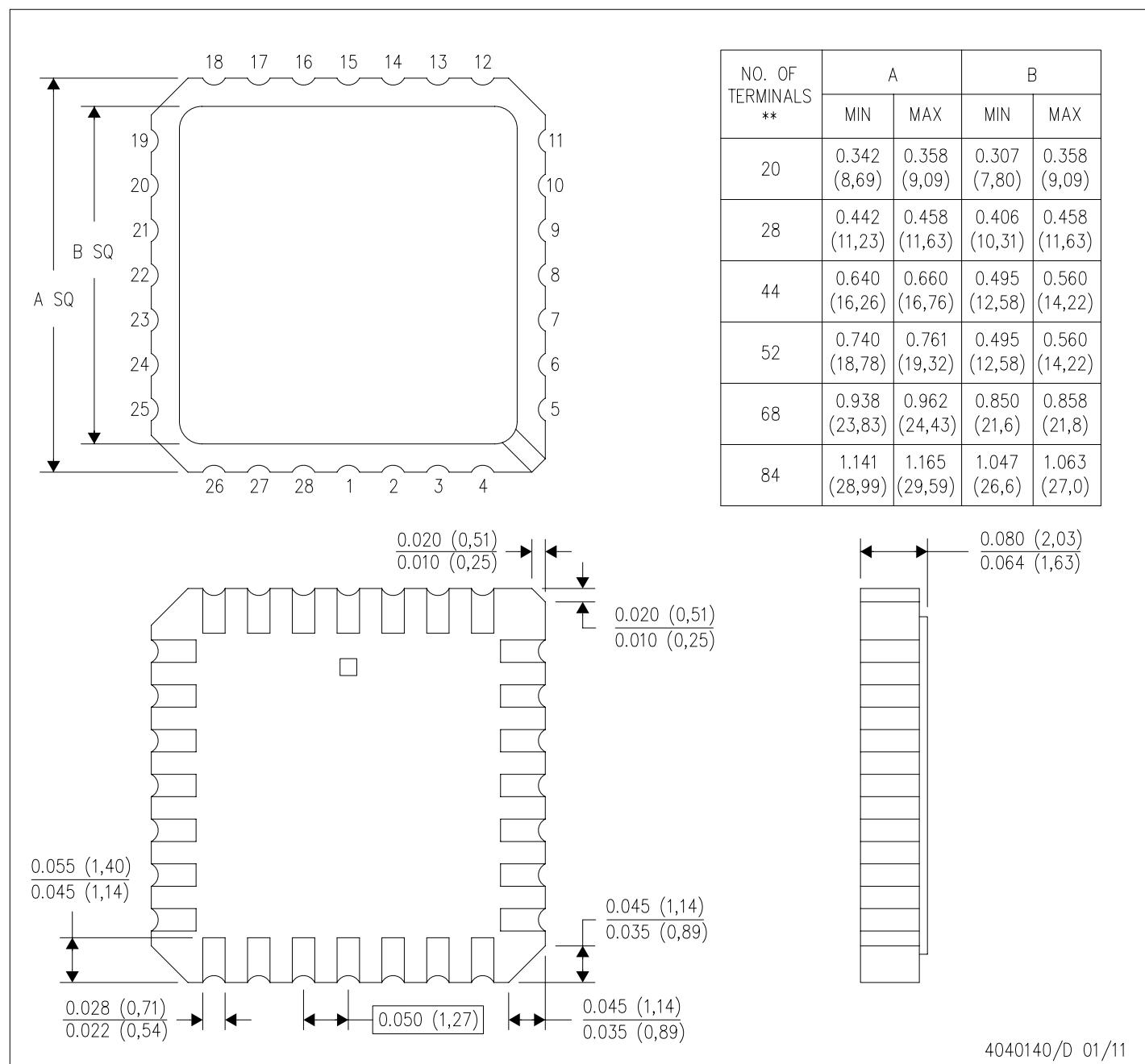


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

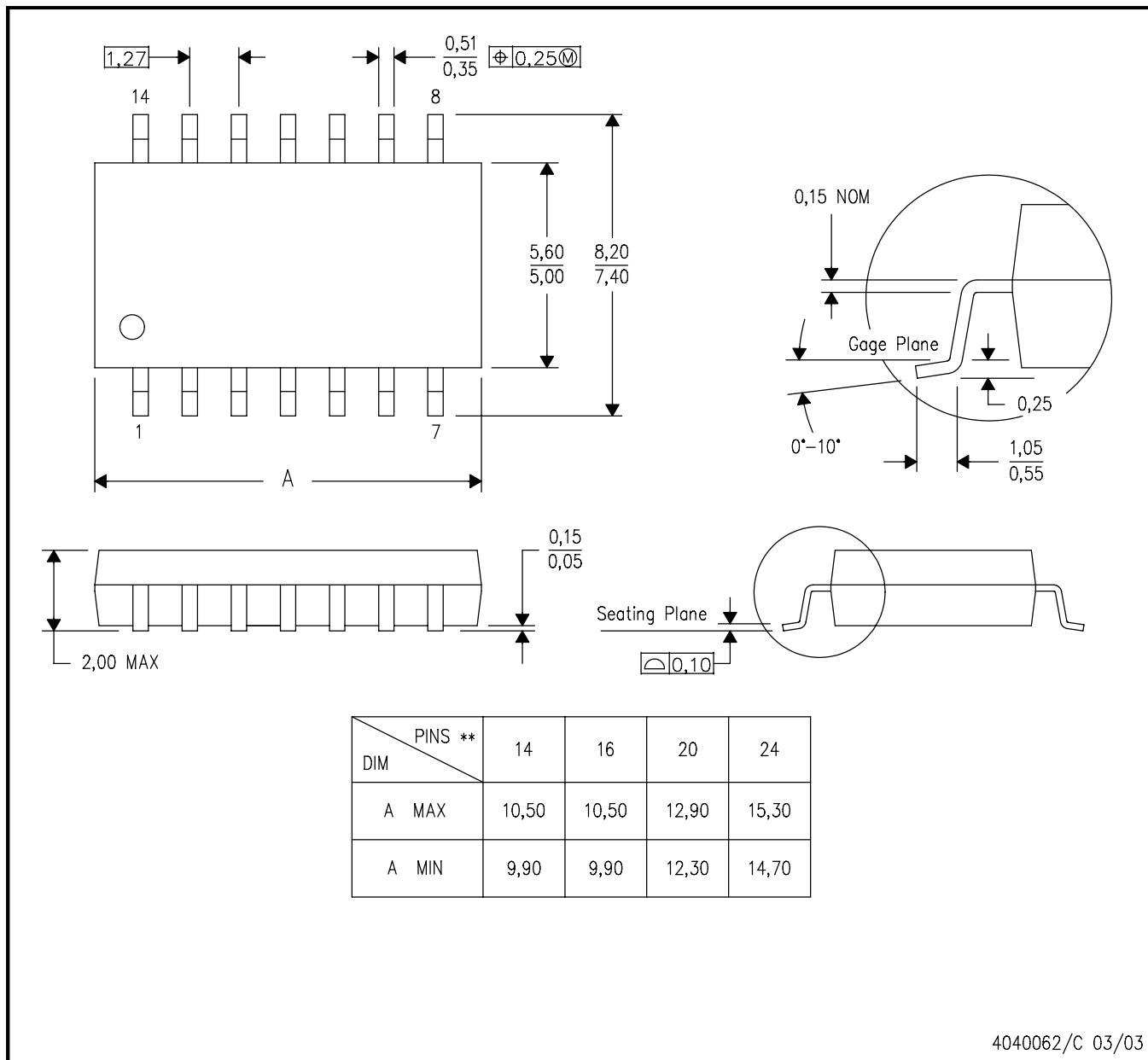
4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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SN5485, SN54LS85, SN54S85  
 SN7485, SN74LS85, SN74S85  
**4-BIT MAGNITUDE COMPARATORS**

SDLS123 – MARCH 1974 – REVISED MARCH 1988

| TYPE  | TYPICAL POWER | TYPICAL DELAY<br>(4-BIT WORDS) |
|-------|---------------|--------------------------------|
| '85   | 275 mW        | 23 ns                          |
| 'LS85 | 52 mW         | 24 ns                          |
| 'S85  | 365 mW        | 11 ns                          |

### description

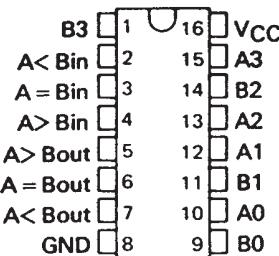
These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE

SN7485 . . . N PACKAGE

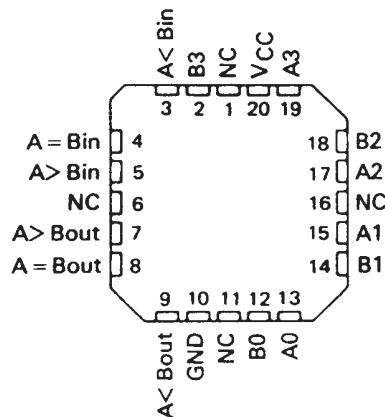
SN74LS85, SN74S85 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS85, SN54S85 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

### FUNCTION TABLE

| COMPARING INPUTS |         |         |         | CASCAADING INPUTS |       |       | OUTPUTS |       |       |
|------------------|---------|---------|---------|-------------------|-------|-------|---------|-------|-------|
| A3, B3           | A2, B2  | A1, B1  | A0, B0  | A > B             | A < B | A = B | A > B   | A < B | A = B |
| A3 > B3          | X       | X       | X       | X                 | X     | X     | H       | L     | L     |
| A3 < B3          | X       | X       | X       | X                 | X     | X     | L       | H     | L     |
| A3 = B3          | A2 > B2 | X       | X       | X                 | X     | X     | H       | L     | L     |
| A3 = B3          | A2 < B2 | X       | X       | X                 | X     | X     | L       | H     | L     |
| A3 = B2          | A2 = B2 | A1 > B1 | X       | X                 | X     | X     | H       | L     | L     |
| A3 = B3          | A2 = B2 | A1 < B1 | X       | X                 | X     | X     | L       | H     | L     |
| A2 = B3          | A2 = B2 | A1 = B1 | A0 > B0 | X                 | X     | X     | H       | L     | L     |
| A3 = B3          | A2 = B2 | A1 = B1 | A0 < B0 | X                 | X     | X     | L       | H     | L     |
| A3 = B3          | A2 = B2 | A1 = B1 | A0 = B0 | H                 | L     | L     | H       | L     | L     |
| A3 = B3          | A2 = B2 | A1 = B1 | A0 = B0 | L                 | H     | L     | L       | L     | H     |
| A3 = B3          | A2 = B2 | A1 = B1 | A0 = B0 | H                 | H     | L     | L       | L     | L     |
| A3 = B3          | A2 = B2 | A1 = B1 | A0 = B0 | L                 | L     | L     | H       | H     | L     |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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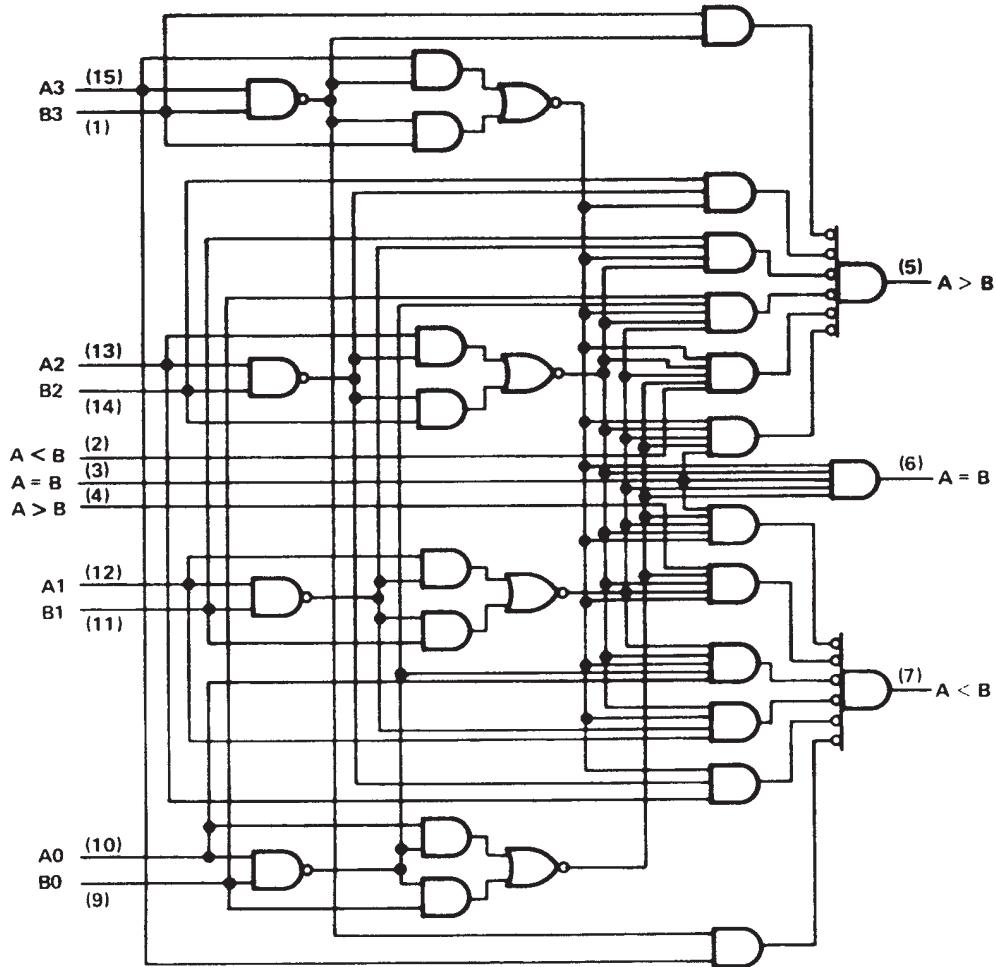


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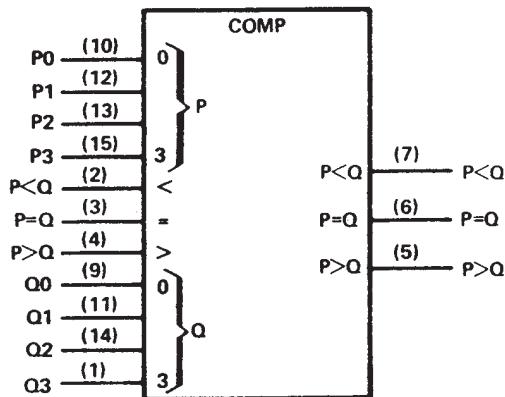
**SN5485, SN54LS85, SN54S85  
SN7485, SN74LS85, SN74S85  
4-BIT MAGNITUDE COMPARATORS**

SDLS123 – MARCH 1974 – REVISED MARCH 1988

logic diagrams (positive logic)

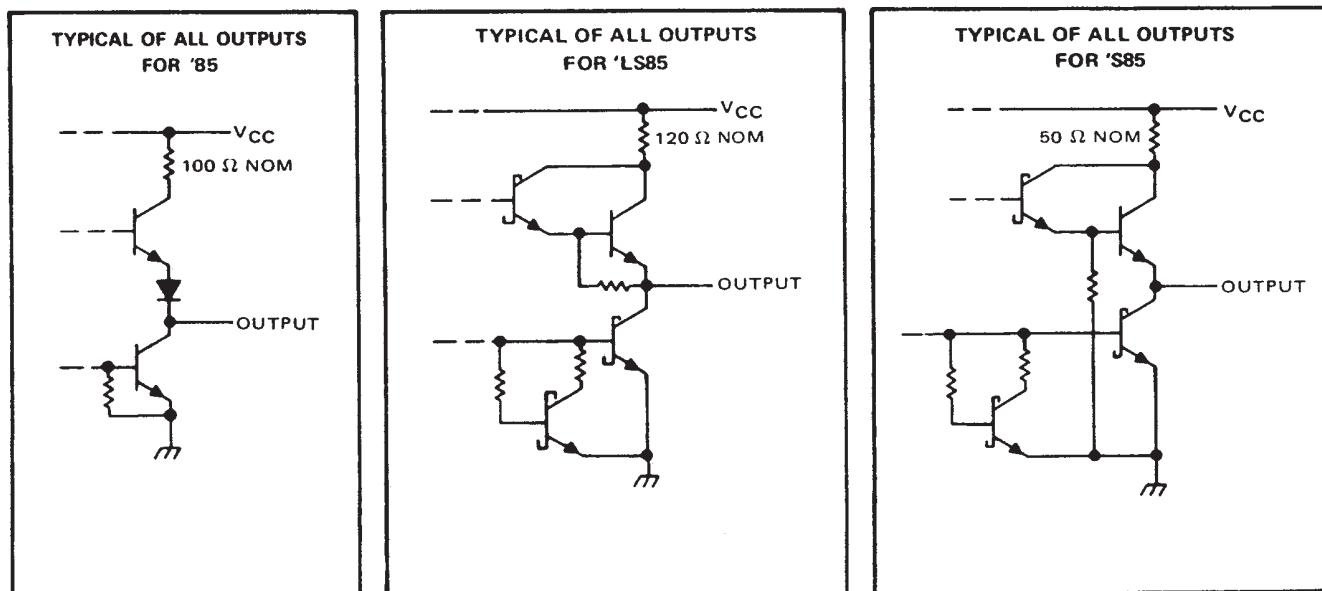
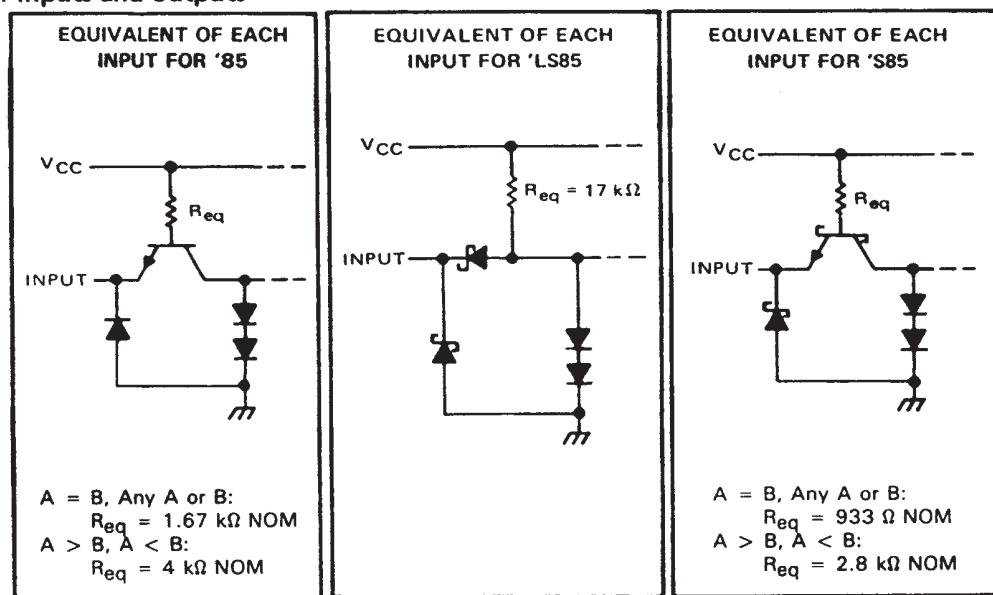


logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|  | SN54'<br>SN54S' | SN54LS' | SN74'<br>SN74S' | SN74LS' | UNIT |
|--|-----------------|---------|-----------------|---------|------|
| Supply voltage, V <sub>CC</sub> (see Note 1) | 7               | 7       | 7               | 7       | V    |
| Input voltage                                | 5.5             | 7       | 5.5             | 7       | V    |
| Interemitter voltage (see Note 2)            | 5.5             |         | 5.5             |         | V    |
| Operating free-air temperature range         | –55 to 125      |         | –0 to 70        |         | °C   |
| Storage temperature range                    | –65 to 150      |         | –65 to 150      |         | °C   |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

**SN5485, SN54LS85, SN54S85  
SN7485, SN74LS85, SN74S85  
4-BIT MAGNITUDE COMPARATORS**

SDLS123 – MARCH 1974 – REVISED MARCH 1988

**recommended operating conditions**

|                                       | SN5485 |     |      | SN7485 |     |      | UNIT        |
|---------------------------------------|--------|-----|------|--------|-----|------|-------------|
|                                       | MIN    | NOM | MAX  | MIN    | NOM | MAX  |             |
| Supply voltage, $V_{CC}$              | 4.5    | 5   | 5.5  | 4.75   | 5   | 5.25 | V           |
| High-level output current, $I_{OH}$   |        |     | -400 |        |     | -400 | $\mu A$     |
| Low-level output current, $I_{OL}$    |        |     | 16   |        |     | 16   | mA          |
| Operating free-air temperature, $T_A$ | -55    |     | 125  | 0      |     | 70   | $^{\circ}C$ |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS <sup>†</sup>                          |  | MIN    | TYP <sup>‡</sup> | MAX | UNIT    |
|--|---|--|--------|------------------|-----|---------|
| $V_{IH}$ High-level input voltage                  |   |  |        | 2                |     | V       |
| $V_{IL}$ Low-level input voltage                   |   |  |        | 0.8              |     | V       |
| $V_{IK}$ Input clamp voltage                       | $V_{CC} = \text{MIN}$ ,                               | $I_I = -12 \text{ mA}$                               |        | -1.5             |     | V       |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = \text{MIN}$ ,<br>$V_{IL} = 0.8 \text{ V}$ , | $V_{IH} = 2 \text{ V}$ ,<br>$I_{OH} = -400 \mu A$    | 2.4    | 3.4              |     | V       |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = \text{MIN}$ ,<br>$V_{IL} = 0.8 \text{ V}$ , | $V_{IH} = 2 \text{ V}$ ,<br>$I_{OL} = 16 \text{ mA}$ | 0.2    | 0.4              |     | V       |
| $I_I$ Input current at maximum input voltage       | $V_{CC} = \text{MAX}$ ,                               | $V_I = 5.5 \text{ V}$                                |        | 1                |     | mA      |
| $I_{IH}$ High-level input current                  | A < B, A > B inputs<br>all other inputs               | $V_{CC} = \text{MAX}$ ,<br>$V_I = 2.4 \text{ V}$     |        | 40               |     | $\mu A$ |
| $I_{IL}$ Low-level input current                   | A < B, A > B inputs<br>all other inputs               | $V_{CC} = \text{MAX}$ ,<br>$V_I = 0.4 \text{ V}$     |        | 120              |     | mA      |
| $I_{OS}$ Short-circuit output current <sup>§</sup> |   | $V_{CC} = \text{MAX}$ , $V_O = 0$                    | SN5485 | -20              | -55 |         |
|  |   |  | SN7485 | -18              | -55 | mA      |
| $I_{CC}$ Supply current                            | $V_{CC} = \text{MAX}$ , See Note 4                    |  |        | 55               | 88  | mA      |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$**

| PARAMETER <sup>¶</sup> | FROM INPUT            | TO OUTPUT    | NUMBER OF GATE LEVELS | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|------------------------|-----------------------|--------------|-----------------------|---|-----|-----|-----|------|
| $t_{PLH}$              | Any A or B data input | A < B, A > B | 1                     | $C_L = 15 \text{ pF}$ ,<br>$R_L = 400 \Omega$ ,<br>See Note 5 | 7   |     |     | ns   |
|                        |                       |              | 2                     |   | 12  |     |     |      |
|                        |                       |              | 3                     |   | 17  | 26  |     |      |
|                        |                       | A = B        | 4                     |   | 23  | 35  |     |      |
| $t_{PHL}$              | Any A or B data input | A < B, A > B | 1                     |   | 11  |     |     | ns   |
|                        |                       |              | 2                     |   | 15  |     |     |      |
|                        |                       |              | 3                     |   | 20  | 30  |     |      |
|                        |                       | A = B        | 4                     |   | 20  | 30  |     |      |
| $t_{PLH}$              | A < B or A = B        | A > B        | 1                     |   | 7   | 11  |     | ns   |
| $t_{PHL}$              | A < B or A = B        | A > B        | 1                     |   | 11  | 17  |     | ns   |
| $t_{PLH}$              | A = B                 | A = B        | 2                     |   | 13  | 20  |     | ns   |
| $t_{PHL}$              | A = B                 | A = B        | 2                     |   | 11  | 17  |     | ns   |
| $t_{PLH}$              | A > B or A = B        | A < B        | 1                     |   | 7   | 11  |     | ns   |
| $t_{PHL}$              | A > B or A = B        | A < B        | 1                     |   | 11  | 17  |     | ns   |

<sup>¶</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

<sup>¶</sup> $t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**recommended operating conditions**

|                                       | SN54LS85 |     |     | SN74LS85 |     |      | UNIT        |
|---------------------------------------|----------|-----|-----|----------|-----|------|-------------|
|                                       | MIN      | NOM | MAX | MIN      | NOM | MAX  |             |
| Supply voltage, $V_{CC}$              | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V           |
| High-level output current, $I_{OH}$   |          |     |     | -400     |     | -400 | $\mu A$     |
| Low-level output current, $I_{OL}$    |          |     |     | 4        |     | 8    | mA          |
| Operating free-air temperature, $T_A$ | -55      |     | 125 | 0        |     | 70   | $^{\circ}C$ |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS <sup>†</sup>  |   | SN54LS85   | SN74LS85         | UNIT    |      |    |    |
|--|---|---|------------|------------------|---------|------|----|----|
|  |   |   | MIN        | TYP <sup>‡</sup> |         |      |    |    |
| $V_{IH}$ High-level input voltage                  |   |   | 2          | 2                | V       |      |    |    |
| $V_{IL}$ Low-level input voltage                   |   |   | 0.7        | 0.7              | V       |      |    |    |
| $V_{IK}$ Input clamp voltage                       | $V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$  |   | -1.5       | -1.5             | V       |      |    |    |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = V_{IL \text{ max}}$ , $I_{OH} = -400 \mu A$ |   | 2.5        | 3.4              | V       |      |    |    |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = \text{MIN}$ ,<br>$V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = V_{IL \text{ max}}$                      | $I_{OL} = 4 \text{ mA}$                       | 0.25       | 0.4              | 0.25    | 0.4  | V  |    |
|  |   | $I_{OL} = 8 \text{ mA}$                       |            |                  | 0.35    | 0.5  |    |    |
| $I_I$ Input current at maximum input voltage       | $A < B$ , $A > B$ inputs  | $V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$   | 0.1        | 0.1              | mA      |      |    |    |
|  | all other inputs  |   | 0.3        | 0.3              |         |      |    |    |
| $I_{IH}$ High-level input current                  | $A < B$ , $A > B$ inputs  | $V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$ | 20         | 20               | $\mu A$ |      |    |    |
|  | all other inputs  |   | 60         | 60               |         |      |    |    |
| $I_{IL}$ Low-level input current                   | $A < B$ , $A > B$ inputs  | $V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$ | -0.4       | -0.4             | mA      |      |    |    |
|  | all other inputs  |   | -1.2       | -1.2             |         |      |    |    |
| $I_{OS}$ Short-circuit output current <sup>§</sup> | $V_{CC} = \text{MAX}$   |   | -20        | -100             | -20     | -100 | mA |    |
| $I_{CC}$ Supply current                            | $V_{CC} = \text{MAX}$   |   | See Note 4 | 10.4             | 20      | 10.4 | 20 | mA |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$**

| PARAMETER <sup>¶</sup> | FROM INPUT            | TO OUTPUT         | NUMBER OF GATE LEVELS | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|------------------------|-----------------------|-------------------|-----------------------|--|-----|-----|-----|------|
| tPLH                   | Any A or B data input | $A < B$ , $A > B$ | 1                     | $C_L = 15 \text{ pF}$ ,<br>$R_L = 2 \text{ k}\Omega$ ,<br>See Note 5 | 14  |     |     | ns   |
|                        |                       |                   | 2                     |  | 19  |     |     |      |
|                        |                       |                   | 3                     |  | 24  | 36  |     |      |
|                        |                       |                   | 4                     |  | 27  | 45  |     |      |
| tPHL                   | Any A or B data input | $A < B$ , $A > B$ | 1                     |  | 11  |     |     | ns   |
|                        |                       |                   | 2                     |  | 15  |     |     |      |
|                        |                       |                   | 3                     |  | 20  | 30  |     |      |
|                        |                       |                   | 4                     |  | 23  | 45  |     |      |
| tPLH                   | $A < B$ or $A = B$    | $A > B$           | 1                     |  | 14  | 22  |     | ns   |
| tPHL                   | $A < B$ or $A = B$    | $A > B$           | 1                     |  | 11  | 17  |     | ns   |
| tPLH                   | $A = B$               | $A = B$           | 2                     |  | 13  | 20  |     | ns   |
| tPHL                   | $A = B$               | $A = B$           | 2                     |  | 13  | 26  |     | ns   |
| tPLH                   | $A > B$ or $A = B$    | $A < B$           | 1                     |  | 14  | 22  |     | ns   |
| tPHL                   | $A > B$ or $A = B$    | $A < B$           | 1                     |  | 11  | 17  |     | ns   |

<sup>¶</sup>tPLH = propagation delay time, low-to-high-level output

tPHL = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

**SN54S85, SN54LS85, SN54S85  
SN74S85, SN74LS85, SN74S85  
4-BIT MAGNITUDE COMPARATORS**

SDLS123 – MARCH 1974 – REVISED MARCH 1988

**recommended operating conditions**

|                                       | SN54S85 |     |     | SN74S85 |     |      | UNIT |
|---------------------------------------|---------|-----|-----|---------|-----|------|------|
|                                       | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5     | 5   | 5.5 | 4.75    | 5   | 5.25 | V    |
| High-level output current, $I_{OH}$   |         |     | -1  |         |     | -1   | mA   |
| Low-level output current, $I_{OL}$    |         |     | 20  |         |     | 20   | mA   |
| Operating free-air temperature, $T_A$ | -55     |     | 125 | 0       |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS <sup>†</sup>   |  | MIN      | TYP <sup>‡</sup> | MAX  | UNIT          |
|--|--|--|----------|------------------|------|---------------|
| $V_{IH}$ High-level input voltage                  |  |  | 2        |                  |      | V             |
| $V_{IL}$ Low-level input voltage                   |  |  |          | 0.8              |      | V             |
| $V_{IK}$ Input clamp voltage                       | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$  |  |          | -1.2             |      | V             |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$<br>$V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ |  | SN54S85  | 2.5              | 3.4  | V             |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$<br>$V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$ |  | SN74S85  | 2.7              | 3.4  |               |
| $I_I$ Input current at maximum input voltage       | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$   |  |          | 1                |      | mA            |
| $I_{IH}$ High-level input current                  | A < B, A > B inputs<br>all other inputs  | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ |          | 50               |      | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                   | A < B, A > B inputs<br>all other inputs  | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ |          | -2               |      | mA            |
| $I_{OS}$ Short-circuit output current <sup>§</sup> | $V_{CC} = \text{MAX}$  |  | -40      |                  | -100 | mA            |
| $I_{CC}$ Supply current                            | $V_{CC} = \text{MAX}, \text{ See Note 4}$  |  |          | 73               | 115  | mA            |
|  | $V_{CC} = \text{MAX}, T_A = 125^\circ\text{C},$<br>See Note 4                                    |  | SN54S85W |                  | 110  |               |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$**

| PARAMETER <sup>¶</sup> | FROM INPUT            | TO OUTPUT    | NUMBER OF GATE LEVELS | TEST CONDITIONS  | MIN  | TYP  | MAX | UNIT |
|------------------------|-----------------------|--------------|-----------------------|--|------|------|-----|------|
| $t_{PLH}$              | Any A or B data input | A < B, A > B | 1                     | $C_L = 15 \text{ pF}, R_L = 280 \Omega,$<br>See Note 5 | 5    |      |     | ns   |
|                        |                       |              | 2                     |  | 7.5  |      |     |      |
|                        |                       |              | 3                     |  | 10.5 | 16   |     |      |
|                        |                       | A = B        | 4                     |  | 12   | 18   |     |      |
| $t_{PHL}$              | Any A or B data input | A < B, A > B | 1                     |  | 5.5  |      |     | ns   |
|                        |                       |              | 2                     |  | 7    |      |     |      |
|                        |                       |              | 3                     |  | 11   | 16.5 |     |      |
|                        |                       | A = B        | 4                     |  | 11   | 16.5 |     |      |
| $t_{PLH}$              | A < B or A = B        | A > B        | 1                     |  | 5    | 7.5  |     | ns   |
| $t_{PHL}$              | A < B or A = B        | A > B        | 1                     |  | 5.5  | 8.5  |     | ns   |
| $t_{PLH}$              | A = B                 | A = B        | 2                     |  | 7    | 10.5 |     | ns   |
| $t_{PHL}$              | A = B                 | A = B        | 2                     |  | 5    | 7.5  |     | ns   |
| $t_{PLH}$              | A > B or A = B        | A < B        | 1                     |  | 5    | 7.5  |     | ns   |
| $t_{PHL}$              | A > B or A = B        | A < B        | 1                     |  | 5.5  | 8.5  |     | ns   |

<sup>¶</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

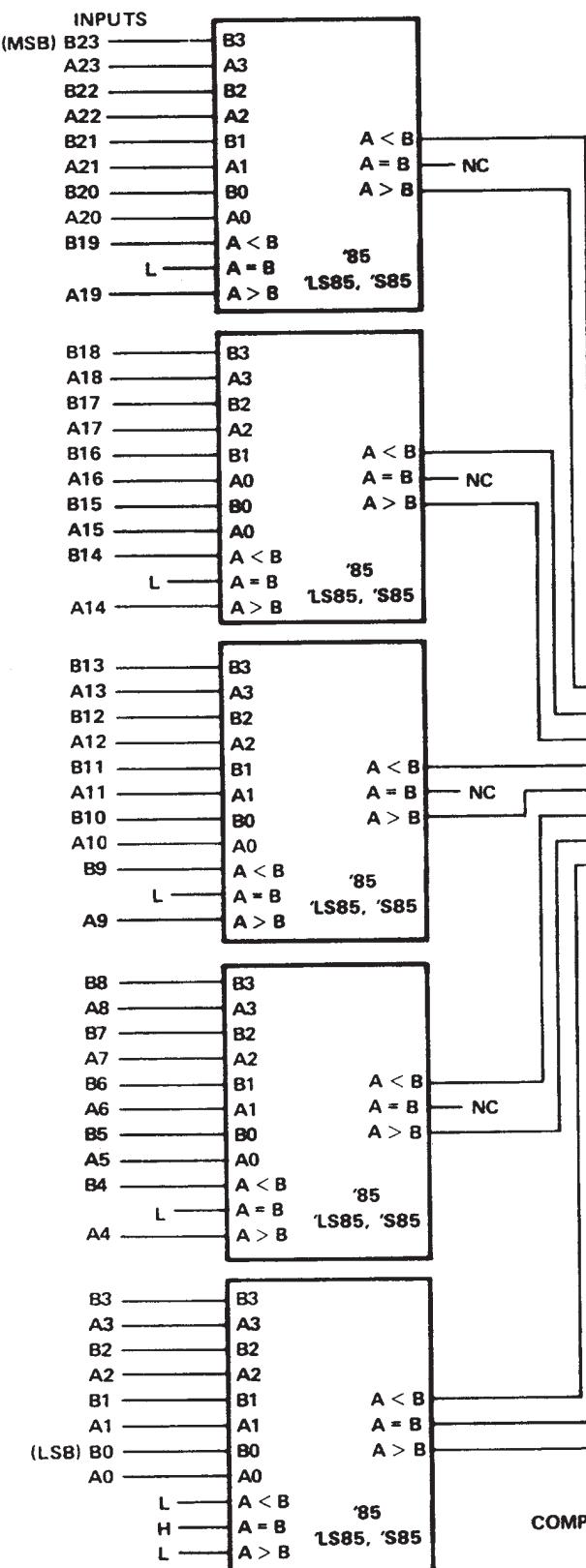
<sup>¶</sup> $t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



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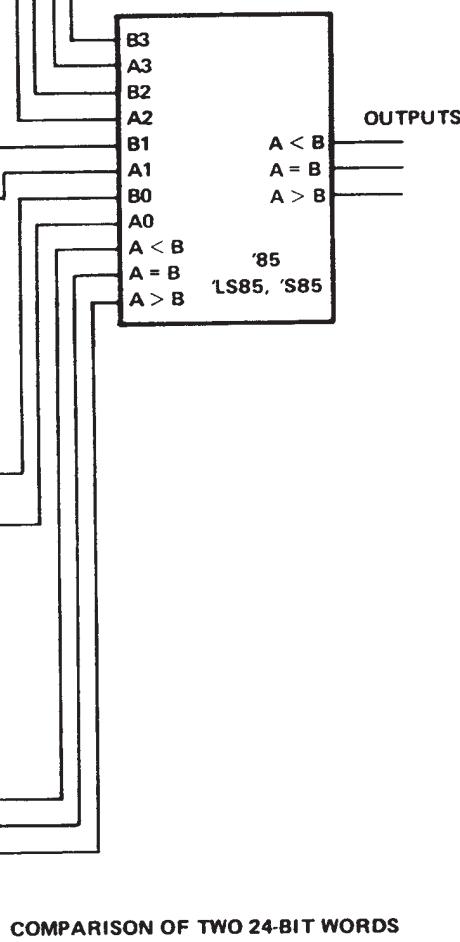
### TYPICAL APPLICATION DATA



### COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

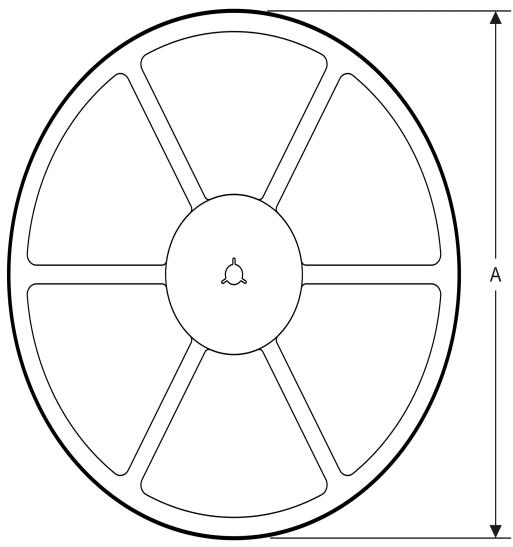
| WORD LENGTH | NUMBER OF PKGS | '85   | 'LS85 | 'S85  |
|-------------|----------------|-------|-------|-------|
| 1-4 bits    | 1              | 23 ns | 24 ns | 11 ns |
| 5-24 bits   | 2-6            | 46 ns | 48 ns | 22 ns |
| 25-120 bits | 8-31           | 69 ns | 72 ns | 33 ns |



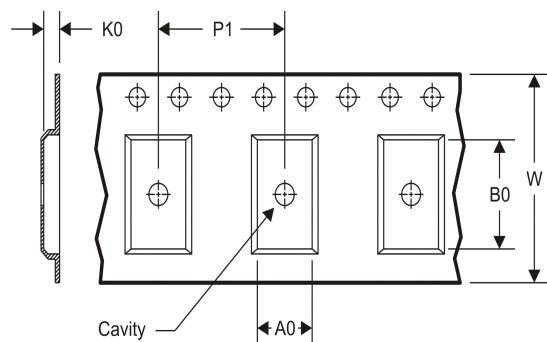
### COMPARISON OF TWO 24-BIT WORDS

## TAPE AND REEL INFORMATION

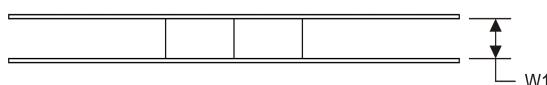
### REEL DIMENSIONS



### TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

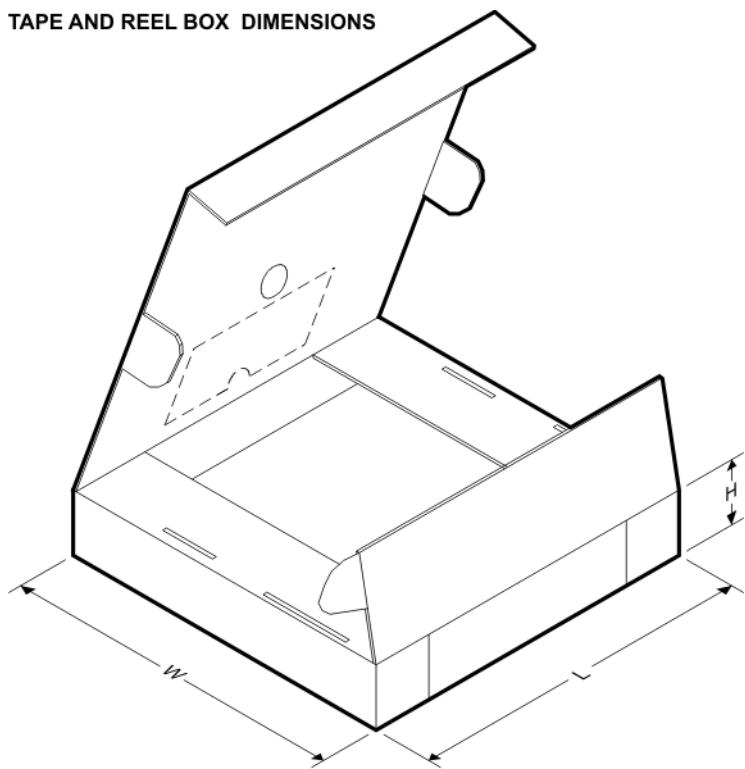


### TAPE AND REEL INFORMATION

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS85DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS85NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS85DR  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74LS85NSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |

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| DLP® Products          | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                    | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers      | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface              | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                  | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt             | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers       | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                   | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Mobile Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity  | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

| TYPE   | TYPICAL AVERAGE        | TYPICAL                 |
|--------|------------------------|-------------------------|
|        | PROPAGATION DELAY TIME | TOTAL POWER DISSIPATION |
| '86    | 14 ns                  | 150 mW                  |
| 'LS86A | 10 ns                  | 30.5 mW                 |
| 'S86   | 7 ns                   | 250 mW                  |

### description

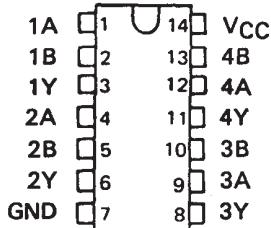
These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions  $Y = A \oplus B = \bar{A}B + A\bar{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

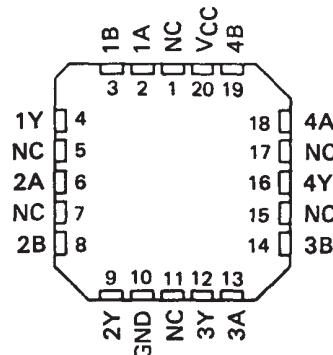
The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE  
 SN7486 . . . N PACKAGE  
 SN74LS86A, SN74S86 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE  
 (TOP VIEW)



NC – No internal connection

### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



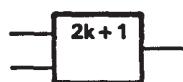
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A=B$ ).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

SN5486, SN54LS86A, SN54S86

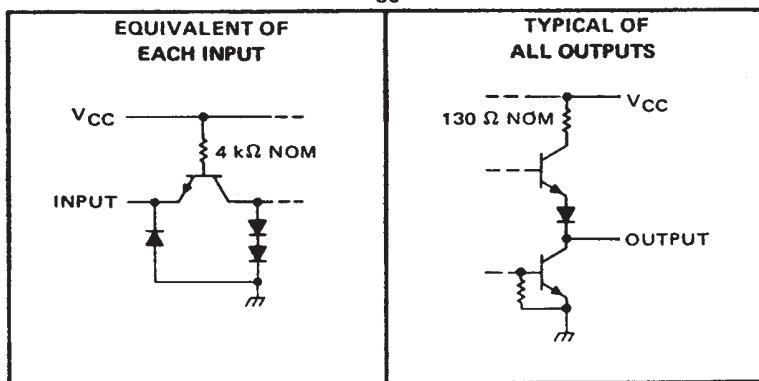
SN7486, SN74LS86A, SN74S86

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

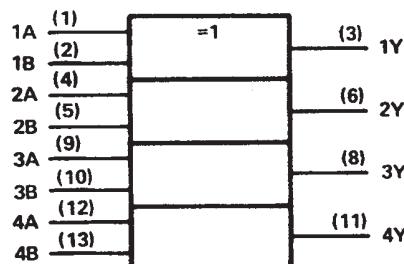
SDLS124 - DECEMBER 1972 - REVISED MARCH 1988

## schematics of inputs and outputs

'86

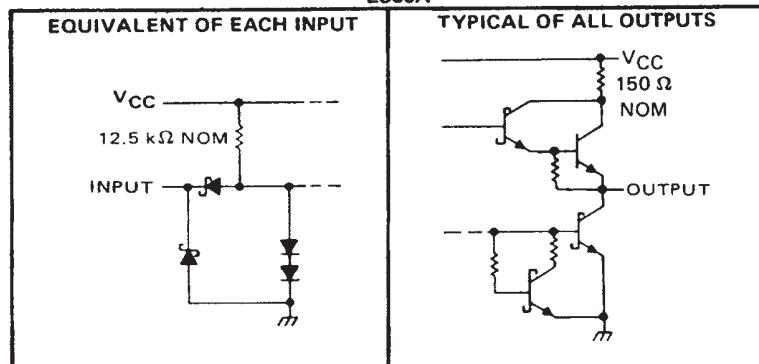


## logic symbol†



†This symbol is in accordance with  
ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, and W packages.

'LS86A

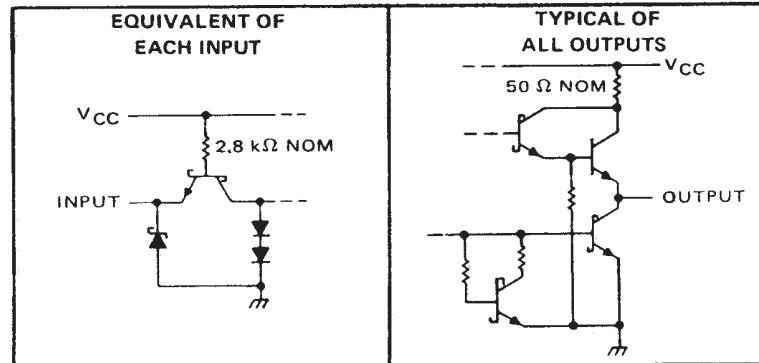


## FUNCTION TABLE

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | H      |
| H      | L | H      |
| H      | H | L      |

H = high level, L = low level

'S86



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|                                       | SN5486 |     |      | SN7486 |     |      | UNIT        |
|---------------------------------------|--------|-----|------|--------|-----|------|-------------|
|                                       | MIN    | NOM | MAX  | MIN    | NOM | MAX  |             |
| Supply voltage, $V_{CC}$              | 4.5    | 5   | 5.5  | 4.75   | 5   | 5.25 | V           |
| High-level output current, $I_{OH}$   |        |     | -800 |        |     | -800 | $\mu A$     |
| Low-level output current, $I_{OL}$    |        |     | 16   |        |     | 16   | mA          |
| Operating free-air temperature, $T_A$ | -55    |     | 125  | 0      |     | 70   | $^{\circ}C$ |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS <sup>†</sup>              | SN5486   |                  |     | SN7486 |                  |      | UNIT    |
|-----------------|---|--|------------------|-----|--------|------------------|------|---------|
|                 |   | MIN  | TYP <sup>‡</sup> | MAX | MIN    | TYP <sup>‡</sup> | MAX  |         |
| V <sub>IH</sub> | High-level input voltage                  |  |                  | 2   |        | 2                |      | V       |
| V <sub>IL</sub> | Low-level input voltage                   |  |                  |     | 0.8    |                  | 0.8  | V       |
| V <sub>IK</sub> | Input clamp voltage                       | V <sub>CC</sub> = MIN, I <sub>I</sub> = -8 mA  |                  |     | -1.5   |                  | -1.5 | V       |
| V <sub>OH</sub> | High-level output voltage                 | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 $\mu$ A | 2.4              | 3.4 |        | 2.4              | 3.4  | V       |
| V <sub>OL</sub> | Low-level output voltage                  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V<br>V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA         |                  | 0.2 | 0.4    |                  | 0.2  | 0.4     |
| I <sub>I</sub>  | Input current at maximum input voltage    | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V  |                  |     | 1      |                  | 1    | mA      |
| I <sub>IH</sub> | High-level input current                  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V  |                  |     | 40     |                  | 40   | $\mu$ A |
| I <sub>IL</sub> | Low-level input current                   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V  |                  |     | -1.6   |                  | -1.6 | mA      |
| I <sub>OS</sub> | Short-circuit output current <sup>§</sup> | V <sub>CC</sub> = MAX  | --20             | -55 | -18    | -55              |      | mA      |
| I <sub>CC</sub> | Supply current                            | V <sub>CC</sub> = MAX, See Note 2  |                  | 30  | 43     |                  | 30   | 50      |

<sup>t</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2:  $I_{OC}$  is measured with the inputs grounded and the outputs open.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER <sup>1</sup> | FROM<br>(INPUT) | TEST CONDITIONS  |  |            | MIN | TYP | MAX | UNIT |
|------------------------|-----------------|------------------|--|------------|-----|-----|-----|------|
| t <sub>PLH</sub>       | A or B          | Other input low  | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 400 Ω, | See Note 3 | 15  | 23  | ns  |      |
| t <sub>PHL</sub>       |                 |                  |  |            | 11  | 17  |     |      |
| t <sub>PLH</sub>       | A or B          | Other input high | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 400 Ω, | See Note 3 | 18  | 30  | ns  |      |
| t <sub>PHL</sub>       |                 |                  |  |            | 13  | 22  |     |      |

$t_{PLH}$  = propagation delay time, low-to-high-level output

**t<sub>PHL</sub>** = propagation delay time, high-to-low-level output

**NOTE 3:** Load circuits and voltage waveforms are shown in Section 1.

## OBSOLETE - No Longer Available

## **SN5486, SN54LS86A, SN54S86**

**SN7486, SN74LS86A, SN74S86**

## **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

SDLS124 – DECEMBER 1972 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|  | SN54LS86A |     |      | SN74LS86A |     |      | UNIT |
|--|-----------|-----|------|-----------|-----|------|------|
|  | MIN       | NOM | MAX  | MIN       | NOM | MAX  |      |
| Supply voltage, V <sub>CC</sub>                | 4.5       | 5   | 5.5  | 4.75      | 5   | 5.25 | V    |
| High-level output current, I <sub>OH</sub>     |           |     | -400 |           |     | -400 | μA   |
| Low-level output current, I <sub>OL</sub>      |           |     | 4    |           |     | 8    | mA   |
| Operating free-air temperature, T <sub>A</sub> | -55       |     | 125  | 0         |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS <sup>†</sup>              | SN54LS86A   |  |     | SN74LS86A |                  |      | UNIT |    |
|-----------------|---|---|--|-----|-----------|------------------|------|------|----|
|                 |   | MIN   | TYP <sup>‡</sup>   | MAX | MIN       | TYP <sup>‡</sup> | MAX  |      |    |
| V <sub>IH</sub> | High-level input voltage                  |   |  | 2   |           | 2                |      | V    |    |
| V <sub>IL</sub> | Low-level input voltage                   |   |  |     | 0.7       |                  | 0.8  | V    |    |
| V <sub>IK</sub> | Input clamp voltage                       | V <sub>CC</sub> = MIN,  | I <sub>I</sub> = -18 mA  |     | -1.5      |                  | -1.5 | V    |    |
| V <sub>OH</sub> | High-level output voltage                 | V <sub>CC</sub> = MIN,  | V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 µA | 2.5 | 3.4       |                  | 2.7  | V    |    |
| V <sub>OL</sub> | Low-level output voltage                  | V <sub>CC</sub> = MIN,  | I <sub>OL</sub> = 4 mA   |     | 0.25      | 0.4              | 0.25 | 0.4  | V  |
|                 |   | V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max | I <sub>OL</sub> = 8 mA   |     |           |                  | 0.35 | 0.5  |    |
| I <sub>I</sub>  | Input current at maximum input voltage    | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 7 V   |     | 0.2       |                  | 0.2  | mA   |    |
| I <sub>IH</sub> | High-level input current                  | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 2.7 V   |     | 40        |                  | 40   | µA   |    |
| I <sub>IL</sub> | Low-level input current                   | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 0.4 V   |     | -0.8      |                  | -0.8 | mA   |    |
| I <sub>OS</sub> | Short-circuit output current <sup>§</sup> | V <sub>CC</sub> = MAX   |  | -20 | -100      | -20              | -100 | mA   |    |
| I <sub>CC</sub> | Supply current                            | V <sub>CC</sub> = MAX,  | See Note 2   |     | 6.1       | 10               | 6.1  | 10   | mA |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

<sup>†</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>†</sup>All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .  
<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2:  $I_{OC}$  is measured with the inputs grounded and the outputs open.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5$  V,  $I_A = 25$  mA

| PARAMETER <sup>1</sup> | FROM<br>(INPUT) | TEST CONDITIONS  |  | MIN | TYP | MAX | UNIT |  |
|------------------------|-----------------|------------------|--|-----|-----|-----|------|--|
| $t_{PLH}$              | A or B          | Other input low  | $C_L = 15 \text{ pF},$<br>$R_L = 2 \text{ k}\Omega,$<br>See Note 3 | 12  | 23  |     | ns   |  |
| $t_{PHL}$              |                 |                  |  | 10  | 17  |     |      |  |
| $t_{PLH}$              |                 | Other input high |  | 20  | 30  |     | ns   |  |
| $t_{PHL}$              |                 |                  |  | 13  | 22  |     |      |  |

$t_{PLH}$  = propagation delay time, low-to-high-level output

**tpHL** = propagation delay time, high-to-low-level output

**NOTE 3:** Load circuits and voltage waveforms are shown in Section 1.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|  | SN54S86 |     |     | SN74S86 |     |      | UNIT |
|--|---------|-----|-----|---------|-----|------|------|
|  | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| Supply voltage, V <sub>CC</sub>                | 4.5     | 5   | 5.5 | 4.75    | 5   | 5.25 | V    |
| High-level output current, I <sub>OH</sub>     |         |     | -1  |         |     | -1   | mA   |
| Low-level output current, I <sub>OL</sub>      |         |     | 20  |         |     | 20   | mA   |
| Operating free-air temperature, T <sub>A</sub> | -55     |     | 125 | 0       |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS <sup>†</sup>              | SN54S86   |                  |      | SN74S86 |                  |      | UNIT |
|-----------------|---|---|------------------|------|---------|------------------|------|------|
|                 |   | MIN   | TYP <sup>‡</sup> | MAX  | MIN     | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IH</sub> | High-level input voltage                  |   |                  | 2    |         | 2                |      | V    |
| V <sub>IL</sub> | Low-level input voltage                   |   |                  |      | 0.8     |                  | 0.8  | V    |
| V <sub>IK</sub> | Input clamp voltage                       | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA  |                  |      | -1.2    |                  | -1.2 | V    |
| V <sub>OH</sub> | High-level output voltage                 | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA | 2.5              | 3.4  |         | 2.7              | 3.4  | V    |
| V <sub>OL</sub> | Low-level output voltage                  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V<br>V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA  |                  |      | 0.5     |                  | 0.5  | V    |
| I <sub>I</sub>  | Input current at maximum input voltage    | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V   |                  | 1    |         | 1                |      | mA   |
| I <sub>IH</sub> | High-level input current                  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V   |                  | 50   |         | 50               |      | μA   |
| I <sub>IL</sub> | Low-level input current                   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V   |                  | -2   |         | -2               |      | mA   |
| I <sub>OS</sub> | Short-circuit output current <sup>§</sup> | V <sub>CC</sub> = MAX   | -40              | -100 | -40     | -100             |      | mA   |
| I <sub>CC</sub> | Supply current                            | V <sub>CC</sub> = MAX, See Note 2   | 50               | 75   | 50      | 75               |      | mA   |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

~~Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.~~

**NOTE 3:**  $I_{OC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

| PARAMETER <sup>1</sup> | FROM<br>(INPUT) | TEST CONDITIONS  |  | MIN | TYP  | MAX | UNIT |
|------------------------|-----------------|------------------|--|-----|------|-----|------|
| t <sub>PLH</sub>       | A or B          | Other input low  | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 280 Ω,<br>See Note 3 | 7   | 10.5 | ns  |      |
| t <sub>PHL</sub>       |                 |                  |  | 6.5 | 10   |     |      |
| t <sub>PLH</sub>       | A or B          | Other input high | See Note 3   | 7   | 10.5 | ns  |      |
| t <sub>PHL</sub>       |                 |                  |  | 6.5 | 10   |     |      |

$t_{\text{tpi}} H$  = propagation delay time, low-to-high-level output

**tPHL** = propagation delay time, high-to-low-level output

**NOTE 3:** Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| JM38510/07501BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/07501BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/07501BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30502B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502B2A | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30502B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/30502BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07501BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07501BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07501BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/07501BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/07501BDA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30502B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30502B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30502B2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/30502B2A        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/30502BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BCA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| M38510/30502BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30502BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/30502BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/30502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS86AJ       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS86AJ              | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS86AJ       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS86AJ              | <span style="background-color: red; color: white;">Samples</span> |
| SN54S86J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S86J                | <span style="background-color: red; color: white;">Samples</span> |
| SN54S86J         | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S86J                | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86AD       | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86AD       | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ADR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ADR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ADRE4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ADRE4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS86A                   | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86AN       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS86AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86AN       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS86AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ANE4     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS86AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ANE4     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS86AN              | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ANSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS86A                 | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS86ANSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS86A                 | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SNJ54LS86AFK     | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AFK            | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS86AFK     | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Non-Green | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AFK            | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS86AJ      | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AJ             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS86AJ      | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AJ             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS86AW      | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AW             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS86AW      | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS86AW             | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S86J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S86J               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54S86J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S86J               | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS86A, SN74LS86A :**

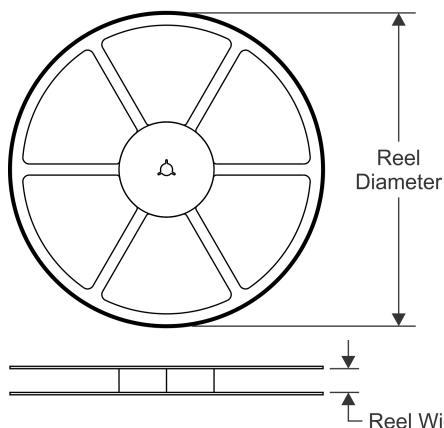
- Catalog: [SN74LS86A](#)
- Military: [SN54LS86A](#)

NOTE: Qualified Version Definitions:

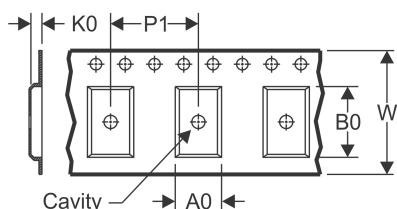
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

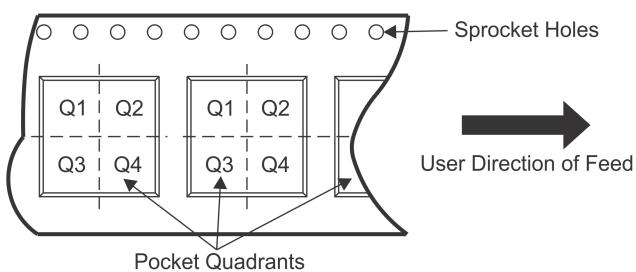


### TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

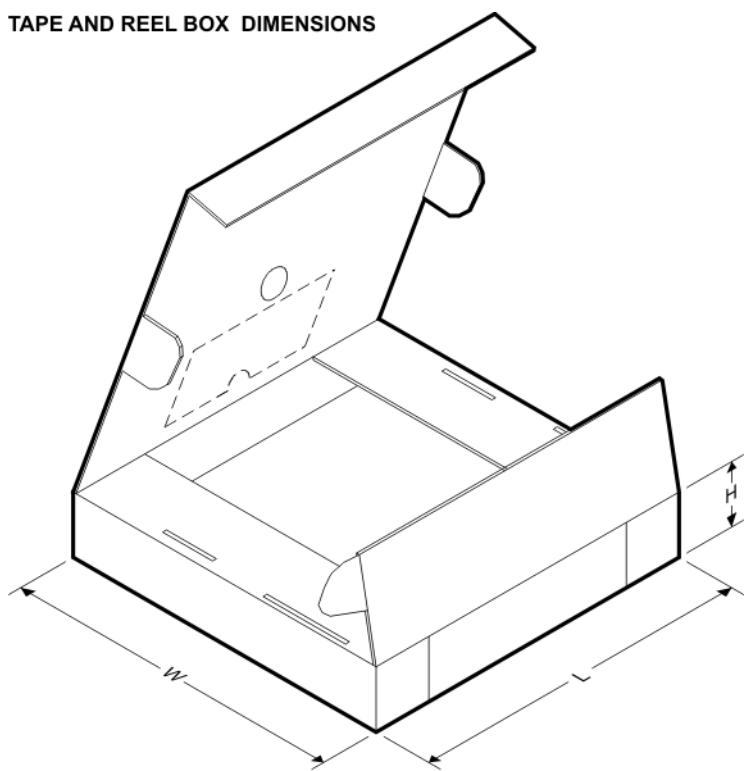
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS86ADR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



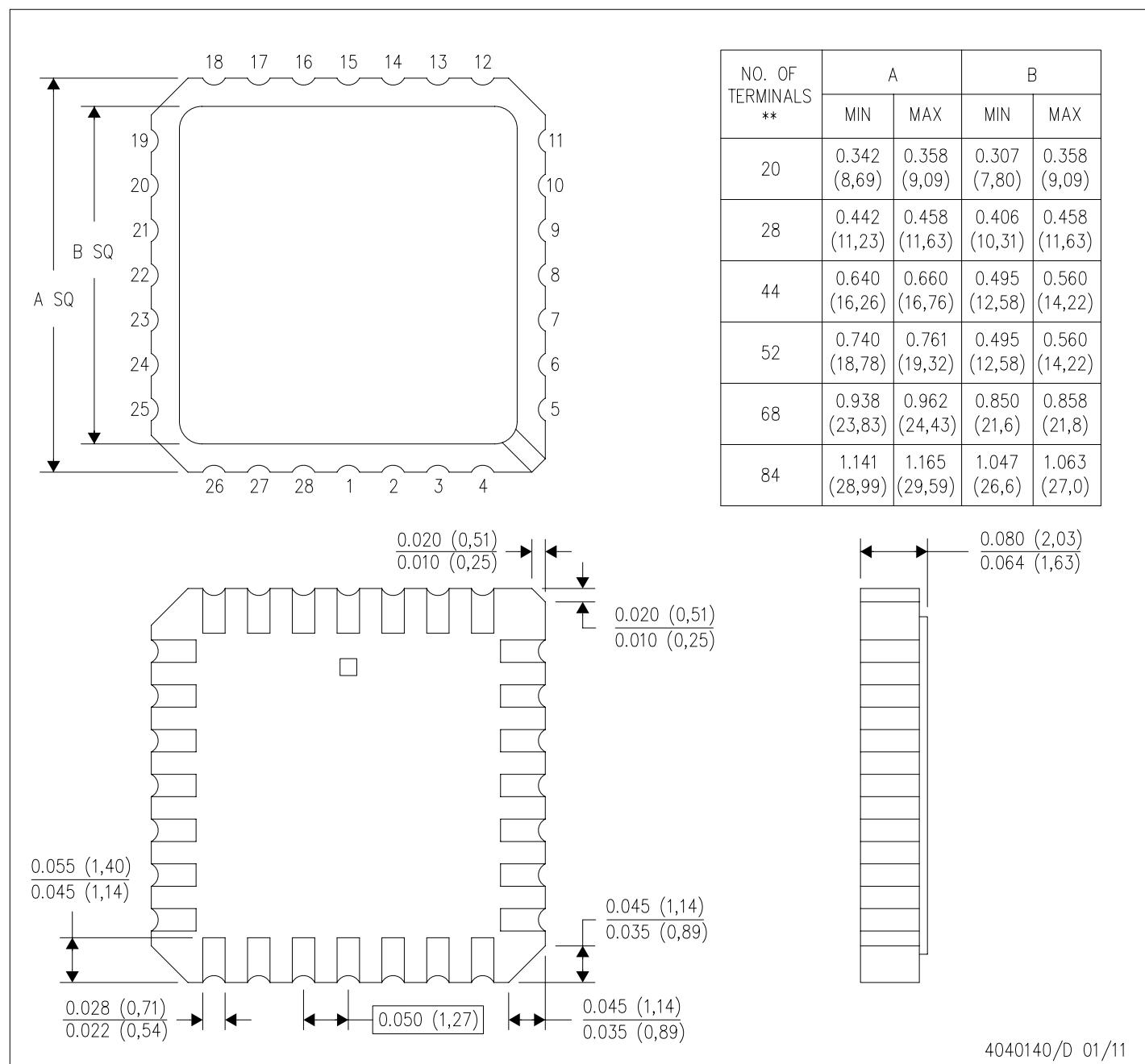
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS86ADR | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

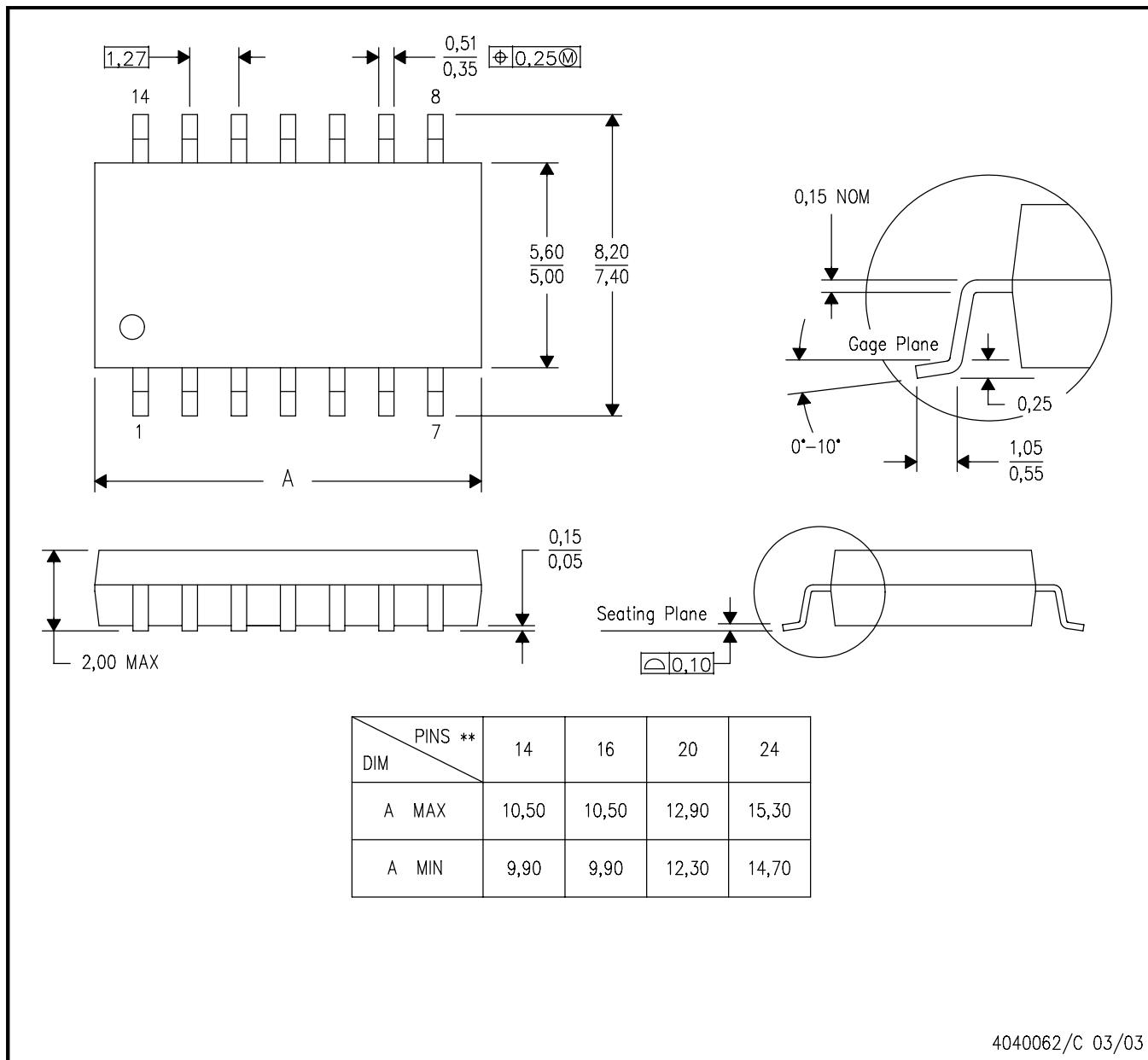
4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

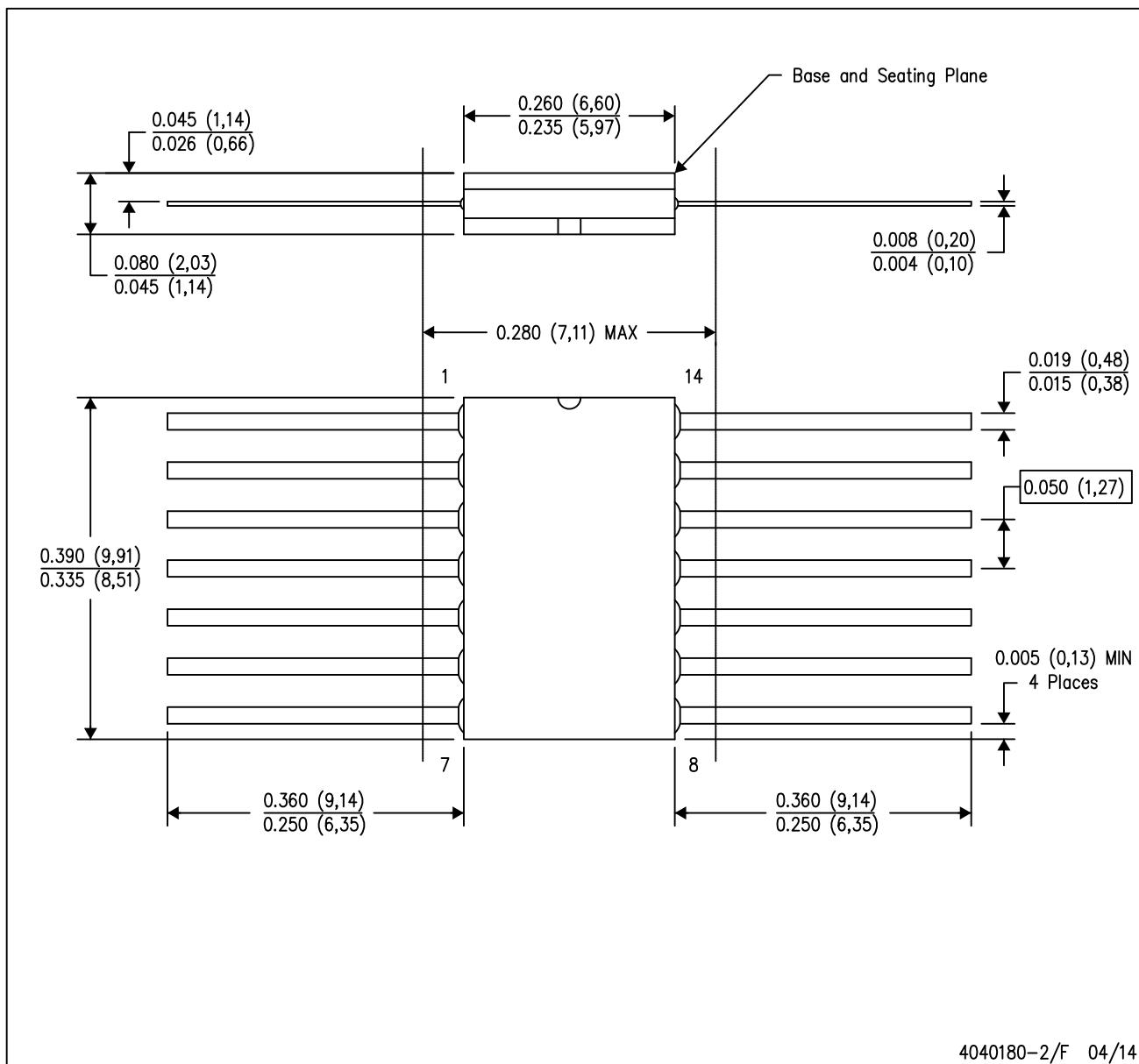


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

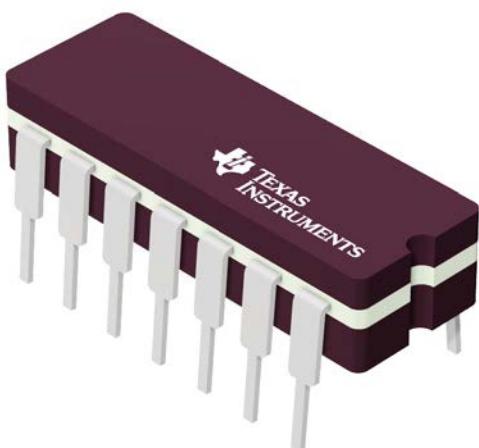
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

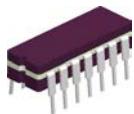
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

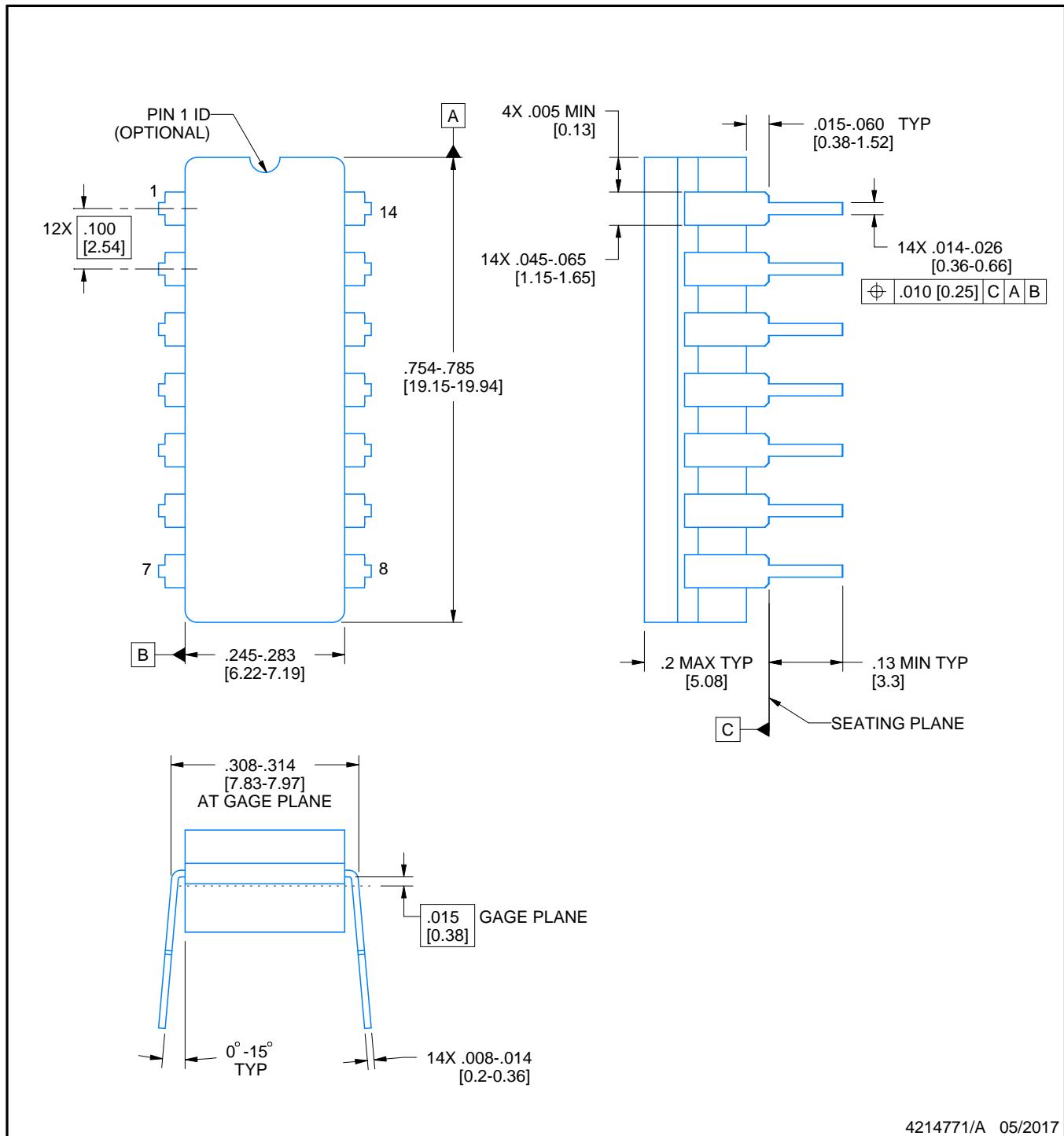
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

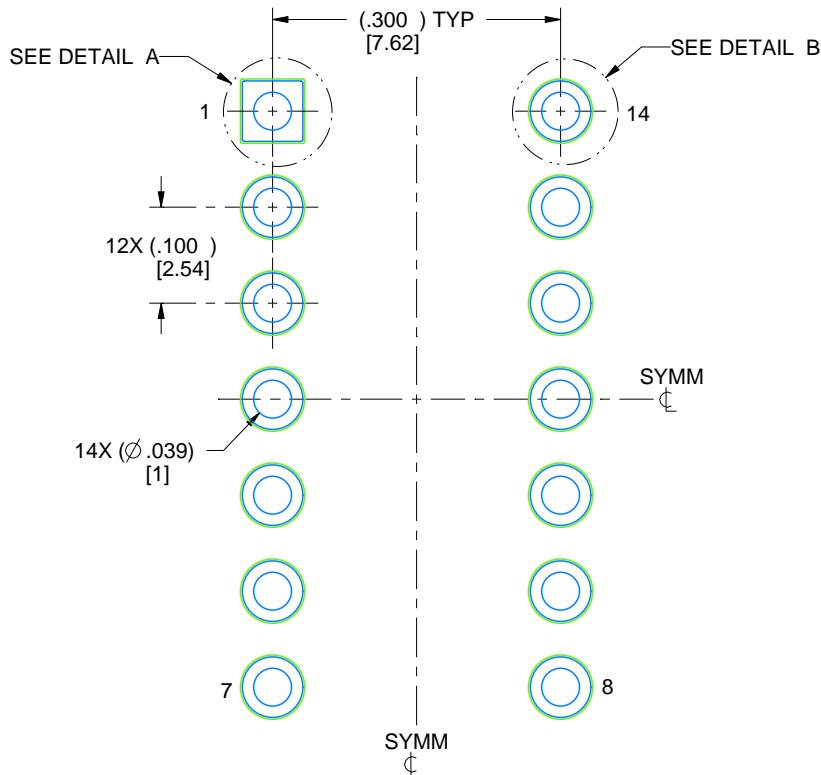
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

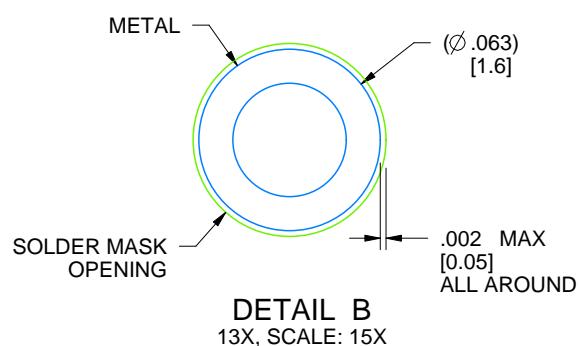
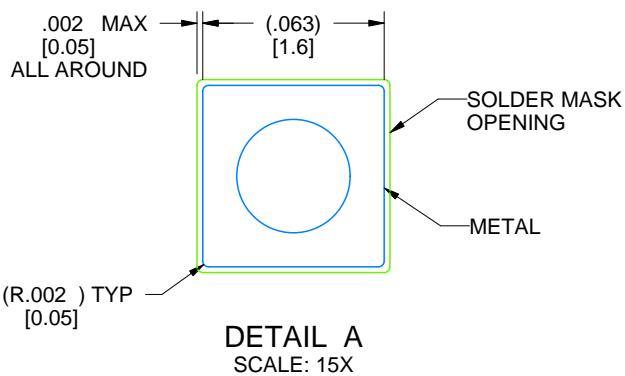
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



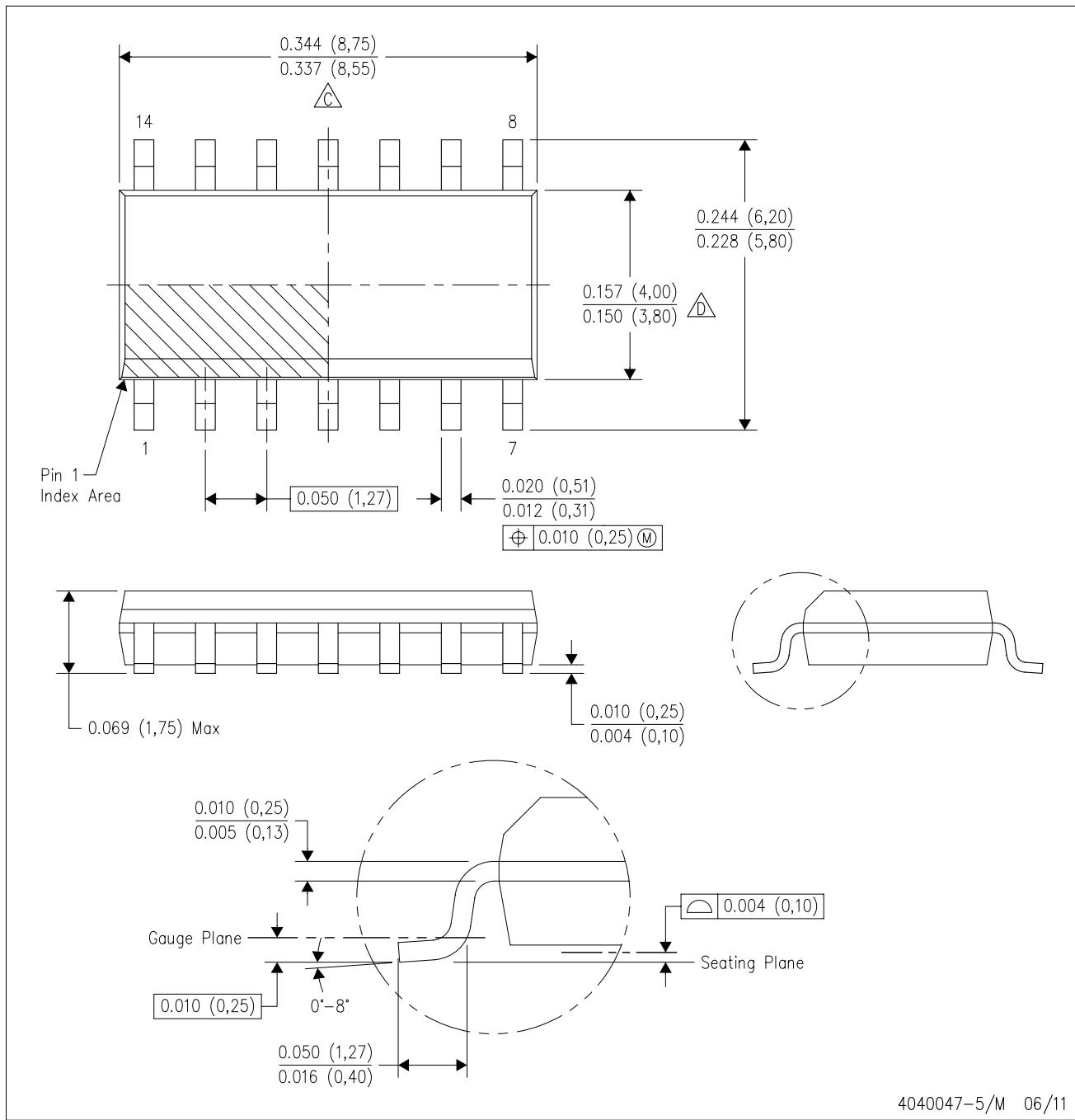
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

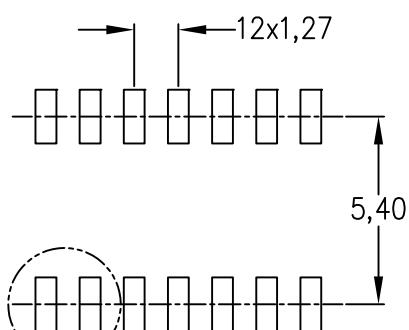
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

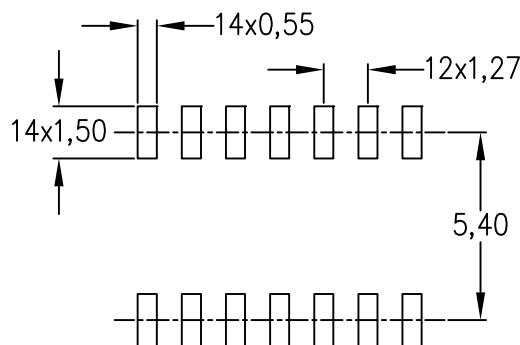
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

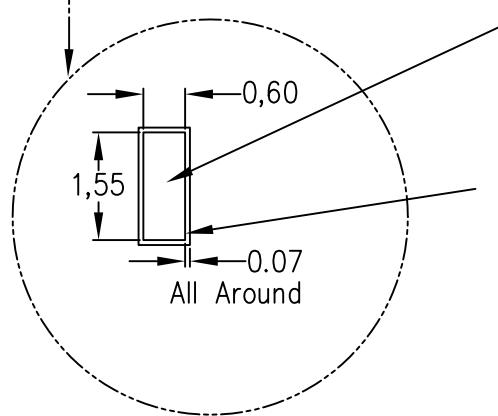
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

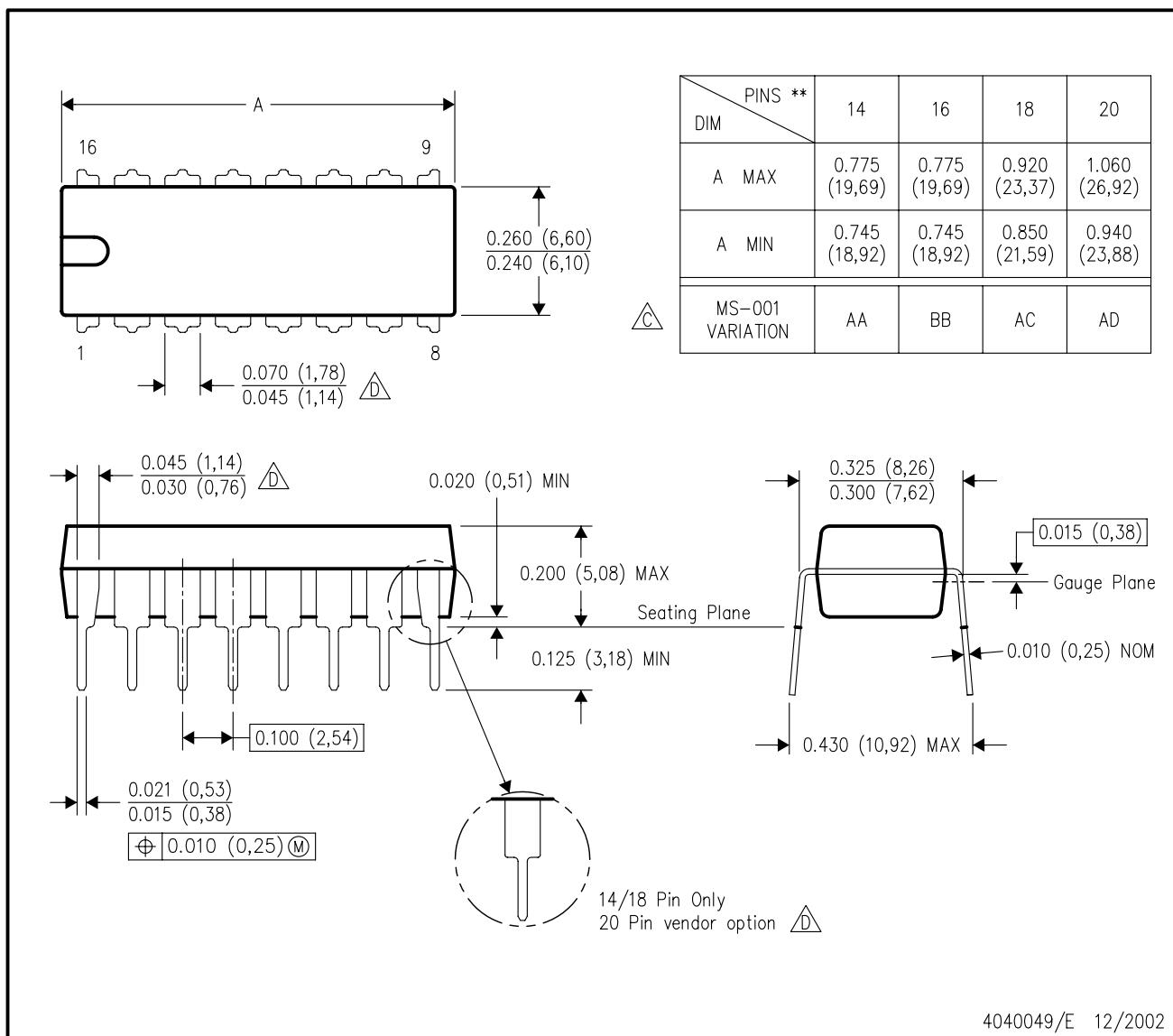
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

- '90A, 'LS90 . . . Decade Counters
- '92A, 'LS92 . . . Divide By-Twelve Counters
- '93A, 'LS93 . . . 4-Bit Binary Counters

| TYPES               | TYPICAL<br>POWER DISSIPATION |
|---------------------|------------------------------|
| '90A                | 145 mW                       |
| '92A, '93A          | 130 mW                       |
| 'LS90, 'LS92, 'LS93 | 45 mW                        |

#### description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

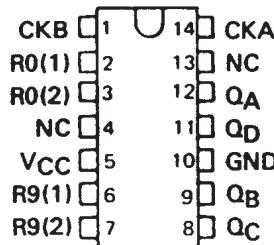
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the QA output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output QA.

**SN5490A, SN54LS90 . . . J OR W PACKAGE**

**SN7490A . . . N PACKAGE**

**SN74LS90 . . . D OR N PACKAGE**

(TOP VIEW)

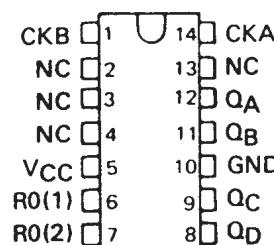


**SN5492A, SN54LS92 . . . J OR W PACKAGE**

**SN7492A . . . N PACKAGE**

**SN74LS92 . . . D OR N PACKAGE**

(TOP VIEW)

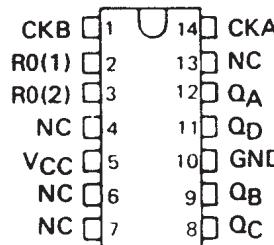


**SN5493A, SN54LS93 . . . J OR W PACKAGE**

**SN7493 . . . N PACKAGE**

**SN74LS93 . . . D OR N PACKAGE**

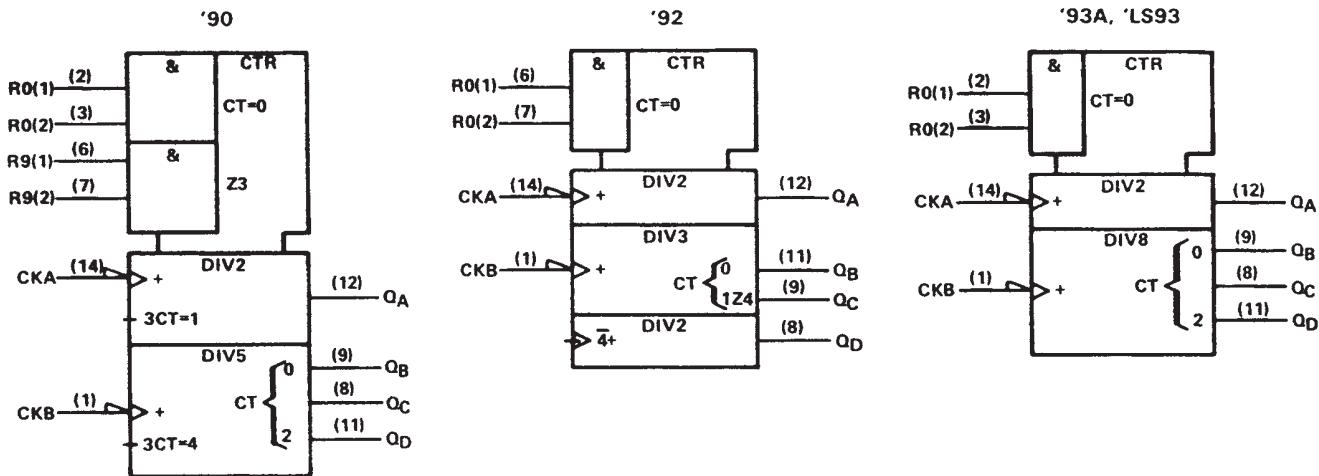
(TOP VIEW)



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic symbols<sup>†</sup>**



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90  
BCD COUNT SEQUENCE  
(See Note A)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | L              | H              | H              | L              |
| 7     | L              | H              | H              | H              |
| 8     | H              | L              | L              | L              |
| 9     | H              | L              | L              | H              |

'90A, 'LS90  
BI-QUINARY (5-2)  
(See Note B)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>A</sub> | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | H              | L              | L              | L              |
| 6     | H              | L              | L              | H              |
| 7     | H              | L              | H              | L              |
| 8     | H              | L              | H              | H              |
| 9     | H              | H              | L              | L              |

'92A, 'LS92  
COUNT SEQUENCE  
(See Note C)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | H              | L              | L              | L              |
| 7     | H              | L              | L              | H              |
| 8     | H              | L              | H              | L              |
| 9     | H              | L              | H              | H              |
| 10    | H              | H              | L              | L              |
| 11    | H              | H              | L              | H              |

'90A, 'LS90  
RESET/COUNT FUNCTION TABLE

| RESET INPUTS      |                   |                   |                   | OUTPUT  |
|-------------------|-------------------|-------------------|-------------------|---|
| R <sub>0(1)</sub> | R <sub>0(2)</sub> | R <sub>9(1)</sub> | R <sub>9(2)</sub> | Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub> |
| H                 | H                 | L                 | X                 | L L L L   |
| H                 | H                 | X                 | L                 | L L L L   |
| X                 | X                 | H                 | H                 | H L L H   |
| X                 | L                 | X                 | L                 | COUNT   |
| L                 | X                 | L                 | X                 | COUNT   |
| L                 | X                 | X                 | L                 | COUNT   |
| X                 | L                 | L                 | X                 | COUNT   |

'92A, 'LS92, '93A, 'LS93  
RESET/COUNT FUNCTION TABLE

| RESET INPUTS      |                   | OUTPUT  |
|-------------------|-------------------|---|
| R <sub>0(1)</sub> | R <sub>0(2)</sub> | Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub> |
| H                 | H                 | L L L L   |
| L                 | X                 | COUNT   |
| X                 | L                 | COUNT   |

- NOTES: A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
B. Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.  
C. Output Q<sub>A</sub> is connected to input CKB.  
D. H = high level, L = low level, X = irrelevant

'93A, 'LS93  
COUNT SEQUENCE  
(See Note C)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | L              | H              | H              | L              |
| 7     | L              | H              | H              | H              |
| 8     | H              | L              | L              | L              |
| 9     | H              | L              | L              | H              |
| 10    | H              | L              | H              | L              |
| 11    | H              | L              | H              | H              |
| 12    | H              | H              | L              | L              |
| 13    | H              | H              | L              | H              |
| 14    | H              | H              | H              | L              |
| 15    | H              | H              | H              | H              |

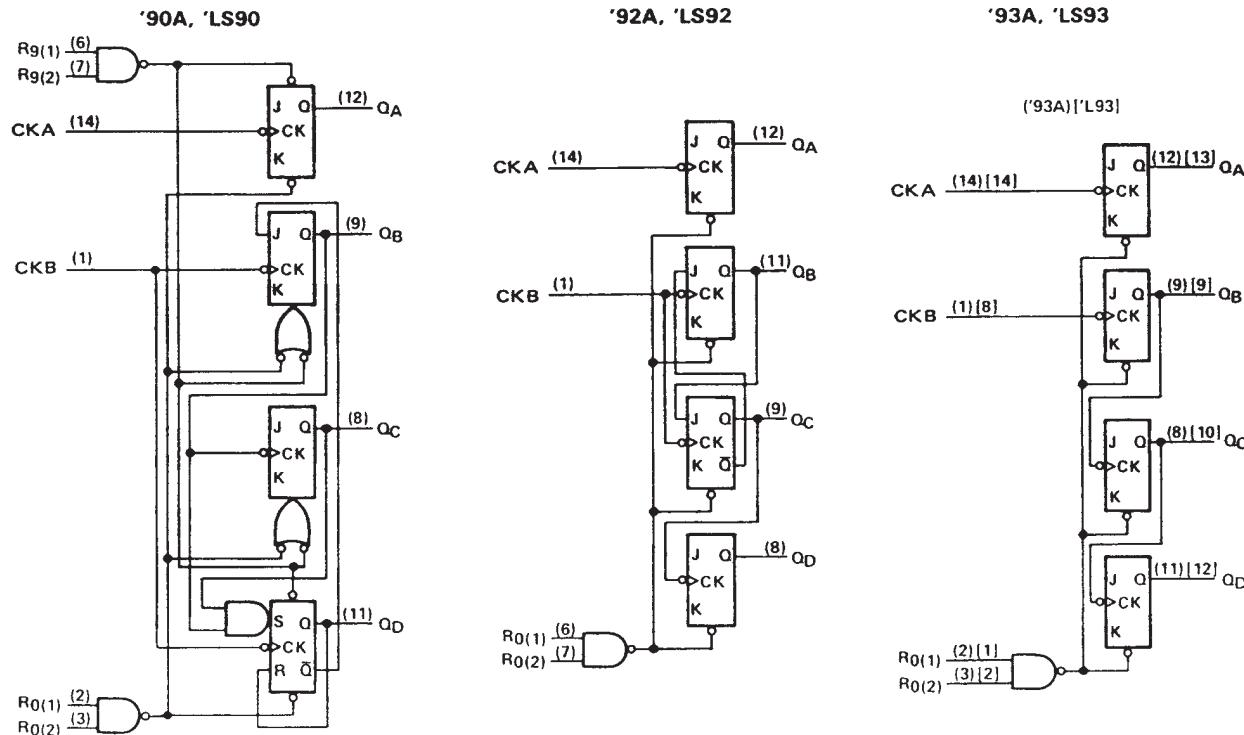


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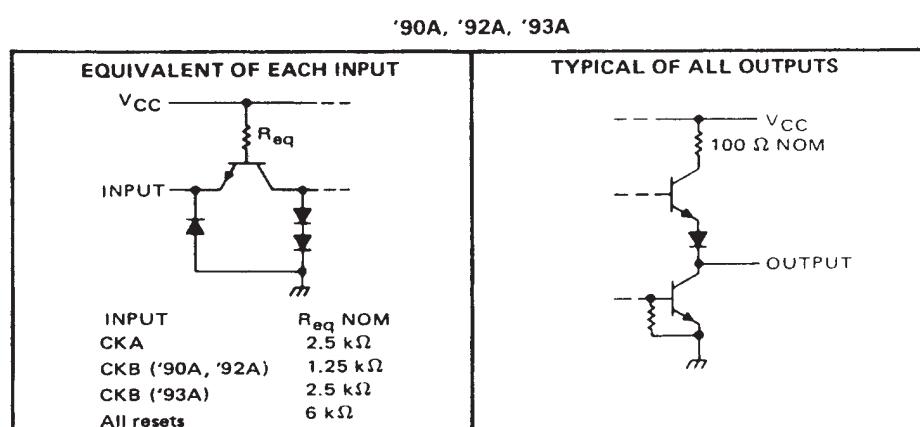
**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic diagrams (positive logic)**



**schematics of inputs and outputs**

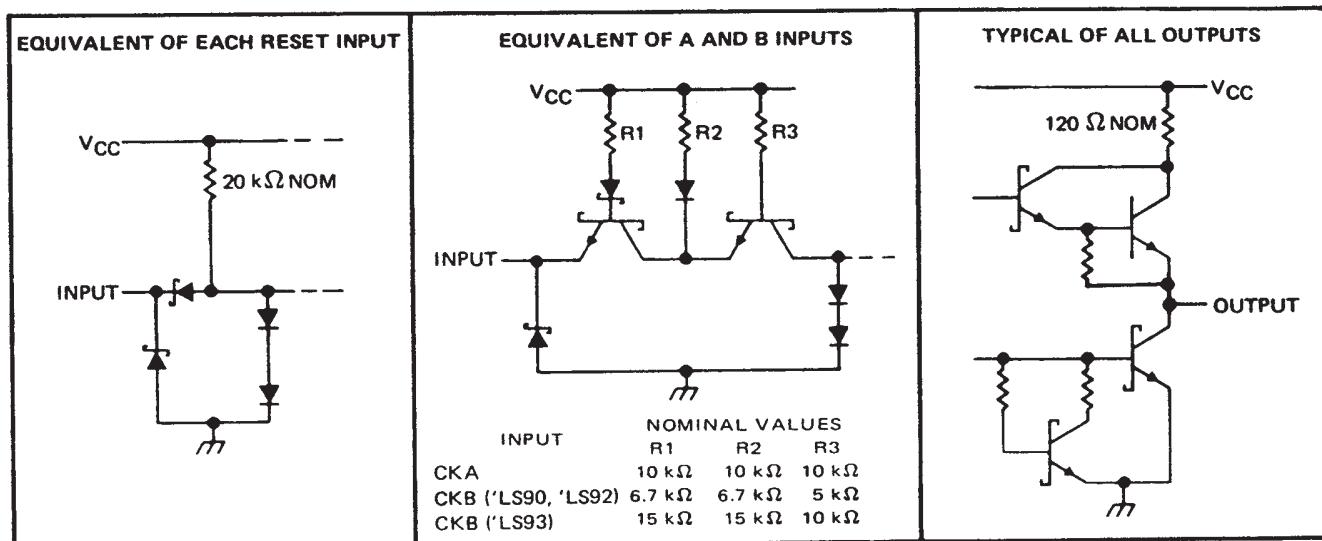


**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**schematics of inputs and outputs (continued)**

'LS90, 'LS92, 'LS93



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

NOTES: 1. Voltage values, except interemitter voltage, etc., with respect to ground.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two  $R_0$  inputs, and for the '90A circuit, it also applies between the two  $R_g$  inputs.

#### **recommended operating conditions**

|   | SN5490A, SN5492A<br>SN5493A | SN7490A, SN7492A<br>SN7493A |      |      | UNIT         |
|---|-----------------------------|-----------------------------|------|------|--------------|
|   |                             | MIN                         | NOM  | MAX  |              |
|   |                             | MIN                         | NOM  | MAX  |              |
| Supply voltage, $V_{CC}$                    | 4.5                         | 5                           | 5.5  | 4.75 | 5 5.25 V     |
| High-level output current, $I_{OH}$         |                             |                             | -800 |      | -800 $\mu A$ |
| Low-level output current, $I_{OL}$          |                             |                             | 16   |      | 16 mA        |
| Count frequency, $f_{count}$ (see Figure 1) | A input                     | 0                           | 32   | 0    | 32 MHz       |
|   | B input                     | 0                           | 16   | 0    | 16           |
| Pulse width, $t_W$                          | A input                     | 15                          |      | 15   | ns           |
|   | B input                     | 30                          |      | 30   |              |
|   | Reset inputs                | 15                          |      | 15   |              |
| Reset inactive-state setup time, $t_{SU}$   |                             | 25                          |      | 25   | ns           |
| Operating free-air temperature, $T_A$       | -55                         | 125                         | 0    | 70   | $^{\circ}C$  |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>1</sup>                                       | TEST CONDITIONS <sup>†</sup>   | '90A  |                  |     | '92A |                  |     | '93A |                  |     | UNIT |    |
|--|--|---|------------------|-----|------|------------------|-----|------|------------------|-----|------|----|
|  |  | MIN   | TYP <sup>‡</sup> | MAX | MIN  | TYP <sup>‡</sup> | MAX | MIN  | TYP <sup>‡</sup> | MAX |      |    |
| V <sub>IH</sub> High-level input voltage                     |  | 2   |                  |     | 2    |                  |     | 2    |                  |     | V    |    |
| V <sub>IL</sub> Low-level input voltage                      |  | 0.8   |                  |     | 0.8  |                  |     | 0.8  |                  |     | V    |    |
| V <sub>IK</sub> Input clamp voltage                          | V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA   | -1.5  |                  |     | -1.5 |                  |     | -1.5 |                  |     | V    |    |
| V <sub>OH</sub> High-level output voltage                    | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 µA            | 2.4   | 3.4              |     | 2.4  | 3.4              |     | 2.4  | 3.4              |     | V    |    |
| V <sub>OL</sub> Low-level output voltage                     | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA <sup>§</sup> | 0.2   | 0.4              |     | 0.2  | 0.4              |     | 0.2  | 0.4              |     | V    |    |
| I <sub>I</sub> Input current at<br>maximum input voltage     | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V  | 1   |                  |     | 1    |                  |     | 1    |                  |     | mA   |    |
| I <sub>IH</sub> High-level<br>input current                  | Any reset  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V |                  |     | 40   |                  |     | 40   |                  |     | 40   |    |
|  | CKA  |   |                  |     | 80   |                  |     | 80   |                  |     | 80   |    |
|  | CKB  |   |                  |     | 120  |                  |     | 120  |                  |     | 80   |    |
| I <sub>IIL</sub> Low-level<br>input current                  | Any reset  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |                  |     | -1.6 |                  |     | -1.6 |                  |     | -1.6 |    |
|  | CKA  |   |                  |     | -3.2 |                  |     | -3.2 |                  |     | -3.2 |    |
|  | CKB  |   |                  |     | -4.8 |                  |     | -4.8 |                  |     | -3.2 |    |
| I <sub>OS</sub> Short-circuit<br>output current <sup>§</sup> | V <sub>CC</sub> = MAX  |   | SN54'            | -20 | -57  | -20              | -57 | -20  | -57              | -20 | mA   |    |
|  |  |   | SN74'            | -18 | -57  | -18              | -57 | -18  | -57              | -18 | mA   |    |
| I <sub>CC</sub> Supply current                               | V <sub>CC</sub> = MAX, See Note 3  |   |                  | 29  | 42   |                  | 26  | 39   |                  | 26  | 39   | mA |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>†</sup>All typical values are at V<sub>CC</sub> = 5 V, TA = 25°C.  
<sup>§</sup>Not more than one output should be shorted at a time.

**Q<sub>A</sub>** outputs are tested at  $I_{OL} = 16 \text{ mA}$  plus the limit value for  $I_{IL}$  for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3:  $I_{CC}$  is measured with all outputs open, both  $R_O$  inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER <sup>†</sup> | FROM<br>(INPUT)  | TO<br>(OUTPUT) | TEST CONDITIONS   | '90A |     |     | '92A |     |     | '93A |     |     | UNIT |
|------------------------|------------------|----------------|---|------|-----|-----|------|-----|-----|------|-----|-----|------|
|                        |                  |                |   | MIN  | TYP | MAX | MIN  | TYP | MAX | MIN  | TYP | MAX |      |
| $f_{max}$              | CKA              | Q <sub>A</sub> | $C_L = 15 \text{ pF}$ ,<br>$R_L = 400 \Omega$ ,<br>See Figure 1 | 32   | 42  |     | 32   | 42  |     | 32   | 42  |     | MHz  |
|                        | CKB              | Q <sub>B</sub> |   | 16   |     |     | 16   |     |     | 16   |     |     |      |
|                        | t <sub>PLH</sub> | CKA            |   | 10   | 16  |     | 10   | 16  |     | 10   | 16  |     | ns   |
|                        | t <sub>PHL</sub> | CKA            |   | 12   | 18  |     | 12   | 18  |     | 12   | 18  |     |      |
|                        | t <sub>PLH</sub> | CKA            |   | 32   | 48  |     | 32   | 48  |     | 46   | 70  |     | ns   |
|                        | t <sub>PHL</sub> | CKA            |   | 34   | 50  |     | 34   | 50  |     | 46   | 70  |     |      |
|                        | t <sub>PLH</sub> | CKB            |   | 10   | 16  |     | 10   | 16  |     | 10   | 16  |     | ns   |
|                        | t <sub>PHL</sub> | CKB            |   | 14   | 21  |     | 14   | 21  |     | 14   | 21  |     |      |
|                        | t <sub>PLH</sub> | CKB            |   | 21   | 32  |     | 10   | 16  |     | 21   | 32  |     | ns   |
|                        | t <sub>PHL</sub> | CKB            |   | 23   | 35  |     | 14   | 21  |     | 23   | 35  |     |      |
| $t_{PLH}$              | CKB              | Q <sub>D</sub> |   | 21   | 32  |     | 21   | 32  |     | 34   | 51  |     | ns   |
|                        | t <sub>PHL</sub> | CKB            |   | 23   | 35  |     | 23   | 35  |     | 34   | 51  |     |      |
|                        | t <sub>PLH</sub> | Set-to-0       | Any   | 26   | 40  |     | 26   | 40  |     | 26   | 40  |     | ns   |
|                        | t <sub>PHL</sub> | Set-to-9       | Q <sub>A</sub> , Q <sub>D</sub>                                 | 20   | 30  |     |      |     |     |      |     |     | ns   |
| t <sub>PHL</sub>       |                  |                | Q <sub>B</sub> , Q <sub>C</sub>                                 | 26   | 40  |     |      |     |     |      |     |     | ns   |

<sup>†</sup> $f_{max}$  = maximum count frequency

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub> (see Note 1)           | 7 V            |
| Input voltage: R inputs                                | 7 V            |
| A and B inputs   | 5.5 V          |
| Operating free-air temperature range: SN54LS' Circuits | -55°C to 125°C |
| SN74LS' Circuits                                       | 0°C to 70°C    |
| Storage temperature range                              | -65°C to 150°C |

**NOTE 1:** Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|   | SN54LS90     |     |     | SN74LS90 |     |      | UNIT        |  |
|---|--------------|-----|-----|----------|-----|------|-------------|--|
|   | SN54LS92     |     |     | SN74LS92 |     |      |             |  |
|   | SN54LS93     |     |     | SN74LS93 |     |      |             |  |
|   | MIN          | NOM | MAX | MIN      | NOM | MAX  |             |  |
| Supply voltage, $V_{CC}$                    | 4.5          | 5   | 5.5 | 4.75     | 5   | 5.25 | V           |  |
| High-level output current, $I_{OH}$         |              |     |     | -400     |     |      | $\mu A$     |  |
| Low-level output current, $I_{OL}$          |              |     |     | 4        |     |      | mA          |  |
| Count frequency, $f_{count}$ (see Figure 1) | A input      | 0   | 32  | 0        | 32  |      | MHz         |  |
|   | B input      | 0   | 16  | 0        | 16  |      |             |  |
| Pulse width, $t_W$                          | A input      | 15  |     | 15       |     |      | ns          |  |
|   | B input      | 30  |     | 30       |     |      |             |  |
|   | Reset inputs | 30  |     | 30       |     |      |             |  |
| Reset inactive-state setup time, $t_{SU}$   | 25           |     |     | 25       |     |      | ns          |  |
| Operating free-air temperature, $T_A$       | -55          | 125 | 0   | 70       |     |      | $^{\circ}C$ |  |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS†  | SN54LS90                                      |       |                         | SN74LS90 |          |      | UNIT |  |
|---|---|---|-------|-------------------------|----------|----------|------|------|--|
|   |   | SN54LS92                                      |       |                         | SN74LS92 |          |      |      |  |
|   |   | MIN   | TYP‡  | MAX                     | MIN      | TYP‡     | MAX  |      |  |
| V <sub>IH</sub> High-level input voltage                    |   |   |       | 2                       | 2        |          |      | V    |  |
| V <sub>IL</sub> Low-level input voltage                     |   |   |       | 0.7                     | 0.8      |          |      | V    |  |
| V <sub>IK</sub> Input clamp voltage                         | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA  |   |       | -1.5                    | -1.5     |          |      | V    |  |
| V <sub>OH</sub> High-level output voltage                   | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 µA |   |       | 2.5 3.4                 | 2.7 3.4  |          |      | V    |  |
| V <sub>OL</sub> Low-level output voltage                    | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max,                           |   |       | I <sub>OL</sub> = 4 mA¶ | 0.25 0.4 | 0.25 0.4 |      | V    |  |
|   |   |   |       | I <sub>OL</sub> = 8 mA¶ | 0.35 0.5 |          |      | V    |  |
| I <sub>I</sub> Input current<br>at maximum<br>input voltage | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V   |       |                         | 0.1      | 0.1      |      |      |  |
|   | CKA   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V |       |                         | 0.2      | 0.2      |      |      |  |
|   | CKB   |   |       |                         | 0.4      | 0.4      |      |      |  |
| I <sub>IIH</sub> High-level<br>input current                | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |       |                         | 20       | 20       |      |      |  |
|   | CKA   |   |       |                         | 40       | 40       |      |      |  |
|   | CKB   |   |       |                         | 80       | 80       |      |      |  |
| I <sub>IIL</sub> Low-level<br>input current                 | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |       |                         | -0.4     | -0.4     |      |      |  |
|   | CKA   |   |       |                         | -2.4     | -2.4     |      |      |  |
|   | CKB   |   |       |                         | -3.2     | -3.2     |      |      |  |
| I <sub>OS</sub> Short-circuit output current§               | V <sub>CC</sub> = MAX   |   |       | -20                     | -100     | -20      | -100 | mA   |  |
| I <sub>ICC</sub> Supply current                             | V <sub>CC</sub> = MAX, See Note 3   |   | 'LS90 | 9 15                    | 9 15     |          |      | mA   |  |
|   |   |   | 'LS92 | 9 15                    | 9 15     |          |      |      |  |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>#</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

**8** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**Q<sub>A</sub>** outputs are tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3:  $I_{CC}$  is measured with all outputs open, both  $R_O$  inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS <sup>†</sup>  | SN54LS93                                      |                  |      | SN74LS93 |                  |      | UNIT |
|---|---|---|------------------|------|----------|------------------|------|------|
|   |   | MIN   | TYP <sup>‡</sup> | MAX  | MIN      | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IH</sub> High-level input voltage                    |   | 2   |                  |      | 2        |                  |      | V    |
| V <sub>IL</sub> Low-level input voltage                     |   |   |                  | 0.7  |          |                  | 0.8  | V    |
| V <sub>IK</sub> Input clamp voltage                         | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA  |   |                  | -1.5 |          |                  | -1.5 | V    |
| V <sub>OH</sub> High-level output voltage                   | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA | 2.5   | 3.4              |      | 2.7      | 3.4              |      | V    |
| V <sub>OL</sub> Low-level output voltage                    | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max                            | I <sub>OL</sub> = 4 mA <sup>§</sup>           | 0.25             | 0.4  | 0.25     | 0.4              |      | V    |
|   |   | I <sub>OL</sub> = 8 mA <sup>§</sup>           |                  |      | 0.35     | 0.5              |      |      |
| I <sub>I</sub> Input current<br>at maximum<br>input voltage | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V   |                  |      | 0.1      |                  | 0.1  | mA   |
|   | CKA or CKB  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V |                  |      | 0.2      |                  | 0.2  |      |
| I <sub>IH</sub> High-level<br>input current                 | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |                  |      | 20       |                  | 20   | μA   |
|   | CKA or CKB  |   |                  |      | 40       |                  | 80   |      |
| I <sub>IIL</sub> Low-level<br>input current                 | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |                  |      | -0.4     |                  | -0.4 | mA   |
|   | CKA   |   |                  |      | -2.4     |                  | -2.4 |      |
|   | CKB   |   |                  |      | -1.6     |                  | -1.6 |      |
| I <sub>OS</sub> Short-circuit output current <sup>§</sup>   | V <sub>CC</sub> = MAX   |   | -20              | -100 | -20      | -100             |      | mA   |
| I <sub>CC</sub> Supply current                              | V <sub>CC</sub> = MAX, See Note 3   |   | 9                | 15   | 9        | 15               |      | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup>Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value for I<sub>IIL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>O</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER <sup>#</sup> | FROM<br>(INPUT) | TO<br>(OUTPUT)                  | TEST CONDITIONS  | 'LS90 |     |     | 'LS92 |     |     | 'LS93 |     |     | UNIT |  |
|------------------------|-----------------|---------------------------------|--|-------|-----|-----|-------|-----|-----|-------|-----|-----|------|--|
|                        |                 |                                 |  | MIN   | TYP | MAX | MIN   | TYP | MAX | MIN   | TYP | MAX |      |  |
| f <sub>max</sub>       | CKA             | Q <sub>A</sub>                  | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 2 kΩ<br>See Figure 1 | 32    | 42  |     | 32    | 42  |     | 32    | 42  |     | MHz  |  |
|                        | CKB             | Q <sub>B</sub>                  |  | 16    |     |     | 16    |     |     | 16    |     |     |      |  |
|                        | CKA             | Q <sub>A</sub>                  |  | 10    | 16  |     | 10    | 16  |     | 10    | 16  |     | ns   |  |
|                        |                 |                                 |  | 12    | 18  |     | 12    | 18  |     | 12    | 18  |     |      |  |
|                        | CKA             | Q <sub>D</sub>                  |  | 32    | 48  |     | 32    | 48  |     | 46    | 70  |     | ns   |  |
|                        |                 |                                 |  | 34    | 50  |     | 34    | 50  |     | 46    | 70  |     |      |  |
|                        | CKB             | Q <sub>B</sub>                  |  | 10    | 16  |     | 10    | 16  |     | 10    | 16  |     | ns   |  |
|                        |                 |                                 |  | 14    | 21  |     | 14    | 21  |     | 14    | 21  |     |      |  |
|                        | CKB             | Q <sub>C</sub>                  |  | 21    | 32  |     | 10    | 16  |     | 21    | 32  |     | ns   |  |
|                        |                 |                                 |  | 23    | 35  |     | 14    | 21  |     | 23    | 35  |     |      |  |
| t <sub>PLH</sub>       | CKB             | Q <sub>D</sub>                  |  | 21    | 32  |     | 21    | 32  |     | 34    | 51  |     | ns   |  |
|                        |                 |                                 |  | 23    | 35  |     | 23    | 35  |     | 34    | 51  |     |      |  |
|                        | Set-to-0        | Any                             |  | 26    | 40  |     | 26    | 40  |     | 26    | 40  |     | ns   |  |
|                        |                 | Q <sub>A</sub> , Q <sub>D</sub> |  | 20    | 30  |     |       |     |     |       |     |     | ns   |  |
| t <sub>PHL</sub>       | Set-to-9        | Q <sub>B</sub> , Q <sub>C</sub> |  | 26    | 40  |     |       |     |     |       |     |     |      |  |

#f<sub>max</sub> = maximum count frequency

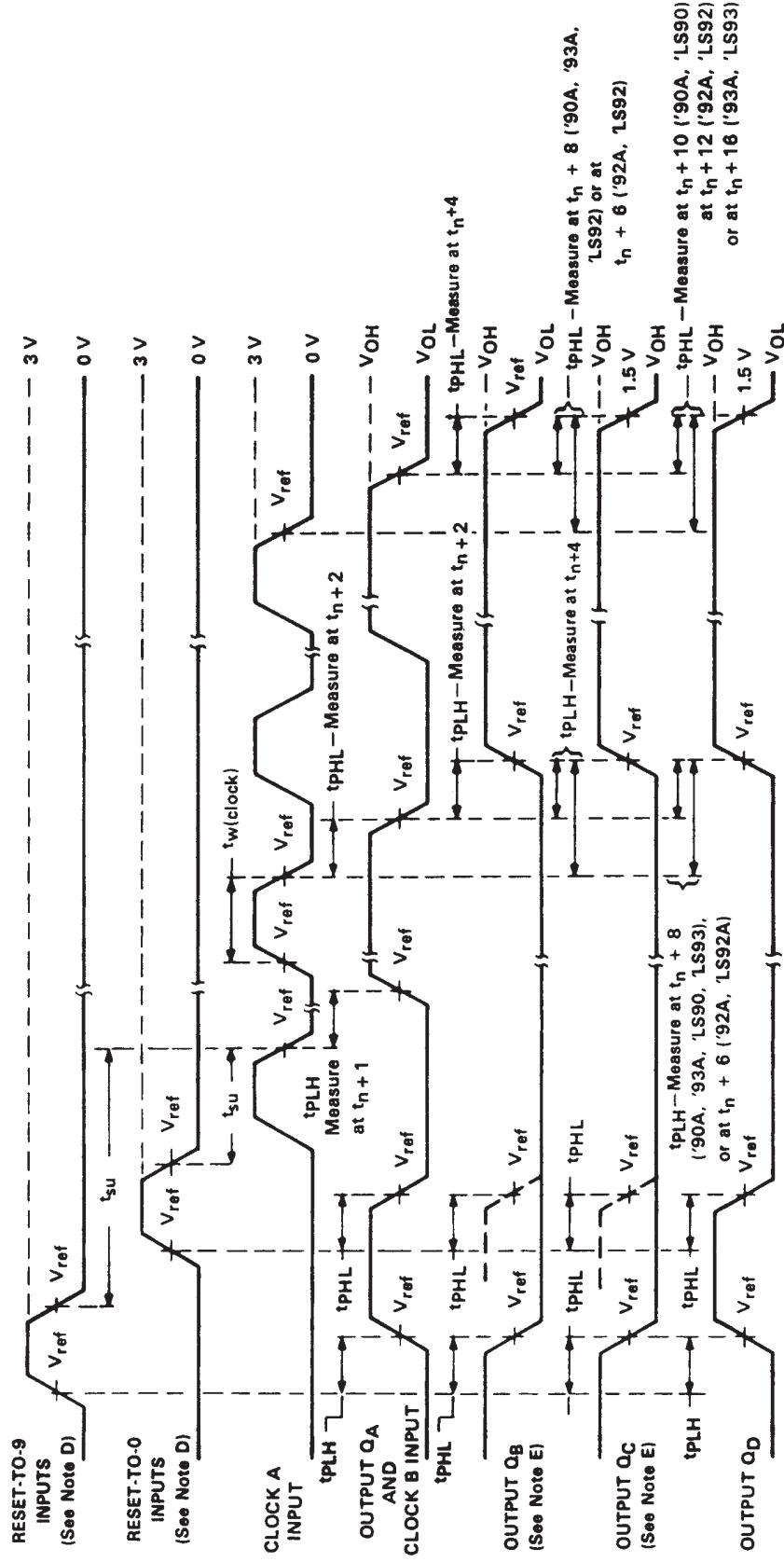
t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
**DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. Input pulses are supplied by a generator having the following characteristics:

for '90A, '92A, '93A, 'LS92, 'LS93,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;

for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.

B.  $C_L$  includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

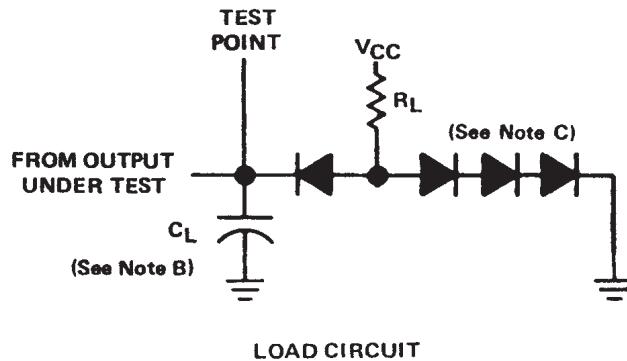
D. Each reset input is tested separately with the other reset at 4.5 V.

E. Reference waveforms are shown with dashed lines.

F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

**FIGURE 1A**

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. Input pulses are supplied by a generator having the following characteristics:  
 for '90A, '92A, '93A,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;  
 for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.
  - B.  $C_L$  includes probe and jig capacitance.
  - C. All diodes are 1N3064 or equivalent.
  - D. Each reset input is tested separately with the other reset at 4.5 V.
  - E. Reference waveforms are shown with dashed lines.
  - F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

FIGURE 1B

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| 7603201CA        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7603201CA SNJ54LS90J    | <span style="background-color: red; color: white;">Samples</span> |
| 7700101CA        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101CA SNJ54LS93J    | <span style="background-color: red; color: white;">Samples</span> |
| 7700101DA        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101DA SNJ54LS93W    | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31501BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31501BCA        | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31502BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BCA        | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31502BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31501BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31501BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31502BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31502BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS90J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS90J               | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS93J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS93J               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DE4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DG4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DRG4     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS90N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS90N               | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74LS90NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   |              | 74LS90                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS92                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS92N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS92                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS93D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS93                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS93N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS93N               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS90J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7603201CA<br>SNJ54LS90J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS93J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101CA<br>SNJ54LS93J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS93W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101DA<br>SNJ54LS93W | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF SN54LS90, SN54LS93, SN74LS90, SN74LS93 :

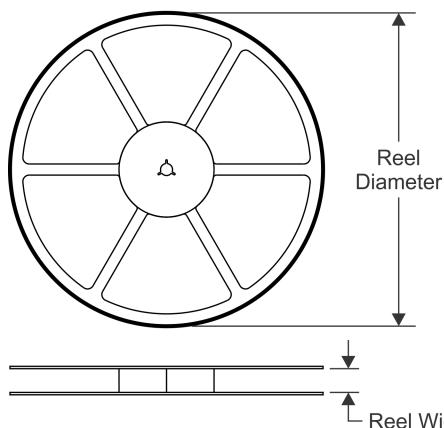
- Catalog: [SN74LS90](#), [SN74LS93](#)
- Military: [SN54LS90](#), [SN54LS93](#)

NOTE: Qualified Version Definitions:

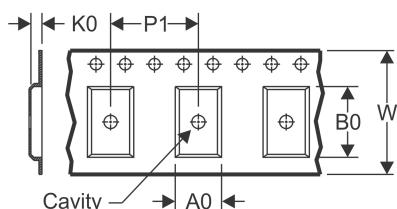
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

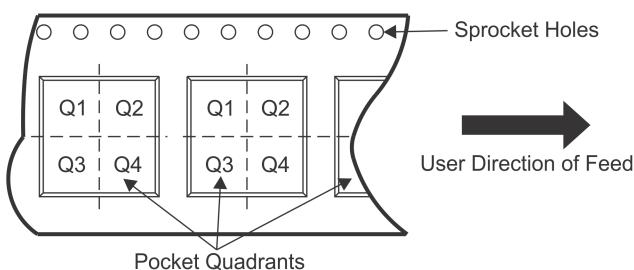


### TAPE DIMENSIONS



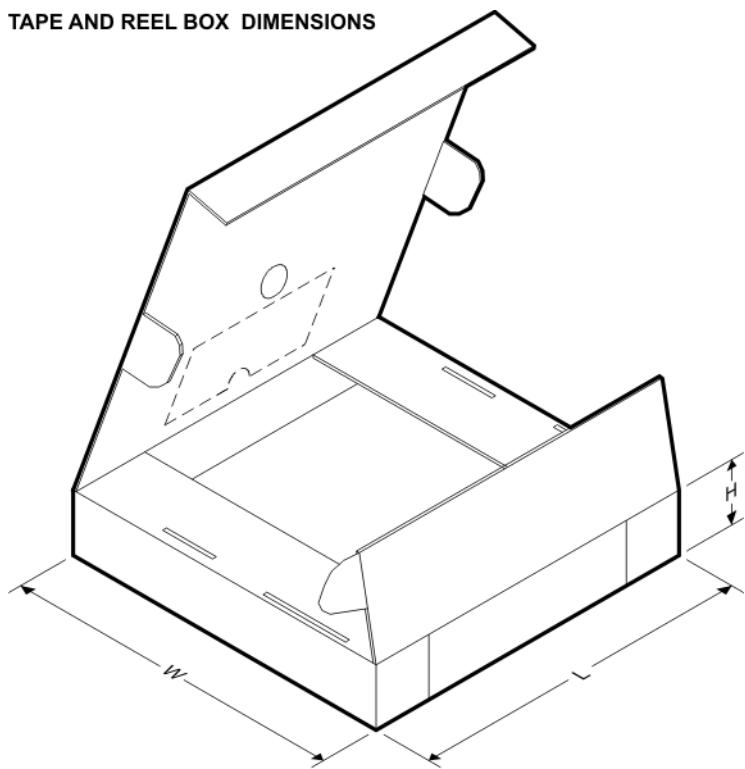
|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS90DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS90NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LS92NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


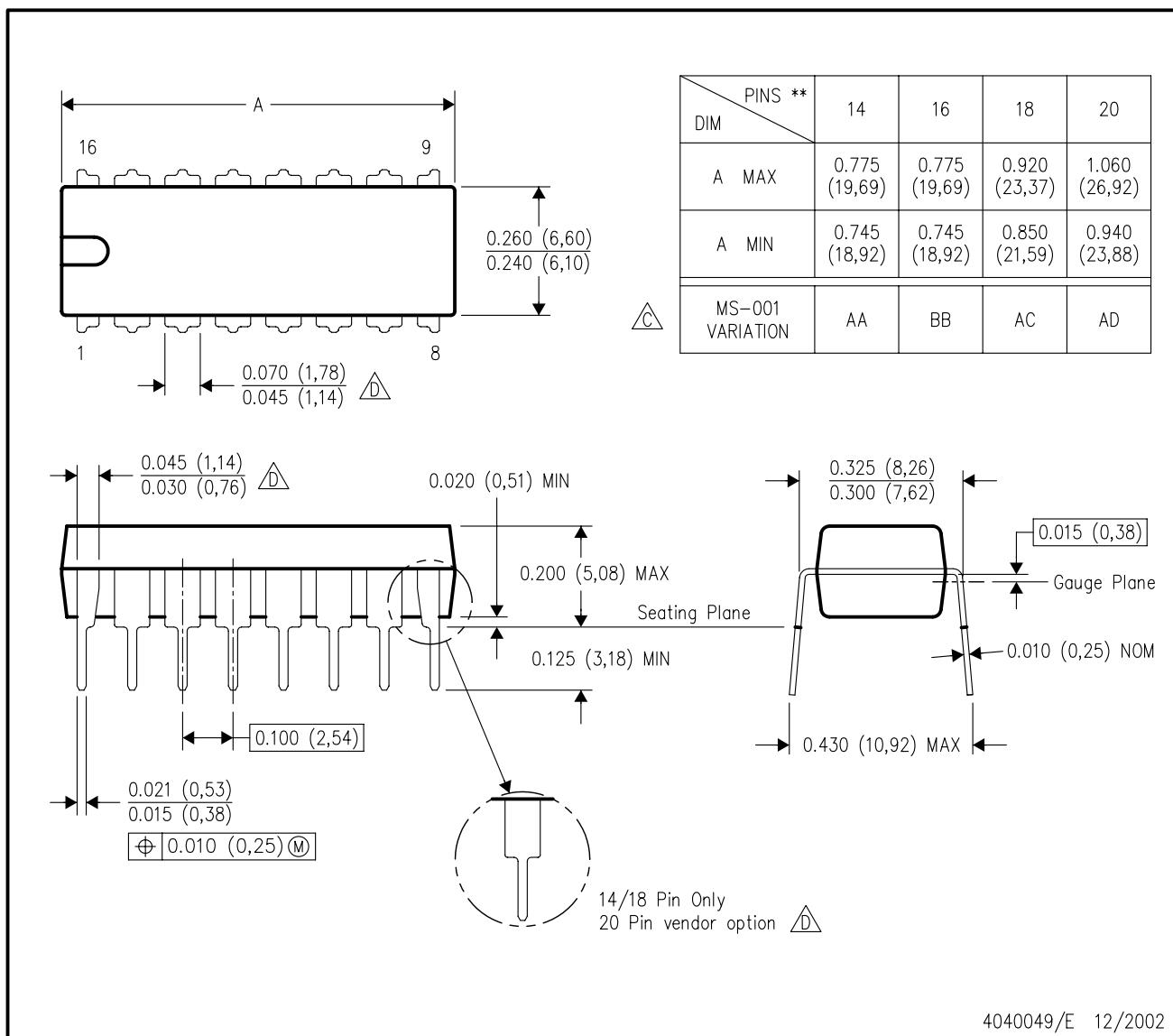
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS90DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LS90NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LS92NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

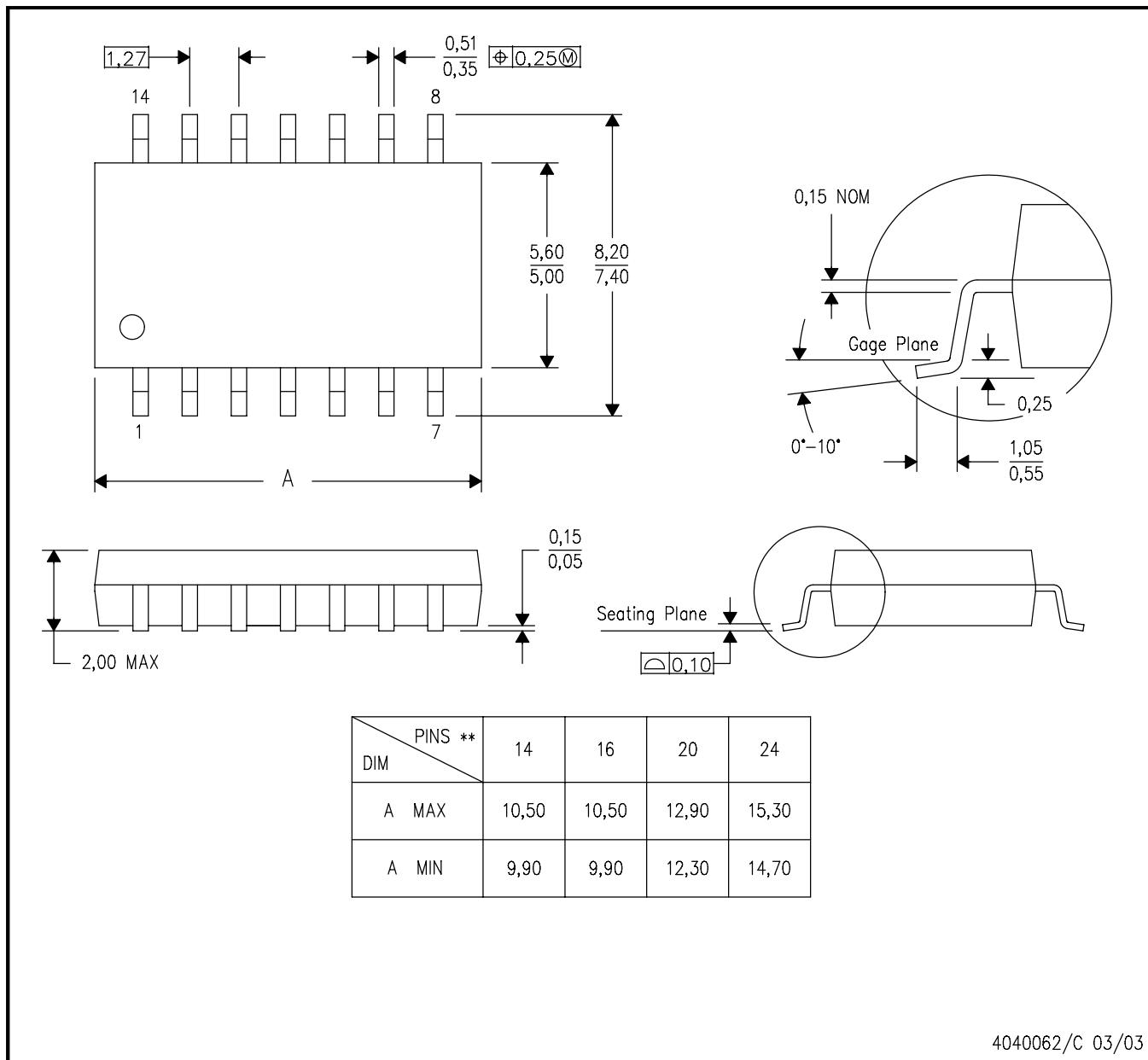
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



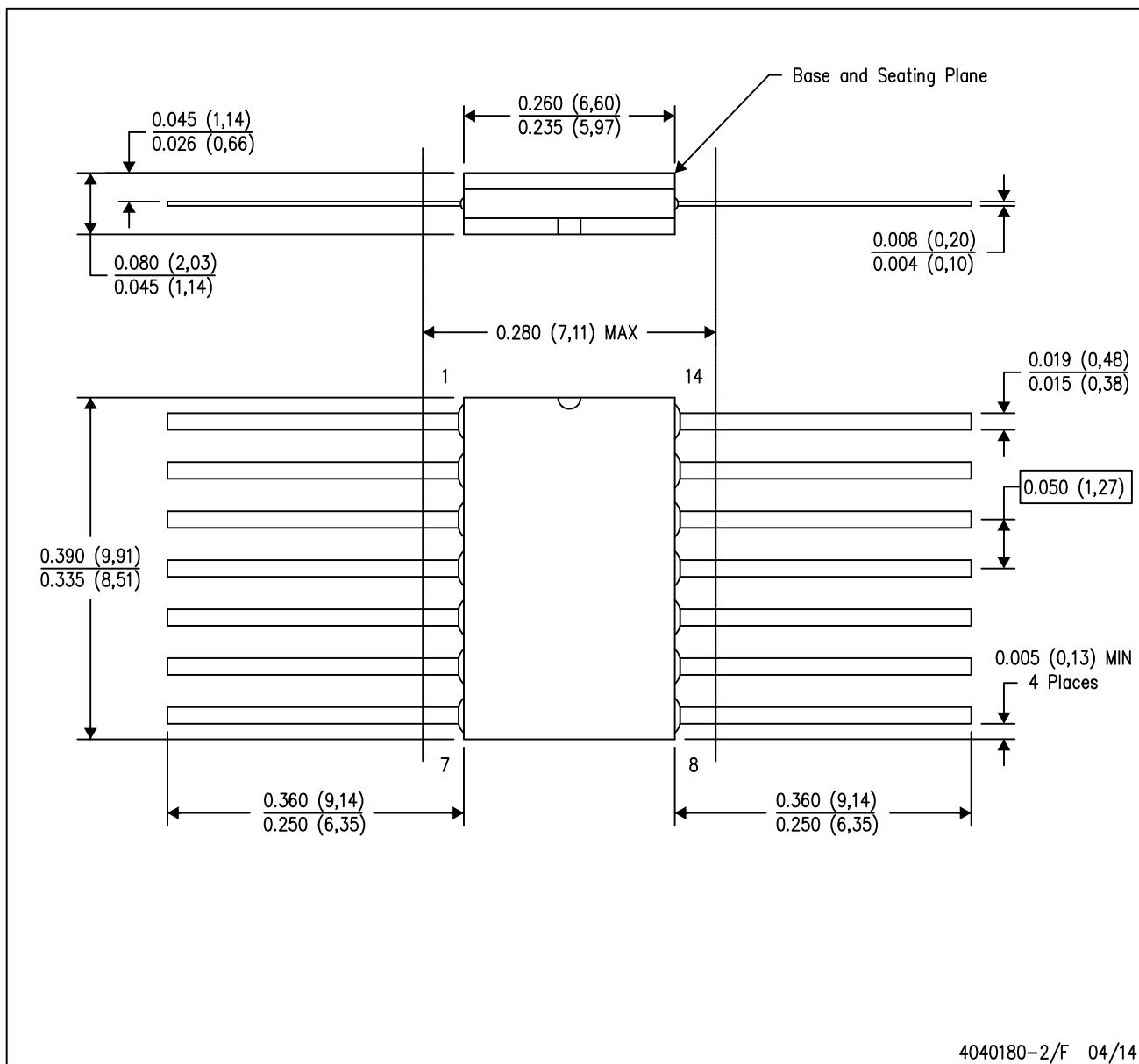
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

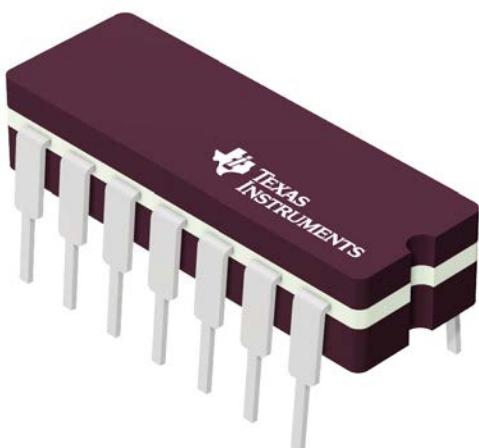
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

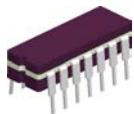
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

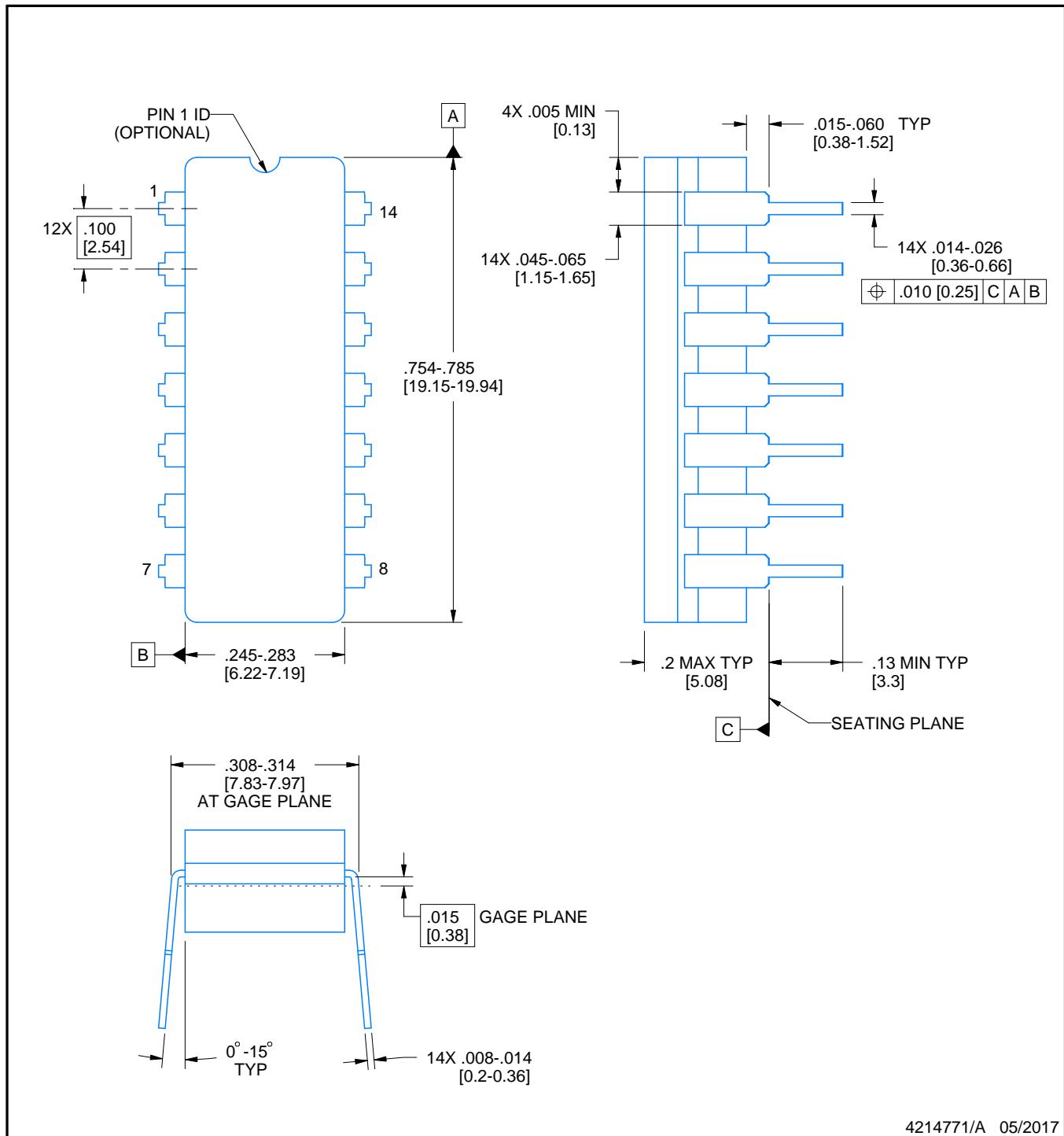
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

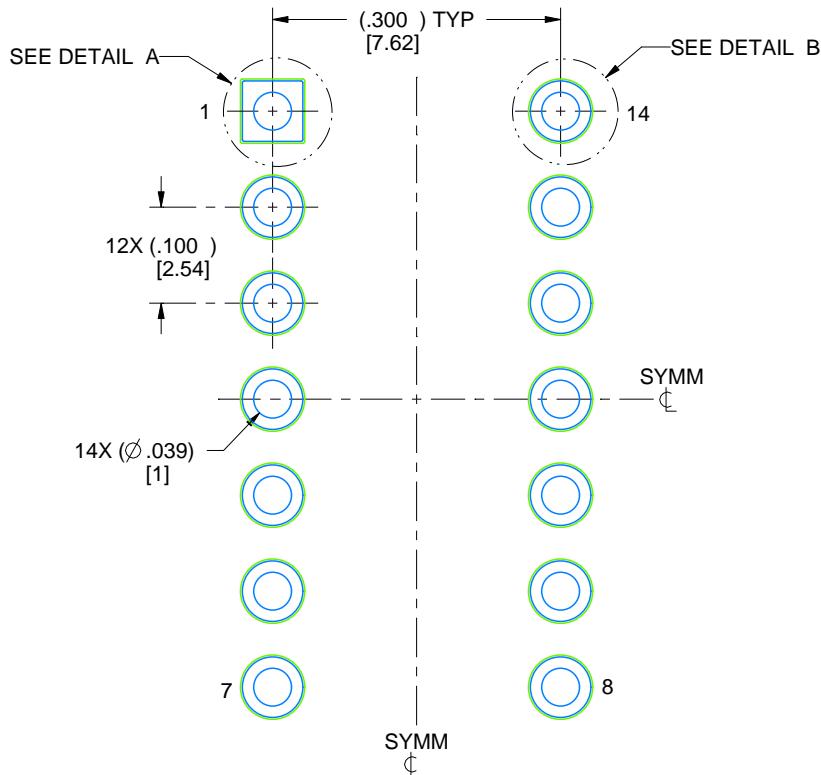
- All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This package is hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
- Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

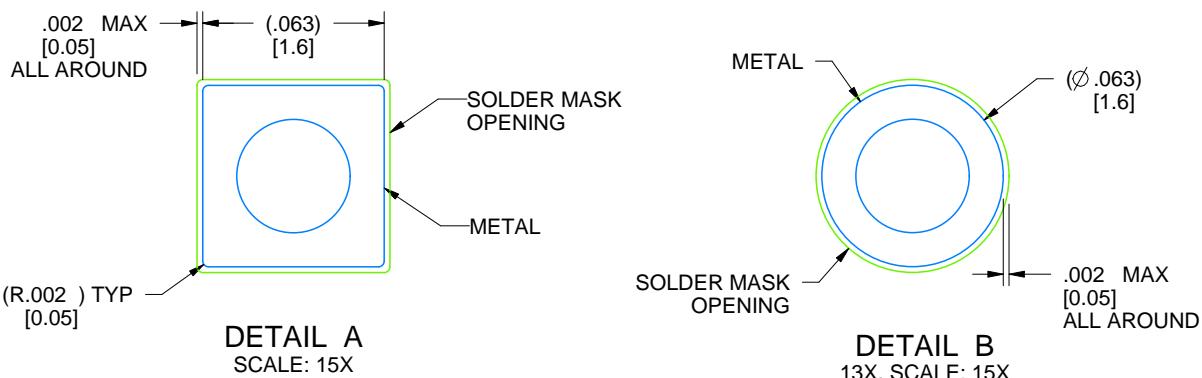
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



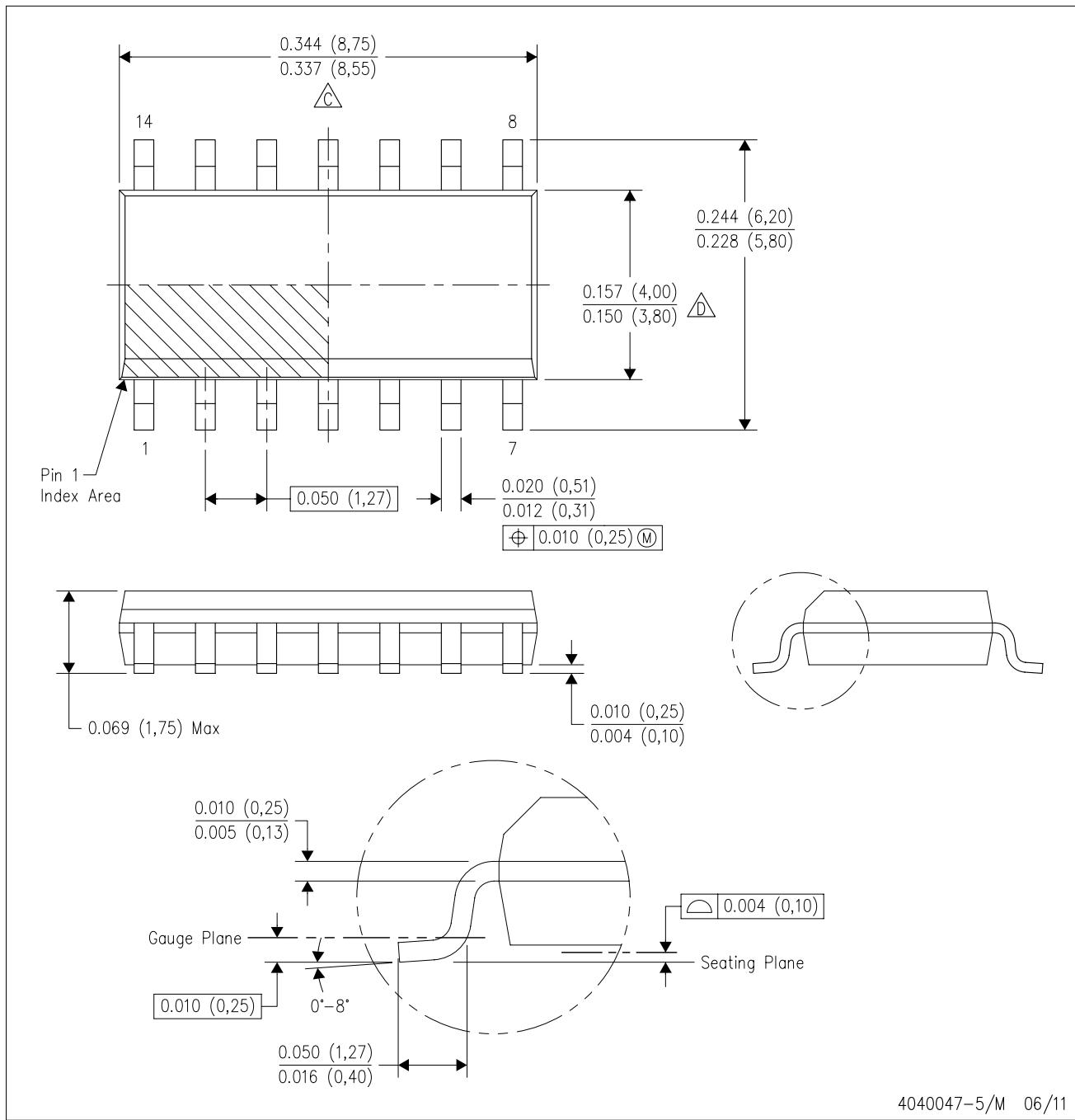
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

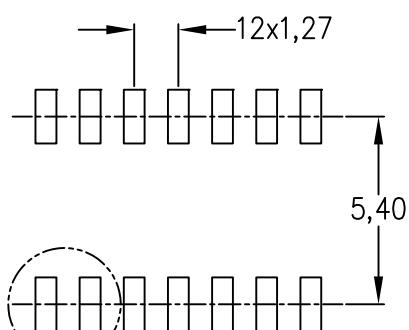
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

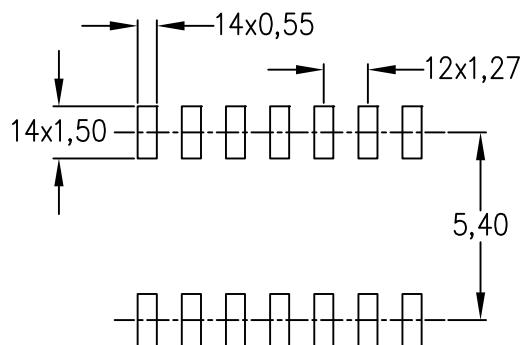
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

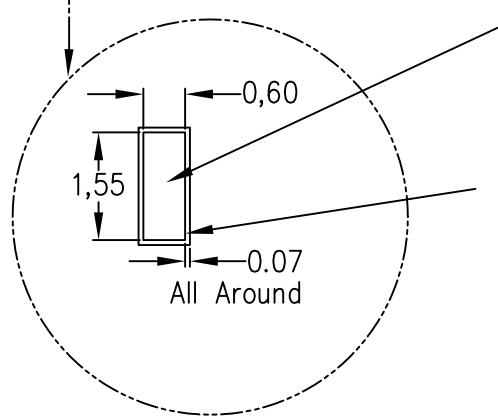
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

- '90A, 'LS90 . . . Decade Counters
- '92A, 'LS92 . . . Divide By-Twelve Counters
- '93A, 'LS93 . . . 4-Bit Binary Counters

| TYPES               | TYPICAL<br>POWER DISSIPATION |
|---------------------|------------------------------|
| '90A                | 145 mW                       |
| '92A, '93A          | 130 mW                       |
| 'LS90, 'LS92, 'LS93 | 45 mW                        |

#### description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

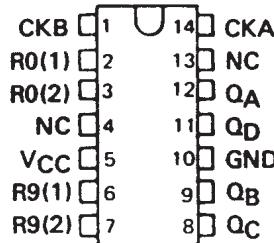
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the QA output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output QA.

**SN5490A, SN54LS90 . . . J OR W PACKAGE**

**SN7490A . . . N PACKAGE**

**SN74LS90 . . . D OR N PACKAGE**

(TOP VIEW)

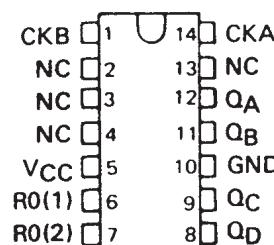


**SN5492A, SN54LS92 . . . J OR W PACKAGE**

**SN7492A . . . N PACKAGE**

**SN74LS92 . . . D OR N PACKAGE**

(TOP VIEW)

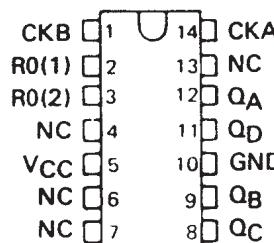


**SN5493A, SN54LS93 . . . J OR W PACKAGE**

**SN7493 . . . N PACKAGE**

**SN74LS93 . . . D OR N PACKAGE**

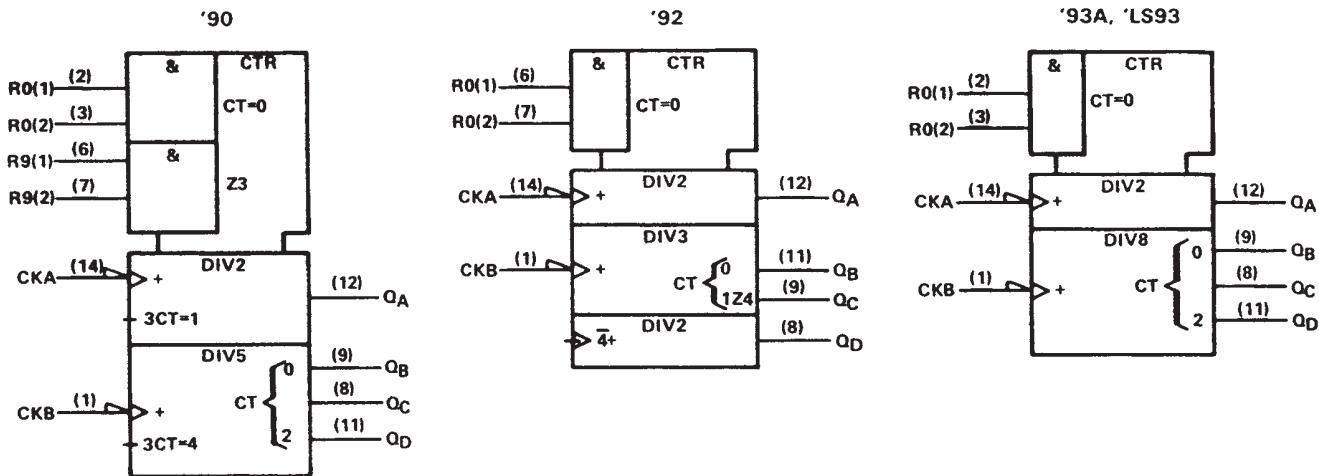
(TOP VIEW)



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic symbols<sup>†</sup>**



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90  
BCD COUNT SEQUENCE  
(See Note A)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | L              | H              | H              | L              |
| 7     | L              | H              | H              | H              |
| 8     | H              | L              | L              | L              |
| 9     | H              | L              | L              | H              |

'90A, 'LS90  
BI-QUINARY (5-2)  
(See Note B)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>A</sub> | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | H              | L              | L              | L              |
| 6     | H              | L              | L              | H              |
| 7     | H              | L              | H              | L              |
| 8     | H              | L              | H              | H              |
| 9     | H              | H              | L              | L              |

'92A, 'LS92  
COUNT SEQUENCE  
(See Note C)

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | H              | L              | L              | L              |
| 7     | H              | L              | L              | H              |
| 8     | H              | L              | H              | L              |
| 9     | H              | L              | H              | H              |
| 10    | H              | H              | L              | L              |
| 11    | H              | H              | L              | H              |

'90A, 'LS90  
RESET/COUNT FUNCTION TABLE

| RESET INPUTS      |                   |                   |                   | OUTPUT  |
|-------------------|-------------------|-------------------|-------------------|---|
| R <sub>0(1)</sub> | R <sub>0(2)</sub> | R <sub>9(1)</sub> | R <sub>9(2)</sub> | Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub> |
| H                 | H                 | L                 | X                 | L L L L   |
| H                 | H                 | X                 | L                 | L L L L   |
| X                 | X                 | H                 | H                 | H L L H   |
| X                 | L                 | X                 | L                 | COUNT   |
| L                 | X                 | L                 | X                 | COUNT   |
| L                 | X                 | X                 | L                 | COUNT   |
| X                 | L                 | L                 | X                 | COUNT   |

'92A, 'LS92, '93A, 'LS93  
RESET/COUNT FUNCTION TABLE

| RESET INPUTS      |                   | OUTPUT  |
|-------------------|-------------------|---|
| R <sub>0(1)</sub> | R <sub>0(2)</sub> | Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub> |
| H                 | H                 | L L L L   |
| L                 | X                 | COUNT   |
| X                 | L                 | COUNT   |

- NOTES: A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
B. Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.  
C. Output Q<sub>A</sub> is connected to input CKB.  
D. H = high level, L = low level, X = irrelevant

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>D</sub> | Q <sub>C</sub> | Q <sub>B</sub> | Q <sub>A</sub> |
| 0     | L              | L              | L              | L              |
| 1     | L              | L              | L              | H              |
| 2     | L              | L              | H              | L              |
| 3     | L              | L              | H              | H              |
| 4     | L              | H              | L              | L              |
| 5     | L              | H              | L              | H              |
| 6     | L              | H              | H              | L              |
| 7     | L              | H              | H              | H              |
| 8     | H              | L              | L              | L              |
| 9     | H              | L              | L              | H              |
| 10    | H              | L              | H              | L              |
| 11    | H              | L              | H              | H              |
| 12    | H              | H              | L              | L              |
| 13    | H              | H              | L              | H              |
| 14    | H              | H              | H              | L              |
| 15    | H              | H              | H              | H              |

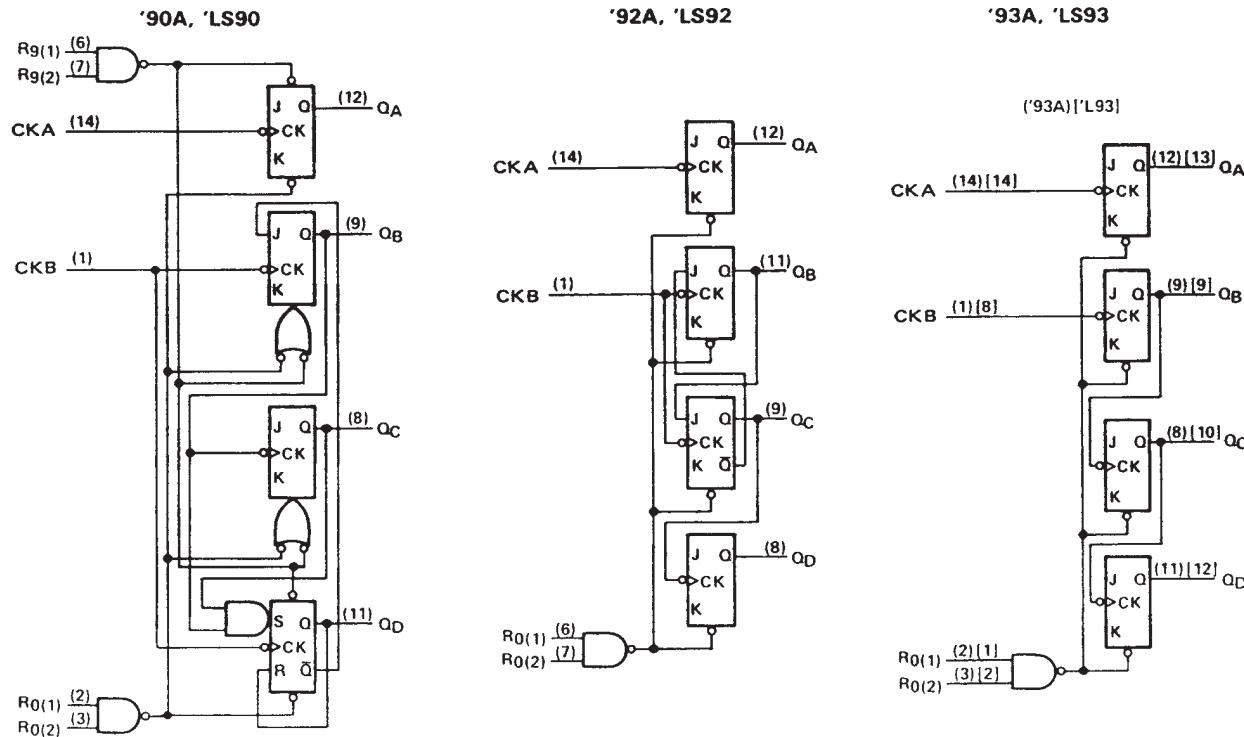


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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

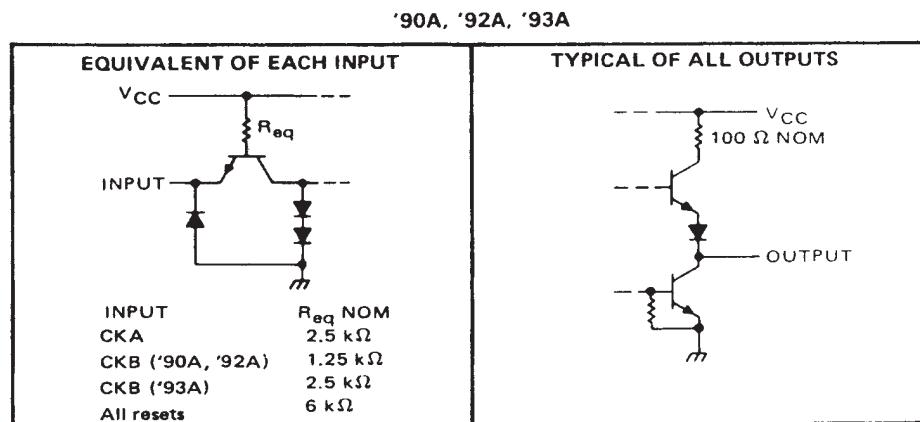
SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic diagrams (positive logic)**



The J and K inputs shown without connection are for reference only and are functionally at a high level.  
Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [ ] are for the 54L93.

**schematics of inputs and outputs**

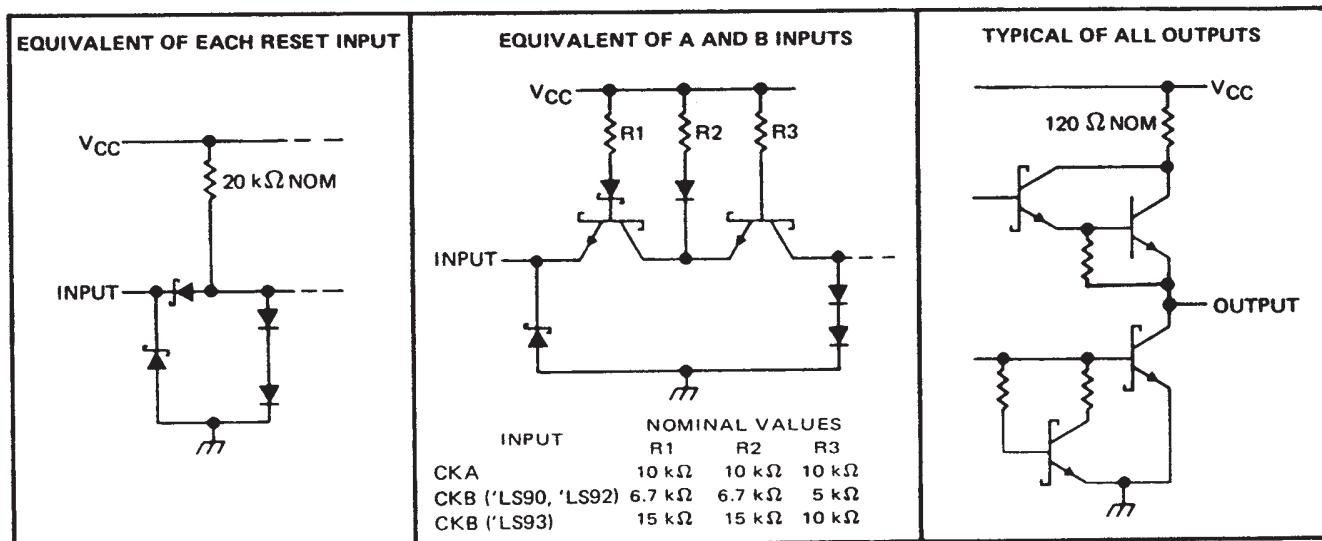


**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**schematics of inputs and outputs (continued)**

'LS90, 'LS92, 'LS93



# SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

NOTES: 1. Voltage values, except interemitter voltage, etc., with respect to ground.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two  $R_0$  inputs, and for the '90A circuit, it also applies between the two  $R_g$  inputs.

#### **recommended operating conditions**

|   | SN5490A, SN5492A<br>SN5493A | SN7490A, SN7492A<br>SN7493A |      |      | UNIT         |
|---|-----------------------------|-----------------------------|------|------|--------------|
|   |                             | MIN                         | NOM  | MAX  |              |
|   |                             | MIN                         | NOM  | MAX  |              |
| Supply voltage, $V_{CC}$                    | 4.5                         | 5                           | 5.5  | 4.75 | 5 5.25 V     |
| High-level output current, $I_{OH}$         |                             |                             | -800 |      | -800 $\mu A$ |
| Low-level output current, $I_{OL}$          |                             |                             | 16   |      | 16 mA        |
| Count frequency, $f_{count}$ (see Figure 1) | A input                     | 0                           | 32   | 0    | 32 MHz       |
|   | B input                     | 0                           | 16   | 0    | 16           |
| Pulse width, $t_W$                          | A input                     | 15                          |      | 15   | ns           |
|   | B input                     | 30                          |      | 30   |              |
|   | Reset inputs                | 15                          |      | 15   |              |
| Reset inactive-state setup time, $t_{SU}$   |                             | 25                          |      | 25   | ns           |
| Operating free-air temperature, $T_A$       | -55                         | 125                         | 0    | 70   | $^{\circ}C$  |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>1</sup>                                       | TEST CONDITIONS <sup>†</sup>   | '90A  |                  |     | '92A |                  |     | '93A |                  |     | UNIT |    |
|--|--|---|------------------|-----|------|------------------|-----|------|------------------|-----|------|----|
|  |  | MIN   | TYP <sup>‡</sup> | MAX | MIN  | TYP <sup>‡</sup> | MAX | MIN  | TYP <sup>‡</sup> | MAX |      |    |
| V <sub>IH</sub> High-level input voltage                     |  | 2   |                  |     | 2    |                  |     | 2    |                  |     | V    |    |
| V <sub>IL</sub> Low-level input voltage                      |  | 0.8   |                  |     | 0.8  |                  |     | 0.8  |                  |     | V    |    |
| V <sub>IK</sub> Input clamp voltage                          | V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA   | -1.5  |                  |     | -1.5 |                  |     | -1.5 |                  |     | V    |    |
| V <sub>OH</sub> High-level output voltage                    | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 µA            | 2.4   | 3.4              |     | 2.4  | 3.4              |     | 2.4  | 3.4              |     | V    |    |
| V <sub>OL</sub> Low-level output voltage                     | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA <sup>§</sup> | 0.2   | 0.4              |     | 0.2  | 0.4              |     | 0.2  | 0.4              |     | V    |    |
| I <sub>I</sub> Input current at<br>maximum input voltage     | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V  | 1   |                  |     | 1    |                  |     | 1    |                  |     | mA   |    |
| I <sub>IH</sub> High-level<br>input current                  | Any reset  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V |                  |     | 40   |                  |     | 40   |                  |     | 40   |    |
|  | CKA  |   |                  |     | 80   |                  |     | 80   |                  |     | 80   |    |
|  | CKB  |   |                  |     | 120  |                  |     | 120  |                  |     | 80   |    |
| I <sub>IIL</sub> Low-level<br>input current                  | Any reset  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |                  |     | -1.6 |                  |     | -1.6 |                  |     | -1.6 |    |
|  | CKA  |   |                  |     | -3.2 |                  |     | -3.2 |                  |     | -3.2 |    |
|  | CKB  |   |                  |     | -4.8 |                  |     | -4.8 |                  |     | -3.2 |    |
| I <sub>OS</sub> Short-circuit<br>output current <sup>§</sup> | V <sub>CC</sub> = MAX  |   | SN54'            | -20 | -57  | -20              | -57 | -20  | -57              | -20 | mA   |    |
|  |  |   | SN74'            | -18 | -57  | -18              | -57 | -18  | -57              | -18 | mA   |    |
| I <sub>CC</sub> Supply current                               | V <sub>CC</sub> = MAX, See Note 3  |   |                  | 29  | 42   |                  | 26  | 39   |                  | 26  | 39   | mA |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>†</sup>All typical values are at V<sub>CC</sub> = 5 V, TA = 25°C.  
<sup>§</sup>Not more than one output should be shorted at a time.

**Q<sub>A</sub>** outputs are tested at I<sub>OL</sub> = 16 mA plus the limit value for I<sub>IL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3:  $I_{CC}$  is measured with all outputs open, both  $R_O$  inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER <sup>†</sup> | FROM<br>(INPUT)  | TO<br>(OUTPUT)                  | TEST CONDITIONS   | '90A |     |     | '92A |     |     | '93A |     |     | UNIT |
|------------------------|------------------|---------------------------------|---|------|-----|-----|------|-----|-----|------|-----|-----|------|
|                        |                  |                                 |   | MIN  | TYP | MAX | MIN  | TYP | MAX | MIN  | TYP | MAX |      |
| $f_{max}$              | CKA              | Q <sub>A</sub>                  | $C_L = 15 \text{ pF}$ ,<br>$R_L = 400 \Omega$ ,<br>See Figure 1 | 32   | 42  |     | 32   | 42  |     | 32   | 42  |     | MHz  |
|                        | CKB              | Q <sub>B</sub>                  |   | 16   |     |     | 16   |     |     | 16   |     |     |      |
|                        | t <sub>PLH</sub> | CKA                             |   | 10   | 16  |     | 10   | 16  |     | 10   | 16  |     | ns   |
|                        | t <sub>PHL</sub> | CKA                             |   | 12   | 18  |     | 12   | 18  |     | 12   | 18  |     |      |
|                        | t <sub>PLH</sub> | CKA                             |   | 32   | 48  |     | 32   | 48  |     | 46   | 70  |     | ns   |
|                        | t <sub>PHL</sub> | CKA                             |   | 34   | 50  |     | 34   | 50  |     | 46   | 70  |     |      |
|                        | t <sub>PLH</sub> | CKB                             |   | 10   | 16  |     | 10   | 16  |     | 10   | 16  |     | ns   |
|                        | t <sub>PHL</sub> | CKB                             |   | 14   | 21  |     | 14   | 21  |     | 14   | 21  |     |      |
|                        | t <sub>PLH</sub> | CKB                             |   | 21   | 32  |     | 10   | 16  |     | 21   | 32  |     | ns   |
|                        | t <sub>PHL</sub> | CKB                             |   | 23   | 35  |     | 14   | 21  |     | 23   | 35  |     |      |
| $t_{PLH}$              | CKB              | Q <sub>D</sub>                  |   | 21   | 32  |     | 21   | 32  |     | 34   | 51  |     | ns   |
|                        | t <sub>PHL</sub> | CKB                             |   | 23   | 35  |     | 23   | 35  |     | 34   | 51  |     |      |
|                        | t <sub>PLH</sub> | Set-to-0                        |   | 26   | 40  |     | 26   | 40  |     | 26   | 40  |     | ns   |
|                        | t <sub>PHL</sub> | Set-to-9                        |   | 20   | 30  |     |      |     |     |      |     |     | ns   |
| t <sub>PHL</sub>       |                  | Q <sub>A</sub> , Q <sub>D</sub> |   | 26   | 40  |     |      |     |     |      |     |     | ns   |
|                        |                  | Q <sub>B</sub> , Q <sub>C</sub> |   |      |     |     |      |     |     |      |     |     | ns   |

<sup>†</sup> $f_{max}$  = maximum count frequency

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output



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# SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub> (see Note 1)           | 7 V            |
| Input voltage: R inputs                                | 7 V            |
| A and B inputs   | 5.5 V          |
| Operating free-air temperature range: SN54LS' Circuits | -55°C to 125°C |
| SN74LS' Circuits                                       | 0°C to 70°C    |
| Storage temperature range                              | -65°C to 150°C |

**NOTE 1:** Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

|   | SN54LS90     |     |     | SN74LS90 |     |      | UNIT        |  |
|---|--------------|-----|-----|----------|-----|------|-------------|--|
|   | SN54LS92     |     |     | SN74LS92 |     |      |             |  |
|   | SN54LS93     |     |     | SN74LS93 |     |      |             |  |
|   | MIN          | NOM | MAX | MIN      | NOM | MAX  |             |  |
| Supply voltage, $V_{CC}$                    | 4.5          | 5   | 5.5 | 4.75     | 5   | 5.25 | V           |  |
| High-level output current, $I_{OH}$         |              |     |     | -400     |     |      | $\mu A$     |  |
| Low-level output current, $I_{OL}$          |              |     |     | 4        |     |      | mA          |  |
| Count frequency, $f_{count}$ (see Figure 1) | A input      | 0   | 32  | 0        | 32  |      | MHz         |  |
|   | B input      | 0   | 16  | 0        | 16  |      |             |  |
| Pulse width, $t_W$                          | A input      | 15  |     | 15       |     |      | ns          |  |
|   | B input      | 30  |     | 30       |     |      |             |  |
|   | Reset inputs | 30  |     | 30       |     |      |             |  |
| Reset inactive-state setup time, $t_{SU}$   | 25           |     |     | 25       |     |      | ns          |  |
| Operating free-air temperature, $T_A$       | -55          | 125 | 0   | 70       |     |      | $^{\circ}C$ |  |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |  | TEST CONDITIONS†                        |                         |                           | SN54LS90 |      | SN74LS90 |      | UNIT |
|------------------|--|---|-------------------------|---------------------------|----------|------|----------|------|------|
|                  |  |   |                         |                           | MIN      | TYP‡ | MAX      | MIN  |      |
| VIH              | High-level input voltage                     |   |                         |                           | 2        |      | 2        |      | V    |
| VIL              | Low-level input voltage                      |   |                         |                           |          | 0.7  |          | 0.8  | V    |
| VIK              | Input clamp voltage                          | V <sub>CC</sub> = MIN,                  | I <sub>I</sub> = -18 mA |                           |          | -1.5 |          | -1.5 | V    |
| VOH              | High-level output voltage                    | V <sub>CC</sub> = MIN,                  | V <sub>IH</sub> = 2 V,  | I <sub>OH</sub> = -400 µA | 2.5      | 3.4  |          | 2.7  | V    |
| VOL              | Low-level output voltage                     | V <sub>CC</sub> = MIN,                  | V <sub>IH</sub> = 2 V,  | I <sub>OL</sub> = 4 mA¶   | 0.25     | 0.4  |          | 0.25 | 0.4  |
|                  |  | V <sub>IIL</sub> = V <sub>IL</sub> max, |                         | I <sub>OL</sub> = 8 mA¶   |          |      | 0.35     | 0.5  | V    |
| I <sub>I</sub>   | Input current<br>at maximum<br>input voltage | Any reset                               | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 7 V      |          | 0.1  |          | 0.1  |      |
|                  | CKA  | V <sub>CC</sub> = MAX,                  | V <sub>I</sub> = 5.5 V  |                           | 0.2      |      | 0.2      | mA   |      |
|                  | CKB  |   |                         |                           | 0.4      |      | 0.4      |      |      |
| I <sub>IH</sub>  | High-level<br>input current                  | Any reset                               | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 2.7 V    |          | 20   |          | 20   |      |
|                  |  | CKA                                     |                         |                           |          | 40   |          | 40   | µA   |
|                  |  | CKB                                     |                         |                           |          | 80   |          | 80   |      |
| I <sub>IIL</sub> | Low-level<br>input current                   | Any reset                               | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 0.4 V    |          | -0.4 |          | -0.4 |      |
|                  |  | CKA                                     |                         |                           |          | -2.4 |          | -2.4 | mA   |
|                  |  | CKB                                     |                         |                           |          | -3.2 |          | -3.2 |      |
| I <sub>OS</sub>  | Short-circuit output current§                | V <sub>CC</sub> = MAX                   |                         |                           | -20      | -100 | -20      | -100 | mA   |
| I <sub>CC</sub>  | Supply current                               | V <sub>CC</sub> = MAX,                  | See Note 3              | 'LS90                     | 9        | 15   |          | 9    | 15   |
|                  |  |   |                         | 'LS92                     | 9        | 15   |          | 9    | 15   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>#</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

**8** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**Q<sub>A</sub>** outputs are tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3:  $I_{CC}$  is measured with all outputs open, both  $R_O$  inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS <sup>†</sup>  | SN54LS93                                      |                  |      | SN74LS93 |                  |      | UNIT |
|---|---|---|------------------|------|----------|------------------|------|------|
|   |   | MIN   | TYP <sup>‡</sup> | MAX  | MIN      | TYP <sup>‡</sup> | MAX  |      |
| V <sub>IH</sub> High-level input voltage                  |   | 2   |                  |      | 2        |                  |      | V    |
| V <sub>IL</sub> Low-level input voltage                   |   |   |                  | 0.7  |          |                  | 0.8  | V    |
| V <sub>IK</sub> Input clamp voltage                       | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA  |   |                  | -1.5 |          |                  | -1.5 | V    |
| V <sub>OH</sub> High-level output voltage                 | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA | 2.5   | 3.4              |      | 2.7      | 3.4              |      | V    |
| V <sub>OL</sub> Low-level output voltage                  | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max                            | I <sub>OL</sub> = 4 mA <sup>§</sup>           | 0.25             | 0.4  | 0.25     | 0.4              |      | V    |
|   |   | I <sub>OL</sub> = 8 mA <sup>§</sup>           |                  |      | 0.35     | 0.5              |      |      |
| I <sub>I</sub> Input current at maximum input voltage     | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V   |                  |      | 0.1      |                  | 0.1  | mA   |
|   | CKA or CKB  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V |                  |      | 0.2      |                  | 0.2  |      |
| I <sub>IH</sub> High-level input current                  | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |                  |      | 20       |                  | 20   | μA   |
|   | CKA or CKB  |   |                  |      | 40       |                  | 80   |      |
| I <sub>IIL</sub> Low-level input current                  | Any reset   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |                  |      | -0.4     |                  | -0.4 | mA   |
|   | CKA   |   |                  |      | -2.4     |                  | -2.4 |      |
|   | CKB   |   |                  |      | -1.6     |                  | -1.6 |      |
| I <sub>OS</sub> Short-circuit output current <sup>§</sup> | V <sub>CC</sub> = MAX   |   | -20              | -100 | -20      | -100             |      | mA   |
| I <sub>CC</sub> Supply current                            | V <sub>CC</sub> = MAX, See Note 3   |   | 9                | 15   | 9        | 15               |      | mA   |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup>Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value for I<sub>IIL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>O</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER <sup>#</sup> | FROM (INPUT) | TO (OUTPUT)                     | TEST CONDITIONS  | 'LS90 |     |     | 'LS92 |     |     | 'LS93 |     |     | UNIT |  |
|------------------------|--------------|---------------------------------|--|-------|-----|-----|-------|-----|-----|-------|-----|-----|------|--|
|                        |              |                                 |  | MIN   | TYP | MAX | MIN   | TYP | MAX | MIN   | TYP | MAX |      |  |
| f <sub>max</sub>       | CKA          | Q <sub>A</sub>                  | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 2 kΩ<br>See Figure 1 | 32    | 42  |     | 32    | 42  |     | 32    | 42  |     | MHz  |  |
|                        | CKB          | Q <sub>B</sub>                  |  | 16    |     |     | 16    |     |     | 16    |     |     |      |  |
| t <sub>PLH</sub>       | CKA          | Q <sub>A</sub>                  |  | 10    | 16  |     | 10    | 16  |     | 10    | 16  |     | ns   |  |
|                        |              |                                 |  | 12    | 18  |     | 12    | 18  |     | 12    | 18  |     |      |  |
| t <sub>PLH</sub>       | CKA          | Q <sub>D</sub>                  |  | 32    | 48  |     | 32    | 48  |     | 46    | 70  |     | ns   |  |
|                        |              |                                 |  | 34    | 50  |     | 34    | 50  |     | 46    | 70  |     |      |  |
| t <sub>PLH</sub>       | CKB          | Q <sub>B</sub>                  |  | 10    | 16  |     | 10    | 16  |     | 10    | 16  |     | ns   |  |
|                        |              |                                 |  | 14    | 21  |     | 14    | 21  |     | 14    | 21  |     |      |  |
| t <sub>PLH</sub>       | CKB          | Q <sub>C</sub>                  |  | 21    | 32  |     | 10    | 16  |     | 21    | 32  |     | ns   |  |
|                        |              |                                 |  | 23    | 35  |     | 14    | 21  |     | 23    | 35  |     |      |  |
| t <sub>PLH</sub>       | CKB          | Q <sub>D</sub>                  |  | 21    | 32  |     | 21    | 32  |     | 34    | 51  |     | ns   |  |
|                        |              |                                 |  | 23    | 35  |     | 23    | 35  |     | 34    | 51  |     |      |  |
| t <sub>PHL</sub>       | Set-to-0     | Any                             |  | 26    | 40  |     | 26    | 40  |     | 26    | 40  |     | ns   |  |
| t <sub>PLH</sub>       | Set-to-9     | Q <sub>A</sub> , Q <sub>D</sub> |  | 20    | 30  |     |       |     |     |       |     |     | ns   |  |
|                        |              | Q <sub>B</sub> , Q <sub>C</sub> |  | 26    | 40  |     |       |     |     |       |     |     |      |  |

#f<sub>max</sub> = maximum count frequency

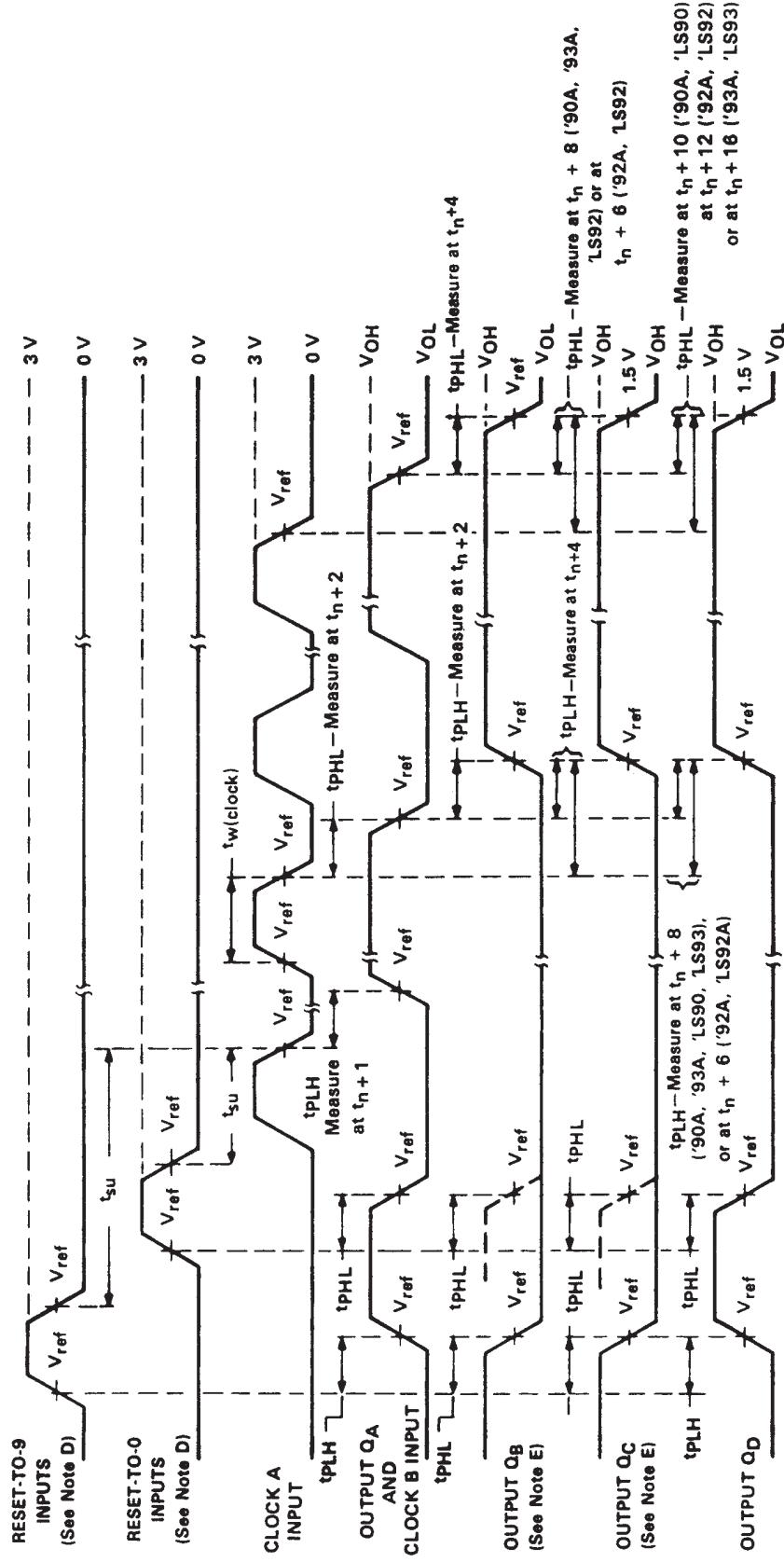
t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
**DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

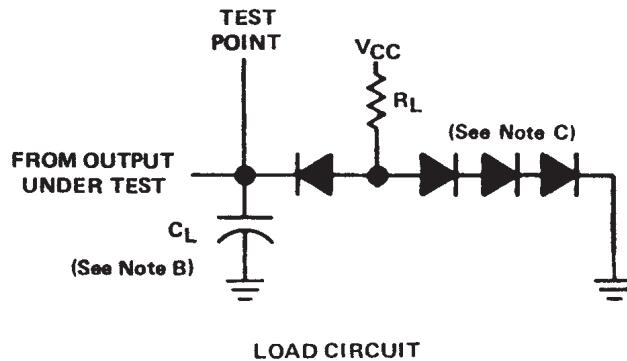
**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:  
 for '90A, '92A, '93A, 'LS92, 'LS93,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;  
 for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.  
 D. Each reset input is tested separately with the other reset at 4.5 V.  
 E. Reference waveforms are shown with dashed lines.  
 F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

**FIGURE 1A**

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. Input pulses are supplied by a generator having the following characteristics:  
 for '90A, '92A, '93A,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;  
 for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.
  - B.  $C_L$  includes probe and jig capacitance.
  - C. All diodes are 1N3064 or equivalent.
  - D. Each reset input is tested separately with the other reset at 4.5 V.
  - E. Reference waveforms are shown with dashed lines.
  - F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

FIGURE 1B

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)      | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| 7603201CA        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7603201CA SNJ54LS90J    | <span style="background-color: red; color: white;">Samples</span> |
| 7700101CA        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101CA SNJ54LS93J    | <span style="background-color: red; color: white;">Samples</span> |
| 7700101DA        | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101DA SNJ54LS93W    | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31501BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31501BCA        | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31502BCA | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BCA        | <span style="background-color: red; color: white;">Samples</span> |
| JM38510/31502BDA | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31501BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31501BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31502BCA  | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BCA        | <span style="background-color: red; color: white;">Samples</span> |
| M38510/31502BDA  | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/31502BDA        | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS90J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS90J               | <span style="background-color: red; color: white;">Samples</span> |
| SN54LS93J        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS93J               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DE4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DG4      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90DRG4     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green         | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS90                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS90N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS90NE4      | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green         | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS90N               | <span style="background-color: red; color: white;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SN74LS90NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   |              | 74LS90                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS92                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS92N               | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS92NSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS92                  | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS93D        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green            | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS93                    | <span style="background-color: red; color: white;">Samples</span> |
| SN74LS93N        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green            | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS93N               | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS90J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7603201CA<br>SNJ54LS90J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS93J       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101CA<br>SNJ54LS93J | <span style="background-color: red; color: white;">Samples</span> |
| SNJ54LS93W       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS &<br>Non-Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7700101DA<br>SNJ54LS93W | <span style="background-color: red; color: white;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF SN54LS90, SN54LS93, SN74LS90, SN74LS93 :

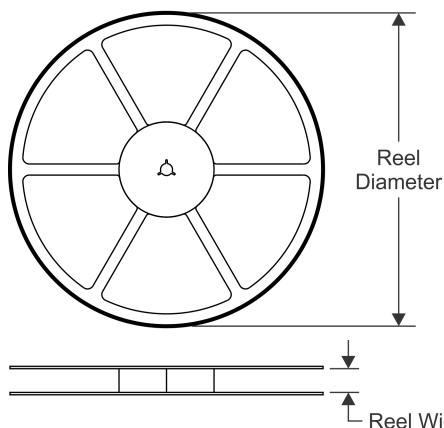
- Catalog: [SN74LS90](#), [SN74LS93](#)
- Military: [SN54LS90](#), [SN54LS93](#)

NOTE: Qualified Version Definitions:

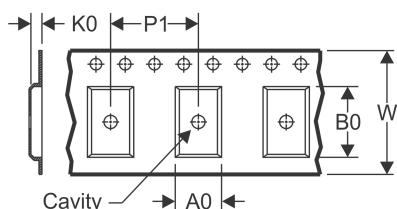
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

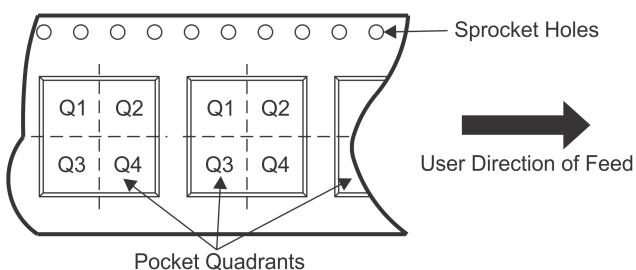


### TAPE DIMENSIONS



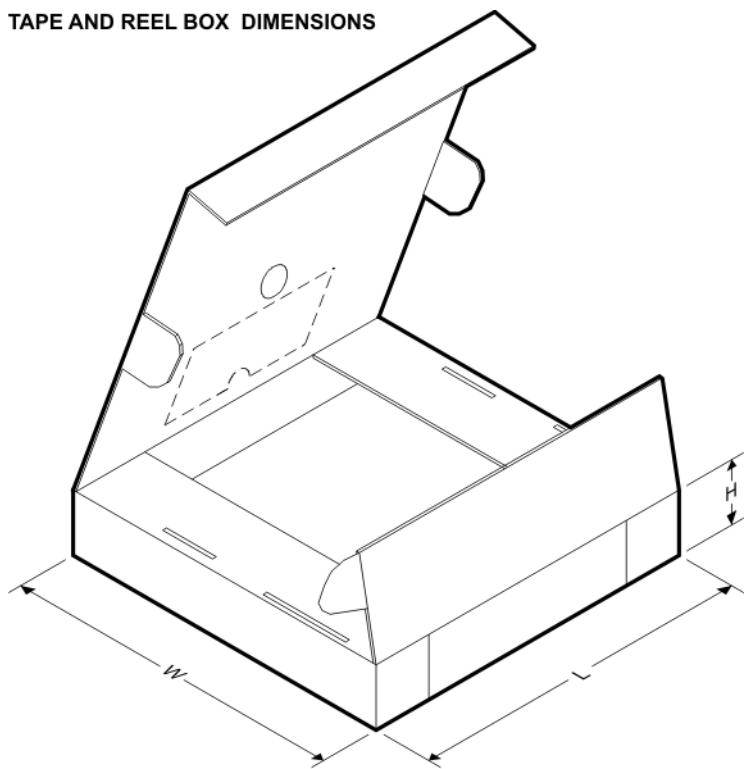
|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS90DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS90NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LS92NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


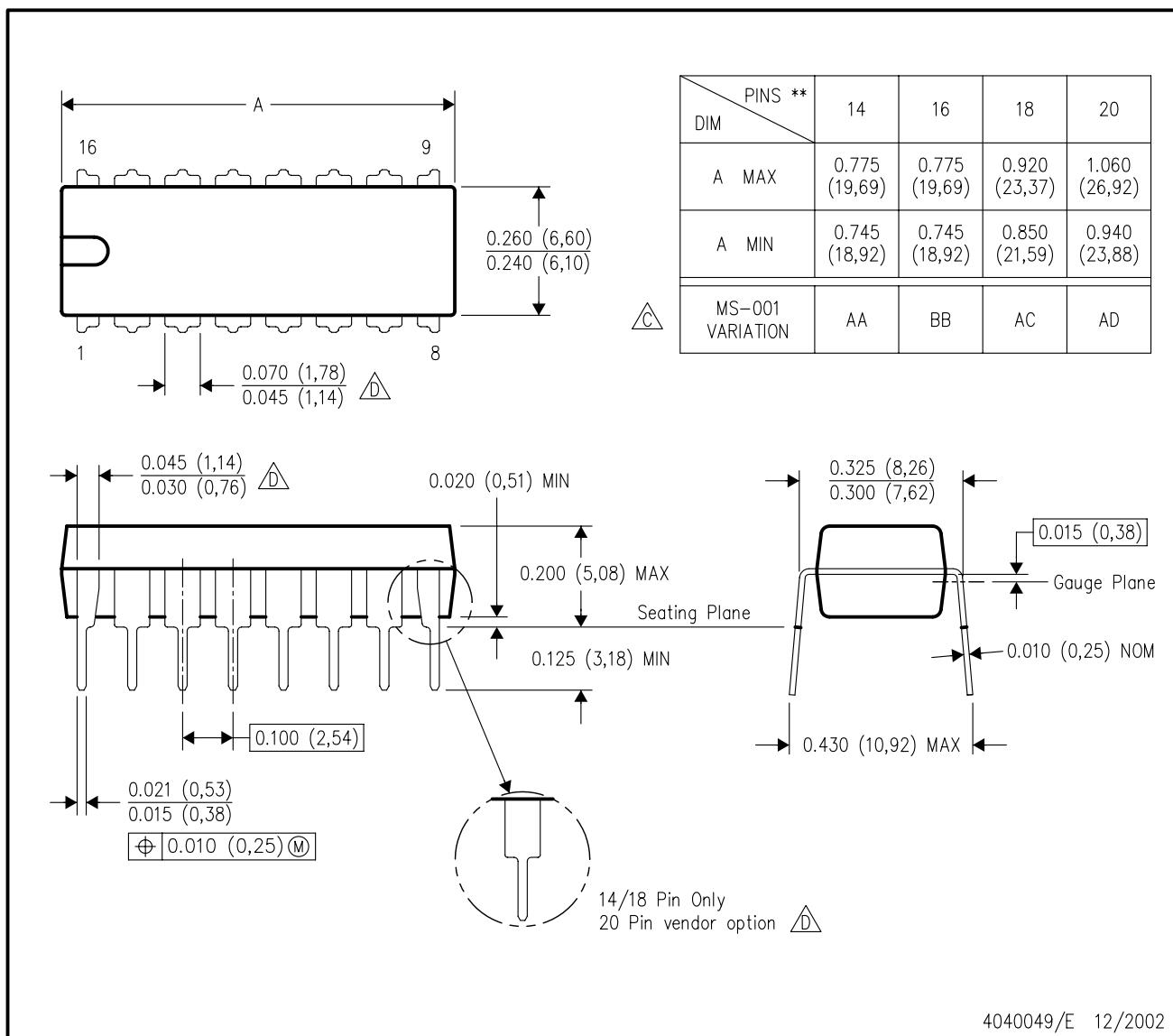
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS90DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LS90NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LS92NSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

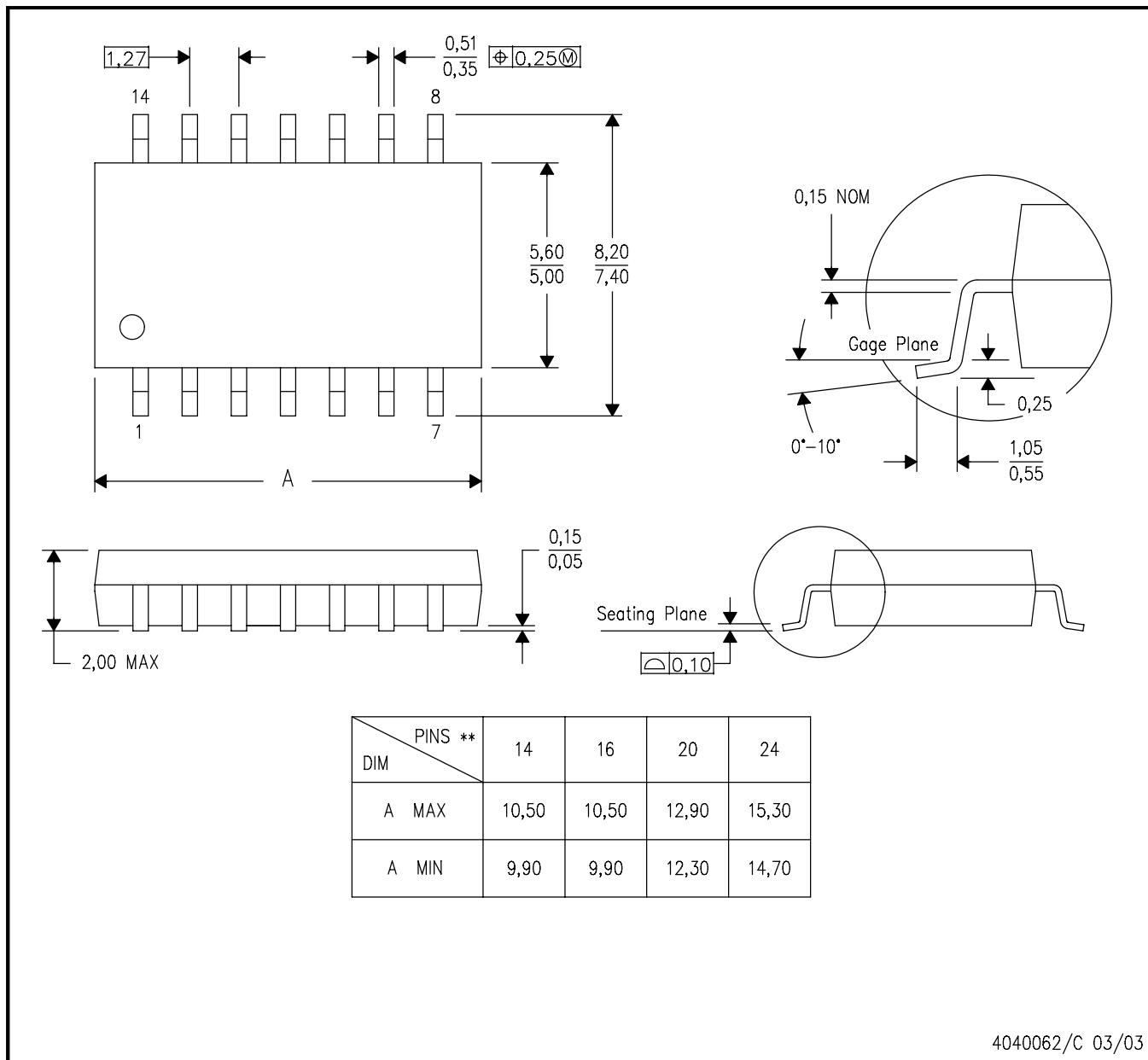
△ D The 20 pin end lead shoulder width is a vendor option, either half or full width.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

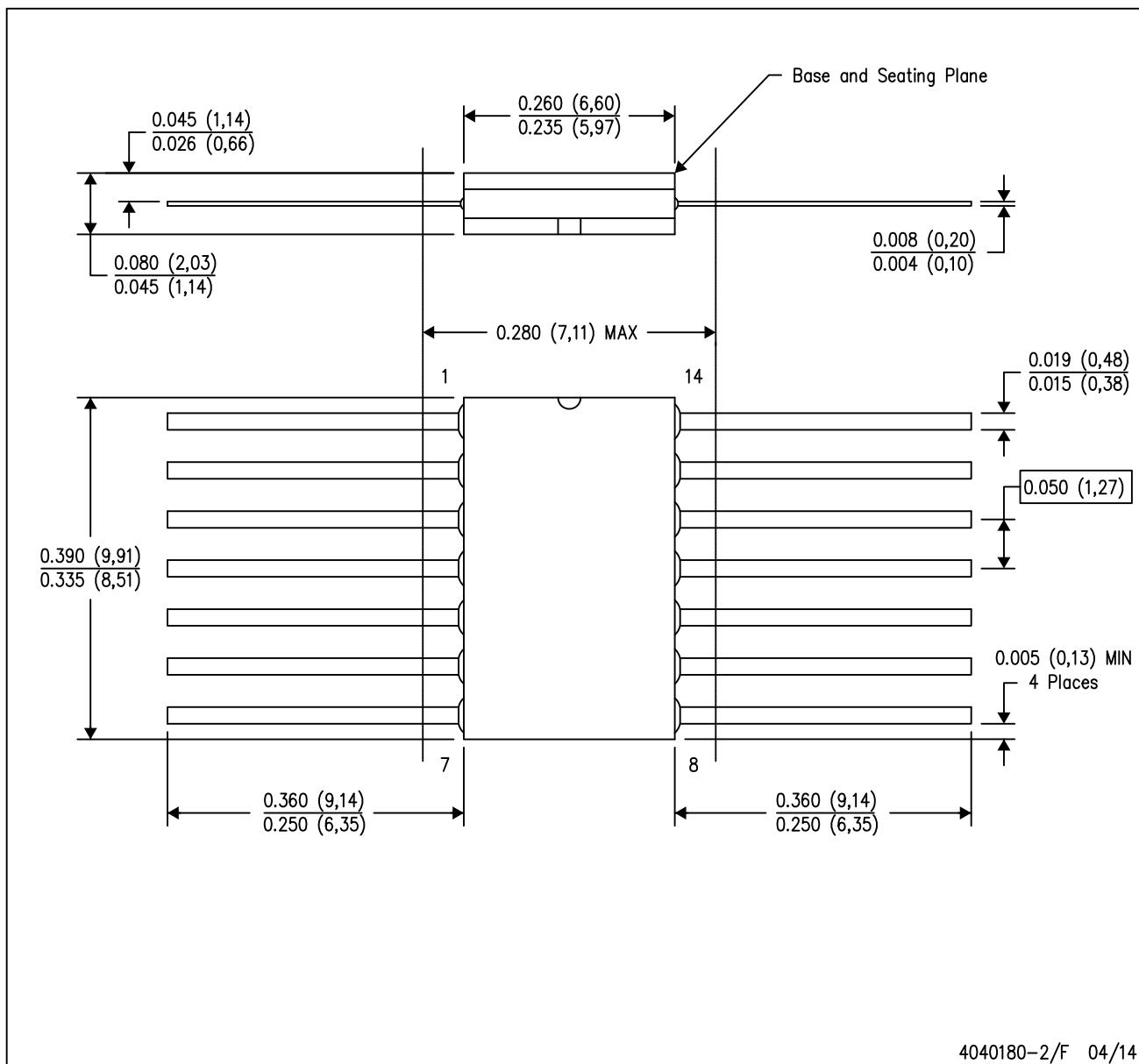


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



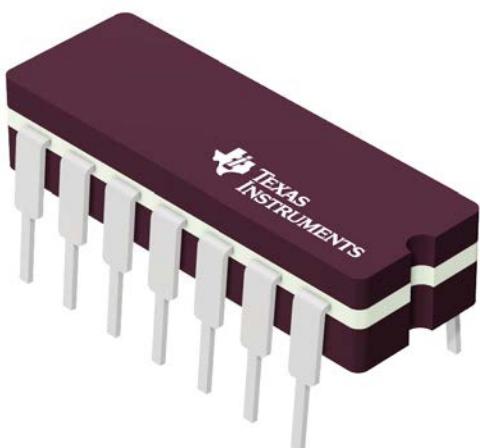
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

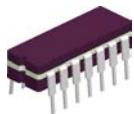
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

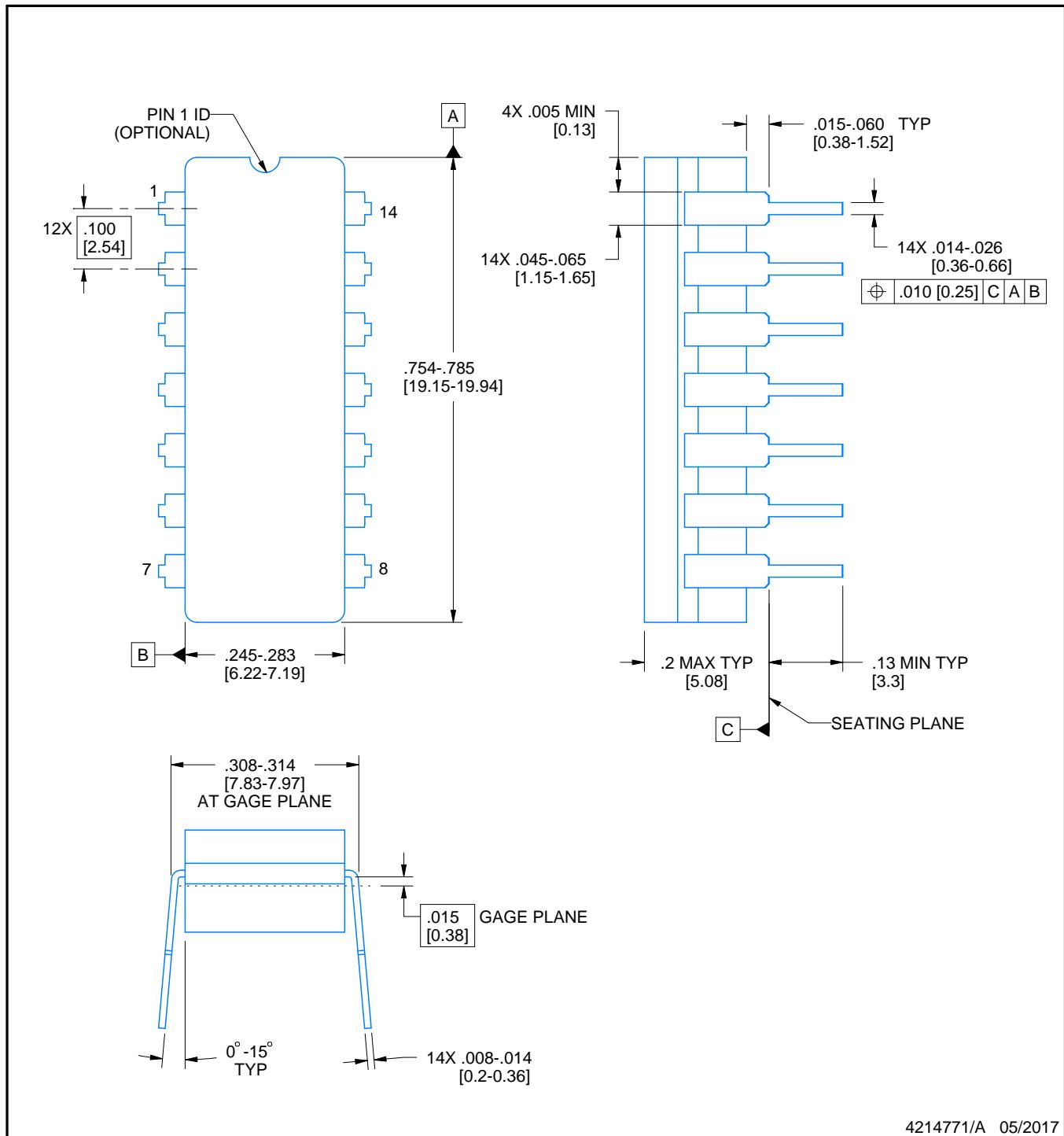
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

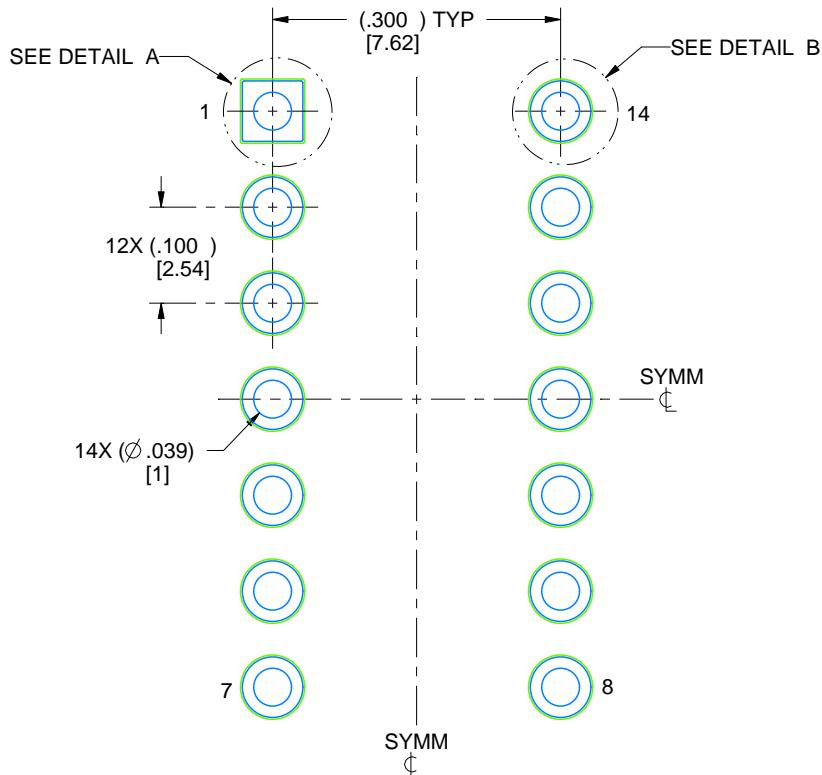
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

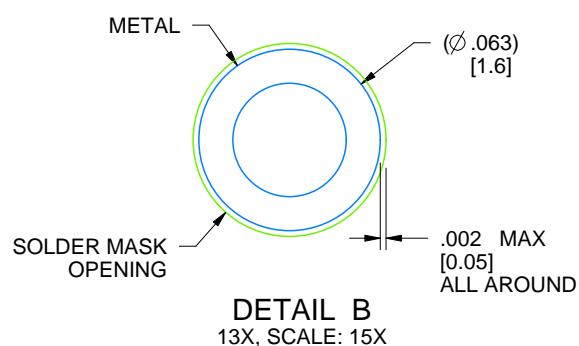
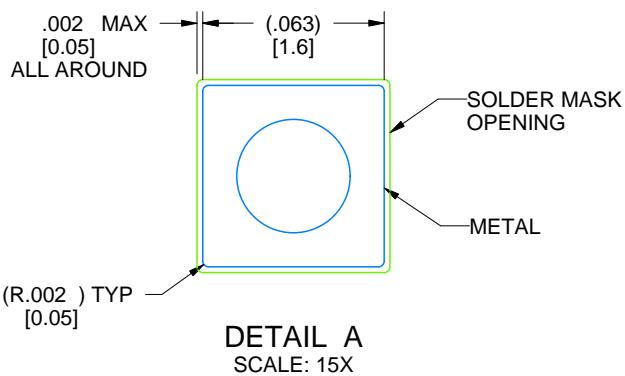
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



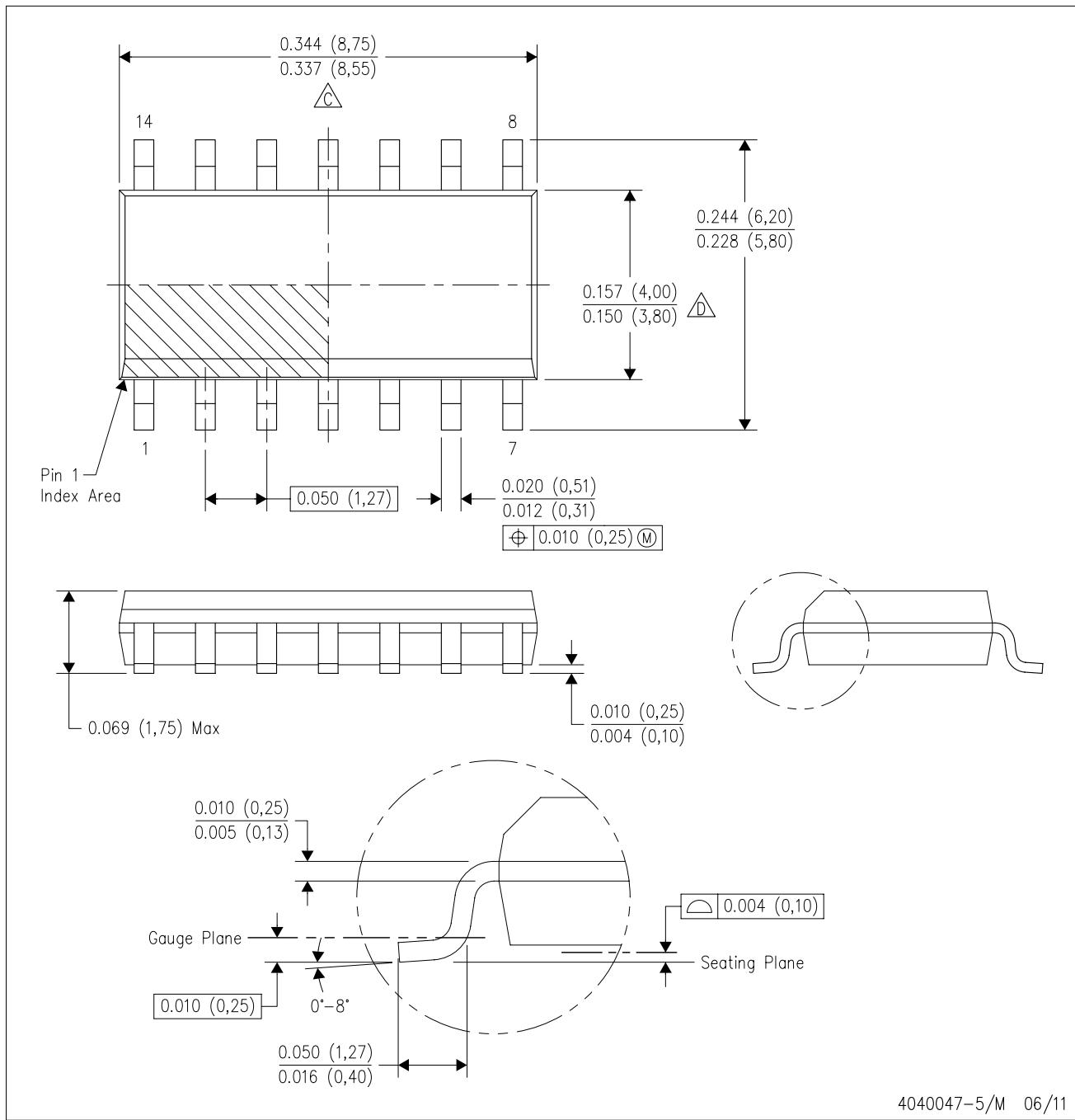
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

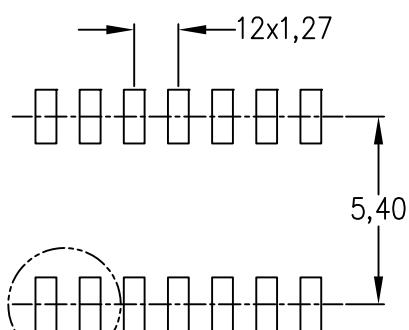
E. Reference JEDEC MS-012 variation AB.

## LAND PATTERN DATA

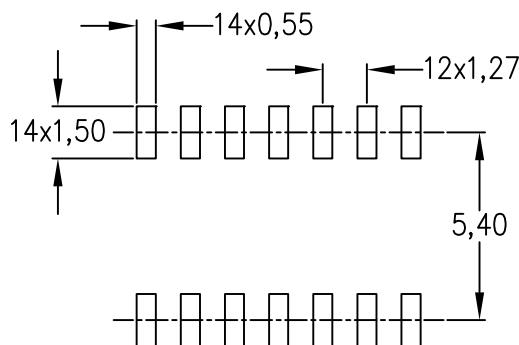
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

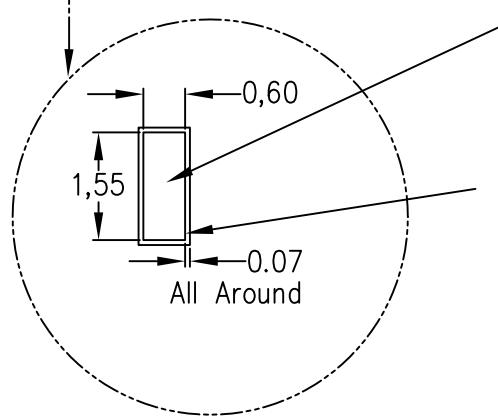
Example Board Layout  
(Note C)



Stencil Openings  
(Note D)



Example  
Non Soldermask Defined Pad



Example  
Pad Geometry  
(See Note C)

Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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