8085 MICROPROCESSOR

1) WHAT IS MICROPROCESSOR AND FUNCTION, MICROCONTROLLER, MICROCOMPUTER, DIGITAL COMPUTER, SSI (SMALL SCALE INTEGRATION), MSI (MEDIUM SCALE INTEGRATION), LSI (LARGE SCALE INTEGRATION), BUS, NIBBLE, WORD, INSTRUCTION, PROGRAM, ASCII, EXTENDED ASCII?

- **MICROPROCESSOR** :- A MICROPROCESSOR IS A MULTIPURPOSE, PROGRAMABLE, CLOCK-DRIVEN REGISTER BASED ELECTRONICS DEVICE THAT READS THE BINARY INSTRUCTIONS FROM A STORAGE DEVICE CALLED MEMORY, ACCEPTS BINARY DATA AS INPUT AND PROCESS DATA ACCORDING TO THOSE INSTRUCTIONS AND PROVIDES RUSULTS AS OUTPUT.
- **MICROCINTROLLER: -** A DEVICE THAT INCLUDES MICROPROCESSOR, MEMORY AND I/O SIGNAL LINES ON A SINGLE CHIP, FABRICATED USING VLSI TECHNOLOGY.
- **MICRO COMPUTER : -** A COMPUTER THAT IS DESIGNED USING A MICROPROCESSOR AS ITS CPU.IT INCLUDES MICROPROCESSOR MEMORY AND I/O.
- **DIGITAL COMPUTER: -** A PROGRAMABLE MACHINES THAT PROCESSES BINARY DATA. IT IS TRADITIONALLY REPRESENT BY FIVE COMPONENTS: CPU, ALU PLUS CONTROL UNIT, MEMORY, INPUT AND OUTPUT.
- **SSI (SMALL SCALE INTEGATION):**- THE PROCESS OF DESINGING A FEW CIRCUIT ON A SINGLE CHIP. THE TURM REFERS TO THE TECHNOLOGY USED TO FABRICATE DISCRETE LOGIC GATES ON A CHIP.
- **MSI (MEDIUM SCALE INTEGRATION):**- THE PROCESS OF DESINGING MORE THAN A HUNDRED GATES ON A SINGLE CHIP.
- **LSI (LARGE SCALE INTEGATION):-** THE PROCESS OF DESIGNING MORE THAN A THOUSAND GATES ON A SINGLE CHIP.SIMILARLY THE TURMS VLSI (VERY LARGE SCALE INTEGRATION) AND SLSI (SUPER LARGE SCALE INTEGRATION) ARE USED TO INDICATE THE SCALE OF INTEGRATION.
- **BUS:** - A GROUP OF LINES USED TO TRANSFER BITS BETWEEN THE MICROPROCESSOR AND OTHER COMPONENT OF THE COMPUTER SYSTEM.
- **NIBBLE: -** A GROUP OF FOUR BITS.
- **WORD:**- A GROUP OF BITS THE COMPUTER RECOGNAZED AND PROCESS AT A TIME
- **INSTRUCTION:** - A COMMAND IN BINARY THAT IS RECOGNISED AND EXECUTE BY THE COMPUTER TO ACCOMPANISED A TASK. SOME INSTUCTION ARE DESIGNED WITH ONE WORD AND SOME REQUIRE MULTIPLE WORD.
- **PROGRAM:**- A SET OF INSTRUCTIONS WRITTEN IN A SPECIFIC SEQUENCE FOR THE COMPUTER TO ACCOMPANISED A GIVEN TASK.
- **ASCII (AMERICAN STANDARD CODE FOR INFORMATION):**- THIS IS A 7 BIT ALPHANUMBERIC CODE WITH 128 COMBINATIONS. EACH COMBINATION IS ASSIGNED EITHER TO A LETTER, DECIMAL DIGIT, SYMBOL OR MACHINE COMMAND.
- **EXTENDED ASCII: -** AN 8 BIT CODE WITH 256 COMBINATIONS. THE ASCII CODE IS EXTENDED FROM SEVEN BITS TO EIGHT BITS TO INCLUDE ADDITIONAL GRAPHIC SYMBOLS.

2) NAME DIFFERENT MICROPROCESSOR OF INTEL WITH THEIR ADDRESS AND DATA BUS?

PROCESSOR	ADDRESS BUS	DATA BUS
8085	16 BITS	8 BITS
8086	20 BITS	16 BITS

3) WHAT ARE LOW LEVEL, MACHINE LANGUAGE, ASSEMBLY LANGUAGE, AND HIGH LEVEL LANGUAGE?

- **LOW LEVEL LANGUAGE:-** A MEDIUM OF COMMUNICATION THAT IS MACHINE DEPEND OR SPECIFIC TO A GIVEN COMPUTER. THE MACHINE AND THE ASSEMBLY LANGUAGES OF A COMPUTER ARE CONSIDERED LOW LEVEL LANGUAGE. PROGRAMME WRITTEN IN THESE LANGUAGES ARE NOT TRANSFERABLE TO DIFFERENT TYPES OF MACHINES.
- **MACHINE LANGUAGE:** - THE BINARY MEDIUM OF COMMUNICATION WITH A COMPUTER THROUGH A DESIGNED SET OF INSTRUCTION SPECIFIC TO EACH COMPUTER.
- **ASSEMBLY LANGUAGE:** - A MEDIUM OF COMMUNICATION WITHA COMPUTER IN WHICH PROGRAMMES ARE WRITTEN IN MNEMONICS. AN ASSEMBLY LANGUAGE IS SPECIFIC TO A GIVEN COMPUTER.
- **HIGH LEVEL LANGUAGE:**- A MEDIUM OF COMMUNICATION THAT IS INDEPENDENT OF A GIVEN COMPUTER . PROGRAMS ARE WRITTEN IN ENGLISH LIKE WORDS, AND THEY CAN BE EXECUTED ONA MACHINE USING A TRANSLATOR (A COMPILER OR AN INTERPRETER).

4) WHAT IS MNEMONICS?

- A COMBINATION OF LETTER TO SUGGEST THE OPERATION OF AN INSTRUCTION.

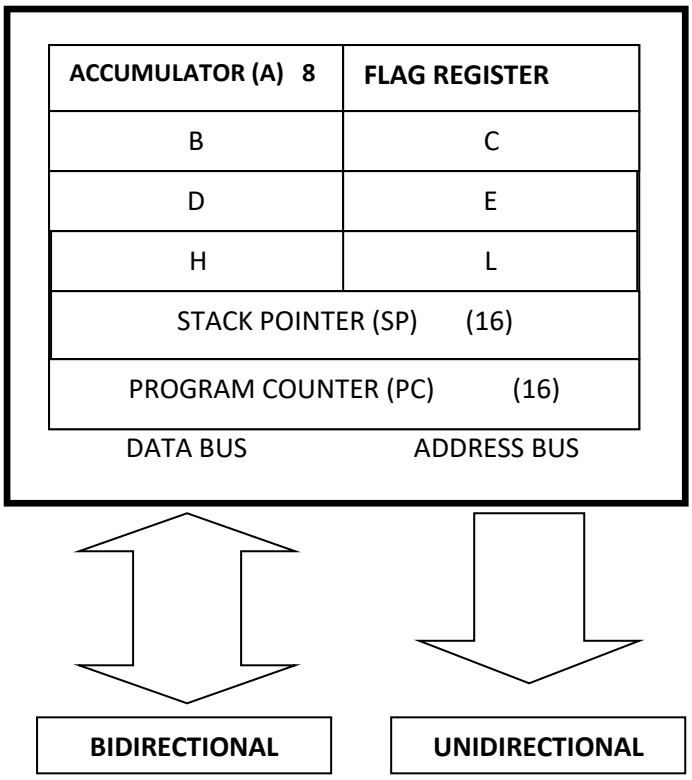
5) WHATS ARE ASSEMBELAR, INTERPRETER AND COMPILER?

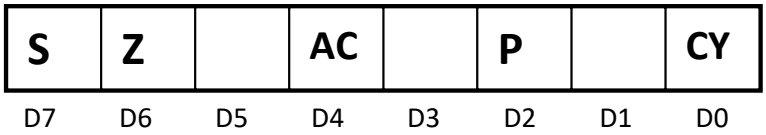
- **ASSEMBLER: -** A COMPUTER PROGRAM THAT TRANSLATES AN ASSEMBLY LANGUAGE PROGRAM FROM MNEMONICS TO THE BINARY MACHINE CODE OF A COMPUTER.

- **INTERPRETER: -** INTERPRETER TAKES THE HIGH LEVEL SOURCE CODES AS AN INPUT AND CONVERTD THIS CODE LINE BY LINE TO THE LOW LEVEL CODE. IT TAKES MORE AMOUNT OF TIME THAN COMPILER BECAUSE ITS CONVERT EACH AN EVERY CODE LINE BY LINE WHEREAS COMPILER CONVERTS ONLY THE SUMMARY OF THE CODE. ADVANTAGE OF USING INTERPRETER IS THAT GENERATES THE SAME VERSION OF THE LOW LEVEL CODE.

- **COMPILER: -** COMPILER IS PROGRAMME WHICH TAKES A HIGH LEVEL LANGUAGE CODE AND THEN CONVERTD IT TO THE LOW LEVEL LANGUAGE AT ASINGLE SHOT. OUTPUT OF DIFFERENT COMPILER WILL MAY VARY FOR THE SAME SOURCE CODE BECAUSE COMPILER ONLY TAKES THE SUMMARY OF THE CODE AND IT THEN CONVERT. DIFFERENT COMPILER MAY PRODUCE DIFFERENT SUMMARY. ADVANTAGE OF COMPILER IS THAT IT TAKES LESS AMOUNT OF TIME FOR CONVERTION.

6) BRIEFLY DISCUSS ABOUT 8085 PROGRAMMING MODEL?





- **REGISTER: -** THE 8085 HAS SIX GENERAL PURPOSE REGISTERS TO STORE 8BIT DATA; THESE ARE IDENTIFIED AS B, C, D, E, H, L AS SHOWN IN THE FIGURE. THEY CAN BE ALSO IDENTIFIED AS REGISTER PAIR BC, DE, and HL TO PERFORM SOME 16 BIT OPERATIONS. THE PROGRAMMERS CAN USE THESE REGISTERS TO STORE OR COPY DATA INTO THE REGISTERS BY UNSING DATA COPY INSTUCTION.
- **ACCUMULATOR:** - THE ACCUMULATOR IS AN 8BIT REGISTER THAT IS PAT OF THE ARITHMETIC/LOGIC UNIT (ALU). THIS RESISTER IS USED TO STORE 8BIT DATA AND TO PERFORM ARITHMETIC AND LOGICAL OPERATIONS. THE RESULT OF AN OPERATION IS STORED IN THE ACCUMULATOR. THE ACCUMULATOR IS ALSO IDENITIFIED AS REGISTER (A).
- **FLAGS:** - 1) Z (ZERO):- THE ZERO FLAG IS SET TO 1 WHEN THE RESULT IS ZERO. OTHERWISE IT IS RESET.
  2) CY (CARRY):- IF AN ARITHMETIC OPERATION RESULT IN A CARRY, THE CY FLAG IS SET OTHERWISE IT IS RESERT.
  3) S (SIGN):- THE SIGN FLAG IS SET IF BIT D7 OF THE RESULT =1, OTHERWISE IT IS RESET.
  4) P (PARITY):- IF THE RESULT HAS AN EVEN NUMBER OF 1S, THE FLAG IS SET FOR AN ODD NUMBER OF 1S THE FLAG IS RESET.
  5) AC (AUXILARY CARRY):- IN AN ARITHMETIC OPERATION, WHEN A CARRY IS GENERATED BY DIGIT D3 AND PASSED TO D4, THE AC FLAG IS SET. RHIS FLAG IS USED INTERNALLY FOR BCD OPERATION. THERE IS NO JUMP INSTRUCTION ASSOCIATED WITH THIS FIAG.

- THE MICROPROCESSOR USES THE PC REGISTER TO SEQUENCE THE EXECITION OF THE INSTRUCTIONS. THE FUNCTION OF THE PROGRAM COUNTER IS TO POINT TO THE MEMORY ADDRESS FROM WHICH THE NEXT BYTE IS TOBE FETCHED. WHEN A BYTE IS BEING FETCHED, THE PROGRAM COUNTER IS INCREMENTED BY ONE TO POINT TO THE NEXT MEMORY LOCATION.
- THE STACK POINTER IS ALSO A 16BIT REGISTER UESD AS A MEMORY POINTER. IT POINTS TO A MEMORY LOCATION IN R/W MEMORY, CALLED THE STACK.THE BEGINNING OF THE STACK IS DEFINED BY LOADING A 16BIT ADDRESS IN THE STACK POINTER.

7) BRIEFLY DISCUSS ABOUT DIFFERENT FLAGS PRESENT IN 8085 MICROPROCESSOR?

- **FLAGS:** - 1) Z (ZERO):- THE ZERO FLAG IS SET TO 1 WHEN THE RESULT IS ZERO. OTHERWISE IT IS RESET.
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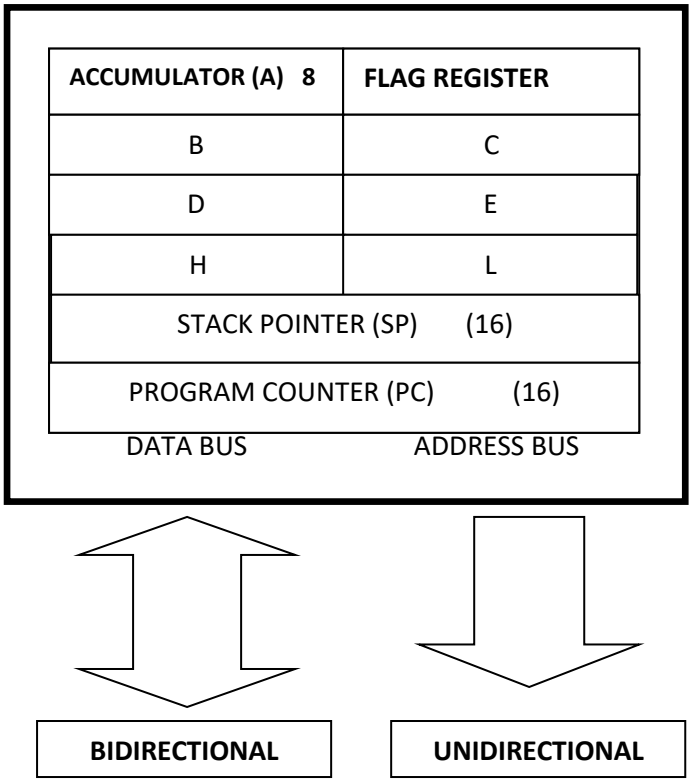
8) WHY DATA BUS IS BUDIRECTIONAL BUT ADDRESS BUS IS UNIDIRECTIONAL?



THE DATA BUS IS A GROUP OF EIGHT LINES UESD FOR DATA FLOW. THESE LINES ARE BIDIRECTIONAL DATA FLOW IN BOTH DIRECTIONS BETWEEN THE MPU AND MEMORY AND PERIPHERAL DEVICES. THE MPU USES THE DATA BUS TO PERFORM THE SECOND FUNCTION; TRANSFERRING BINARY INFORMATION.

THE ADDRESS BUS IS A GROUP OF 16 LINES GRNERALLY IDENTIFIED AS A0 TO A15. THE ADDRESS BUS IS UNIDIRECTIONAL; BITS FLOW IN ONE DIRECTION FROM THE MPU TO PERIPHERAL DEVICES.THE MPU USES THE ADDRESS BUS TO PERFROM THE FIRST FUNCTION; IDENIFING A PERIPHERAL OR A MEMORY LOCATION.

9) WHAT IS THE FUCTION OF ACCUMULATOR?

- **ACCUMULATOR:** - THE ACCUMULATOR IS AN 8BIT REGISTER THAT IS PAT OF THE ARITHMETIC/LOGIC UNIT (ALU). THIS RESISTER IS USED TO STORE 8BIT DATA AND TO PERFORM ARITHMETIC AND LOGICAL OPERATIONS. THE RESULT OF AN OPERATION IS STORED IN THE ACCUMULATOR. THE ACCUMULATOR IS ALSO IDENITIFIED AS REGISTER (A).

10) WRITE THE FUCTION OF PC (PROGRAM COUNTER) AND SP (STACK POINTER) IN 8085 MICROPROCESSOR?

- THE MICROPROCESSOR USES THE PC REGISTER TO SEQUENCE THE EXECITION OF THE INSTRUCTIONS. THE FUNCTION OF THE PROGRAM COUNTER IS TO POINT TO THE MEMORY ADDRESS FROM WHICH THE NEXT BYTE IS TOBE FETCHED. WHEN A BYTE IS BEING FETCHED, THE PROGRAM COUNTER IS INCREMENTED BY ONE TO POINT TO THE NEXT MEMORY LOCATION.
- THE STACK POINTER IS ALSO A 16BIT REGISTER UESD AS A MEMORY POINTER. IT POINTS TO A MEMORY LOCATION IN R/W MEMORY, CALLED THE STACK.THE BEGINNING OF THE STACK IS DEFINED BY LOADING A 16BIT ADDRESS IN THE STACK POINTER.

11) WHY SP AND PC ARE 16BIT REGISTERS IN LENGTH?

- THE MICROPROCESSOR USES THE PC REGISTER TO SEQUENCE THE EXECITION OF THE INSTRUCTIONS. THE FUNCTION OF THE PROGRAM COUNTER IS TO POINT TO THE MEMORY ADDRESS FROM WHICH THE NEXT BYTE IS TOBE FETCHED. WHEN A BYTE IS BEING FETCHED, THE PROGRAM COUNTER IS INCREMENTED BY ONE TO POINT TO THE NEXT MEMORY LOCATION.
- THE STACK POINTER IS ALSO A 16BIT REGISTER UESD AS A MEMORY POINTER. IT POINTS TO A MEMORY LOCATION IN R/W MEMORY, CALLED THE STACK.THE BEGINNING OF THE STACK IS DEFINED BY LOADING A 16BIT ADDRESS IN THE STACK POINTER.

12) IF THE 8085 HAS FETCH THE MACHINE CODE LOCATED AT 207F H. SPECIFY THE MACHINE CODE LOCATED AT 207F H. SPECIFY THE CONTENT OF PROGRAM COUNTER?

- **2080H**

13) WHILE EXECUTING A PROGRAM WHEN THE 8085 MICROPROCESSOR COMPLETES THE FETCHING OF THE MACHINE CODE LOCATED AT THE MEMORY ADDRESS 2057H, WHAT IS THE CINTENT OF THE PROGRAM COUNTER?

- 2058H.

14) IF THE 8085 MICROPROCESSOR HAS FETCHED THE MEMORY MACHINE CODE LOCATED AT MEMOMY LOCATION 207FH, SPECIFY THE CONTENT OF PC?

- 2080H.

15) SPECIFY THE CONTROL SIGNAL AND THE DIRECTION OF THE DATA FLOW ON THE DATA BUS IN A MEMORY WRITE OPERATION?

$\overline{\text{MEMW}}$

16) WHAT ARE THE CONTROL SIGNALS REQIRED FOR MEMORY OPERATIONS (READ AND WRITE)?

$\overline{\text{RD}}$, $\overline{\text{WR}}$

17) HOW MANY FLAG ARE PRESENT IN 8085 MICROPROCESSOR?

18) **FLAGS:** - 1) Z (ZERO):- THE ZERO FLAG IS SET TO 1 WHEN THE RESULT IS ZERO. OTHERWISE IT IS RESET.
2) CY (CARRY):- IF AN ARITHMETIC OPERATION RESULT IN A CARRY, THE CY FLAG IS SET OTHERWISE IT IS RESERT.
3) S (SIGN):- THE SIGN FLAG IS SET IF BIT D7 OF THE RESULT =1, OTHERWISE IT IS RESET.
4) P (PARITY):- IF THE RESULT HAS AN EVEN NUMBER OF 1S, THE FLAG IS SET FOR AN ODD NUMBER OF 1S THE FLAG IS RESET.

5) AC (AUXILARY CARRY):- IN AN ARITHMETIC OPERATION, WHEN A CARRY IS GENERATED BY DIGIT D3 AND PASSED TO D4, THE AC FLAG IS SET. RHIS FLAG IS USED INTERNALLY FOR BCD OPERATION. THERE IS NO JUMP INSTRUCTION ASSOCIATED WITH THIS FIAG.

19) DISCUSS ABOUT DIFFERENT INSTRUCTION SET OF 8085 MICROPROCESSOR?

- THESE GROUP OF INSTRUCTIONS COPIES DATA FROM A LOCATION CALLED A SOURCE TO ANOTHER LOCATION CALLED DESTINATION WITHOUT MODIFING THE CINTENTS OF THE SOURCE. IN TECNICAL MANUALS, THE TERM DATA TRANSFER IS USED FOR THIS CPOYING FUNCTION.

TYPES	EXAMPLE
BETWEEN REGISTERS	COPY THE CONTENTS OF REGISTER B INTO REGISTER D
SPECIFIC DATA BYTE TO A REGISTER OR A MEMORY LOCATION	LOAD REGISTER B WITH THE DATA BYTE 32H
BETWEEN A MEMORY LOCATION AND A REGISTER	FROM THE MEMORY LOCATION 2000H TO REGISTER B
BETWEEN AN I/O DEVICE AND THE ACCUMULATOR	FROM AN INPUT KEYBOARD TO THE ACCUMULATOR

- ARITHMETIC OPERATION:-

1. ADDITION: - ANY 8 BIT NUMBER OR THE CONTENTS OF A REGISTER OR THE CONTENTS OF A MEMORY LOCATION CAN BE ADDED TO THE CONTENTS OF THE ACCUMULATOR AND THE SUM IS STORE IN THE ACCUMULATOR.THE INSTUCTION DAD IS AN EXCEPTION; IT ADDS 16 BIT DATA DIRECTLY IN REGISTER PAIRS.
2. SUBTRACTION:- ANY 8BIT NUMBER OR THE CONTENT OF A REGISTER, OR THE CONTENT OF A MEMORY LOCATION CAN BE SUBTRACT FROM THE CONTENTS OF THE ACCUMULATOR AND THE RESULTS STORE IN THE ACCUMULATOR.
3. INCREMENT/DECREMENT: - THE 8 BIT CANTENTS OF A REGISTER OR A MEMORY LOCATION CAN BE INCREMENTED OR DECREMENTED BY 1.

- LOGICAL OPERATION:-

1. AND, OR, EXVLUSIVE OR: - ANY 8BIT NUMBER OR THE CONTENT OF A REGISTER OR OF A MEMORY LOCATION CAN BE LOGICALLY ANDED, ORED OR EXCLUSIVE ORED WITH THE CONTENTS OF THE ACCUMULATOR. THE RESULT IS STORED IN THE ACCUMULATOR.
2. ROTATE: - EACH BIT IN THE ACCUMULATOR CAN BE SHIEFTED EITHER LEFT OR RIGHT TO THE NEXT POSITION.
3. COMPARE: - ANY 8 BIT NUMBER OR THE CONTENTS OF A REGISTER OR A MEMORY LOCATION CAN BE COMPARED FOR EQULITY GREATERTHAN, OR LESSTHAN WITH THE CONTENTS OF THE ACCUMULATOR.
4. COMPLEMENT: - THE CONTENTS OF THE ACCUMULATOR CAN BE COMPLIMENTD ALL 0S ARE REPLACE BY 1S AND ALL 1S ARE REPLACE BY 0S.

- BRANCHING OPERATIONS:-

1. JUMP: - CONDITIONAL JUMPS ARE AN IMPORTANT ASPECT OF THE DECITION MAKING PROCESS IN PROGRAMMING. THESE INSTUCTIONS TEST FOR A CERTAIN CONDITION AND ALTER THE PROGRAM SEQUENCE WHEN THE CONDITION IS MET. IN ADDITION THE INSTUCTION SET INCLUDES AN INSTUCTION CALLED UNCONDITIONAL JUMP.
2. CALL, RETURN AND RESTART: - THESE INSTUCTIONS CHANGE THE SEQUENCE OF A PROGRAM EITHER BY CALLING A SUBROUTINE OR RUTURNING FROM A SUBROUTINE. THE CONDITIONAL CALL AND RETURN INSTUCTIONS ALSO CAN TEST CONDITION FLAG.

- MACHINE CINTROL OPERATION:- THESE INSTUCTION CONTROL MACHINE FUNCTIONS SUCH AS HALT, INTERRUPT OR DO NOTHING

20)DISCUSS DIFFERENT TYPE OF DATA TRANSFER (MOVEMENT) INSTRCTIONS PRESENT IN 8085?

TYPES	EXAMPLE
BETWEEN REGISTERS	COPY THE CONTENTS OF REGISTER B INTO REGISTER D
SPECIFIC DATA BYTE TO A REGISTER OR A MEMORY LOCATION	LOAD REGISTER B WITH THE DATA BYTE 32H
BETWEEN A MEMORY LOCATION AND A REGISTER	FROM THE MEMORY LOCATION 2000H TO REGISTER B
BETWEEN AN I/O DEVICE AND THE ACCUMULATOR	FROM AN INPUT KEYBOARD TO THE ACCUMULATOR

21) DISCUSS DIFFERENT ARITHMETIC INSTUCTIONS FORMAT IN 8085?

- ARITHMETIC OPERATION:-

1) ADDITION: - ANY 8 BIT NUMBER OR THE CONTENTS OF A REGISTER OR THE CONTENTS OF A MEMORY LOCATION CAN BE ADDED TO THE CONTENTS OF THE ACCUMULATOR AND THE SUM IS STORE IN THE ACCUMULATOR.THE INSTUCTION DAD IS AN EXCEPTION; IT ADDS 16 BIT DATA DIRECTLY IN REGISTER PAIRS.
2) SUBTRACTION:- ANY 8BIT NUMBER OR THE CONTENT OF A REGISTER, OR THE CONTENT OF A MEMORY LOCATION CAN BE SUBTRACT FROM THE CONTENTS OF THE ACCUMULATOR AND THE RESULTS STORE IN THE ACCUMULATOR.
3) INCREMENT/DECREMENT: - THE 8 BIT CANTENTS OF A REGISTER OR A MEMORY LOCATION CAN BE INCREMENTED OR DECREMENTED BY 1.

22) EXPLAIN DIFFERENT BRANCHING INTUCTON OF 8085?

- BRANCHING OPERATIONS:-
  1) JUMP: - CONDITIONAL JUMPS ARE AN IMPORTANT ASPECT OF THE DECITION MAKING PROCESS IN PROGRAMMING. THESE INSTUCTIONS TEST FOR A CERTAIN CONDITION AND ALTER THE PROGRAM SEQUENCE WHEN THE CONDITION IS MET. IN ADDITION THE INSTUCTION SET INCLUDES AN INSTUCTION CALLED UNCONDITIONAL JUMP.
  2) CALL, RETURN AND RESTART: - THESE INSTUCTIONS CHANGE THE SEQUENCE OF A PROGRAM EITHER BY CALLING A SUBROUTINE OR RUTURNING FROM A SUBROUTINE. THE CONDITIONAL CALL AND RETURN INSTUCTIONS ALSO CAN TEST CONDITION FLAG.

23) DISCUSS ABOUT DIFFERENT INSTRUCTION FORMAT IN 8085?

- AN INSTRUCTION IS A COMMAND TO THE MICROPROCESSOR TO PERFROM A GIVEN TASK ON SPECIFIED DATA. EACH INSTRUCTION HAS TWO PARTS; ONE IS THE TASK TO BE PERFROMED, CALLED THE OPWRATION CODE(OP CODE) AND THE SECOND IS THE DATA TO BE OPERATED ON CLLED THE OPERAND. THE OPERAND CAN BE SPECIFIED IN VARIOUS WAYS.
- 1BYTE INSTRUCTION:-

TASK	OPCODE	OPERAND	BINARY CODE	HEX CODE
1) COPY THE CONTENTS OF THE ACCUMULATOR IN REGISTER C	MOV	C,A	0100 1111	4F H

2) ADD THE CONTENTS OF REGISTER B TO THE CONTENT OF THE ACCUMULATOR	ADD	B	1000 0000	80 H

- 2 BYTE INSTRUCTION:-

TASK	OPCODE	OPERAND	BINARY CODE	HEX CODE
LOAD 8 BIT DATA BYTE IN THE ACCUMULATOR	MVI	A, 32 H	0011 1110 0011 0010	3E 32
LOAD AN 8BIT DATA BYTE IN REGISTER B	MVI	B, F2 H	0000 0110 1111 0010	06 F2

- 3 BYTE INSTRUCTION:-

TASK	OPCODE	OPERAND	BINARY CODE	HEX CODE
LOAD CONTENTS 2050H INTO A	LDA	2050 H	0011 1010 0101 0000 0010 0000	3A 50 20

24) HOW DOES A MICROPROCESSOR DIFFERENTIATE BETWEEN DATA AND INSTRUCTION CODE?

- THE ANSWER LIES IN THE FACT THAT THE MICROPROCESSOR INTERPRETS THE FIRST BYTE IT FETCHES AS AN OPCODE. WHEN THE 8085 IS RESET, ITS PROGRAM COUNTER IS CLEARED TO 0000H AND IT FETCHES THE FIRST CODE FROM THE LOCATION 0000H. IF WE TELL THE PROCESSOR THAT OUR PROGRAM BEGINS AT LOCATION 2000H. THE FIRST CODE IT FETCHES IS 3EH. WHEN IT DECODE THAT CODE, IT KNOWNS ASSUME THAT THE SECOND CODE 32H, IS A DATA BYTE. IF WE FORGET TO ENTER 32H AND ENTER THE NEXT CODE, 06H, INSTEAD, THE 8085 WILL LOA 06H IN THE ACCUMULATOR, INTERPRET THE NEXT CODE, 48H, AS AN OPCODE AND CONTINUE THE EXECUTION IN SEQUENCE.

25) WHITE DOWN THE BASIC OPERARIONS OF 8085(LIST THE FOUR OPERATIONS COMMONLY PERFROMED BY THE MPU/SPECIFIC THE FOUR CONTROL SIGNALS COMMONLY USED BY 8085).

1) MEMORY READ: READS DATA (OR INSTRUCTIONS) FROM MEMORY
2) MEMORY WRITE: WRITES DATA (OR INSTRUCTIONS) INTO MEMORY
3) I/O READ: ACCEPTS DATA FROM INPUT DEVICES
4) I/O WRITE: SENDS DATA TO OUTPUT DEVICES.

26) BRIEFLY DISCUSS ABOUT ADDRESS, DATA AND CONTROL BUS OF 8085.

- ADDRESS BUS: - THE ADDRESS BUS IS A GROUP OF 16 LINES GRNERALLY IDENTIFIED AS A0 TO A15. THE ADDRESS BUS IS UNIDIRECTIONAL; BITS FLOW IN ONE DIRECTION FROM THE MPU TO PERIPHERAL DEVICES.THE MPU USES THE ADDRESS BUS TO PERFROM THE FIRST FUNCTION; IDENIFING A PERIPHERAL OR A MEMORY LOCATION.
- DATA BUS:- THE DATA BUS IS A GROUP OF EIGHT LINES UESD FOR DATA FLOW. THESE LINES ARE BIDIRECTIONAL DATA FLOW IN BOTH DIRECTIONS BETWEEN THE MPU AND MEMORY AND PERIPHERAL DEVICES. THE MPU USES THE DATA BUS TO PERFORM THE SECOND FUNCTION; TRANSFERRING BINARY INFORMATION.

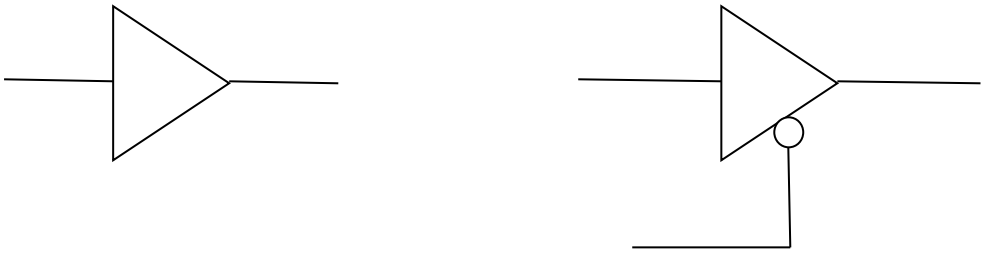
- CONTROL BUS:- THE CONTROL BUS IS COMPRISED OF VARIOUS SINGLE LINES THAT CARRY SYNVHRONIZATION SIGNALS. THE MPU USES SUCH LINES TO PERFROM THE THIRD FUNCTION; PROVIDING TIMING SIGNALS.

THE TERM BUS IN RELATION TO THE CONTROL SIGNALS , IS

SOME WHAT CONFUSING .THESE ARE NOT GROUP OF LINES LIKE ADDRESS AND DATA BUSES, BUT INDIVISUAL INLES THAT PROVODE A PULSE TO INDICATE AN MPU OPERATION.

27) DISCUSS ABOUT TRISTATE BUFFER OR DEVICE?

- THE TURM TRI STATE IS A TRADEMARK OF NATIONAL SEMICONDUCTOR AND IS USED TO REPRESENT THREE LOGIC SATES. A TRI STATE LOGIC DEVICE HAS A THIRD LINE CALLED ENABLE. WHEN THIS LINE IS ACTIVATED, THE TRI STATE DEVICE FUNCTIONS THE SAME WAY AS ODINARY LOGIC DEVICES. WHEN THE THIRD LINE IS DISABLED, THE LOGIC DEVICE GOES INTO THE HIGH IMPEDENCE STATE – AS IF IT WERE DISCONNECTED FROM THE SYSTEM.



28) CALCULATE THE NUMBER OF MEMORY CHIPS NEEDED TO DESIGN 8K BYTE MEMORY IF THE MEMORY CHIP SIZE IS 1024X1.

- THE CHIP 1024 X 1 HAS 1024(AK) REGISTERS AND EACH REGISTER CAN STORE ONE BIT WITH ONE DATA LINE. WE NEED EIGHT DATA LINES FOR BYTE SIZE MEMORY. THEREFORE, EIGHT CHIPS ARE NECESSARY FOR 1K BYTE MEMORY. FOR 8K BYTE MEMORY, WE WILL NEED 64 CHIPS. WE CAN ARRIVE AT THE SAME ANSWER BY DIVIDING 8K BYTE BY 1K X 1 AS FOLLOWS

8192 X 8 / 1024 X 1 = 64

29) HOW MANY MEMORY LOCATIONS CAN BE ADDRESSED BY 8085 MICROPROCESSOR?

2^{16} ----→ 65536 = 64K.

30) HOW MANY MEMORY LOCATIONS CAN BE ADDRESS BY A MICROPROCESSOR WITH 14 ADDRESS LINE?

2^{14} = 16384

31) HOW MANY ADDRESS LINES ARE NEEDED TO ADDRESS 2MB (2048 BYTE) OF MEMORY?

2 MB (2048 BYTES) -> 2048K

2^{11} $2^{10} = 2^{21}$

SO 11 NO . OF ADDRESS BUS.

32) WRITE THR DIFFERENT BETWEEN SRAM (STATIC RAM) ABD DRAMS (DYNAMIC RAM)?

- STATIC MEMORY (SRAM):- THIS MEMORY MADE OF FLIP FLOPS AND IT STORES THE BIT AS A VOLTAGE. EACH MEMORY CELL REQUIRES SIX TRANSISTORS; THEREFORE THE MEMORY CHIP HAS LOW DENSITY BUT HIGH SPEED. THIS MEMORY IS MORE EXPENSIVE AND CONSUMES MORE POWER THAN DYNAMIC MEMORY. IN HIGH SPEED PROCESSOR (SUCH AS INTEL 486 AND PENTIUM) , SRAM KNOWN AS CACHE MEMORY IS INCLUDED ON THE PROCESSOR CHIP. IN ADDITION HIGH SPEED CACHE MEMORY IS ALSO INCLUDED EXTERNAL TO THE PROCESSOR TO IMPROVE THE PERFORMANCE OF A SYSTEM.
- DYNAMIC MEMORY: - THIS MEMORY IS MADE UP OF MOS (METAL OXIDE SEMICONDUCTOR) TRANSISTOR GATES AND IT STORES THE BIT AS A CHAREGE. THE ADVANTAGE OF DYNAMIC MEMORY ATE THAT IT HAS HIGH DENSITY AND LOW POWER CONSUMPTION AND IS CHEAPER THAN STATIC MEMORY. THE DISADVANTAGES IS THAT THE CHARGE (BIT INFORMATION) LEAKS; THEREFORE STORED INFORMATION NEEDS TO BE READ AND WRITTEN AGAIN EVERY FEW MILLISECONDS. THIS IS CALLED REFRESHING THE MEMORY, AND IT REQUIRES EXTRA CIRCUITRY, ADDING TO THE COST OF THE SYSTEM.

33) DEFINE MASKED ROM, PROM, EPROM, EE-PROM, FLASH MEMORY.

- MASKED ROM: - IN THIS ROM, A BIT PATTERN IS PERMANENTLY RECORDED BY THE MASKING AND METALIZATION PROCESS. MEMORY MANUFACTURERS ARE GENERALLY EQUIPPED TO DO THIS RPCESS. IT IS AN EXPENSIVE AND SPECIALIZED PROCESS BUT ECONOMICAL FOR LARGE PRODUCTION QUANTITIES.
- PROM (PROGRAMMABLE READ ONLY MEMORY):- THIS MEMORY HAS NICROME OR POLYSILICON WIRES ARRANGED IN A MATRIX; THESE WIRE CAN BE FUNCTIONALLY VIEWED AS DIODES OR FUSES. THIS MEMORY CAN BE PROGRAMMED BY THE USER WITH A SPECIAL PROM PROGRAMMER THAT SELECTIVELY BURNS THE FUSES ACCORDING TO THE BIT PATTERN TO BE STORED. THE PROCESS IS KNOWN AS “BURNING THE PROM”. AND THE INFORMATION STORED IS PERMANENT.
- EP ROM (ERASEABLE PROGRAMMABLE READ ONLY MEMORY):- THIS MEMORY STORES A BIT BY CHARGING THE FLOTING GATE OF AN FW. INFORMATION IS STORED BY USING AN EPROM PROGRAMMER, WHICH APPLIES HIGH VOLTAGE TO CHARGE THE GATE. ALL THE INFORMATION CAN BE ERASED BY EXPOSING THE CHIP TO ULTRAVIOLET LIGHT THROUGH ITS QUARTZ WINDOW, AND THE CHIP CAN BE REPROMMED. BECAUSE THE CHIP CAN BE REUSED MANY TIMES, THIS MEMORY IS IDEALLY SUITED FOR PRODUCT DEVELOPMENT, EXPERIMENTAL PROJECTS AND COLLEGE LABORA TORIES. THE DISADVANTAGE OF EPROM ARE –
  I) IT MUST BE TAKEN OUT OF THE CIRCUIT TO ERASE IT.
  II) THE ENTIRE CHIP MUST BE ERASED
  III) THE ERASING PROCESS TAKES 15 TO 20 MINITUS.

- EE PROM(ELECTRICALLY ERASABLE PROM):- THIS MEMORY IS FUNCTIONALLY SIMILAR TO EPROM, EXCEPT THAT INFORMATION CAN BE ALTERED BY USING ELECTRICAL SIGNALS AT THE REGISTER LEVEL RATHER THAN ERASING ALL THE INFORMATION. THIS HAS AN ADVANTAGE IN FIELD AND REOMOTE CONTROL APPLICATIONS. IN MICROPROCESSOR SYSTEM, SOFTWARE UPDATE IS COMMON OCCURRENCE. IF EE-PROMS ARE UESD IN THE SYSTEM, THEY CAN BE UPDATED FROM A CENTRAL COMPUTER BY USING A REMOTE LINK VIA TELEPHONE LINES. SIMILARLY IN A PROCESS CONTROL WHERE TIMING INFORMATION NEEDS TO BE CHANGED IT CAN BE CHANGED BY SENDING ELECTRICAL SIGNALS FROM A CENTRAL PLACE. THIS MEMORY ALSO INCLUDES A CHIP ERASE MODE WHEREBY THE ENTIRE CHIP CAN BE ERASED IN 10MS IN 15 TO 20MIN, TO ERASE AN EPROM. HOWEVER THIS MEMORY IS EEXPENSIVE COMPARED TO EOROM OR FLOSH MEMORY.

34) WHAT IS EI AND DI?

- EI(ENABLE INTERRUPT)
  - THIS IS A 1BYTE INSTUCTION
  - THE INSTRUCTION SETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLES THE INTERRUPT PROECSS
  - SYSTEM RESET OR AN INTERRUPT DISABLES THE INTERRUPT PROCESS
- DI(DISABLE INTERRUPT)
  - THIS IS A 1BYTE INSTRUTION
  - THE INSTRUCTION RESETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLE THE INTERRUPT PROCESS
  - IT SHOULD AN INTERRUPT FROM AN OURSIDE SOURCE CAN NOT BE TOLERATED

35) DISCUSS DIFFERENT STEPS OF 8085 INTERRUPT PROCESS?

- EI(ENABLE INTERRUPT)
  - THIS IS A 1BYTE INSTUCTION
  - THE INSTRUCTION SETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLES THE INTERRUPT PROECSS
  - SYSTEM RESET OR AN INTERRUPT DISABLES THE INTERRUPT PROCESS
- DI(DISABLE INTERRUPT)
  - THIS IS A 1BYTE INSTRUTION
  - THE INSTRUCTION RESETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLE THE INTERRUPT PROCESS
  - IT SHOULD AN INTERRUPT FROM AN OURSIDE SOURCE CAN NOT BE TOLERATED
- WHEN THE MICROPROCESSOR IS EXECUTING A PROGRAM, IT CHECKS THE INTR LINE DURING THE EXECUTION OF EACH INSTRUCTION.
- IF THE LINE INTR IS HIGH AND THE INTERRUPT IS ENABLES THE MICROPROCESSOR COMPLETES THE CURRENT INSTRUCTION, DISABLES THE INTERRUPT ENABLES FLIP FLOP AND SENDS A SIGNAL CALLED $\overline{I}\,\overline{N}\,\overline{T}\,\overline{R}$ - INTERRUPT ACKNOELEDGE(ACTIVE LOW). THE PROCESSOR CANNOT ACCEPT ANY INTERRUPT REQUESTS UNTIL THE INTERRUPT FLIP FLOP IS ENABLES AGAGIN.
- THE SIGNAL INTA IS USED TO INSERT A RESTSRT (RST) INSTRCTION (OR A CALL INSTRUTION) THROUGH EXTERNAL HARDWARE. THE RST INSTRCTION IS A 1 BYTE CALL INSTRUCTION THAT TRANSFERS THE PROGRAM COUNTER TO A SPECIFIC MEMORY LOCATION ON PAGE 00H AND RESTART THE EXEXUTION AT THAT MEMORY LOCATION AFTER EXECUTING NEXT STEP.
- WHEN THE MICROPROCESSOR RECEIVES AN RST INSTRUCTION, IT SAVES THE MEMORY ADDRESS OF THE NEXT INSTRUCTION ON THE STACK. THIS IS SIMILAR TO INSERTING A BOOKMARK. THE PROGRAM IS TRANSFERRED TO THE CALL LOCATION.
- ASSUMING THAT THE TASK TO BE PERFROMED IS WRITTEN AS A SUBROUTINE AT THE SPECIFIED LOCATION , THE PROCESSOR PERFROMS THE TASK .THE SUBROUTINE IS KNOWN AS AN INTERRUPT SERVICE ROUTINE(ISR)
- THE SERVICE ROUTINE SHOULD INCLUDE THE INSTRUCTION EI TO ENABLE THE INTERRUPT AGAIN. THIS IS SIMILAR TO PUTTING THE RECEIVER BACK ON THE BOOK.
- AT THE END OF THE SUNROUTINE, THE RET INSTRUCTION RETRIEVES THE MEMORY ADDRESS WHERE THE PROGRAM WAS INTERRUPTED AND CONTINUES THE EXECUTION. WE WILL ERABORATE FURTHER ON THE RESTSRT INSTRCTIONS ADDITIONAL HARDWARE MENTIONED IN STEP 4AND MULTIPLE INTERRUPTS.

36) DRAW THE PIN DIAGRAM OF 8085 AND WRITE THE FUNCTION OF ALL PINS.

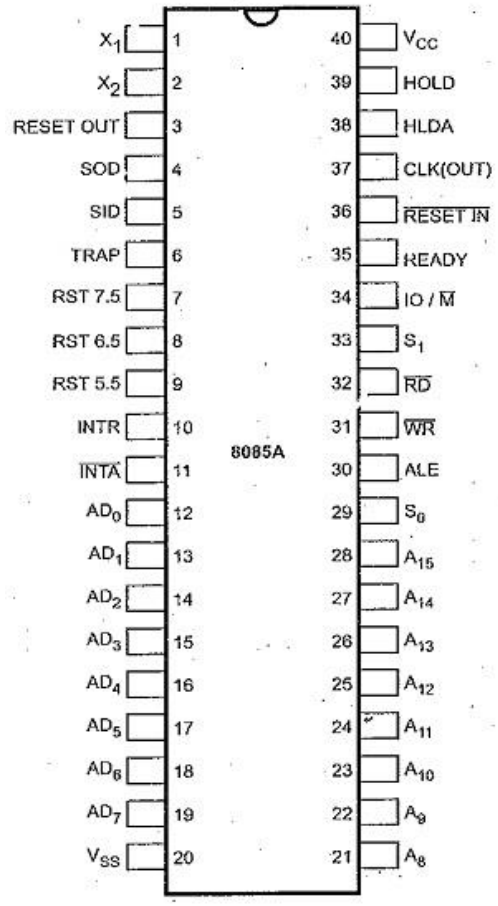


Fig. 1.3 (a) Pin configuration

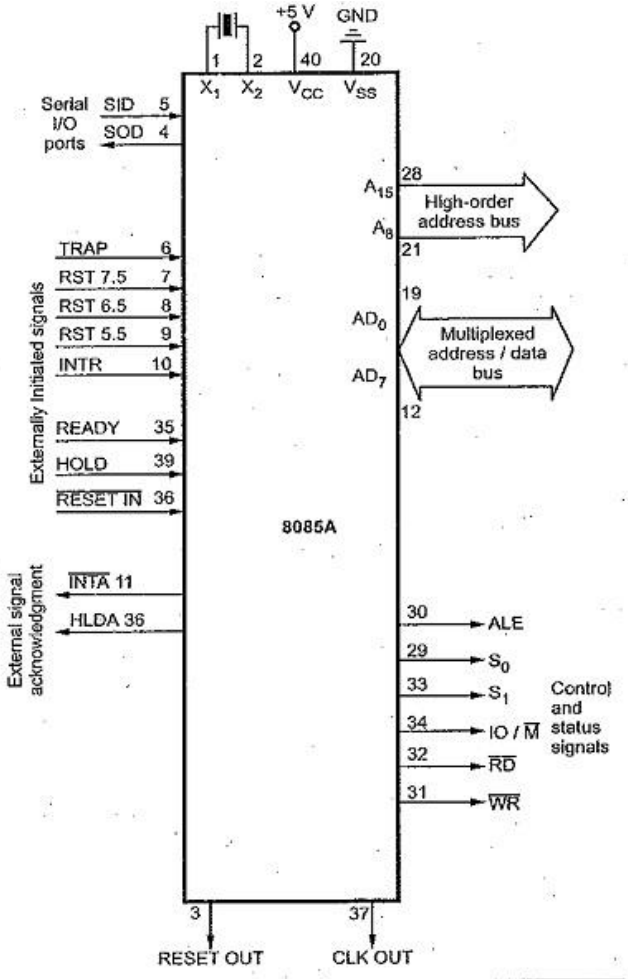


Fig. 1.3 (b) Functional pin diagram

- MULTIPLEXED ADDRESS/ DATA BUS:-

  THE SIGNAL LINES AD7 – ADO ARE BIDIRECTIONAL, THEY SERVE A DUAL PURPOSE. THEY ARE UESD AS THE LOW ORDER ADDRESS BUS AS WELL AS DATA BUS.IN EXECUTING AN INSTRUCTION DURING THE EARLIER PART OF THE CYCLE THESE LINES ARE USED AS THE LOW ORDER ADDRESS BUS. DURING THE LATER PART OF THE CYCLE THESE LINES ARE USED AS THE DATA BUS (THIS IS ALSO KNOWN AS MULTIPLEXING THE BUS). HOWEVER THE LOW PRDER ADDRESS BUS CAN BE SEPARETED FROM THESE SIGNALS BY USING A LATCH.

- CONTROL AND STATUS SIGNALS:-

  - ALE (ADDRESS LATCH ENABLE):- THIS IS A POSITIVE GOING PULSE GENERATED EVERY TIME THE 8085 BEGINS AN OPERATION (MACHINE CYCLE), IT INDICATES THAT THE BITS ON AD7 TO AD0 ARE ADDRESS BITS. THIS SIGNAL IS UESD PRIMARILY TO LATCH THE LOW ORDER ADDRESS FROM THE MULTIPLEXED BUS AND GENERATE A SEPERATE SET OF EIGHT ADDRESS LINES A7 –A0
  - $\overline{R}$ $\overline{D}$ (READ):- THIS IS A READ CONTROL SIGNAL(ACTIVE LOW). THIS SIGNAL INDICATES THET THE SELECTED I/O OR MEMORY DEVICE IS TO BE REAR AND DATA ARE AVAILABLE ON THE DATABUS.
  - $\overline{W}$ $\overline{R}$ (WRITE):- THIS IS A WRITE CONTROL SIGNAL (ACTIVE LOW. THIS SIGNAL INDICATES THAT THE DATA ON THE DATABUS ARE TO BE WRITTEN INTO A SELECTED MEMORY OR I/O LOCATION.

- IO/ $\overline{M}$: - THIS IS A STSTUS SIGNAL USED TO DIFFERENTIATE BETWEEN I/O AND MEMORY OPERATION. WHEN IT IS HIGH, IT INDICATES AN I/O OPERATION, AND WHEN IT IS LOW IT INDICATES A MEMORY OPERATION.THIS SIGNAL IS COMBINED WITH $\overline{R}$ $\overline{D}$ (READ) AND $\overline{W}$ $\overline{R}$ (WRITE) TO GENERATE I/O AND MEMORY CONTROL SIGNALS.

- S1 AND S0:- THESE STATUS SIGNALS, SIMILAR TO IO/ $\overline{M}$, CAN INDENTIFY VARIOUS OPERATIOS, BUT THEY ARE RARELY UESD IN SMALL SYSTEMS.

❖ POWER SUPPLY AND CLOCK FREQUENCY:-

- VCC :- +5 VOLT POWER SUPPLY
- VSS:- GROUND REFERANCE
- X1, X2:- A CRYSTAL IS CONNECTED AT THESE TWO PINS. THE FREQUENCY IS INTERNALLY DIVIDED BY TWO, THERREFORE TO OPERATE A SYSTEM AT 3MHZ THE CRYSTAL SHOULD HAVE A FREQUENCY OF 6 MHZ.
- CLK (OUT):- THIS SIGNAL CAN BE USED AS THE SYSTEM CLOCKS FOR OTHER DEVICES.

		STATUS		
MACHINE CYCLE	IO/ $\overline{M}$	S1	S0	CONTROL SIGNAL
OPCODE FETCH	0	1	1	$\overline{R}$ $\overline{D}$ =0
MEMORY READ	0	1	0	$\overline{R}$ $\overline{D}$ =0
MEMORY WRITE	0	0	1	$\overline{W}$ $\overline{R}$ =0
I/O READ	1	1	0	$\overline{R}$ $\overline{D}$ =0
I/O WRITE	1	0	1	$\overline{W}$ $\overline{R}$ =0
INTERRUPT ACKNOWLEDGEMENT	1	1	1	$\overline{I}$ $\overline{N}$ $\overline{T}$ $\overline{A}$ =0
HALT	Z	0	0	$\overline{R}$ $\overline{D}$, $\overline{W}$ $\overline{R}$ =Z AND $\overline{I}$ $\overline{N}$ $\overline{T}$ $\overline{A}$=1
HOLD	Z	X	X	
RESET	Z	X	X	

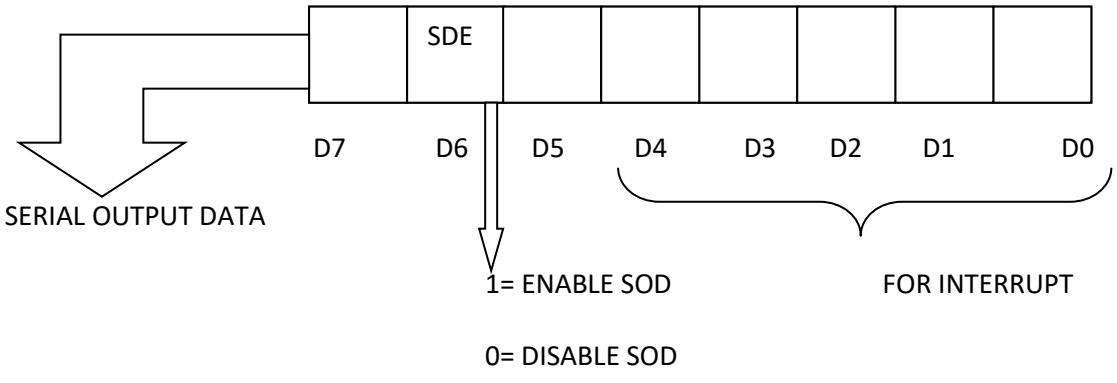
- INTERRUPT:-
  - INTR (INPUT) INTERRUPT REQUEST: - THIS IS USED AS A GENERAL PURPOSE INTERRUPT. IT IS SIMILAR TO THE INT SIGNAK OF THE 8080A
  - $\overline{I}\ \overline{N}\ \overline{T}\ \overline{A}$(OUTPUT) INTERRUPT ACKNOWLEDGEMENT:- THIS IS USED TO ACKNOWLEDGE AN INTERRUPT
  - RST 7.5, RST 6.5, RST 5.5 RESTART INTERRUPT: - THESE ARE VECTORED INTERRUPT THAT TRANFER THE PROGRAM CONTROL TO SPECIFIC MEMORY LOCATIONS. THEY HAVE HIGHER PRIORITIES THAN THE INTR INTERRUPT. AMONG THESE THREE, THE PRIORITY ORDER IS 7.5, 6.5 AND 5.5
  - TRAP (INPUT):- THIS IS NON MASKABLE INTERRUPT AND HAS HIGHEST PRIORITY.
  - HOLD(INPUT):- THIS SIGNAL INDICATES THAT A PERIPHERAL SUCH AS A DMA(DIRECT MEMORY ACCESS) CONTROLLER IS REQUESTING THE USE OF THE ADDRESS AND DATA BUSES
- HLDA (OUTPUT): THIS SIGNAL ACKOWLEDGES THE HOLD REQUEST.

- READY(INPUT): THIS SIGNAL IS USED TO DELAY THE MICROPROCESSOR READ OR WRITE CYCLES UNTIL A SLOW RESPONDING PERIPHERAL IS READY TO SEND OR ACCEPT DATA. WHEN THIS SIGNAL GOES LOW, THE MICROPROCESSOR WAITS FOR AN INTEGRAL NUMBER OF CLOCK CYCLES UNTIL IT GOES HIGH. SIGNAL CALLED HLDA(HOLD ACKNOWLEDGE)

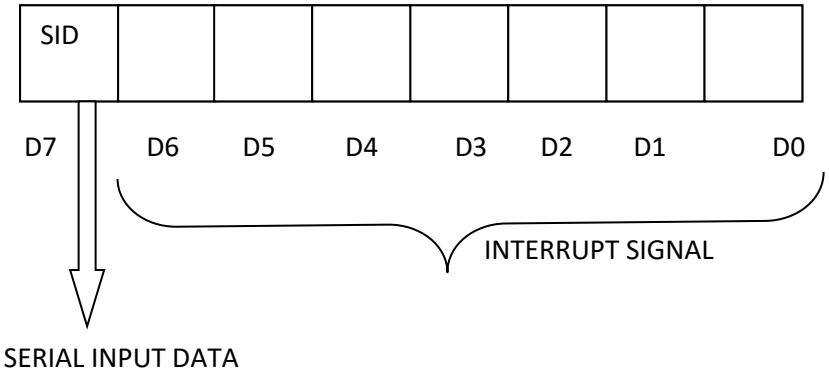
- $\overline{R}\ \overline{E}\ \overline{S}\ \overline{E}\ \overline{T}\ \overline{I}\ \overline{N}$:- WHEN THE SIGNAL ON THIS PIN GOES LOW, THE PROGRAM COUNTER IS SET TO ZERO, THE BUSES ARE TRI-STATED , AND THE MPU IS RESET.

- RESET OUT: - THIS SIGNAL INDICATES THAT THE MPU IS BEING RESET. THE SIGNAL CAN BE USED TO RESET OTHER DEVICE.

- SOD (SERIAL OUTPUT DATA):- THE INSTRUCTION SIM IS NECESSARY TO OUTPUT DATA SERIALLY FROM THE SOD LINE. IT CAN BE INTERPRETED FOR SERIAL OUTPUT AS IN THE LOWER FIGURE



- SID(SERIAL INPUT DTA):- THE INSTRUCTION RIM IS USED TO INPUT SERIAL DATA THROUGH THE SID LINE INSTRUCTION RIM CAN BE INTERRUPT FRO SERIAL I/O AS IN RHE BELOW FIGURE



37) WHAT HAPPEND IN A SINGLE BOARD MICROPROCESSIR WHEN THE POWER IS TURNED IN AND THE RESET KEY IS PUSHED?

- WHEN THE POWER IS TURNED ON, THE MONITOR PROGRAM STORED EITHER IN EPROM OR ROM COMES ALIVE. THE RESET KEY CLEARS THE PROGRAM COUNTER, AND THE PROGRAM COUNTER HOLDS THE MEMORY ADDRESS 0000H. SOME SYSTEMS ARE AUTOMATICALLY RESET WHEN THE POWER IS TURNED ON. (CALLED POWER –ON-RESET)

38) HOW DOES THE MICROPROCESSOR KNOW HOW AND WHEN TO START?

- AS SOON AS THE RESET KEY IS PUSHED, THE PROGRAM COUNTER PLACES THE MEMORY ADDRESS 0000H ON THE ADDRESS BUS, THE INSTRUCTION AT THAT LOCATION IS FETCHED AND THE EXECUTION OF THE KEY MONITOR PROGRAM BEGINS. THEREFORE, THE KEY MONITOR PROGRAM IS STORED ON PAGE 00H.

39) WHAT IS MINITOR PROGRAM?

- IN A SINGLE BOARD MICRO COMPUTER WITH A HEX KEYBOARD, THE INSTRCTIONS ENTERED IN R/W MEMORY THROUGH THE KEYBOARD. THE KEY MONITOR PROGRAM IS A SET OF INSTRUCTIONS THAT CONTINUOUSLY CHECKS WHETHER A KEY IS PRESSED AND STORES THE BINARY EQUIVALENT OF A PRESSED KEY IN A MEMORY LOCATION.

40) HOW DOES MICROPROCESSOR KNOW WHAT OPERATION TO PERFROM FIRST(READ/WRITE MEMORY OR READ/WRITE I/O)?

- THE FIRST OPERATION IS ALWAYS A FETCH INSTRCTION.

41) HOW DOES THE MICROPROCESSOR DIFFERENTIATE AMONG A POSITIVE NUMBER, A NEGATIVE NUMBER, AND A BIT PATTERN?

- IT DOES NOT KNOW THE DIFFERENT. THE MICROPROCESSOR VIEWS ANY DATA BYTE AS EIGHT BANARY DUGUTS. THE PROGRAMMER IS RESPONSIBLE FOR PROVIDING THE INTERPRETATION. FOR EXAMPLE, AFTER AN ARITHMETIC OR LOGIC OPERATION, IF THE BITS IN THE ACCUMULATOR ARE,

  1 1 1 1 0 0 1 0= F2 H
  THE SIGN FLAG IS SET BECAUSE D7=1. THIS DOES NOT MEAN IT IS A NEGATIVE NUMBER, EVEN IF THE SIGN FLAG IS SET. THE SIGN FLAG INDICATES ONLY THAT D7=1. THE EIGHT BITS IN THE ACCUMULATOR COULD BE A BIT PATTERN, OR A POSITIVW NUMBER LARGER THAN 127_{10} OR 2'S COMPLIMENT OF A NUMBER.

42) IF THE PROGRAM COUNTER IS ALWAYS ONE COUNT AHEAD OF THE MEMORY LOCATION FROM WHICH THE MACHINE CODE IS BEING FETCHED, HOW DOES THE MICROPROCESSOR CHANGE THE SEQUENCE OF PROGRAM EXECUTION WITH A JUMP INSTRUCTION?

- WHEN A JUMP INSTRUCTION IS FETCHED, ITS SECOND AND THIRD BYTES (A NEW MEMORY LOCATION) ARE PLACE IN THE W AND Z REGISTERS OF THE MICROPROCESSOR. AFTER THE EXECUTION OF JUMP INSTRUCTION, THE CINTENTS OF THE W AND Z REGISTERS ARE PLACED ON THE ADDRESS BUS TO FETCH THE INSTRUCTION FROM A NEW MEMORY LOCATION, AND THE PROGRAM COUNTER IS LOADED BY UPDATING THE CONTENT OF THE W AND Z REGISTERS.

43) IS THERE A MINIMUM PULSE WIDTH REQUIRED FOR THE INTR SIGNAL?

- THE MICROPROCCSSOR CHECKS INTR, ONE CLOCK PERIOS BEFORE THE LAST T-STATE OF AN INSTRUCTION CYCLE. IN THE 8085, THE CALL INSTRUCTIONS REQUIRE 18 T-STATES; THEREFORE, THE INTR PULSE SHOULD BE HIGH AT LEAST FOR 17.5 T-STATES. IN A SYSTEM WITH 3MHZ CLOCK FREQUENCY INTR SHOULD BE AT LEAT 5.8µS LONG.

44) HOW LONG CAN THE INTR PULSE STAY HIGH?

- THE INTR PULSE CAN REMAIN HIGH UNTIL THE INTERRUPT, FLIPFLOP IS SET BY THE EI (ENABLE INTERRUPT) INSTRUCTION IN THE SERVICE ROUTINE. IF IT REMAINS HIGH AFTER THE EXECUTION OF THE EI INSTRUCTION, THE PROCESSOR WILL BE INTERRUPTED AGAIN, AS IF IT WERE A NEW INTERRUPT. THE MANUAL BUTTON WILL KEEP THE INTR HIGH FOR MORE THAN 20MS; HOWEVER, THE SERVICE ROUTINE HAS A DELAY OF 1 SECOND, AND THE EI INSTRUCTION IS EXECUTED AT THE END OF THE SERVICE ROUTINE.

45) CAN THE MICROPROCESSOR BE INTERRUPTED AGAIN BEFORE THE COMPLITION OF THE FIRST INTERRUPT SERVICE ROUTINE?

- THE ANSWER TO THIS QUESTION IS DETERMINED BY THE PROGRAMMER. AFTER THE FIRST INTERRUPT, THE INTERRUPT PROCSS IS AUTOMATICALLY DISABLED. THE SERVICE ROUTINE ENABLES THE INTERRUPT AT THE END OF THE SERVICE ROUTINE; IN THIS CASE, THE MICROPROCESSOR CAN NOT BE INTERRUPTED BEFORE THE COMPLIETION OF THIS BEGINNING OF THE ROUTINE, THE MICROPROCESSOR CAN BE INTERRUPTED AGAIN DURING THE SERVICE ROUTINE.

46) ENABLE ALL THE INTERRUPT IN AN 8085 SYSTEM?

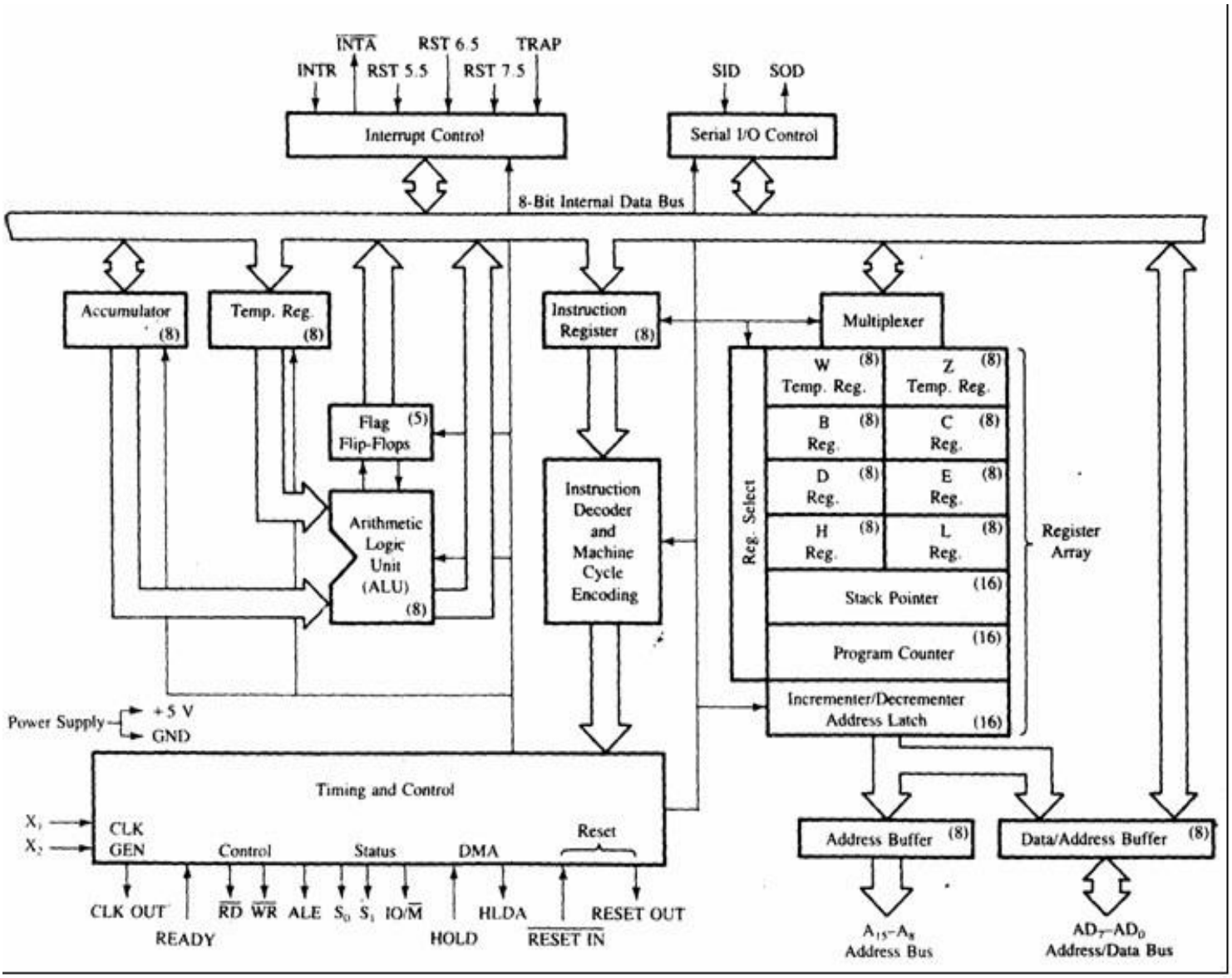
- EI :ENABLE INTERRUPT
  MVI A, 08H : LOAD BIT PATTERN TO ENABLE RST 7.5, 6.5, 5.5
  SIM : ENABLE RST 7.5, 6.5, 5.5

  BIT D3= 1 IN THE ACCUMULATOR MAKES THE INTRUCTION SIM FUNCTIONAL AND BITS D2, D1, AND D0 =0 AENABLE THE INTERRUPTS 7.5, 6.5, 5.5

47) RESET THE 7.5 INTERRUPT?

- MVI A,18H ; SET D4=1
  SIM ; RESET 7.5 INTERRUPT FLIP FLOP.

48) DISCUSS THE ARCHITECTURE OF 8085 MICROPROSSOR WITH THE HELP OF BLOCK DIAGRAM.



- **REGISTER: -** THE 8085 HAS SIX GENERAL PURPOSE REGISTERS TO STORE 8BIT DATA; THESE ARE IDENTIFIED AS B, C, D, E, H, L AS SHOWN IN THE FIGURE. THEY CAN BE ALSO IDENTIFIED AS REGISTER PAIR BC, DE, and HL TO PERFORM SOME 16 BIT OPERATIONS. THE PROGRAMMERS CAN USE THESE REGISTERS TO STORE OR COPY DATA INTO THE REGISTERS BY UNSING DATA COPY INSTUCTION.
- **ACCUMULATOR:** - THE ACCUMULATOR IS AN 8BIT REGISTER THAT IS PAT OF THE ARITHMETIC/LOGIC UNIT (ALU). THIS RESISTER IS USED TO STORE 8BIT DATA AND TO PERFORM ARITHMETIC AND LOGICAL OPERATIONS. THE RESULT OF AN OPERATION IS STORED IN THE ACCUMULATOR. THE ACCUMULATOR IS ALSO IDENITIFIED AS REGISTER (A).
- **FLAGS:** - 1) Z (ZERO):- THE ZERO FLAG IS SET TO 1 WHEN THE RESULT IS ZERO. OTHERWISE IT IS RESET.
  2) CY (CARRY):- IF AN ARITHMETIC OPERATION RESULT IN A CARRY, THE CY FLAG IS SET OTHERWISE IT IS RESERT.
  3) S (SIGN):- THE SIGN FLAG IS SET IF BIT D7 OF THE RESULT =1, OTHERWISE IT IS RESET.
  4) P (PARITY):- IF THE RESULT HAS AN EVEN NUMBER OF 1S, THE FLAG IS SET FOR AN ODD NUMBER OF 1S THE FLAG IS RESET.
  5) AC (AUXILARY CARRY):- IN AN ARITHMETIC OPERATION, WHEN A CARRY IS GENERATED BY DIGIT D3 AND PASSED TO D4, THE AC FLAG IS SET. RHIS FLAG IS USED INTERNALLY FOR BCD OPERATION. THERE IS NO JUMP INSTRUCTION ASSOCIATED WITH THIS FIAG.

- THE MICROPROCESSOR USES THE PC REGISTER TO SEQUENCE THE EXECITION OF THE INSTRUCTIONS. THE FUNCTION OF THE PROGRAM COUNTER IS TO POINT TO THE MEMORY ADDRESS FROM WHICH THE NEXT BYTE IS TOBE FETCHED. WHEN A BYTE IS BEING FETCHED, THE PROGRAM COUNTER IS INCREMENTED BY ONE TO POINT TO THE NEXT MEMORY LOCATION.
- THE STACK POINTER IS ALSO A 16BIT REGISTER UESD AS A MEMORY POINTER. IT POINTS TO A MEMORY LOCATION IN R/W MEMORY, CALLED THE STACK.THE BEGINNING OF THE STACK IS DEFINED BY LOADING A 16BIT ADDRESS IN THE STACK POINTER.

  - MULTIPLEXED ADDRESS/ DATA BUS:-

    THE SIGNAL LINES AD7 – ADO ARE BIDIRECTIONAL, THEY SERVE A DUAL PURPOSE. THEY ARE UESD AS THE LOW ORDER ADDRESS BUS AS WELL AS DATA BUS.IN EXECUTING AN INSTRUCTION DURING THE EARLIER PART OF THE CYCLE THESE LINES ARE USED AS THE LOW ORDER ADDRESS BUS. DURING THE LATER PART OF THE CYCLE THESE LINES ARE USED AS THE DATA BUS (THIS IS ALSO KNOWN AS MULTIPLEXING THE BUS). HOWEVER THE LOW PRDER ADDRESS BUS CAN BE SEPARETED FROM THESE SIGNALS BY USING A LATCH.
  - CONTROL AND STATUS SIGNALS:-
    - ALE (ADDRESS LATCH ENABLE):- THIS IS A POSITIVE GOING PULSE GENERATED EVERY TIME THE 8085 BEGINS AN OPERATION (MACHINE CYCLE), IT INDICATES THAT THE BITS ON AD7 TO AD0 ARE ADDRESS BITS. THIS SIGNAL IS UESD PRIMARILY TO LATCH THE LOW ORDER ADDRESS FROM THE MULTIPLEXED BUS AND GENERATE A SEPERATE SET OF EIGHT ADDRESS LINES A7 –A0
    - $\overline{R}$ $\overline{D}$ (READ):- THIS IS A READ CONTROL SIGNAL (ACTIVE LOW). THIS SIGNAL INDICATES THET THE SELECTED I/O OR MEMORY DEVICE IS TO BE REAR AND DATA ARE AVAILABLE ON THE DATABUS.
    - $\overline{W}$ $\overline{R}$ (WRITE):- THIS IS A WRITE CONTROL SIGNAL (ACTIVE LOW. THIS SIGNAL INDICATES THAT THE DATA ON THE DATABUS ARE TO BE WRITTEN INTO A SELECTED MEMORY OR I/O LOCATION.

    - IO/ $\overline{M}$: - THIS IS A STSTUS SIGNAL USED TO DIFFERENTIATE BETWEEN I/O AND MEMORY OPERATION. WHEN IT IS HIGH, IT INDICATES AN I/O OPERATION, AND WHEN IT IS LOW IT INDICATES A MEMORY

OPERATION.THIS SIGNAL IS COMBINED WITH $\overline{R}$ $\overline{D}$ (READ) AND $\overline{W}$ $\overline{R}$ (WRITE) TO GENERATE I/O AND MEMORY CONTROL SIGNALS.

- S1 AND S0:- THESE STATUS SIGNALS, SIMILAR TO IO/ $\overline{M}$, CAN INDENTIFY VARIOUS OPERATIOS, BUT THEY ARE RARELY UESD IN SMALL SYSTEMS.

❖ <u>POWER SUPPLY AND CLOCK FREQUENCY</u>:-

- VCC :- +5 VOLT POWER SUPPLY
- VSS:- GROUND REFERANCE
- X1, X2:- A CRYSTAL IS CONNECTED AT THESE TWO PINS. THE FREQUENCY IS INTERNALLY DIVIDED BY TWO, THERREFORE TO OPERATE A SYSTEM AT 3MHZ THE CRYSTAL SHOULD HAVE A FREQUENCY OF 6 MHZ.
- CLK (OUT):- THIS SIGNAL CAN BE USED AS THE SYSTEM CLOCKS FOR OTHER DEVICES.

		STATUS		
MACHINE CYCLE	IO/ $\overline{M}$	S1	S0	CONTROL SIGNAL
OPCODE FETCH	0	1	1	$\overline{R}$ $\overline{D}$ =0
MEMORY READ	0	1	0	$\overline{R}$ $\overline{D}$ =0
MEMORY WRITE	0	0	1	$\overline{W}$ $\overline{R}$ =0
I/O READ	1	1	0	$\overline{R}$ $\overline{D}$ =0
I/O WRITE	1	0	1	$\overline{W}$ $\overline{R}$ =0
INTERRUPT ACKNOWLEDGEMENT	1	1	1	$\overline{I}$ $\overline{N}$ $\overline{T}$ $\overline{A}$ =0
HALT	Z	0	0	$\overline{R}$ $\overline{D}$, $\overline{W}$ $\overline{R}$ =Z AND $\overline{I}$ $\overline{N}$ $\overline{T}$ $\overline{A}$=1
HOLD	Z	X	X	
RESET	Z	X	X	

❖ <u>INTERRUPT</u>:-

- INTR (INPUT) INTERRUPT REQUEST: - THIS IS USED AS A GENERAL PURPOSE INTERRUPT. IT IS SIMILAR TO THE INT SIGNAK OF THE 8080A
- $\overline{I}\ \overline{N}\ \overline{T}\ \overline{A}$(OUTPUT) INTERRUPT ACKNOWLEDGEMENT:- THIS IS USED TO ACKNOWLEDGE AN INTERRUPT
- RST 7.5, RST 6.5, RST 5.5 RESTART INTERRUPT: - THESE ARE VECTORED INTERRUPT THAT TRANFER THE PROGRAM CONTROL TO SPECIFIC MEMORY LOCATIONS. THEY HAVE HIGHER PRIORITIES THAN THE INTR INTERRUPT. AMONG THESE THREE, THE PRIORITY ORDER IS 7.5, 6.5 AND 5.5
- TRAP (INPUT):- THIS IS NON MASKABLE INTERRUPT AND HAS HIGHEST PRIORITY.
- HOLD(INPUT):- THIS SIGNAL INDICATES THAT A PERIPHERAL SUCH AS A DMA(DIRECT MEMORY ACCESS) CONTROLLER IS REQUESTING THE USE OF THE ADDRESS AND DATA BUSES

❖ HLDA (OUTPUT): THIS SIGNAL ACKOWLEDGES THE HOLD REQUEST.

❖ READY(INPUT): THIS SIGNAL IS USED TO DELAY THE MICROPROCESSOR READ OR WRITE CYCLES UNTIL A SLOW RESPONDING PERIPHERAL IS READY TO SEND OR ACCEPT DATA. WHEN THIS SIGNAL GOES LOW, THE MICROPROCESSOR WAITS FOR AN INTEGRAL NUMBER OF CLOCK CYCLES UNTIL IT GOES HIGH. SIGNAL CALLED HLDA(HOLD ACKNOWLEDGE)

❖ $\overline{R}\ \overline{E}\ \overline{S}\ \overline{E}\ \overline{T}\ \overline{I}\ \overline{N}$:- WHEN THE SIGNAL ON THIS PIN GOES LOW, THE PROGRAM COUNTER IS SET TO ZERO, THE BUSES ARE TRI-STATED , AND THE MPU IS RESET.

❖ RESET OUT: - THIS SIGNAL INDICATES THAT THE MPU IS BEING RESET. THE SIGNAL CAN BE USED TO RESET OTHER DEVICE.

❖ SOD (SERIAL OUTPUT DATA):- THE INSTRUCTION SIM IS NECESSARY TO OUTPUT DATA SERIALLY FROM THE SOD LINE. IT CAN BE INTERPRETED FOR SERIAL OUTPUT AS IN THE LOWER FIGURE

❖ SID(SERIAL INPUT DTA):- THE INSTRUCTION RIM IS USED TO INPUT SERIAL DATA THROUGH THE SID LINE INSTRUCTION RIM CAN BE INTERRUPT FRO SERIAL I/O AS IN RHE BELOW FIGURE

49) WRITE THE DIFFERENT BETWEEN MEMORY MAPPED I/O AND PERIPHERAL I/O?

50) WRITE INSTRUCTIONS WHICH ARE NEEDED IN MEMORY MAPPED I/O AND PERIPHERAL I/O?

51) HOW MANY ADDRESS LINES ARE USED TO IDENTIFY AN I/O PORT IN MEMORY MAPPED I/O AND PERIPHERAL I/O METHOD?

CHARACTERISTICS	MEMORY-MAPPED I/O	PERIFHERAL I/O
1. DEVICE ADDRESS	16 BIT	8 BIT
2. CONTROL SIGNALS FOR INPUT/OUTPUT	$\overline{M}$ $\overline{E}$ $\overline{M}$ $\overline{R}$/ $\overline{M}$ $\overline{E}$ $\overline{M}$ $\overline{W}$	$\overline{I}$ $\overline{O}$ $\overline{R}$/ $\overline{I}$ $\overline{0}$ $\overline{W}$
3. INSTRUCTIONS AVAILABLE	MEMORY RELATED INSTRUCTIONS SUCH AS STA; LDA; LDAX; STAX; MOV M, R; ADD M; SUB M; ANA M ETC	IN AND OUT
4. DATA TRANSFER	BETWEEN ANY REGISTER AND I/O	ONLY BETWWEN I/O AND THE ACCUMULATOR.
5. MAXIMUM NUMBER OF I/OS POSSIBLE	THE MEMORY MAP(64K) IS SHARED BETWEEN I/O S AND SYSTEM MEMORY .	THE I/O MAP IS INDEPEND OF THE MEMORY MAP; 256 INPUT DEVICES AND 256 OUTPUT DEVICES CAN BE CONNECTED.
6. EXECUTION SPEED	13 T STATE(STA,LDA) 7 T STATE (MOV)	10 T STATE.
7. HARDWARE REQUIREMENTS	MORE HARDWARE IS NEEDED TO DECODE 16 BIT ADDRESS.	LESS HARDWARE IS NEEDED TO DECODE 8 BIT ADDRESS.
8. OTHER FREATURE	ARITHMETIC OR LOGICAL OPERATION CAN BE DIRECTLY PERFROM WITH I/O DATA.	NOT AVAILABLE.

52) EXPLAIN WHY THE NUMBER OF OUTPUT PORTS IN PERIPHERAL MAPPES I/O IS RESTRICTED TO 256 PORTS OF 8085 MICROPROCESSOR?

- MEMORY – MAPPED I/O IS IN MANY WAYS SIMILAR TO PERIPHERAL I/O, EXCEPT THAT IN MEMORY MAPPED I/O, THE DEVICE HAS A 16BIT ADDRESS, AND MEMORY RELATED CONTROL SIGNALS ARE REQUIRED TO IDENTIFY THE DEVICE.

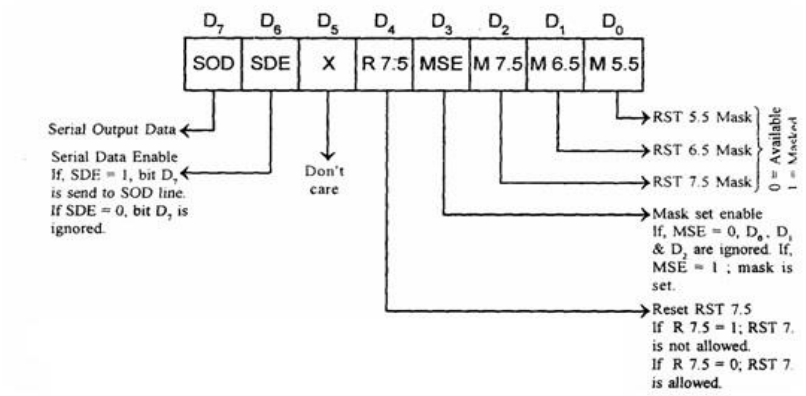
IN THE COMPARISON OF MEMORY- MAPPED I/O AND PERIPHERAL I/O WE SHOWS THAT THE SELECTION OF THE I/O TECHNIQUE WILL BE DETERMINED PRIMARILY BY THE TYPE OF APPLICATION; THE ADVANTAGE SEEM TO BALACE THE DISADVANTAGES. IN SYSTEMS IN WHICH 64K MEMORY IS A REQUIREMENT, PERIPHERAL I/O

BECOMES ESSENTIALS; ON THE OTHER HAND, IN CONTROL APPLICATIONS IN WHICH THE NUMBER IF I/OS EXCEED THE LIMIT (256) AND DIRECT DATA MANIPULATION IS PREFERRED, MEMORY- MAPPED I/O MAY HAVE AN ADVANTAGE.

53) BRIEFLY DISCUSS ABOUT RIM AND SIM INSTRUCTION?

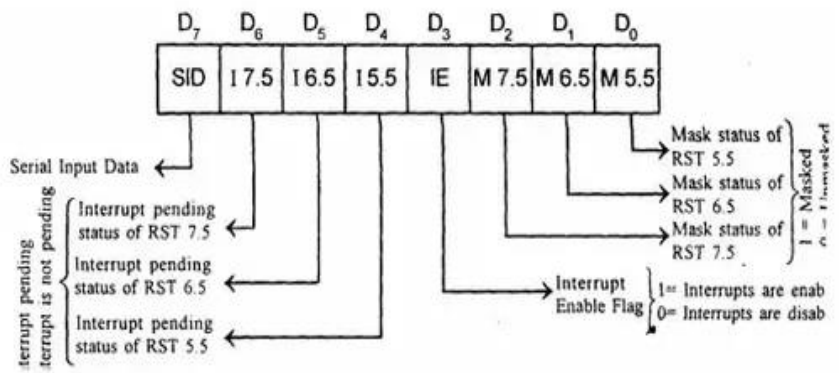
- SIM: SET INTERRUPR MASK. THIS 1-BYTE INSTRUCTION AND CAN BE USED FOR THREE DIFFERENT FUNCTION
  - ONE FUNCTION IS TO SET MASK FOR RST 7.5, 6.5, 5.5 INTERRUPTS.THIS INSTRUCTION READS THE CONTENT OF THE ACCUMULATOR AND ENABLES OR DISABLES THE INTERRUPTS ACCORDING TO THE CONTENT OF THE ACCUMULATOR BIT D3 IS A CONTROL BIT ABD SHOULD =1 FOR BITS D0, D1, AND D2 TO BE EFFECTIVE.LOGIC 0 ON D0, D1, AND D2 WILL ENBLE THE CORRESPODING INTERRUPTS ABD LOGIC 1 WILL DISABLE THE INTERRUPTS.
  - THE SECOND FUNCTION IS TO RESET RST 7.5, FLIP FLOP.BIT D4 IS ADDITIONAL CONTROL FOR RST 7.5. IF D4=1, RST 7.5 IS RESET. THIS IS USED TO OVERRIDE RST 7.5 WITHOUT SERVICING IT.
  - THE THIRD FUNCTION IS TO IMPLEMENT SERIAL I/O. BITS D7 AND D6 OF THE ACCUMULATOR ARE USED FOR SERIAL I/O AND DO NOT AFFECT THE INTERRUPTS. BIT D6=1 ENABLES THE SERIAL I/O AND BIT D7 IS USED TO TRANSMIT BITS.

SIM Instruction



- RIM (READ INTERRUPT MASK):
  - TO READ INTERRUPT MASKS. THIS INSTRUCTION LOADS THE ACCUMULATOR WITH 8 BITS INDICATING THE CURRENT STATUS OF THE INTERRUPT MASKS.
  - TO IDENTIFY PENDING INTERRUPTS, BITS D4, D5 AND D6 IDENTIFY THE PENDING INTERRUPT.
  - TO RECEIVE SERIAL DATA, BITS D7 IS USED TO RECEIVE SERIAL DATA

RIM Instruction



54) CAN AN INPUT PORT AND AN OUTPUT PORT HAVE THE SAME PORT ADDRESS?

- YES. THEY WILL BE DIFFERENTIATED BY CONTROL SIGNAL. THE $\overline{R}$ $\overline{D}$ IS USED TO ENABLE THE INPUT PORT AND THE $\overline{W}$ $\overline{R}$ IS USED TO ENABLE THE OUTPUT PORT.

55) HOW WILL THE PORT NUMBER BE AFFECTED IF WE DECODE THE HIGH ORDER ADDRESS LINES A15-A8 RATHER THAN A7-A0?

- THE PORT ADDRESS WILL REMAIN THE SAME BECAUSE THE I/O PORT ADDRESS IS DUPLICATED ON BITH SEGMENTS OF THE ADDRESS BUS.

56) IF HIGH ORDER LINES ARE PARTIALLY DECODED, HOW CAN ONE DETERMINE WHETHER IT IS PERIPHERAL I/O OR MEMORY MAPPED I/O?

- TO RECOGNIZE THE TYPE OF I/O, EXAMINE THE CONTROL SIGNAL. IF THE CONTROL SIGNAL IS $\overline{I}$ $\overline{O}$ $\overline{W}$(OR $\overline{I}$ $\overline{O}$ $\overline{R}$), IT MUST BE A PERIPHERAL I/O, AND IF THE CONTROL SIGNAL IS $\overline{M}$ $\overline{E}$ $\overline{M}$ $\overline{W}$(OR $\overline{M}$ $\overline{E}$ $\overline{M}$ $\overline{R}$) IT MUST BE MEMORY MAPPED I/O

57) IN A MEMORY MAPPED I/O, HOW DOES THE MICROPROCESSOR DIFFERENTIATE BETWEEN AN I/O AND MEMORY? CAN AN I/O HAVE THE SAME ADDRESS AS A MEMORY REGISTER?

- IN MEMORY –MAPPED I/O THE MICROPROCESSOR CAN NOT DIFFERENTIATE BETWEEN AN I/O AND MEMORY; IT TREATS AN I/O AS IF IT IS MEMORY. THEREFORE, AN I/O AND MEMORY REGISTER CAM NOT HAVE THE SAME ADDRESS; THE ENTIRE MEMORY MAP (64K) OF THE SYSTEM HAS TO BE SHARED BETWEEN MEMORY AND I/O.

58) WHYY IS A 16BIT ADDRESS STORED IN MEMORY IN THE REVERSED ORDER – THE LOW ORDER BYTE FIRST, FOLLOWING BY THE HIGH ORDER BYTE?

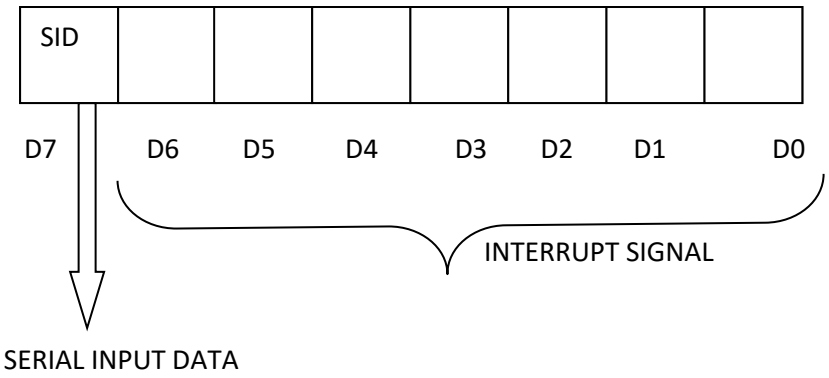
- THIS HAS TO DO WITH THE DESIGN OF THE 8085 MICROPROCESSOR. THE INSTRUCTION DECODER OR THE ASSOCIATED MICROPROGRAM IS DESIGN TO RECOGNIZE THE SECOND BYTE AS THE LOW- ORDER BYTE IN A THREE – BYTE INSTRUCTION.

59) COMPARE BETWEEN 8BIT AND 16 BIT MICROPROCESSOR?

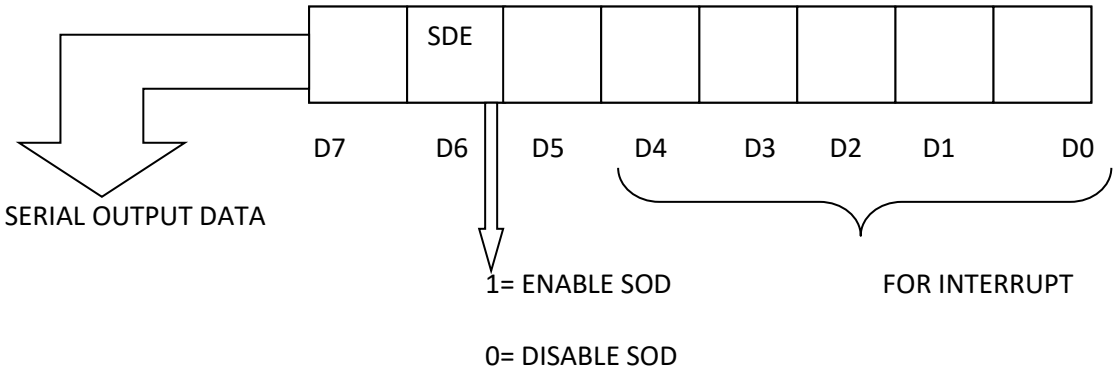
- DIFFERENT BETWEEN 8085 AND 8086 MICROPROCESSOR.

60) WHAT IS THE FUNCTION OF SID, SOD AND READY PIN IN 8085 MICROPROCESSOR?

- SID(SERIAL INPUT DTA):- THE INSTRUCTION RIM IS USED TO INPUT SERIAL DATA THROUGH THE SID LINE INSTRUCTION RIM CAN BE INTERRUPT FRO SERIAL I/O AS IN RHE BELOW FIGURE



- SOD (SERIAL OUTPUT DATA):- THE INSTRUCTION SIM IS NECESSARY TO OUTPUT DATA SERIALLY FROM THE SOD LINE. IT CAN BE INTERPRETED FOR SERIAL OUTPUT AS IN THE LOWER FIGURE



- READY(INPUT): THIS SIGNAL IS USED TO DELAY THE MICROPROCESSOR READ OR WRITE CYCLES UNTIL A SLOW RESPONDING PERIPHERAL IS READY TO SEND OR ACCEPT DATA. WHEN THIS SIGNAL GOES LOW, THE MICROPROCESSOR WAITS FOR AN INTEGRAL NUMBER OF CLOCK CYCLES UNTIL IT GOES HIGH. SIGNAL CALLED HLDA(HOLD ACKNOWLEDGE)

61) WRITE THE FUNCTION OF ALE AND IO/ $\overline{M}$?

- ALE (ADDRESS LATCH ENABLE):- THIS IS A POSITIVE GOING PULSE GENERATED EVERY TIME THE 8085 BEGINS AN OPERATION (MACHINE CYCLE), IT INDICATES THAT THE BITS ON AD7 TO AD0 ARE ADDRESS BITS. THIS SIGNAL IS UESD PRIMARILY TO LATCH THE LOW ORDER ADDRESS FROM THE MULTIPLEXED BUS AND GENERATE A SEPERATE SET OF EIGHT ADDRESS LINES A7 –A0
- IO/ $\overline{M}$: - THIS IS A STSTUS SIGNAL USED TO DIFFERENTIATE BETWEEN I/O AND MEMORY OPERATION. WHEN IT IS HIGH, IT INDICATES AN I/O OPERATION, AND WHEN IT IS LOW IT INDICATES A MEMORY

OPERATION.THIS SIGNAL IS COMBINED WITH $\overline{R}$ $\overline{D}$ (READ) AND $\overline{W}$ $\overline{R}$ (WRITE) TO GENERATE I/O AND MEMORY CONTROL SIGNALS.

62) BRIEFLY DISCUSS ABOUT CONTROL AND SIGNALS OF 8085 MICROPROCESSOR?

- CONTROL AND STATUS SIGNALS:-
  - ALE (ADDRESS LATCH ENABLE):- THIS IS A POSITIVE GOING PULSE GENERATED EVERY TIME THE 8085 BEGINS AN OPERATION (MACHINE CYCLE), IT INDICATES THAT THE BITS ON AD7 TO AD0 ARE ADDRESS BITS. THIS SIGNAL IS UESD PRIMARILY TO LATCH THE LOW ORDER ADDRESS FROM THE MULTIPLEXED BUS AND GENERATE A SEPERATE SET OF EIGHT ADDRESS LINES A7 –A0
  - $\overline{R}$ $\overline{D}$ (READ):- THIS IS A READ CONTROL SIGNAL (ACTIVE LOW). THIS SIGNAL INDICATES THET THE SELECTED I/O OR MEMORY DEVICE IS TO BE REAR AND DATA ARE AVAILABLE ON THE DATABUS.
  - $\overline{W}$ $\overline{R}$ (WRITE):- THIS IS A WRITE CONTROL SIGNAL (ACTIVE LOW. THIS SIGNAL INDICATES THAT THE DATA ON THE DATABUS ARE TO BE WRITTEN INTO A SELECTED MEMORY OR I/O LOCATION.

  - IO/ $\overline{M}$: - THIS IS A STSTUS SIGNAL USED TO DIFFERENTIATE BETWEEN I/O AND MEMORY OPERATION. WHEN IT IS HIGH, IT INDICATES AN I/O OPERATION, AND WHEN IT IS LOW IT INDICATES A MEMORY OPERATION.THIS SIGNAL IS COMBINED WITH $\overline{R}$ $\overline{D}$ (READ) AND $\overline{W}$ $\overline{R}$ (WRITE) TO GENERATE I/O AND MEMORY CONTROL SIGNALS.

63) DISCUSS DIFFERENT TYPE OF INTERRUPT PRESENT IN 8085. LIST THE NAMES OF IERRUPTS PRESENT IN 8085 IN THEIR PRIORITY ORDER?

- RST 7.5:- THIS IS POSITIVE EDGE SENSITIVE AND CAN BE TRIGGERED WITH A SHORT PULSE. THE REQUEST IS STORED INTERNALLY BY THE D FLIP FLOP INTIL THE MICROPROCESSOR RESPONDS TO THE REQUEST OR UNTIL IT IS CLEARED BY RESET OR BY BIT D4 IN THE SIM INSTRUCTION.
- RST 6.5 AND RST 5.5:- THESE INTERRUPTS ARE LEVEL –SENSITIVE , MEANING THAT THE TRIGGERING LEVEL SHOULD BE ON UNTIL THE MICROPROCESSOR COMPLETES THE EXECUTION OF THE CURRENT INSTRUCTION.IF THE MICROPROCESSOR IS UNABLE TO RESPOND TP THESE REQUESTS IMMEDIATELY THEY SHOULD BE STORED OR HELD BY EXTERNAL HARDWARE.
  THESE ARE VECTORED INTREEUPT THAT TRANSFER THE PROGRAM CONTROL TO SPECIFIC MEMORY LOCATIONS. THEY HAVE HIGHER PRIORITIES THAN THE INTR TERRUPT. AMONG THESE THREE THE PRIORITY ORDER IS 7.5, 6.5 AND 5.5.

  - TRAP (INPUT):- THIS IS NON MASKABLE INTERRUPT AND HAS HIGHEST PRIORITY.

- EI(ENABLE INTERRUPT)
  - THIS IS A 1BYTE INSTUCTION
  - THE INSTRUCTION SETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLES THE INTERRUPT PROECSS
  - SYSTEM RESET OR AN INTERRUPT DISABLES THE INTERRUPT PROCESS
- DI(DISABLE INTERRUPT)
  - THIS IS A 1BYTE INSTRUTION
  - THE INSTRUCTION RESETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLE THE INTERRUPT PROCESS
  - IT SHOULD AN INTERRUPT FROM AN OURSIDE SOURCE CAN NOT BE TOLERATED

64) WRITE DIFFERENT EXTERNALLY INICIATED OPERATIONS OR SIGNALS INCLUDING INTERRUPTS OF 8085?

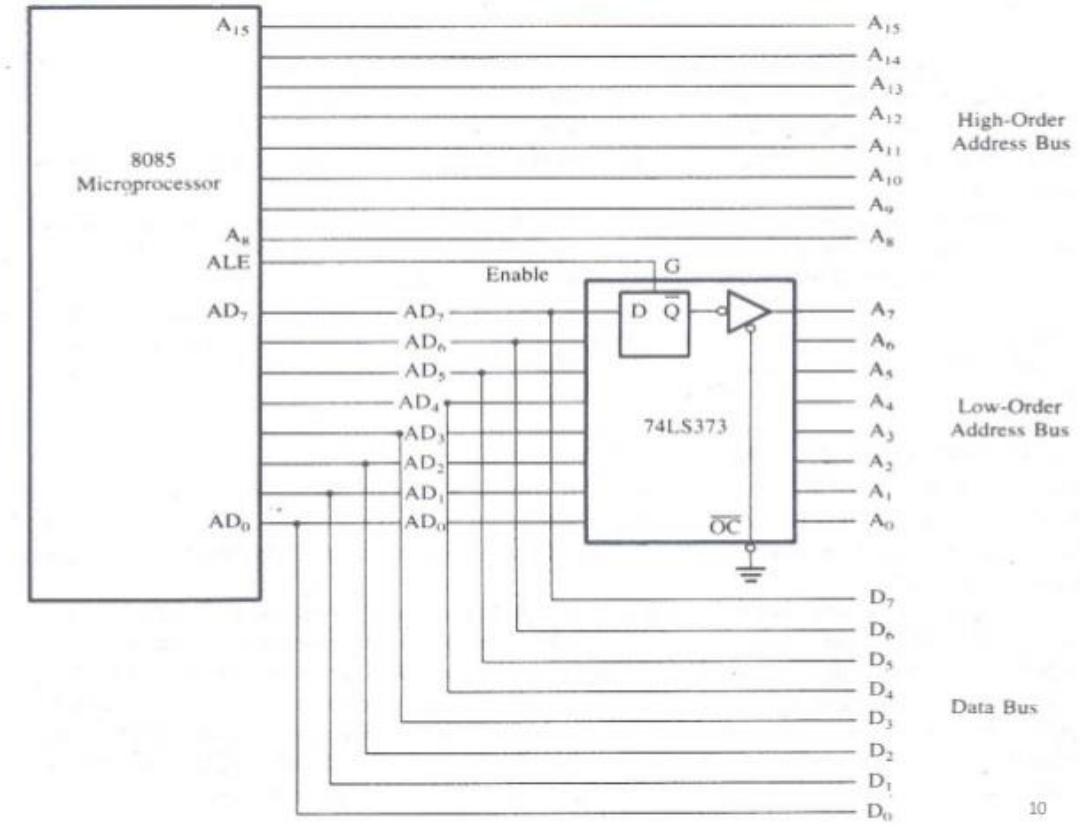
- INTR (INPUT) INTERRUPT REQUEST: - THIS IS USED AS A GENERAL PURPOSE INTERRUPT. IT IS SIMILAR TO THE INT SIGNAK OF THE 8080A
- HOLD(INPUT):- THIS SIGNAL INDICATES THAT A PERIPHERAL SUCH AS A DMA(DIRECT MEMORY ACCESS) CONTROLLER IS REQUESTING THE USE OF THE ADDRESS AND DATA BUSES
- HLDA (OUTPUT): THIS SIGNAL ACKOWLEDGES THE HOLD REQUEST.
- READY(INPUT): THIS SIGNAL IS USED TO DELAY THE MICROPROCESSOR READ OR WRITE CYCLES UNTIL A SLOW RESPONDING PERIPHERAL IS READY TO SEND OR ACCEPT DATA. WHEN THIS SIGNAL GOES LOW, THE MICROPROCESSOR WAITS FOR AN INTEGRAL NUMBER OF CLOCK CYCLES UNTIL IT GOES HIGH. SIGNAL CALLED HLDA(HOLD ACKNOWLEDGE)
- $\overline{R}\ \overline{E}\ \overline{S}\ \overline{E}\ \overline{T}\ \ \overline{I}\ \overline{N}$:- WHEN THE SIGNAL ON THIS PIN GOES LOW, THE PROGRAM COUNTER IS SET TO ZERO, THE BUSES ARE TRI-STATED , AND THE MPU IS RESET.
- RESET OUT: - THIS SIGNAL INDICATES THAT THE MPU IS BEING RESET. THE SIGNAL CAN BE USED TO RESET OTHER DEVICE.

65) DISCUSS DIFFERENT TIMING AND CONTROL SIGNALS OF 8085 MICROPROCESSOR?

- <u>CONTROL AND STATUS SIGNALS</u>:-
  - ALE (ADDRESS LATCH ENABLE):- THIS IS A POSITIVE GOING PULSE GENERATED EVERY TIME THE 8085 BEGINS AN OPERATION (MACHINE CYCLE), IT INDICATES THAT THE BITS ON AD7 TO AD0 ARE ADDRESS BITS. THIS SIGNAL IS UESD PRIMARILY TO LATCH THE LOW ORDER ADDRESS FROM THE MULTIPLEXED BUS AND GENERATE A SEPERATE SET OF EIGHT ADDRESS LINES A7 –A0
  - $\overline{R}\ \overline{D}$ (READ):- THIS IS A READ CONTROL SIGNAL (ACTIVE LOW). THIS SIGNAL INDICATES THET THE SELECTED I/O OR MEMORY DEVICE IS TO BE REAR AND DATA ARE AVAILABLE ON THE DATABUS.
  - $\overline{W}\ \overline{R}$ (WRITE):- THIS IS A WRITE CONTROL SIGNAL (ACTIVE LOW. THIS SIGNAL INDICATES THAT THE DATA ON THE DATABUS ARE TO BE WRITTEN INTO A SELECTED MEMORY OR I/O LOCATION.
  - IO/ $\overline{M}$: - THIS IS A STSTUS SIGNAL USED TO DIFFERENTIATE BETWEEN I/O AND MEMORY OPERATION. WHEN IT IS HIGH, IT INDICATES AN I/O OPERATION, AND WHEN IT IS LOW IT INDICATES A MEMORY OPERATION.THIS SIGNAL IS COMBINED WITH $\overline{R}\ \overline{D}$ (READ) AND $\overline{W}\ \overline{R}$ (WRITE) TO GENERATE I/O AND MEMORY CONTROL SIGNALS.

66) EXPLAIN NEED OF DEMULTIPLEX AD0 – AD7.

- THE LOWER FIGURE SHOWS A SCHEMATIC THAT USES A LATCH AND THE ALE SIGNAL TO DEMULTIPLEX THE BUS. THE BUS AD7 – AD0 IS CONNECTED AS THE INPUT TO THE LATCH 74LS373. THE ALE SIGNAL IS CONNECTED TO THE ENABLE (G) PIN OF THE LATCH , AND THE OUTPUT CONTROL SIGNAL OF THE LATCH IS GROUNDED.



67) WHAT IS THE DIFFERENT BETWEEN INR B AND INX B?

- INR B (INCREMENT CONTENT OF REGISTER B):- THE CONTENTS OF THE DESIGNATED REGISTER ARE INCREMENTED BY 1 AND THE RESULTS ARE STORED IN THE SAME PLACE. IF THE OPERAND IS A MEMORY LOCATION, IT IS SPECIFIED BY THE CONTENT OF HL REGISTER PAIR.
- INX B (INCREMENT REGISTER PAIR BY 1):- THE CONTENT OF THE SPECIFIED REGISTER PAIR ARE INCREMENTED BY 1. THE INSTRUCTION VIEWS THE CONTENT OF THE TWO REGISTERS AS A 16 BIT NUMBER.

68) WHITE THE DIFFERENT BETWEEN JUMP AND CALL INSTRUCTION?

- JMP: - THE PROGRAM SEQUENCE IS TRANSFERRED TO THE MEMORY LOCATION SPECIFIED BY THE 16BIT ADDRESS. THIS IS A 3 BYTE INSTRUCTION; THE SECOND BYTE SPECIFIES THE LOW ORDER BYTE AND THE THIIRD BYTE SPECIFIES THE HIGH ORDER BYTE.
- CALL: - THE PROGRAM SEQUENCE IS TRANSFERRED TO THE ADDRESS SPECIFIED BY THE OPERAND. BEFORE THE TRANFER, THE ADDRESS OF THE NEXT INSTRUCTION TO CALL IS PUSHED ON THE STACK.

69) WRITE THE DIFFERENCE BETWEEN CALL AND RETURN INSTRUCTION?

- CALL:-
  - IT'S TAKES 16 BIT MEMORY ADDRESS AS OPERAND.
  - IT CALLS SUBROUTINE UNCONDITIONALLY.
  - THIS IS A 3 BYTE INSTRUCTION THAT TRANSFROM, THE PROGRAM SEQUENCE TO A SUBROUTINE ADDRESS.
  - SAVES THE CONTENT OF TWO PC (PROGRAM COUNTER) ON THE STACK.
  - DECREMENT THE STACK POINTER REGISTER BY TWO.
  - JUMP UNCONDITIONALLY TO THE MEMORY LOCATON SPECIFIED BY THE 2^{ND} AND 3^{RD} BYTE. THE 2^{ND} BYTE SPECIFIES A LINE NUMBER AND THE 3^{RD} BYTE SPECIFIES A PAGE NUMBER.
  - THIS INSTRUCTION IS ACCOMPANIED BY A RETURN INSTRUCTION IN THE SUBROUTINE.
- RET:-
  - RETURN FROM SUBROUTINE UNCONDITIONALLY
  - THIS IS 1 BYTE INSTRUCTION.
  - INSERT THE TWO BYTE FROM THE TOP OF THE STACK INTO THE PROGRAM COUNTER, AND INCREMENTS THE STACK POINTER BY TWO.

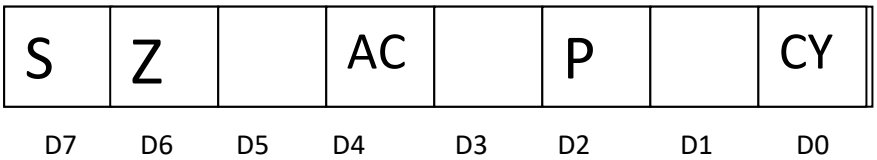
70) DISCUSS THE SEQUENCE OF EVENTS TAKE PLACE WHILE EXECUTING CALL INSTRUCTION?

- WE ARE ASSUMING TO TAKE AN EXAMPLE ACCORING TO THE ANSWER OF THIS QUESTION.

MEMORY ADDRESS	MACHINE CODE	MNEMONICS	COMMENTS
2040	CP	CALL 2070 H;	CALL SUBROUTINE LOCATED AT LOCATION 2070 H.
2041	70		
2042	20		
2043	NEXT	INSTRUCTION	

MACHINE	STACK PINTER	ADDRESS BUS	PROGRAM COUNTER	DATA BUS	INTERNAL REGISTER
M1 OPCODE FETCH	23FF (SP-1)	2040	2041	CD OPCODE	
M2 OPCODE MEMORY READ		2041	2042	70 H →	70
M3 MEMORY READ	23FF	2042	2043	20 H →	20
M4 MEMORY WRITE	23FE (SP-1)	23FF	20 43 →	20(PCH)	
M5 MEMORY WRITE	23FF	23FE	20 43 →	43(PCL)	(2070)
M1 OPCODE FETCH		2070	20 (W) 71 (Z)		20 (W) 70 (Z)

71) WHAT IS PSW?



- IN THE ABOVE FIGURE FIVE BIT INDICATE THE FIVE STATUS FLAG AND 3 BITS ARE UNDEFINE. THE COMBINATION OF 8 BITS IS PROGRAM STATUS WORD. THE PSW AND ACCUMULATOR ARE TREATED AS 16 BITS.

72) DEFINE T -SATE, INSTRUCTION CYCLE, MACHINE CYCLE?

- T STATE IS DEFINE AS ANE SUBDIVITION OF THE OPERATION PERFROMED IN ONE CLOCK PERIOD. THESE SUBDIVITIONS ARE INTERNAL STATUS SYNCHRONIZED WITH THE SYSTEM CLOC, AND EACH T-STATE IS PRECISELY EQUAL TO ONE CLOCK PERIOD. THE TERMS T-SATE AND CLOCK PERIOD. THE TURMS T-STATE AND CLOCK PERIOD ARE OFTEN USED SYMALTANIOULY.
- INSTRUCTION CYCLE IS DEFINED AS THE TIME REQUIRED COMPLETE THE EXECUTION OF AN INSTRUCTION. THE 8085 INSTRUCTION CYCLE CONSISTS OF ONE TO SIX MACHINE CYCLES OR ONE TO SIX OPERATION
- MACHINE CYCLE IS DEFINED AS THE TIME REQUIRED COMPLETE ONE OPERATION OF ACCESSING MEMORY I/O OR ACKNOWLEDGING AN EXTERNAL REQUEST. THIS CYCLE MAY CONSIST OF TO THREE TO SIX T-STATE. THE INSTRUCTION CYCLE AND MACHINE ARE THE SAME

73) WHAT IS THE DIFFERENT BETWEEN VECTORED AND NON VECTOR INTERRUPT? WRITE THE NAME OF 8085 VECTORED INTERRUPTD ACCORDING TO THEIR PRIORITY VALUES.

- WHEN MICROPROCESSOR RECEIVES ANY INTERRUPT SIGNAL FROM PERIPHERAL(S) WHICH ARE REQUESTING ITS SERVICES, IT STOPS ITS CURRENT EXECUTION AND PROGRAM CONTROL IS TRANSFERRED TO A SUB-ROUTINE BY GENERATING **CALL** SIGNAL AND AFTER EXECUTING SUB-ROUTINE BY GENERATING **RET**SIGNAL AGAIN PROGRAM CONTROL IS TRANSFERRED TO MAIN PROGRAM FROM WHERE IT HAD STOPPED.
  WHEN MICROPROCESSOR RECEIVES INTERRUPT SIGNALS, IT SENDS AN ACKNOWLEDGEMENT (INTA) TO THE PERIPHERAL WHICH IS REQUESTING FOR ITS SERVICE.
- **HARDWARE AND SOFTWARE INTERRUPTS –**
  WHEN MICROPROCESSORS RECEIVE INTERRUPT SIGNALS THROUGH PINS (HARDWARE) OF MICROPROCESSOR, THEY ARE KNOWN AS *HARDWARE INTERRUPTS*. THERE ARE 5 HARDWARE INTERRUPTS IN 8085 MICROPROCESSOR. THEY ARE – *INTR, RST 7.5, RST 6.5, RST 5.5, TRAP*

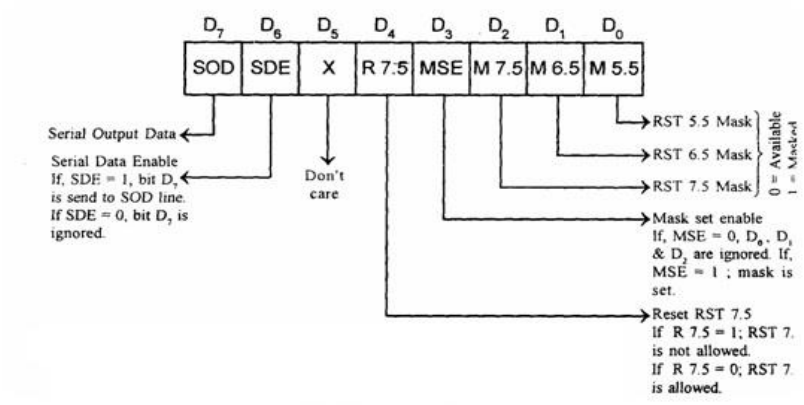
SOFTWARE INTERRUPTS ARE THOSE WHICH ARE INSERTED IN BETWEEN THE PROGRAM WHICH MEANS THESE ARE MNEMONICS OF MICROPROCESSOR. THERE ARE 8 SOFTWARE INTERRUPTS IN 8085 MICROPROCESSOR. THEY ARE – *RST 0 TO RST 7*

- **VECTORED AND NON-VECTORED INTERRUPTS –***VECTORED INTERRUPTS* ARE THOSE WHICH HAVE FIXED VECTOR ADDRESS (STARTING ADDRESS OF SUB-ROUTINE) AND AFTER EXECUTING THESE, PROGRAM CONTROL IS TRANSFERRED TO THAT ADDRESS.

NON-VECTORED INTERRUPTS ARE THOSE IN WHICH VECTOR ADDRESS IS NOT PREDEFINED. THE INTERRUPTING DEVICE GIVES THE ADDRESS OF SUB-ROUTINE FOR THESE INTERRUPTS. *INTR* IS THE ONLY NON-VECTORED INTERRUPT IN 8085 MICROPROCESSOR.

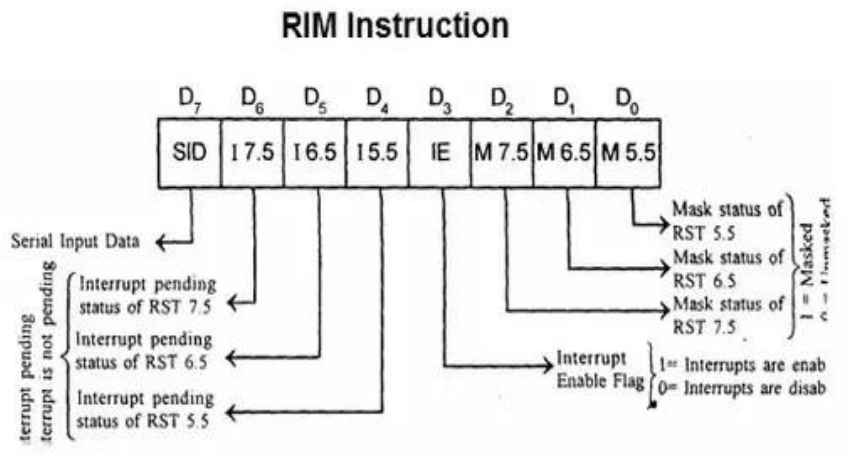
- **MASKABLE AND NON-MASKABLE INTERRUPTS –**
  MASKABLE INTERRUPTS ARE THOSE WHICH CAN BE DISABLED OR IGNORED BY THE MICROPROCESSOR. THESE INTERRUPTS ARE EITHER EDGE-TRIGGERED OR LEVEL-TRIGGERED, SO THEY CAN BE DISABLED. *INTR*, *RST 7.5*, *RST 6.5*, *RST 5.5* ARE MASKABLE INTERRUPTS IN 8085 MICROPROCESSOR.
  NON-MASKABLE INTERRUPTS ARE THOSE WHICH CANNOT BE DISABLED OR IGNORED BY MICROPROCESSOR. *TRAP* IS A NON-MASKABLE INTERRUPT. IT CONSISTS OF BOTH LEVEL AS WELL AS EDGE TRIGGERING AND IS USED IN CRITICAL POWER FAILURE CONDITIONS.
- **PRIORITY OF INTERRUPTS –**
  WHEN MICROPROCESSOR RECEIVES MULTIPLE INTERRUPT REQUESTS SIMULTANEOUSLY, IT WILL EXECUTE THE INTERRUPT SERVICE REQUEST (ISR) ACCORDING TO THE PRIORITY OF THE INTERRUPTS.
- EI(ENABLE INTERRUPT)
  - THIS IS A 1BYTE INSTUCTION
  - THE INSTRUCTION SETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLES THE INTERRUPT PROECSS
  - SYSTEM RESET OR AN INTERRUPT DISABLES THE INTERRUPT PROCESS
- DI(DISABLE INTERRUPT)
  - THIS IS A 1BYTE INSTRUTION
  - THE INSTRUCTION RESETS THE INTERRUPT ENABLE FLIP FLOP AND ENABLE THE INTERRUPT PROCESS
  - IT SHOULD AN INTERRUPT FROM AN OURSIDE SOURCE CAN NOT BE TOLERATED
  - SIM: SET INTERRUPR MASK. THIS 1-BYTE INSTRUCTION AND CAN BE USED FOR THREE DIFFERENT FUNCTION
    - ONE FUNCTION IS TO SET MASK FOR RST 7.5, 6.5, 5.5 INTERRUPTS.THIS INSTRUCTION READS THE CONTENT OF THE ACCUMULATOR AND ENABLES OR DISABLES THE INTERRUPTS ACCORDING TO THE CONTENT OF THE ACCUMULATOR BIT D3 IS A CONTROL BIT ABD SHOULD =1 FOR BITS D0, D1, AND D2 TO BE EFFECTIVE.LOGIC 0 ON D0, D1, AND D2 WILL ENBLE THE CORRESPODING INTERRUPTS ABD LOGIC 1 WILL DISABLE THE INTERRUPTS.
    - THE SECOND FUNCTION IS TO RESET RST 7.5, FLIP FLOP.BIT D4 IS ADDITIONAL CONTROL FOR RST 7.5. IF D4=1, RST 7.5 IS RESET. THIS IS USED TO OVERRIDE RST 7.5 WITHOUT SERVICING IT.
    - THE THIRD FUNCTION IS TO IMPLEMENT SERIAL I/O. BITS D7 AND D6 OF THE ACCUMULATOR ARE USED FOR SERIAL I/O AND DO NOT AFFECT THE INTERRUPTS. BIT D6=1 ENABLES THE SERIAL I/O AND BIT D7 IS USED TO TRANSMIT BITS.

SIM Instruction



- RIM (READ INTERRUPT MASK):

- TO READ INTERRUPT MASKS. THIS INSTRUCTION LOADS THE ACCUMULATOR WITH 8 BITS INDICATING THE CURRENT STATUS OF THE INTERRUPT MASKS.
- TO IDENTIFY PENDING INTERRUPTS, BITS D4, D5 AND D6 IDENTIFY THE PENDING INTERRUPT.
- TO RECEIVE SERIAL DATA, BITS D7 IS USED TO RECEIVE SERIAL DATA



74) WHITE A PROGRAM USING 8085 INSTRUCTION TO CLEAR ALL FLAGS?

- LXI H, 0000H
  PUSH H
  POP PSW

75) HOW TO CLEAR CY FLAG?

- CLC / MVO A,00 H / ANI FE H

76) HOW TO CLEAR ALL FLAGS?

- LXI H,2050H
  MOV A, M
  ANI 00H
  STA 2000 H
  HLT

77) SIMULATE XCHG USING MOV INSTRUCTION?

- MOV C, A
  MOV A, B
  MOV B, C

78) WRITE DIFFERENT JUMP INSTRUCTION?

- DIFFERENT JUMP INSTRUCTIONS ARE-
  1) JC (JUMP IF CARRY):-THE PROGRAM SEQUENCE IS TRANSFERRED TO A PARTICULAR LEVEL OR A 16 BIT ADDRESS IF C=1.

2) JNC (JUMP IF NOT CARRY):- THE PROGRAM SEQUENCE IS TRANSFERRED TO A PARTICULAR LEVEL OR A 16 BIT ADDRESS IF C=O.
3) JZ (JUMP IF ZERO):- THE PROGRAM SEQUENCE IS TRANSFERRED TO A PARTICULAR LEVEL OR A 16 BIT ADDRESS IF Z=1.
4) JNZ (JUMP IS NOT ZERO):- THE PROGRAM SEQUENCE IS TRANSFERRED TO A PARTICULAR LEVEL OR 16 BIT ADDRESS IF Z=0.

79) WHAT IS VECTORED INTERRUPT? GIVE AN EXAMPLE?

VECTORED INTERRUPT ARE THOSE WHICH HAVE FIXED VECTOR ADDRESS(STARTING ADDRESS OF SUB –ROUTINE) AND AFTER EXECUTING THESE, PROGRAM CONTROL IS TRANSFERRED TO THAT ADDRESS.

THE 8085 HAS FIVE INTERRUPT INPUTS. ONE IS CALLED INTR, THREE ARE CALLED RST 5.5, 6.6 AND 7.5 RESPECTIVELY AND THE FIFTH IS CALLED TRAP, A NONMASKABLE INTERRUPT. THESE LAST FOUR ARE AUTOMATICALLY VECTORED TO SPECIFIED LOCATIONS ON MEMORY PAGE 00H WITHOUT ANY EXTERNAL HARDWARE. THEY DO NOT REQUIRE INTA SIGNAL OR AN INPUT PORT; THE NECESSARY HARDWARE IS ALREADY IMPLEMENTED INSIDE THE 8085.