FPGA Microcontroller

This document is to introduce the side project named FPGA Microcontroller. This side project is implemented by this development board and it covers the block diagram, FPGA IO pin descriptions, and testing results. However, this project hasn't been complete and there're still some issues that are under troubleshooting by myself. Anyway, it's a draft of this side project.

Outline

- ✓ Block Diagram of Side Project
- ✓ FPGA IO Pinout Description
- ✓ Test Result of Each Modules

Block Diagram of Side Project

The FPGA consists of several modules, uart controller, I2Cbus controller, SPIbus controller, VGA Controller and BCD debugging module for debugging only. Each modules have responsible dedicated input and output port assigned by the top module. Also, the i_clk refers to a system clock running 100Mhz around and i_rst_n is for reset function to the FPGA.

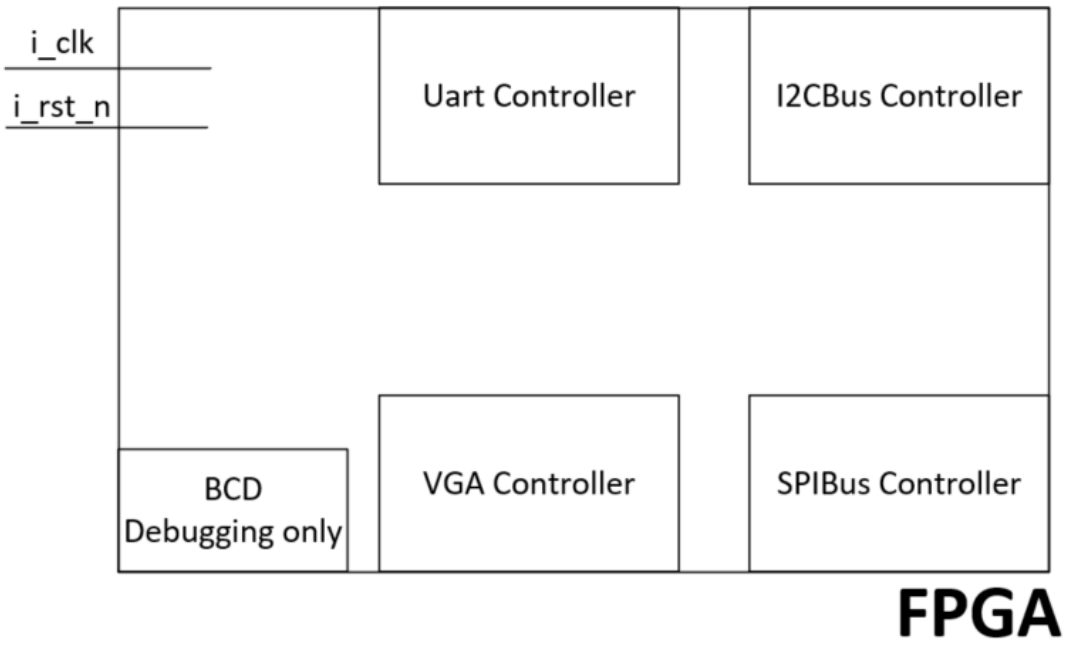

Figure 1

FPGA IO Pinout Descriptions

There's a picture to show the whole pinout assignments on this project. Also, a following table gives the descriptions and functions for each pinout. Please refer to the figure 2 and table 1 for more information.

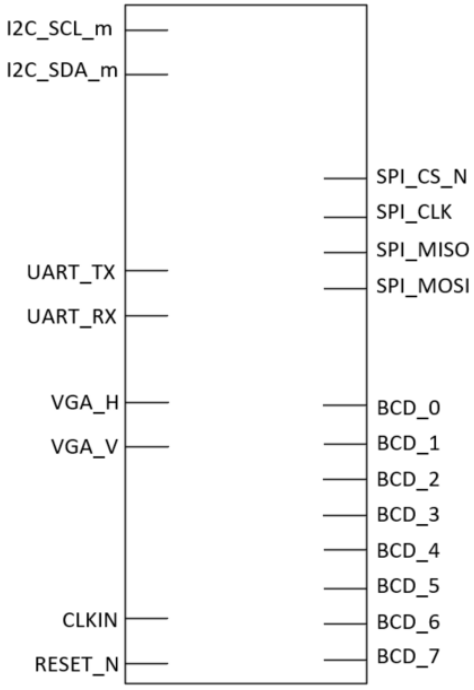

Figure 2

Pinout Name	IO Type	Voltage Level	Description
CLKIN	Input	3.3v	System clock input with 100Mhz
RESET_N	Input	3.3v	System reset input, low active.
UART_TX	Output	3.3v	Transmitter of uart module. Recommend to run 115200 baudrate.
UART_RX	Input	3.3v	Receiver of uart module. Recommend to run 115200 baudrate.
I2C_SCL_m	Bi-directional, open drain	External VCC	Master of I2Cbus, I2C clock pin.
I2C_SDA_m	Bi-directional, open drain	External VCC	Master of I2Cbus, I2C data pin.
SPI_CS_N	Output	3.3v	Master of SPIbus, chip select.
SPI_CLK	Output	3.3v	Master of SPIbus, SPI clock.
SPI_MISO	Input	3.3v	Master of SPIbus, SPI MISO.
SPI_MOSI	Output	3.3v	Master of SPIbus, SPI MOSI.
VGA_H	Output	3.3v	VGA horizon display pin.
VGA_V	Output	3.3v	VGA vertical display pin.
BCD_0~7	Output	3.3v	BCD to display seven segments for debugging only.

Table 1

Test Results of Each Module

This session will show some testing results through putty or 3rd tool, AccessPort to see if the following communication and function are working or not.

UART Controller Module

Send testing data from PC and wait for the same sent from FPGA to PC side through Accessport to see whether tx_uart and rx_uart are working or not. Also, make sure that the COM port selected is correct and baudrate is 115200 from the setting window.

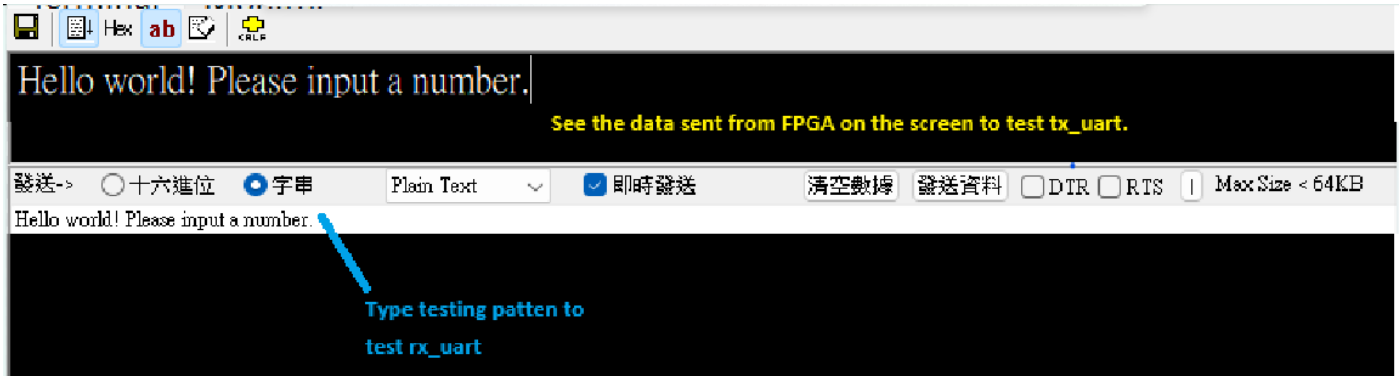

Figure 3

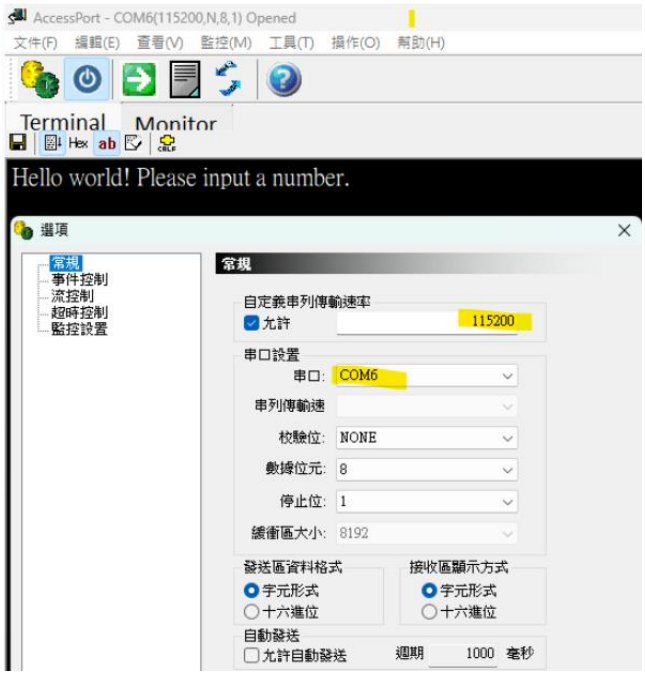

Figure 4

I2Cbus Controller Module

Try to read data from an EEPROM, AT24C02. The slave address of AT24C20 is 0x50h

SPI bus Controller Module

Try to read status registers from SPI flash, W25Q32JV.

VGA Controller Module

Try to enable VGA Monitor with a bule, red and green background.