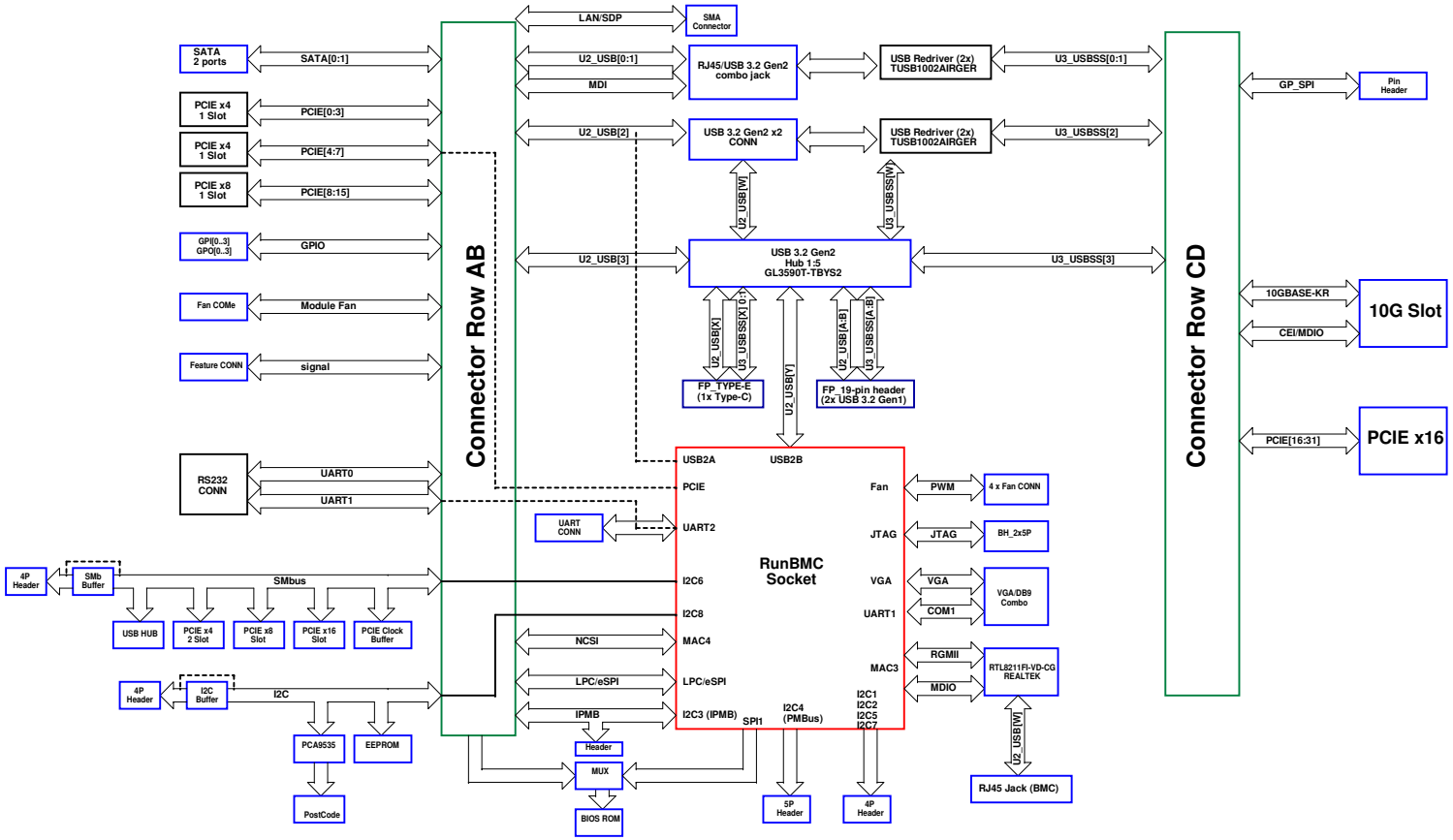
Express-BASE7 R3.1 Rev.A1

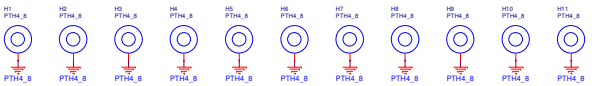
COM-Express Base Board
PICMG COM.0 Rev 3.1

PCB Size : 304.8 mm x 243.84 mm (12000mils x 9600mils)

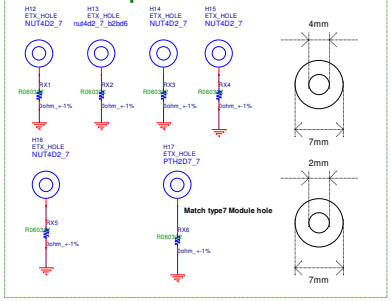
ADLINK P/N : 77109-0A10-A0

Block Diagram





COM-Express Screw Hole



Page

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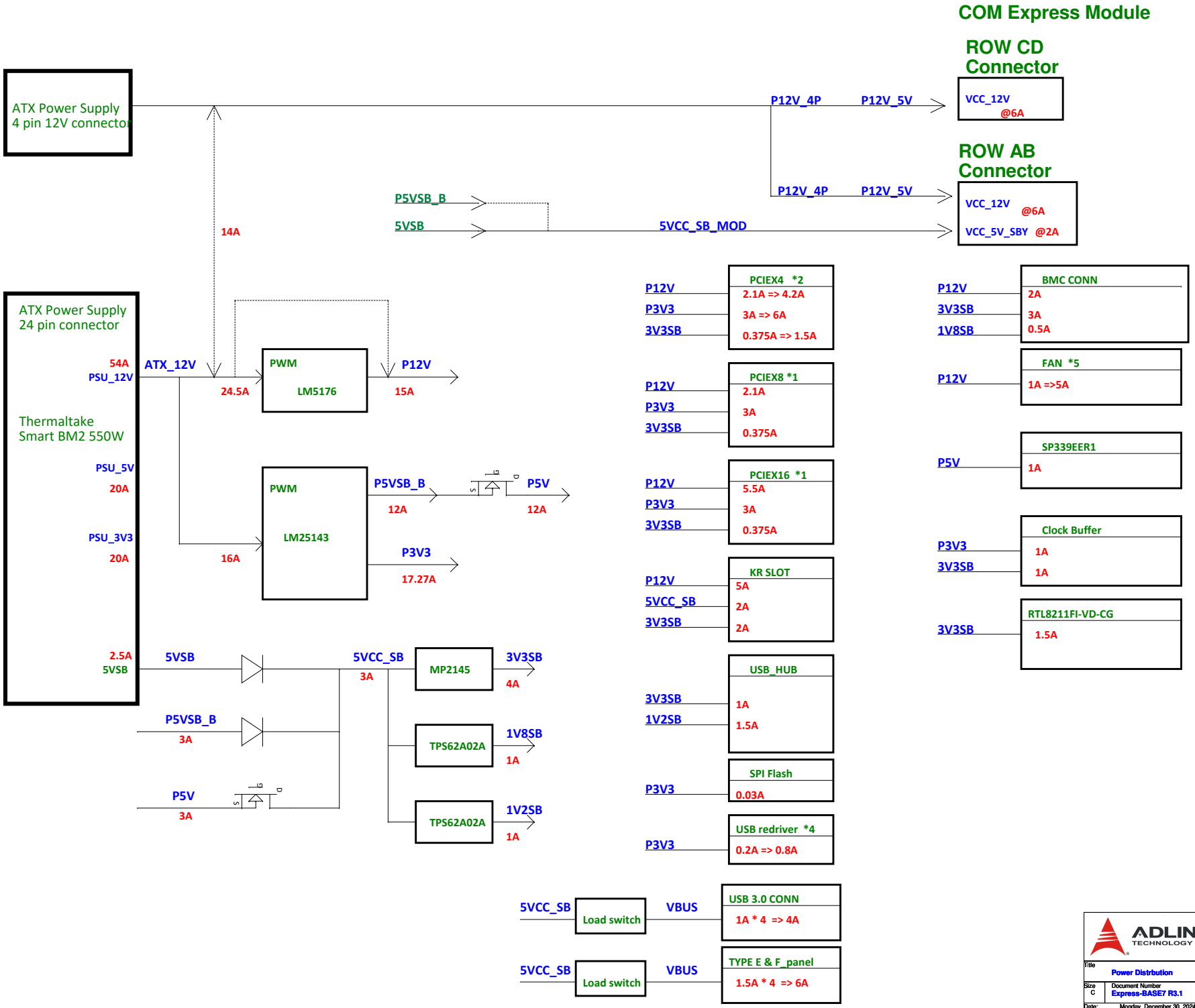
Title: Cover Page & BLOCK Diagrams

Size: D | Document Number: Express-BASE7 R3.1 | Rev: A1

Date: Monday, December 30, 2024 | Sheet 1 of 39


COM Express Module
ROW CD Connector
VCC_12V
@6A
ROW AB Connector
VCC_12V
@6A
VCC_5V_SBY @2A
ATX Power Supply
4 pin 12V connector
P12V_4P
P12V_5V
P12V_4P
P12V_5V
P5VSB_B
5VSB
5VCC_SB_MOD
14A
ATX Power Supply
24 pin connector
54A
PSU_12V
ATX_12V
24.5A
PWM
LM5176
P12V
15A
Thermaltake
Smart BM2 550W
PSU_5V
20A
PSU_3V3
20A
PWM
LM25143
16A
P5VSB_B
12A
P5V
12A
P3V3
17.27A
2.5A
5VSB
5VSB
5VCC_SB
3A
MP2145
3V3SB
4A
P5VSB_B
3A
TPS62A02A
1V8SB
1A
P5V
3A
TPS62A02A
1V2SB
1A
P12V
P3V3
3V3SB
PCIEX4 *2
2.1A => 4.2A
3A => 6A
0.375A => 1.5A
P12V
P3V3
3V3SB
PCIEX8 *1
2.1A
3A
0.375A
P12V
P3V3
3V3SB
PCIEX16 *1
5.5A
3A
0.375A
P12V
5VCC_SB
3V3SB
KR SLOT
5A
2A
2A
3V3SB
1V2SB
USB_HUB
1A
1.5A
P3V3
SPI Flash
0.03A
P3V3
USB redriver *4
0.2A => 0.8A
5VCC_SB
Load switch
VBUS
USB 3.0 CONN
1A * 4 => 4A
5VCC_SB
Load switch
VBUS
TYPE E & F_panel
1.5A * 4 => 6A
P12V
3V3SB
1V8SB
BMC CONN
2A
3A
0.5A
P12V
FAN *5
1A =>5A
P5V
SP339EER1
1A
P3V3
3V3SB
Clock Buffer
1A
1A
3V3SB
RTL8211FI-VD-CG
1.5A
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Title
Power Distrbution
Size
C
Document Number
Express-BASE7 R3.1
Rev
A1
Date:
Monday, December 30, 2024
Sheet
2
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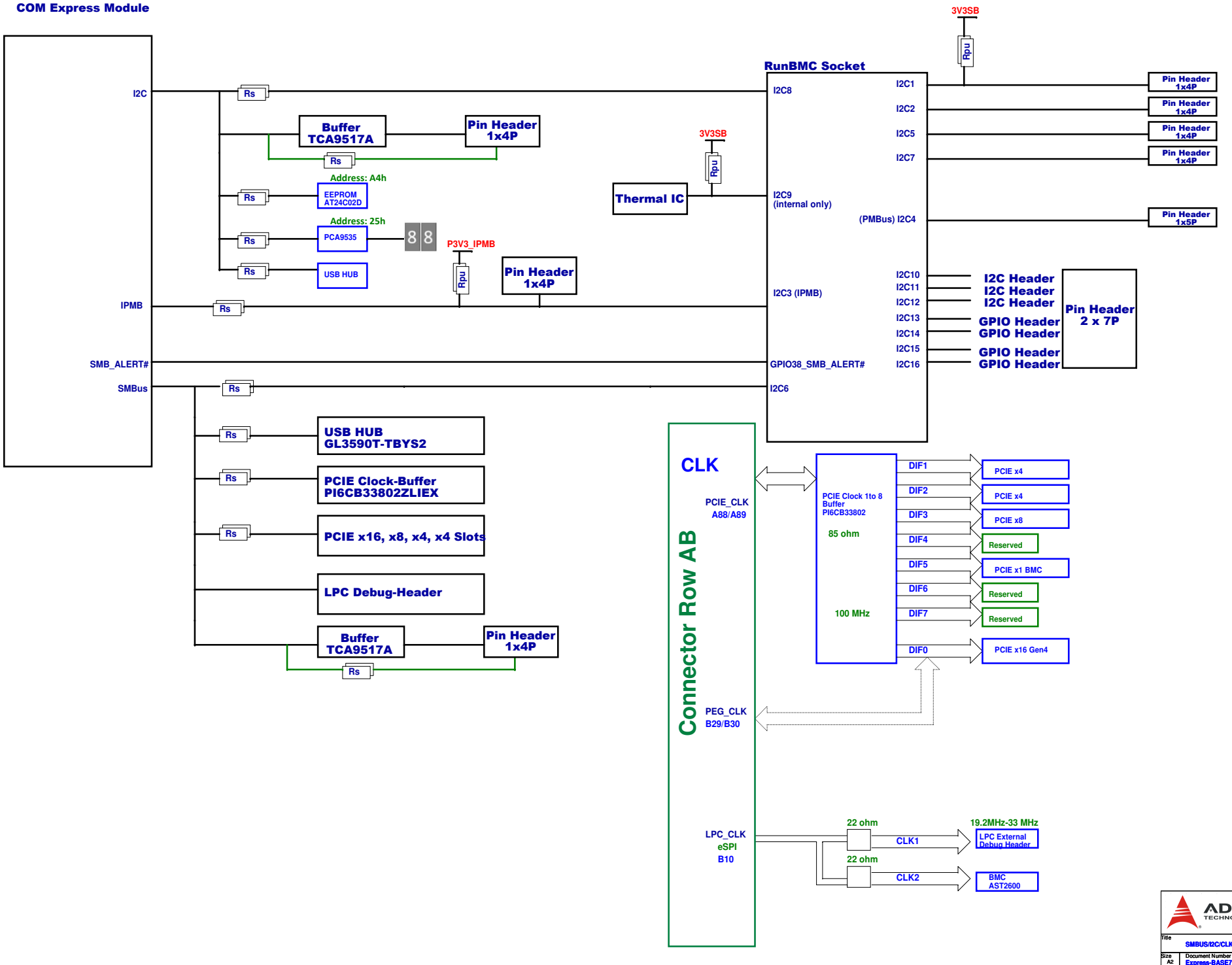
39



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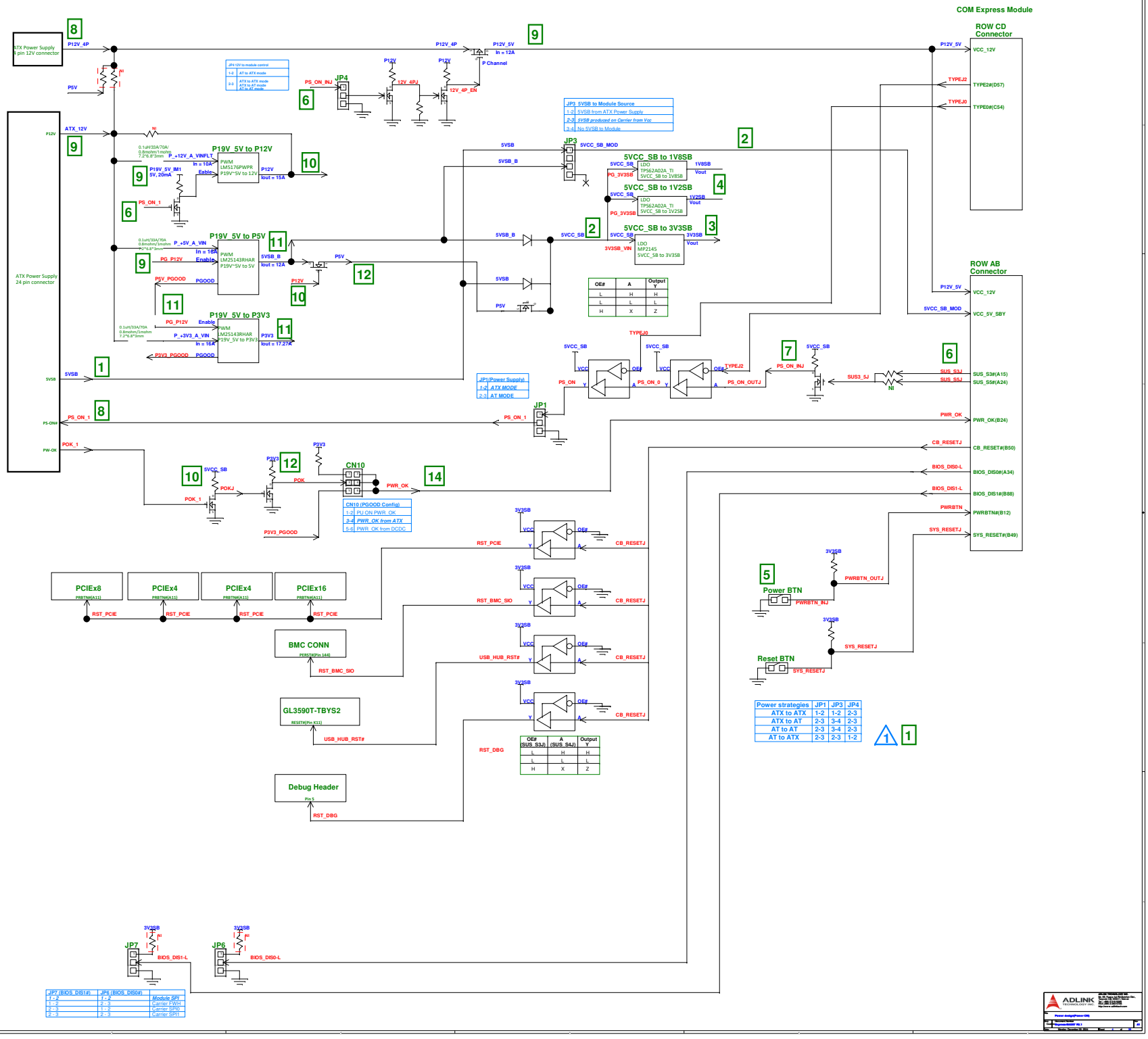
Title	SMBUS/I2C/CLK Design	
Size A2	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 3 of 39	


COM Express Module
ROW CD Connector
ROW AB Connector
ATX Power Supply 4 pin 12V connector
ATX Power Supply 24 pin connector
P12V_4P
P12V_5V
In = 12A
P Channel
P5V
ATX_12V
P19V_5V to P12V
P19V_5V to P5V
P19V_5V to P3V3
5VCC_SB to 1V8SB
5VCC_SB to 1V2SB
5VCC_SB to 3V3SB
JP1(Power Supply)
1-2 ATX MODE
2-3 AT MODE
JP3 5VSB to Module Source
1-2 5VSB from ATX Power Supply
2-3 5VSB produced on Carrier from Vcc
3-4 No 5VSB to Module
JP4 12V to module control
1-2 AT to ATX mode
2-3 ATX to ATX mode / ATX to AT mode / AT to AT mode
CN10 (PGOOD Config)
1-2 PU ON PWR_OK
3-4 PWR_OK from ATX
5-6 PWR_OK from DCDC
PS_ON_INJ
PS_ON_1
POK_1
PWR_OK
PCIEx8
PCIEx4
PCIEx4
PCIEx16
RST_PCIE
BMC CONN
RST_BMC_SIO
GL3590T-TBYS2
USB_HUB_RST#
Debug Header
RST_DBG
Power BTN
PWRBTN_INJ
PWRBTN_OUTJ
Reset BTN
SYS_RESETJ
CB_RESETJ
BIOS_DIS0-L
BIOS_DIS1-L
PWRBTN
SYS_RESET
SUS3_5J
SUS_S3J
SUS_S5J
JP7 (BIOS_DIS1#)
JP6 (BIOS_DIS0#)
1 - 2 Module SPI
1 - 2 2 - 3 Carrier FWH
2 - 3 1 - 2 Carrier SPI0
2 - 3 2 - 3 Carrier SPI1
Power strategies JP1 JP3 JP4
ATX to ATX 1-2 1-2 2-3
ATX to AT 2-3 3-4 2-3
AT to AT 2-3 3-4 2-3
AT to ATX 2-3 2-3 1-2
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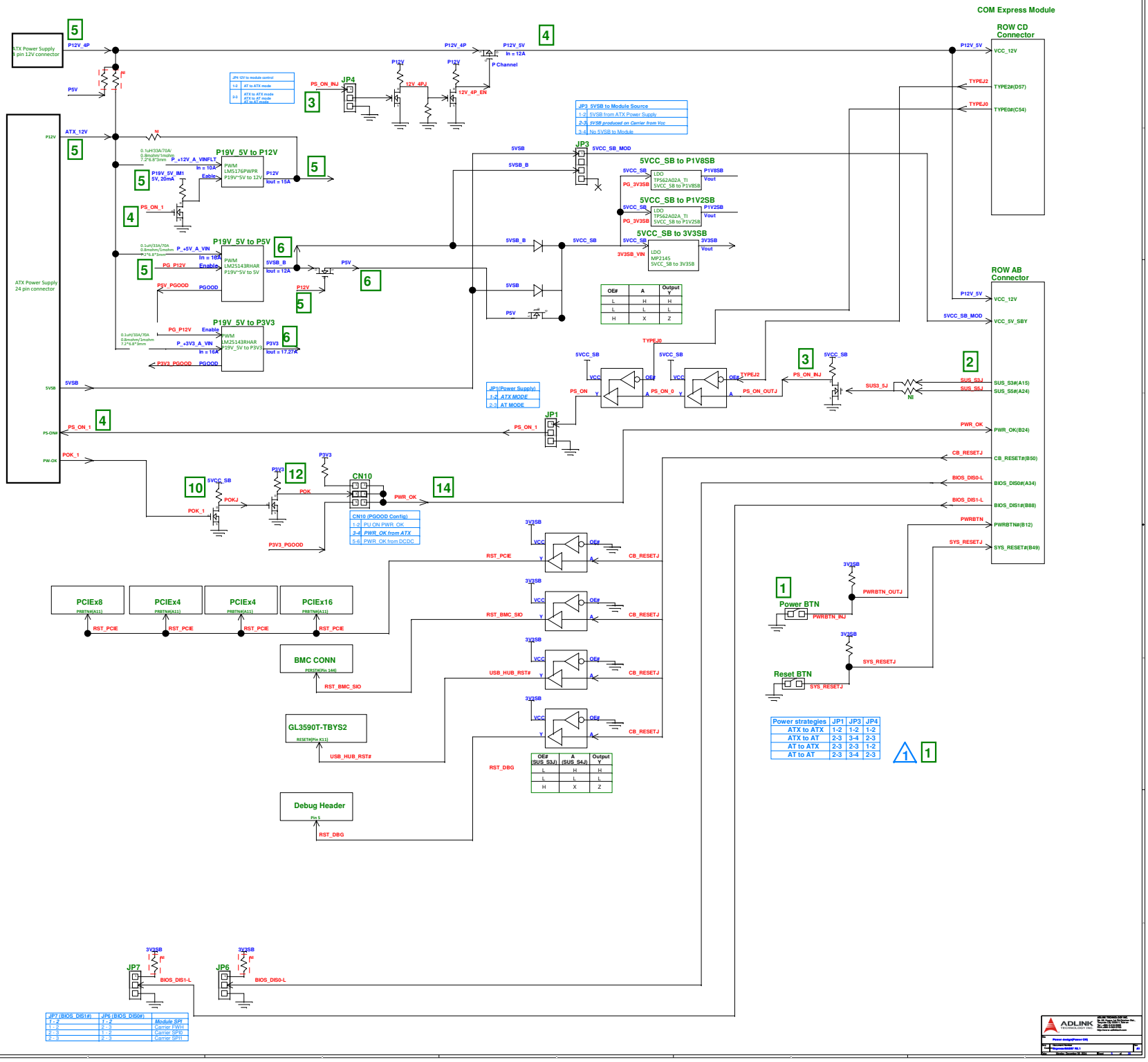
COM Express Module
ROW CD Connector
ROW AB Connector
ATX Power Supply 4 pin 12V connector
ATX Power Supply 24 pin connector
P12V_4P
P12V_5V
In = 12A
P Channel
P5V
ATX_12V
PS_ON_INJ
JP4
12V_4P_EN
JP3_5VSB to Module Source
1-2 5VSB from ATX Power Supply
2-3 5VSB produced on Carrier from Vcc
3-4 No 5VSB to Module
P19V_5V to P12V
P19V_5V to P5V
P19V_5V to P3V3
PWM
LM25143RHAR
P19V~5V to 5V
P19V~5V to P3V3
P19V_5V_IM1
5V, 20mA
PS_ON_1
PG_P12V
PGOOD
P5V_PGOOD
P3V3_PGOOD
P_+12V_A_VINFLT
P_+5V_A_VIN
P_+3V3_A_VIN
In = 10A
In = 16A
Enable
P12V
P5V
P3V3
5VSB
5VSB_B
5VCC_SB
5VCC_SB_MOD
5VCC_SB to P1V8SB
5VCC_SB to P1V2SB
5VCC_SB to 3V3SB
LDO
TPS62A02A_TI
5VCC_SB to P1V8SB
5VCC_SB to P1V2SB
LDO
MP2145
5VCC_SB to 3V3SB
PG_3V3SB
3V3SB_VIN
P1V8SB
P1V2SB
3V3SB
Vout
OE# | A | Output Y
L | H | H
L | L | L
H | X | Z
JP1(Power Supply)
1-2 ATX MODE
2-3 AT MODE
JP1
PS_ON_1
PS_ON
PS_ON_0
PS_ON_OUTJ
TYPEJ0
TYPEJ2
SUS3_5J
SUS_S3J
SUS_S5J
SUS_S3#(A15)
SUS_S5#(A24)
VCC_12V
VCC_5V_SBY
TYPEJ2
TYPE2#(D57)
TYPEJ0
TYPE0#(C54)
PWR_OK
PWR_OK(B24)
CB_RESETJ
CB_RESET#(B50)
BIOS_DIS0-L
BIOS_DIS0#(A34)
BIOS_DIS1-L
BIOS_DIS1#(B88)
PWRBTN
PWRBTN#(B12)
SYS_RESETJ
SYS_RESET#(B49)
POK_1
POKJ
POK
CN10
CN10 (PGOOD Config)
1-2 PU ON PWR_OK
3-4 PWR_OK from ATX
5-6 PWR_OK from DCDC
PCIEx8
PCIEx4
PCIEx4
PCIEx16
PRBTN#(A11)
RST_PCIE
BMC CONN
PRBTN#(Pin 144)
RST_BMC_SIO
GL3590T-TBYS2
RESET#(Pin K11)
USB_HUB_RST#
Debug Header
Pin 5
RST_DBG
Power BTN
PWRBTN_INJ
PWRBTN_OUTJ
Reset BTN
SYS_RESETJ
Power strategies | JP1 | JP3 | JP4
ATX to ATX | 1-2 | 1-2 | 1-2
ATX to AT | 2-3 | 3-4 | 2-3
AT to ATX | 2-3 | 2-3 | 1-2
AT to AT | 2-3 | 3-4 | 2-3
JP7 (BIOS_DIS1#) | JP6 (BIOS_DIS0#)
1 - 2 | 1 - 2 | Module SPI
1 - 2 | 2 - 3 | Carrier FWH
2 - 3 | 1 - 2 | Carrier SPI0
2 - 3 | 2 - 3 | Carrier SPI1
JP7
JP6
3V3SB
BIOS_DIS1-L
BIOS_DIS0-L
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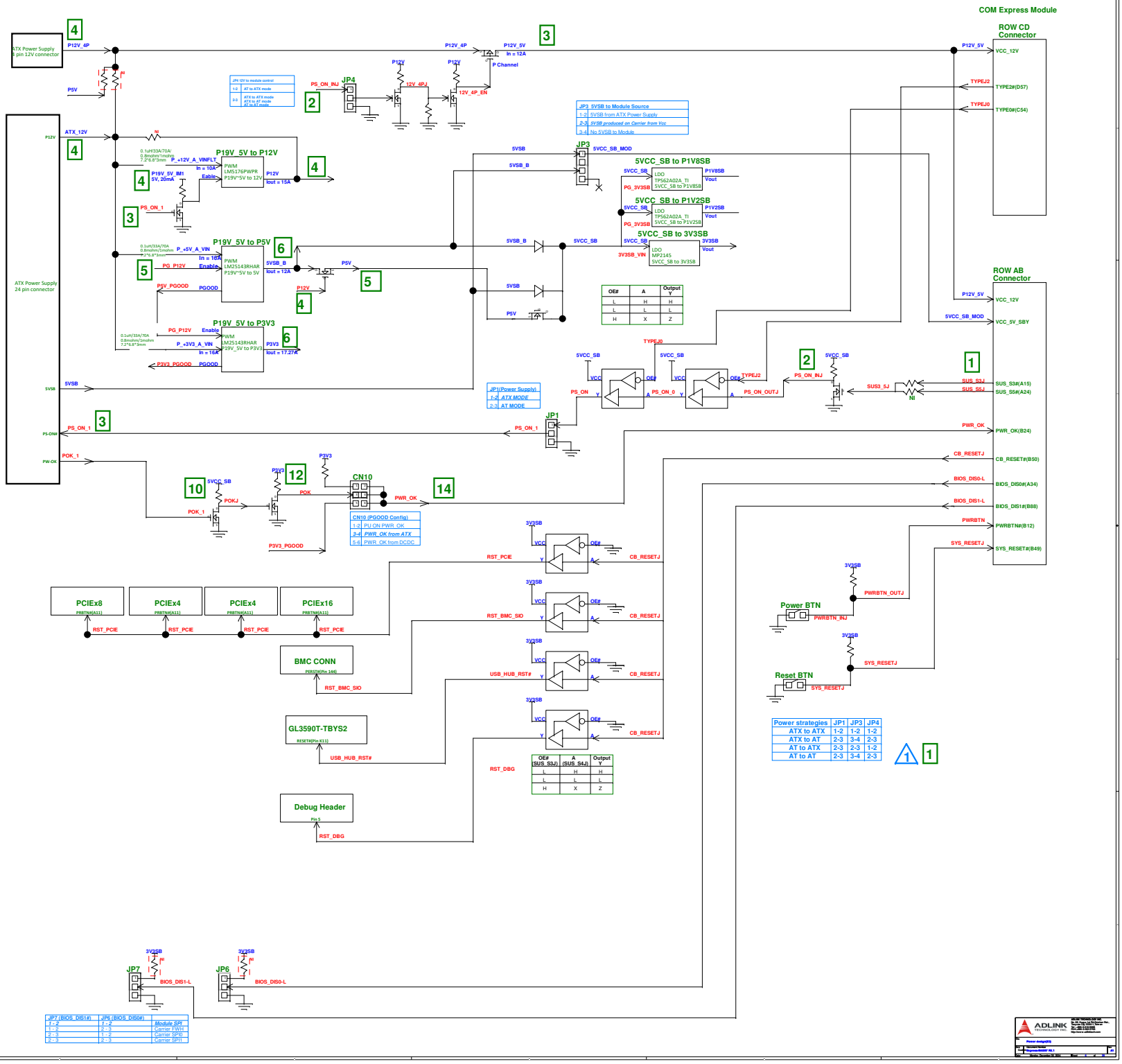
COM Express Module
ROW CD Connector
ROW AB Connector
ATX Power Supply 4 pin 12V connector
ATX Power Supply 24 pin connector
P12V_4P
P12V_5V
P5V
ATX_12V
P19V_5V to P12V
P19V_5V to P5V
P19V_5V to P3V3
PWM LM5176PWPR P19V~5V to 12V
PWM LM25143RHAR P19V~5V to 5V
PWM LM25143RHAR P19V_5V to P3V3
P12V_4PJ
12V_4P_EN
P Channel
In = 12A
In = 10A
In = 16A
Iout = 15A
Iout = 12A
Iout = 17.27A
Enable
PGOOD
PG_P12V
P5V_PGOOD
P3V3_PGOOD
P_+12V_A_VINFLT
P_+5V_A_VIN
P_+3V3_A_VIN
P19V_5V_IM1
5V, 20mA
JP4 12V to module control
1-2 AT to ATX mode
3-3 ATX to ATX mode / ATX to AT mode / AT to AT mode
PS_ON_INJ
JP3_5VSB to Module Source
1-2 5VSB from ATX Power Supply
2-3 5VSB produced on Carrier from Vcc
3-4 No 5VSB to Module
5VCC_SB_MOD
5VCC_SB to P1V8SB
5VCC_SB to P1V2SB
5VCC_SB to 3V3SB
LDO TPS62A02A_TI 5VCC_SB to P1V8SB
LDO TPS62A02A_TI 5VCC_SB to P1V25B
LDO MP2145 5VCC_SB to 3V3SB
P1V8SB Vout
P1V25B Vout
3V3SB Vout
PG_3V3SB
3V3SB_VIN
OE# A Output Y
L H H
L L L
H X Z
JP1(Power Supply)
1-2 ATX MODE
2-3 AT MODE
PS_ON_OUTJ
SUS3_5J
SUS_S3J
SUS_S5J
SUS_S3#(A15)
SUS_S5#(A24)
PWR_OK
PWR_OK(B24)
CB_RESETJ
CB_RESET#(B50)
BIOS_DIS0-L
BIOS_DIS0#(A34)
BIOS_DIS1-L
BIOS_DIS1#(B88)
PWRBTN
PWRBTN#(B12)
SYS_RESETJ
SYS_RESET#(B49)
TYPEJ0
TYPEJ2
TYPE2#(D57)
TYPE0#(C54)
CN10
CN10 (PGOOD Config)
1-2 PU ON PWR_OK
3-4 PWR_OK from ATX
5-6 PWR_OK from DCDC
POK_1
POKJ
PWR_OK
RST_PCIE
RST_BMC_SIO
USB_HUB_RST#
RST_DBG
PCIEx8
PCIEx4
PCIEx4
PCIEx16
BMC CONN
GL3590T-TBYS2
Debug Header
Power BTN
Reset BTN
PWRBTN_OUTJ
PWRBTN_INJ
Power strategies JP1 JP3 JP4
ATX to ATX 1-2 1-2 1-2
ATX to AT 2-3 3-4 2-3
AT to ATX 2-3 2-3 1-2
AT to AT 2-3 3-4 2-3
JP7
JP6
BIOS_DIS1-L
BIOS_DIS0-L
JP7 (BIOS_DIS1#) JP6 (BIOS_DIS0#)
1 - 2 1 - 2 Module SPI
1 - 2 2 - 3 Carrier FWH
2 - 3 1 - 2 Carrier SPI0
2 - 3 2 - 3 Carrier SPI1
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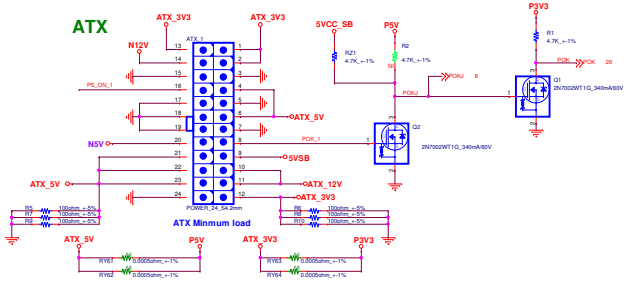
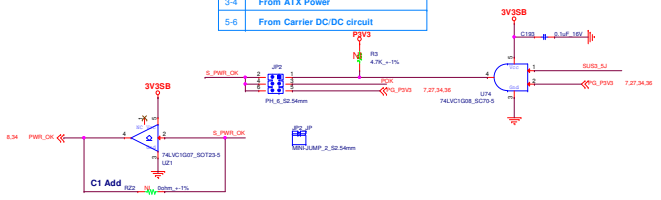
ATX



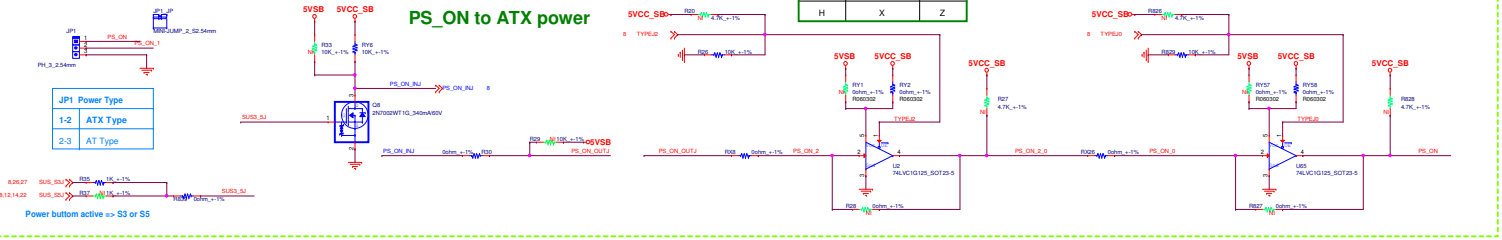
Carrier Board Power OK

JP2	PWR_OK Source
1-2	For AT to ATX mode
3-4	From ATX Power
5-6	From Carrier DC/DC circuit



OE# (TYPEJ2)	A (PS_ON_OUTJ)	Output Y
L	H	H
L	L	L
H	X	Z

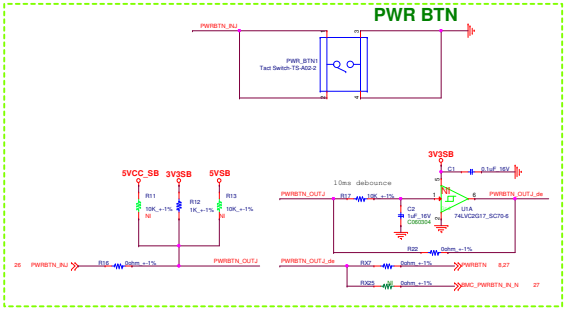
PS_ON to ATX power



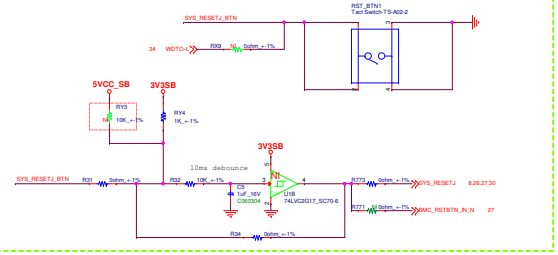
JP1	Power Type
1-2	ATX Type
2-3	AT Type

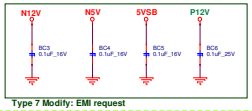
Power buttom active => S3 or S5

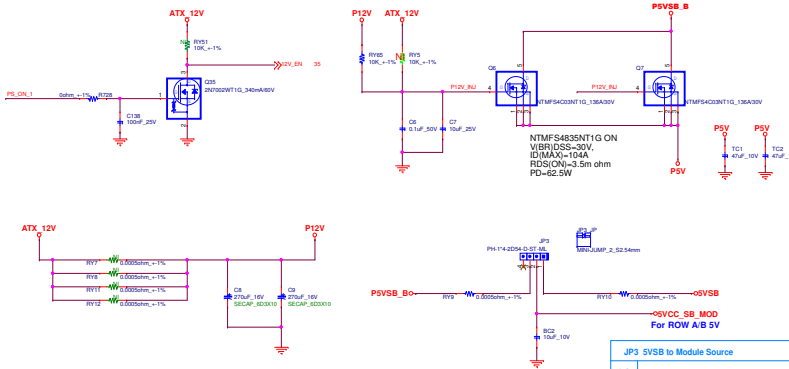
PWR BTN



RST BTN

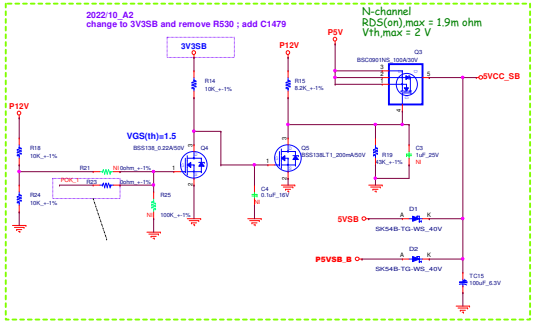




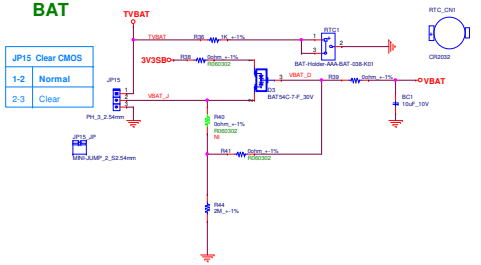


JP3	5VSB to Module Source
1-2	5VSB from ATX Power Supply
2-3	5VSB produced on Carrier from Vcc
3-4	No 5VSB to Module

Power strategies	JP1	JP2	JP3	JP4
ATX PSU / ATX to Module	1-2	3-4	1-2	2-3
ATX PSU / AT to Module	2-3	3-4	3-4	2-3
AT PSU / ATX to Module	1-2	1-2	2-3	1-2
AT PSU / ATX to Module	2-3	3-4	3-4	2-3



BAT



JP15	Clear CMOS
1-2	Normal
2-3	Clear

follow base6 R3.1 A2 & remove SIO relate schematic 2024/06/13

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Title	Power	
Size: A1	Document Number: Express-BASE7 R3.1	Rev: A1
Date: Monday, December 30, 2024	Sheet 7 of 39	

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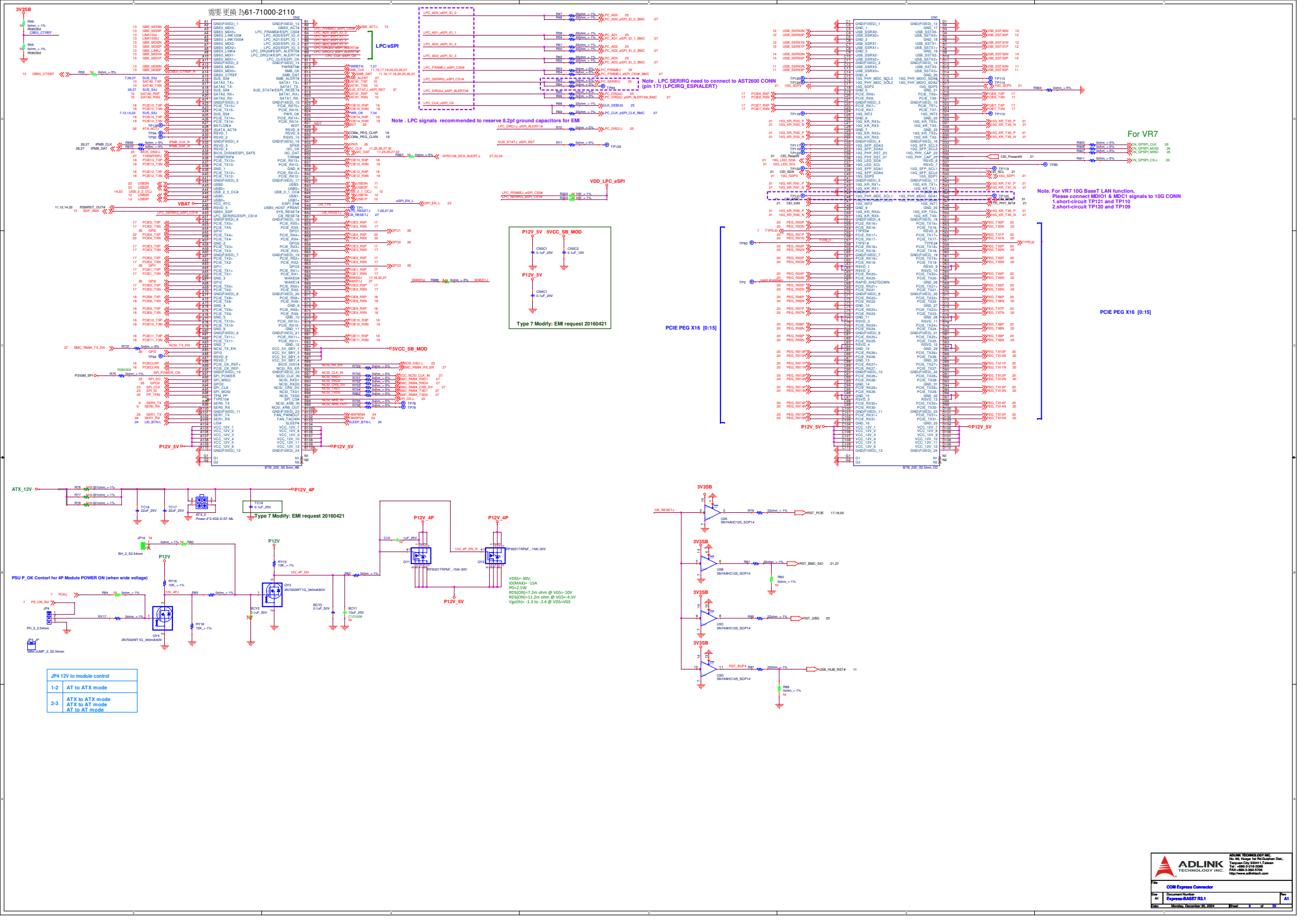
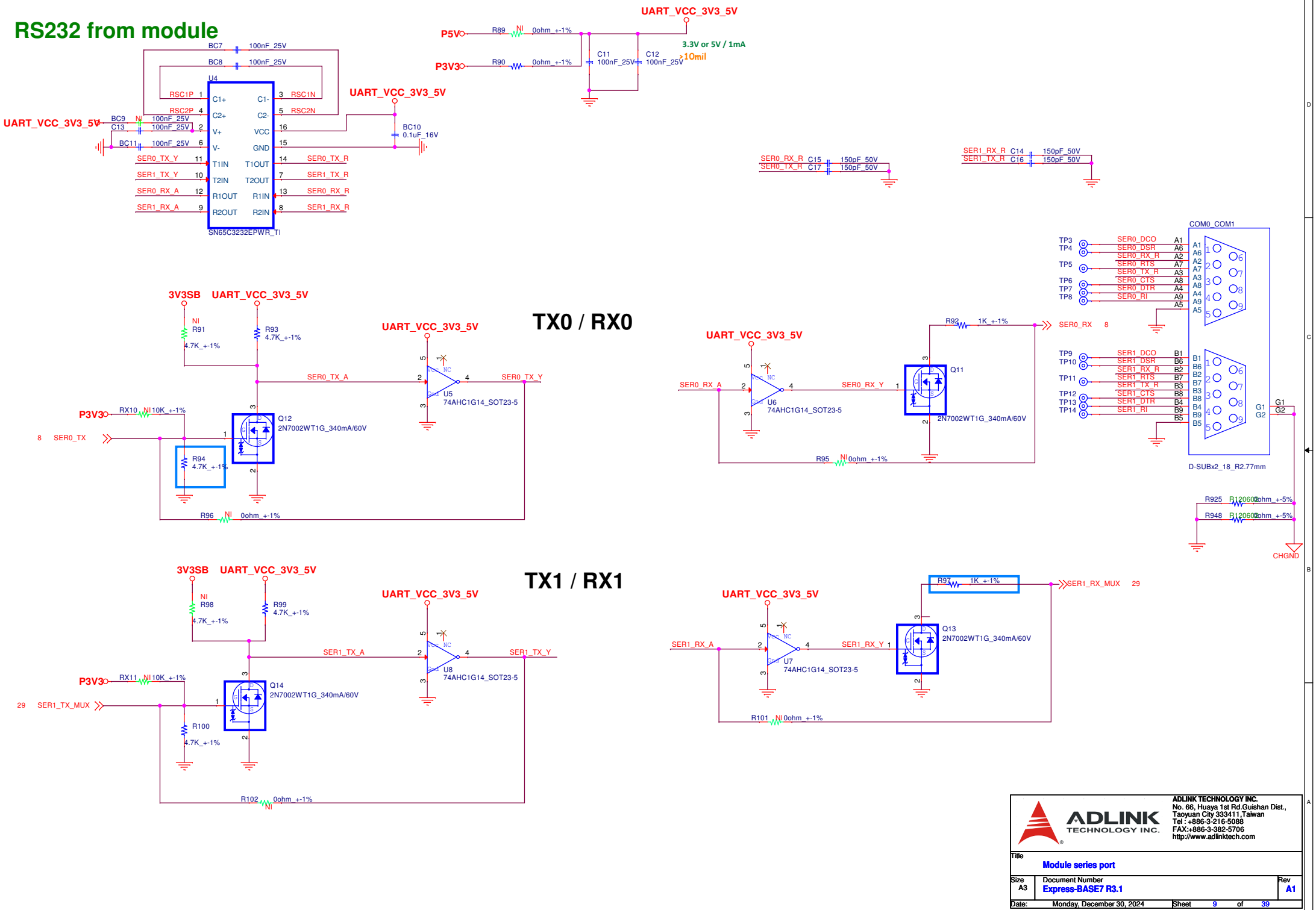


RS232 from module



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Title	Module series port	
Size A3	Document Number Express-BASE7 R3.1	Rev A1
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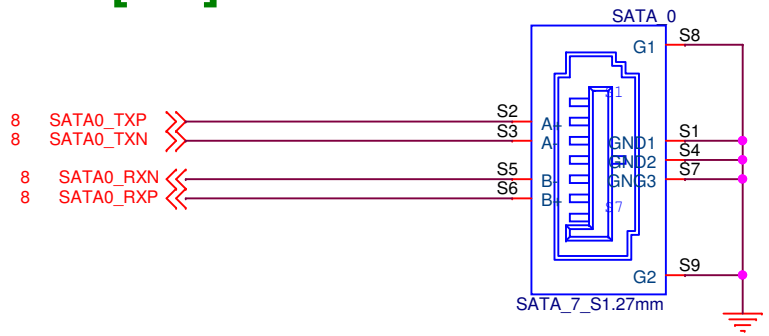
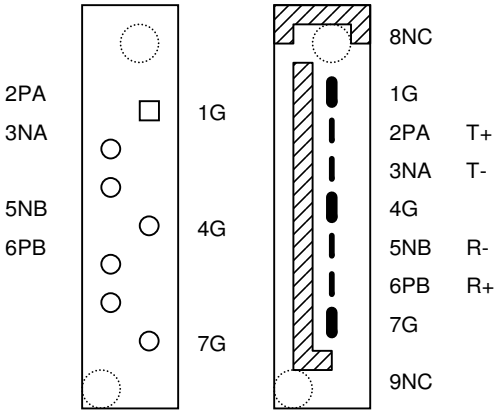
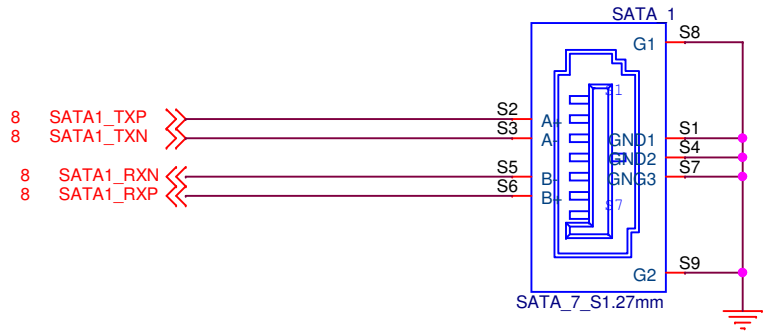
SATA [0:1]

SATA 0





SATA 1



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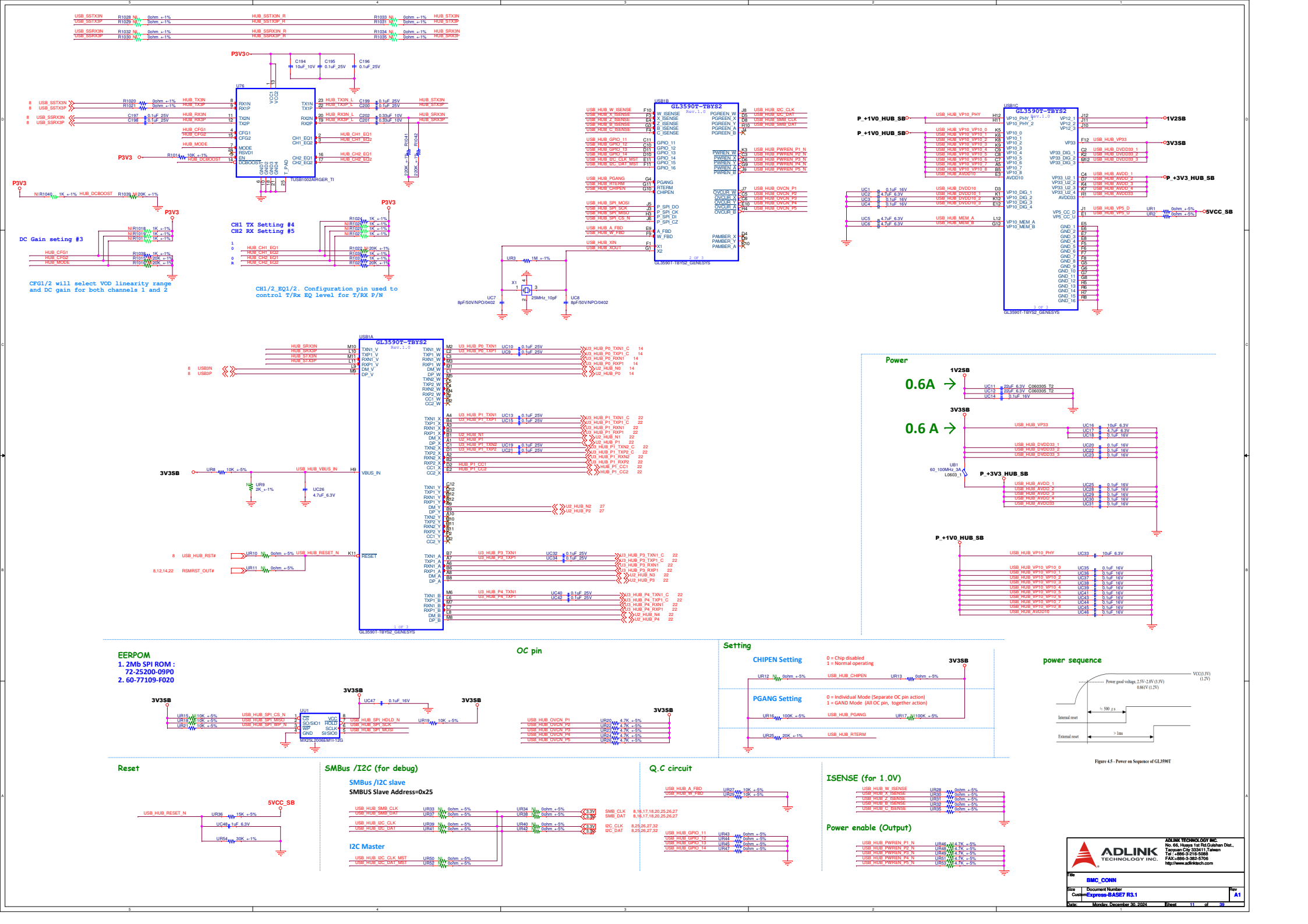
Title: SATA		
Size: A4	Document Number: Express-BASE7 R3.1	Rev: A1
Date: Monday, December 30, 2024	Sheet 10 of 39	



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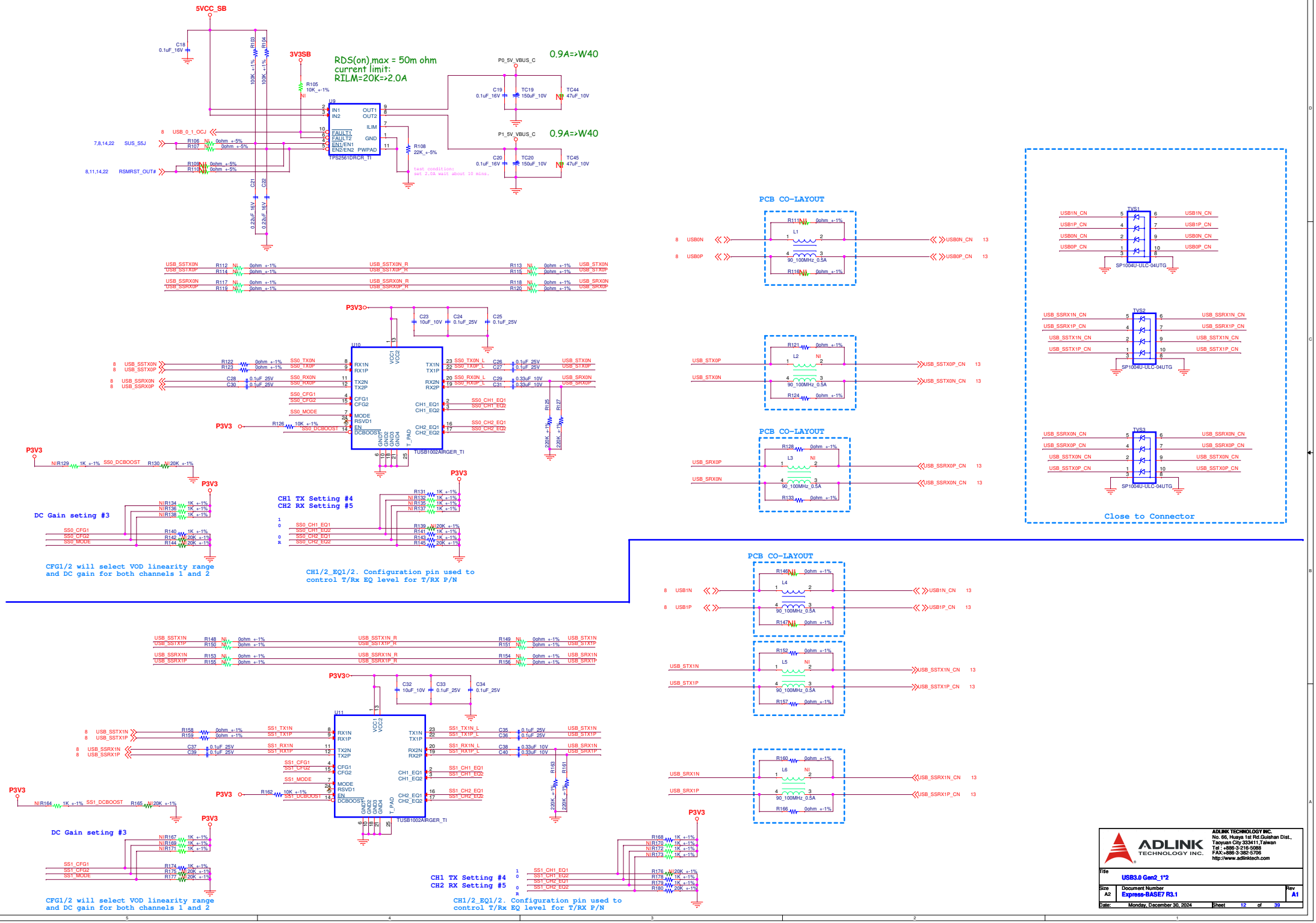
Title	BMC_CONN		
Size	Document Number		Rev
Custom	Express-BASE7 R3.1		A1
Date:	Monday, December 30, 2024	Sheet	11 of 39



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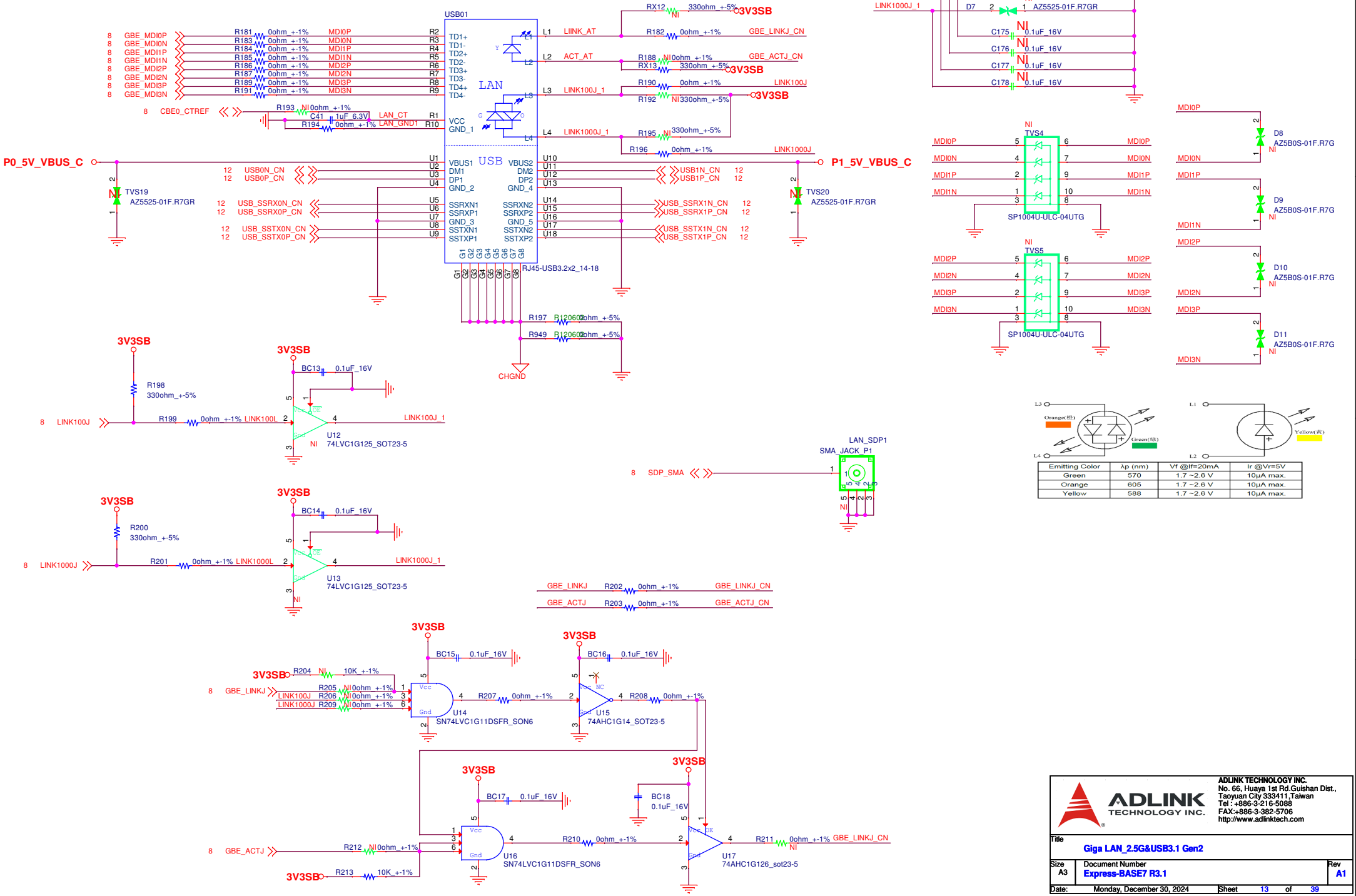
Title	USB3.0 Gen2_1*2		
Size A2	Document Number Express-BASE7 R3.1		Rev A1
Date: Monday, December 30, 2024	Sheet 12 of 39		

Giga LAN (2.5G)_RJ45+USB3.1 Gen2

USB[0:1]



Emitting Color	λp (nm)	Vf @If=20mA	Ir @Vr=5V
Green	570	1.7 ~2.6 V	10μA max.
Orange	605	1.7 ~2.6 V	10μA max.
Yellow	588	1.7 ~2.6 V	10μA max.

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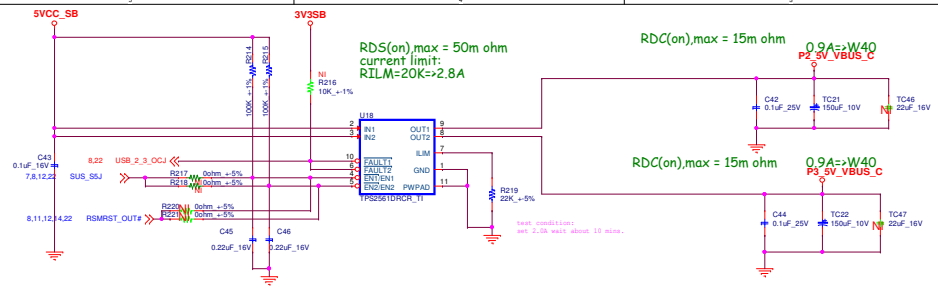
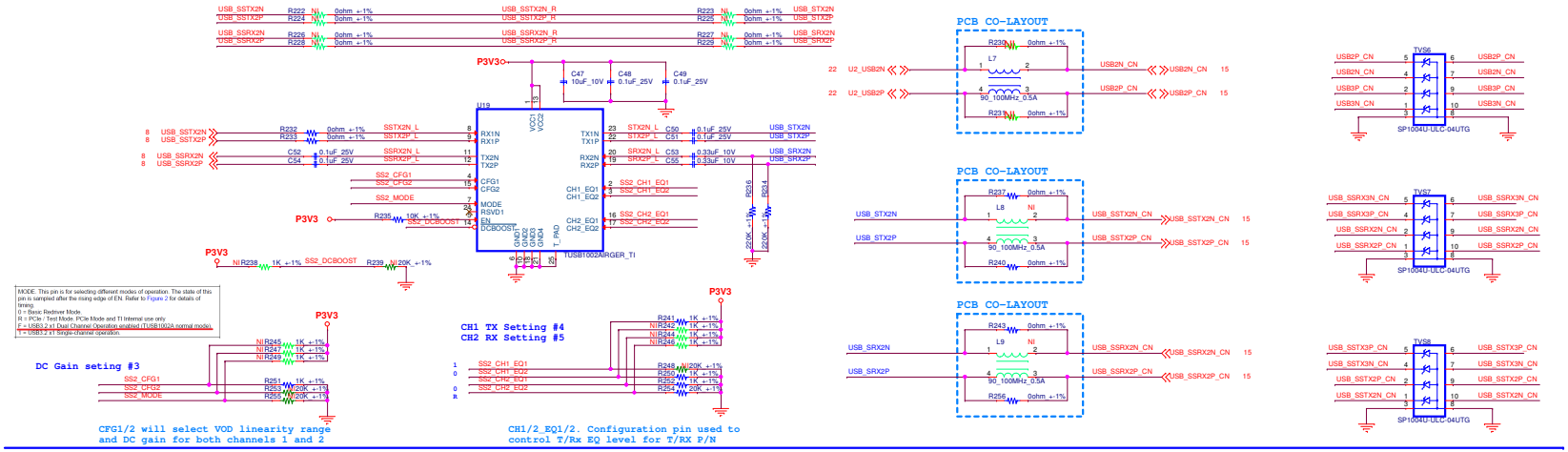
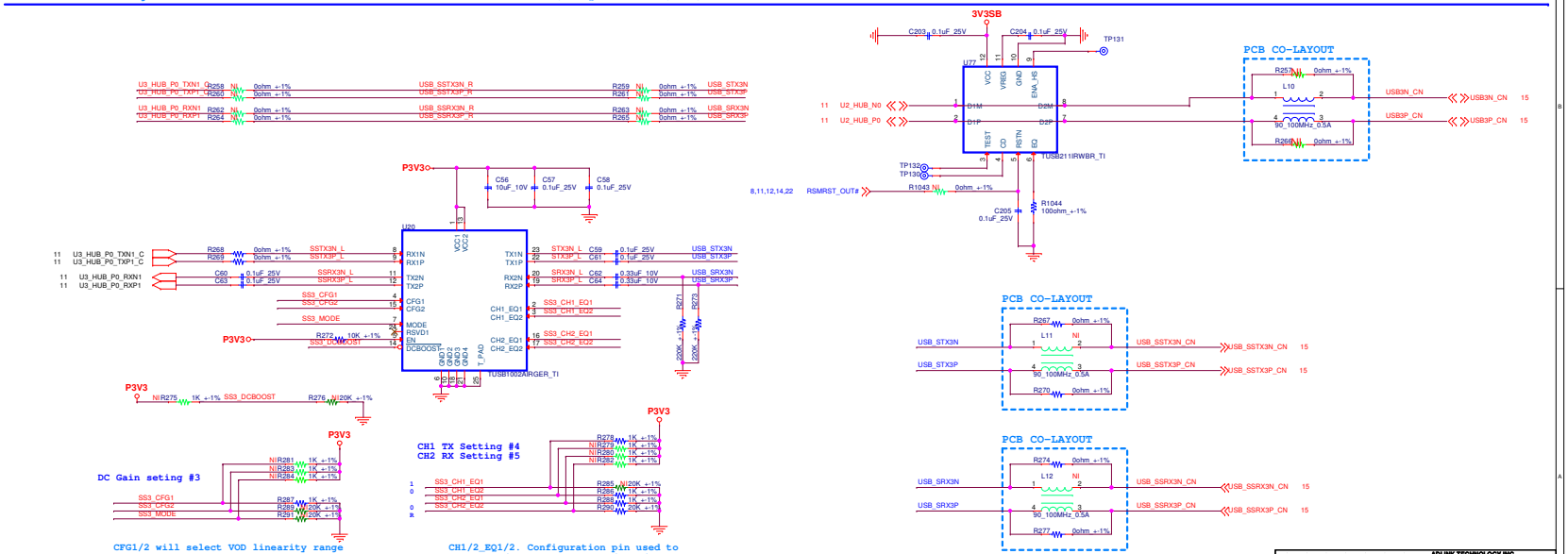
Title	Giga LAN_2.5G&USB3.1 Gen2		
Size A3	Document Number Express-BASE7 R3.1		Rev A1
Date: Monday, December 30, 2024	Sheet 13 of 39		



DEVICE (1)	AMBIENT TEMPERATURE (2)	ENABLE	SON (3) (DRC)	MARKING	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT PER CHANNEL
TPS2560	–40°C to 85°C	Active low	TPS2560DRC	2560	2.5 A
TPS2561		Active high	TPS2561DRC	2561	





MODE: This pin is for selecting different modes of operation. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing.
0 = Basic Redriver Mode.
R = PCIe / Test Mode. PCIe Mode and TI Internal use only
F = USB3.2 x1 Dual Channel Operation enabled (TUSB1002A normal mode).
1 = USB3.2 x1 Single-channel operation.

MODE: This pin is for selecting different modes of operation. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing.
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1 = USB3.2 x1 Single-channel operation.

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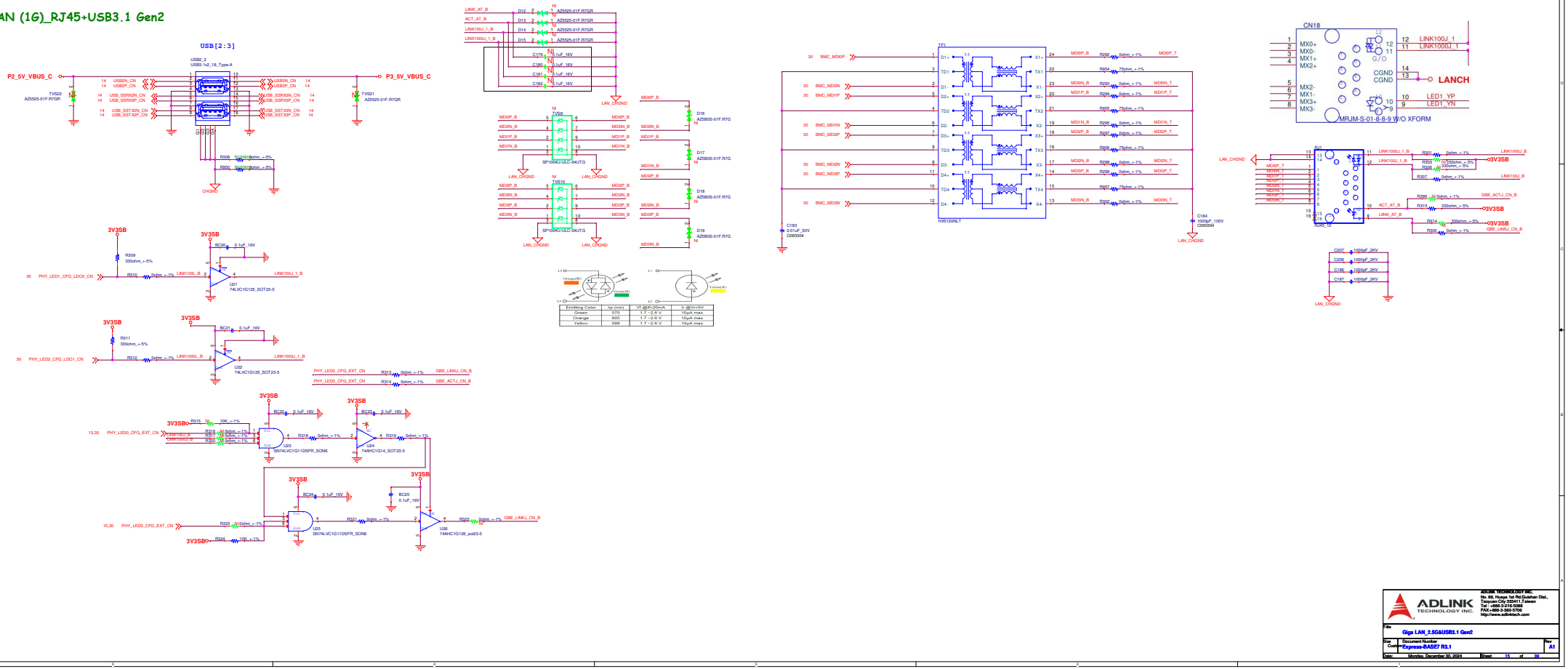
Title: USB3.0_Rear IO
Size: Custom | Document Number: Express-BASE7 R3.1 | Rev: A1
Date: Monday, December 30, 2024 | Sheet 14 of 39

Giga LAN (1G)_RJ45+USB3.1 Gen2



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Title	Giga LAN_2.5G&USB3.1 Gen2	
Size: Custom	Document Number: Express-BASE7 R3.1	Rev: A1
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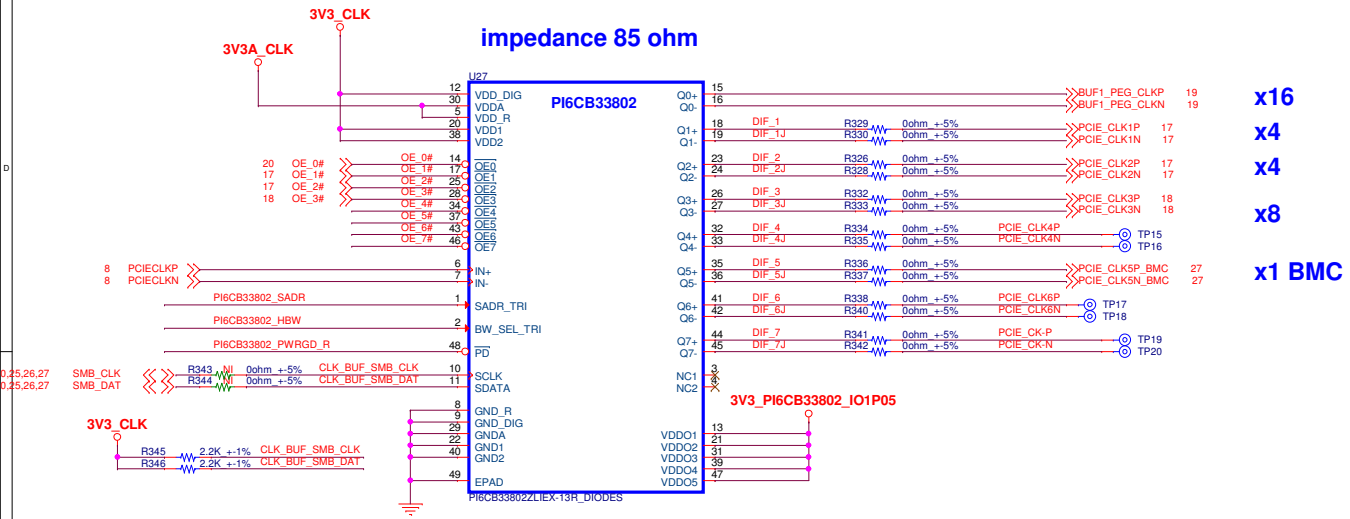
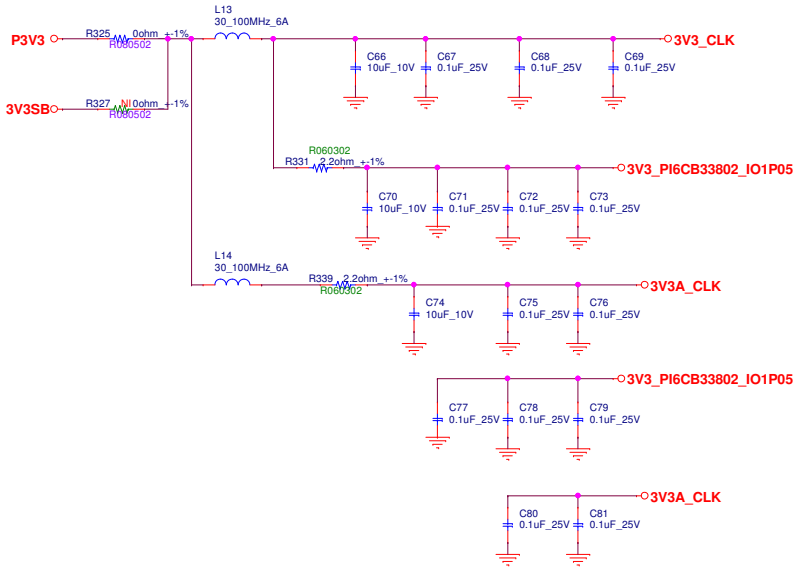
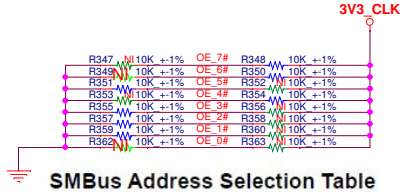


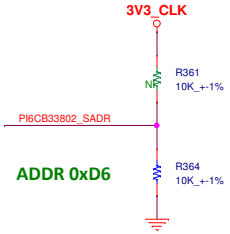




SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	X
	M	1101100	X
	1	1101101	X

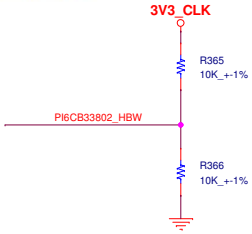
Note: If not using CKPWRGD (CKPWRGD tied to VDD3.3), all 3.3V VDD need to transition from 2.1V to 3.135V in <300usec.



ADDR 0xD6

PLL Operating Mode

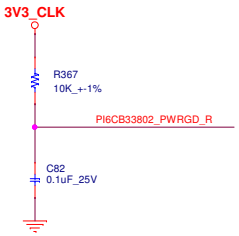
HIBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11



Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low[1]	Low[1]	Off
1	Running	0	X	Low[1]	Low[1]	On[2]
1	Running	1	0	Running	Running	On[2]
1	Running	1	1	Low[1]	Low[1]	On[2]

1. The output state is set by B11[1:0] (Low/Low default)
2. If Bypass mode is selected, the PLL will be off, and outputs will be running.



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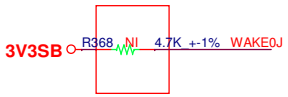
Title: Clock Buffer

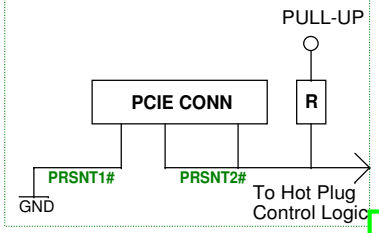
Size: Custom | Document Number: Express-BASE7 R3.1 | Rev: A1

Date: Monday, December 30, 2024 | Sheet 16 of 39

The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks.



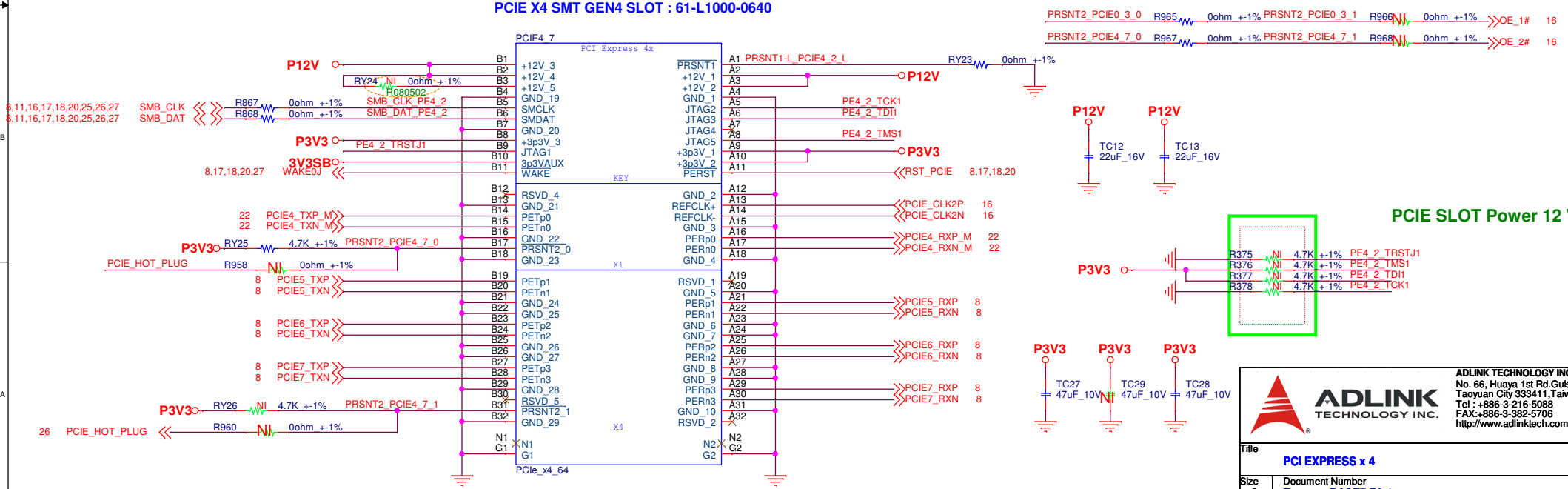
PCI Express Hot-Plug controller detects



PCIE X4 SMT GEN4 SLOT : 61-L1000-0640

PCIE SLOT Power 3.3V CAP

PCIE X4 SMT GEN4 SLOT : 61-L1000-0640



PCIE SLOT Power 12 V CAP

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Title	PCI EXPRESS x 4	
Size: Custom	Document Number: Express-BASE7 R3.1	Rev: A1
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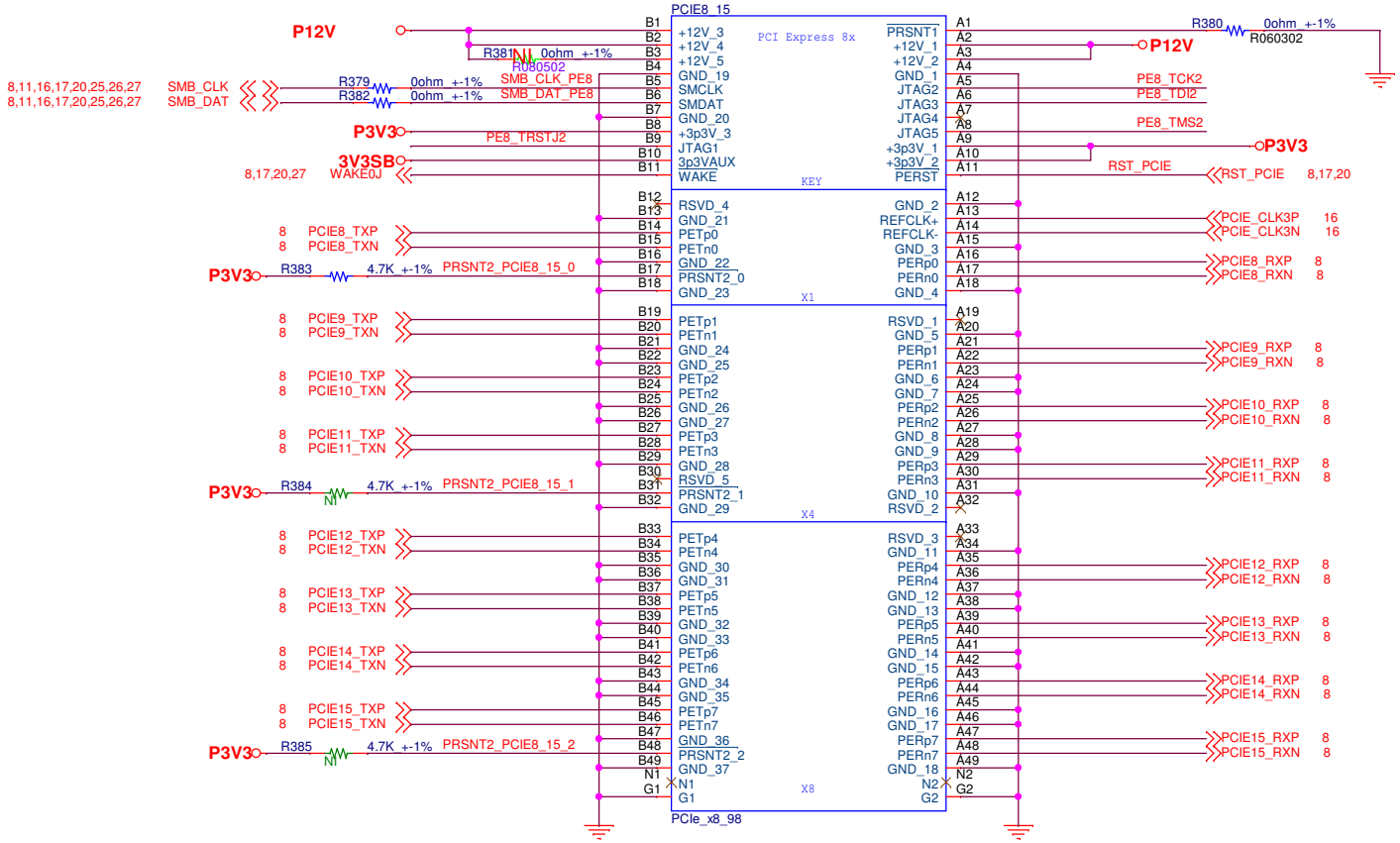
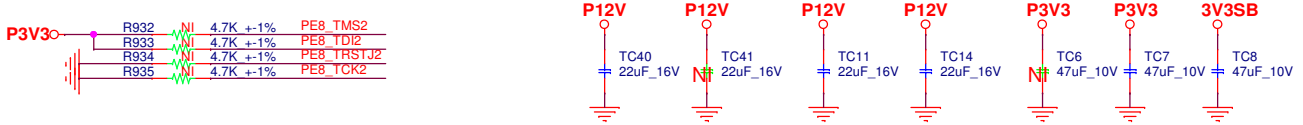
61-L1002-0980





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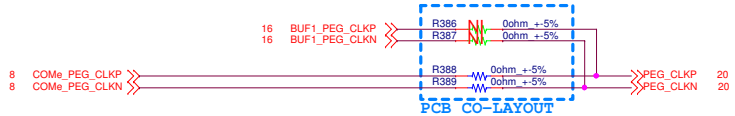
Title	Audio_1_ALC888	
Size B	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 18 of 39	



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Title	Clock Buffer_PEG_GEN5	
Size: Custom	Document Number: Express-BASE7 R3.1	Rev: A1
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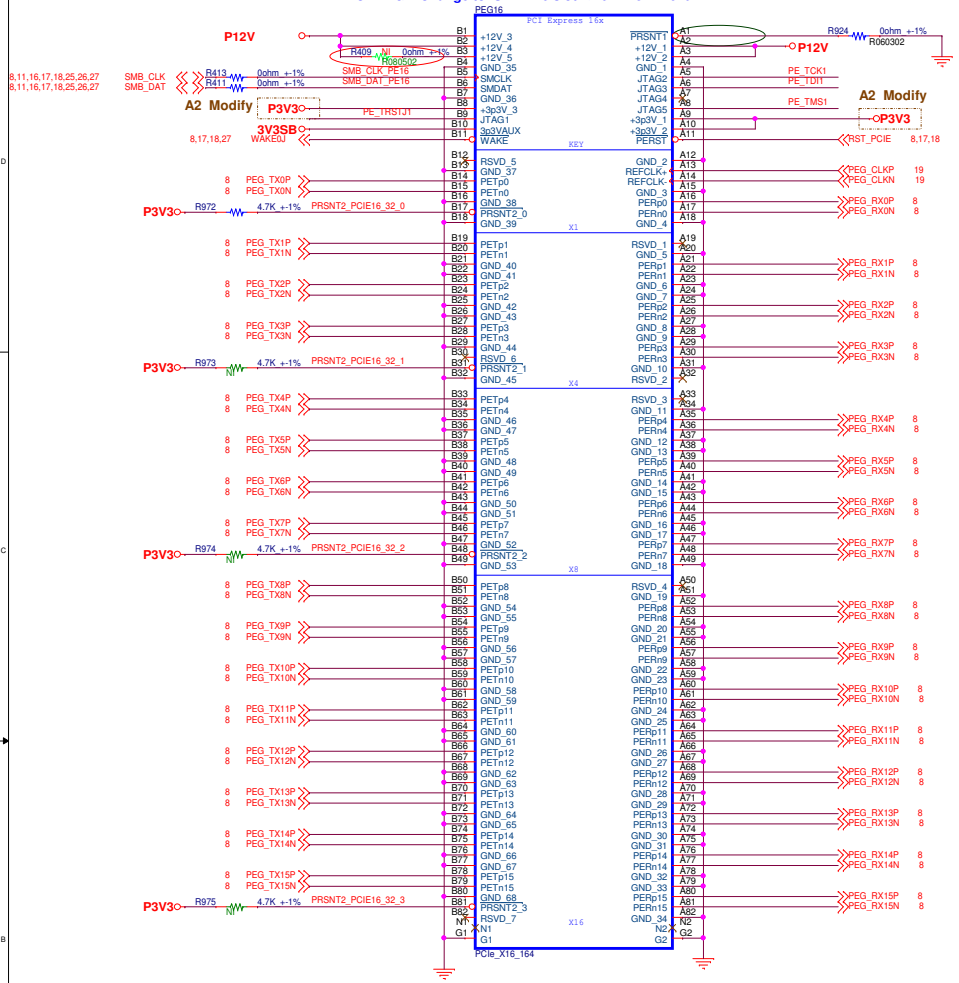
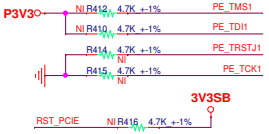
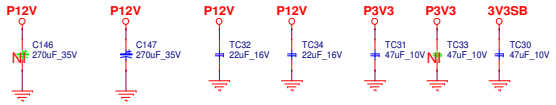
20200911
1. C1 PEG1 Change to SMD x16 slot => 61-L1521-1640







Power Supply Rail Requirements

Power Rail	x1 Connector	x16 Connector
+3.3V		
Voltage tolerance	9%	9%
Supply Current	3.0 A	3.0 A
Capacitive Load	1000 uF	1000 uF
+12V		
Voltage tolerance	8%	8%
Supply Current	0.5 A	4.4 A
Capacitive Load	300 uF	2000 uF
+3.3Vaux		
Voltage tolerance	9%	9%
Supply Current		
Wakeup Enabled	375 mA	375 mA
Non-wakeup Enabled	20 mA	20 mA
Capacitive Load	150 uF	150 uF
	25 W	60 W

The power supply rails available at the PCI Express connectors, based on the number of PCI Express lanes supported by the connectors.

Table 4-1: Power Supply Rail Requirements

Power Rail	10 W Slot	25 W Slot	150W-ATX Power Connector	75 W Slot
+3.3V				
Voltage tolerance	± 9% (max)	± 9% (max)	N/A	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)		3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)		1000 µF (max)
+12V				
Voltage tolerance	± 8%	± 8%	+5% / -8% (max)	± 8%
Supply Current	0.5 A (max)	2.1 A (max)		5.5 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	6.25 A (max)	2000 µF (max)
+3.3Vaux			N/A	
Voltage tolerance	± 9% (max)	± 9% (max)		± 9% (max)
Supply Current				
Wakeup Enabled	375 mA (max)	375 mA (max)		375 mA (max)
Non-wakeup Enabled	20 mA (max)	20 mA (max)		20 mA (max)
Capacitive Load	150 µF (max)	150 µF (max)		150 µF (max)

Notes:
1. The maximum current slew rate for each add-in card shall be no more than 0.1 A/µs.
2. Each add-in card shall limit its bulk capacitance on each power rail to less than the values shown in Table 4-1.
3. System boards that support Hot-Plug add-in cards shall limit the voltage slew rate so that the inrush current to the card shall not exceed the specified maximum current. This is calculated by the equation dV/dt = I/C; where:
   I = maximum allowed current (A)
   C = maximum allowed bulk capacitance (F)
   dV/dt = maximum allowed voltage slew rate (V/s)
4. The maximum voltage variation between +12V inputs is 1.92 V.

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Title: PCI EXPRESS x 16 & DP DDI3

Size	Document Number	Rev
C	Express-BASE7 R3.1	A1

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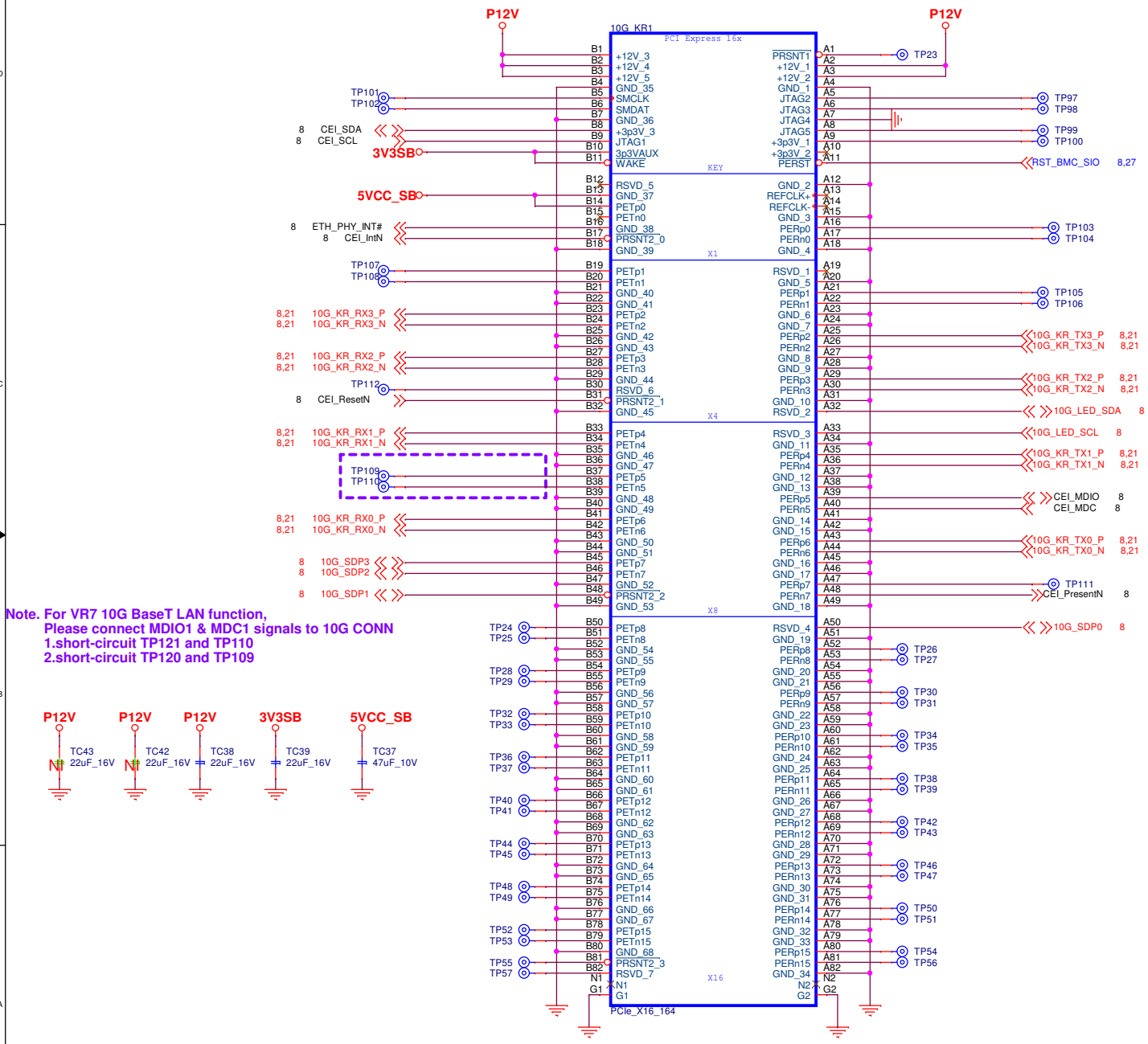
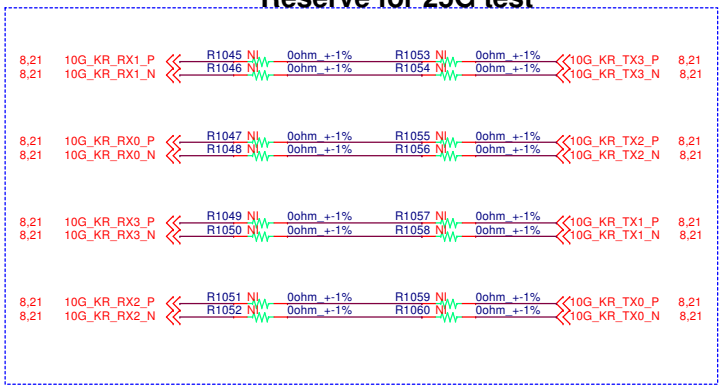


Note. For VR7 10G BaseT LAN function,
Please connect MDIO1 & MDC1 signals to 10G CONN
1.short-circuit TP121 and TP110
2.short-circuit TP120 and TP109

Reserve for 25G test



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Title	10G_KR	
Size A3	Document Number Express-BASE7 R3.1	Rev A1
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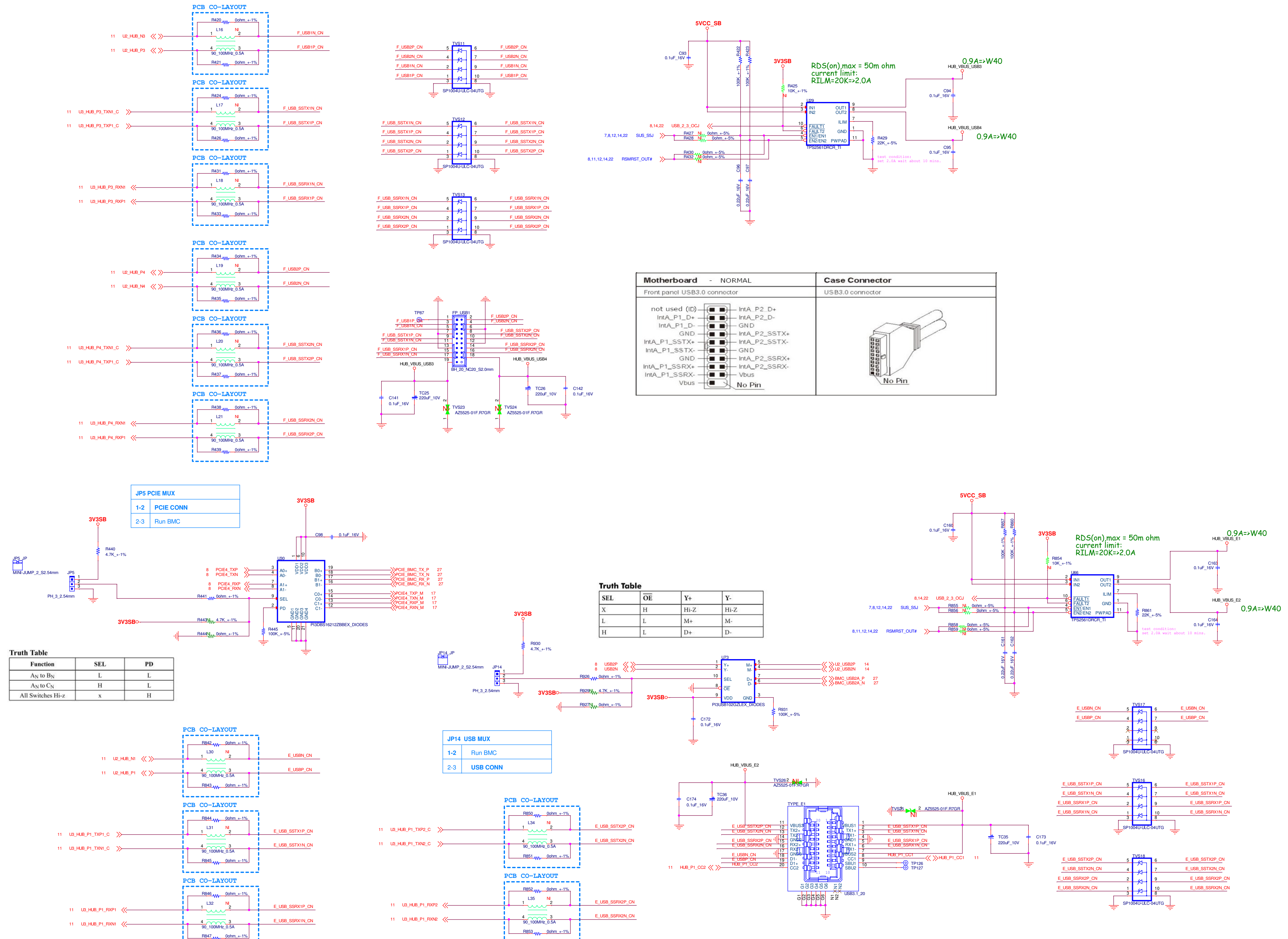

Motherboard - NORMAL	Case Connector
Front panel USB3.0 connector	USB3.0 connector

JP5 PCIE MUX	
1-2	PCIE CONN
2-3	Run BMC

Truth Table

Function	SEL	PD
A_N to B_N	L	L
A_N to C_N	H	L
All Switches Hi-z	x	H

Truth Table

SEL	$\overline{OE}$	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

JP14 USB MUX	
1-2	Run BMC
2-3	USB CONN

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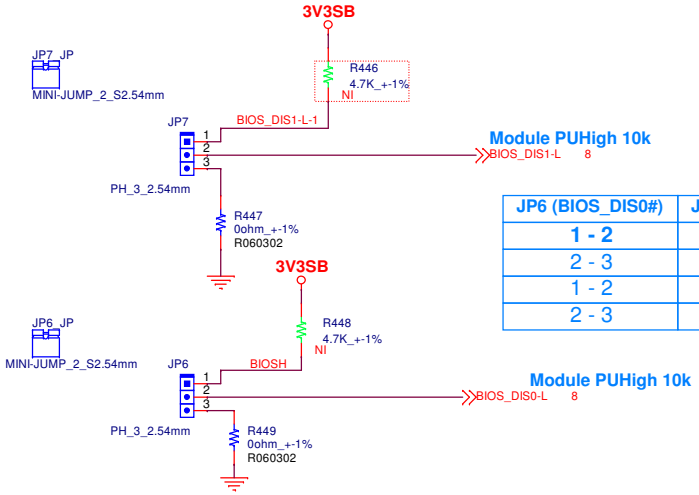
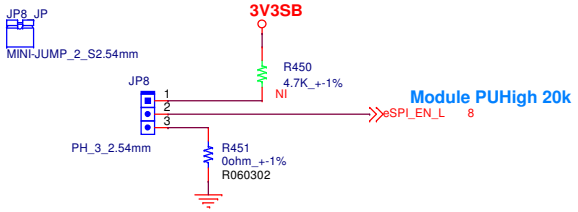
Title: PCIE_MUX & USB_F panel & E

Size	Document Number	Rev
Custom	Express-BASE7 R3.1	A1



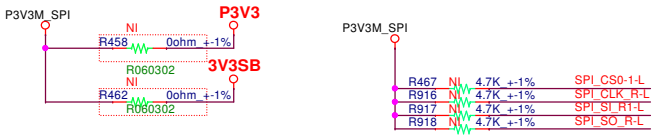
JP6 (BIOS_DIS0#)	JP7 (BIOS_DIS1#)	BIOS Boot Device Select
1 - 2	1 - 2	Module SPI0 / SPI1
2 - 3	1 - 2	FWH on Carrier (on longer supported)
1 - 2	2 - 3	Carrier SPI0 / Module SPI1
2 - 3	2 - 3	Module SPI0 / Carrier SPI1

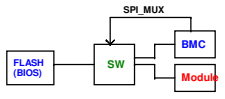


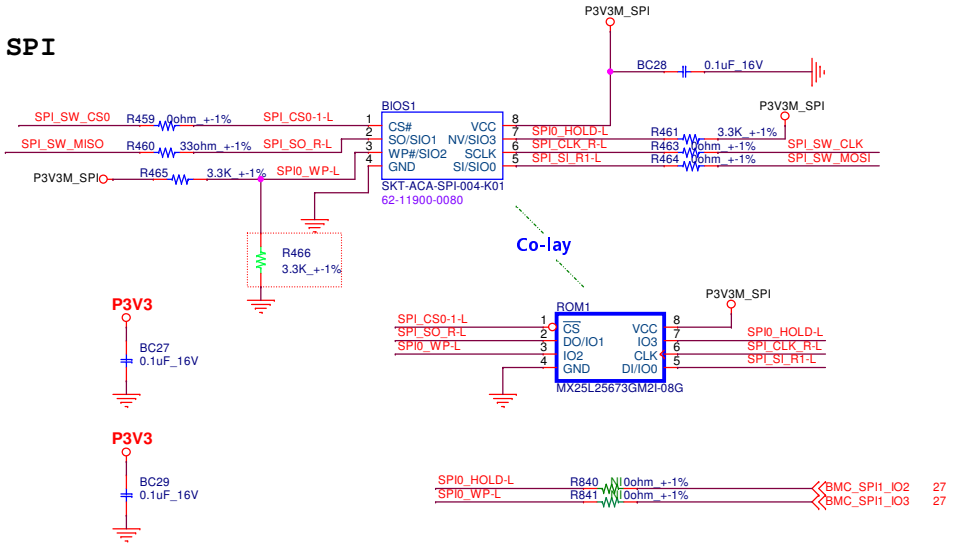
JP8 (eSPI_EN#)	LPC or eSPI switch
1 - 2	**LPC Mode (default)**
2 - 3	eSPI mode

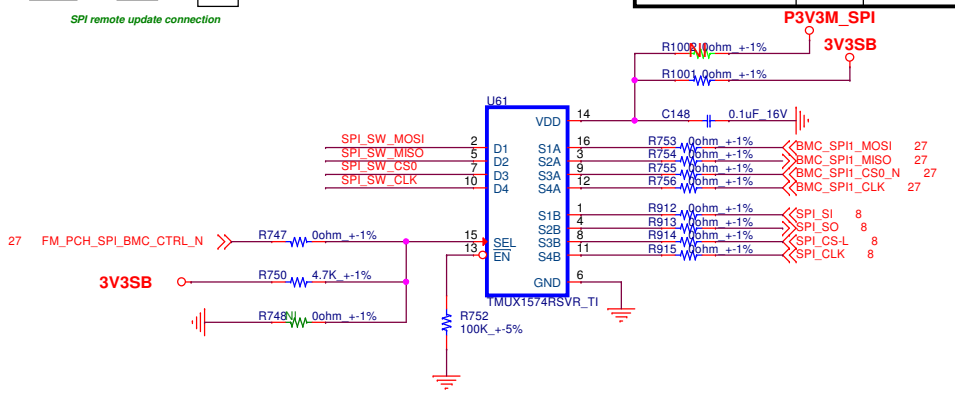
SPI select (High:Module, Low:BMC)

FM_PCH_SPI_BMC_CTRL_N		SPI From
H (Default)	B	Module
L	A	BMC









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Title: External BIOS& SPI connector

Size	Document Number	Rev
A3	Express-BASE7 R3.1	A1

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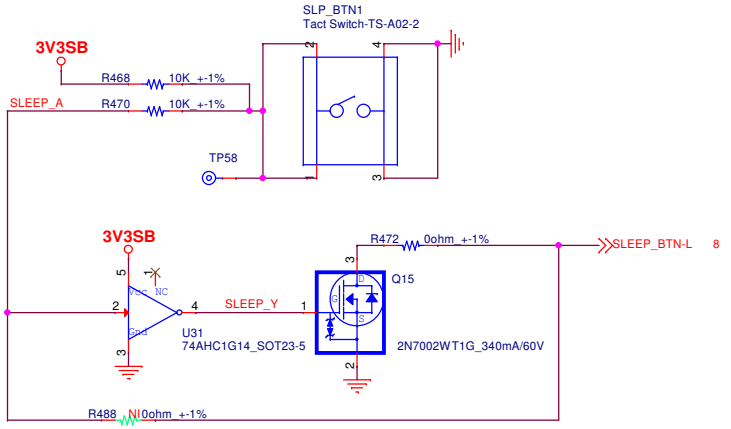
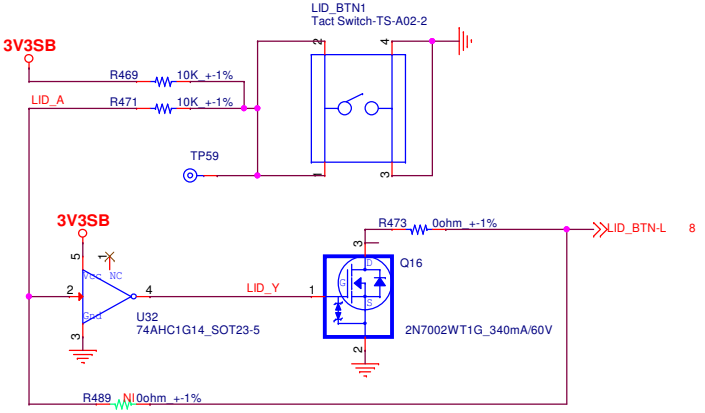
SLEEP BTN

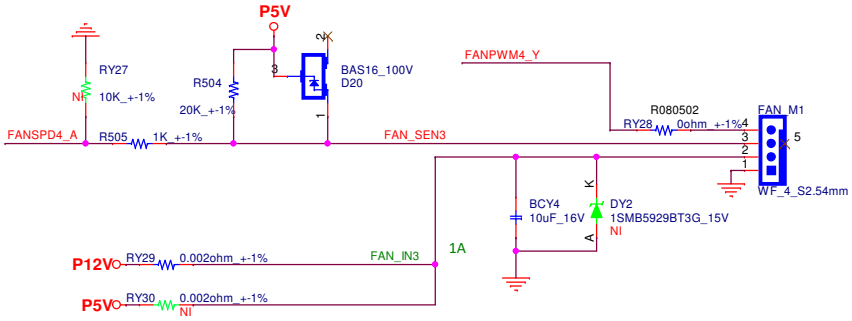


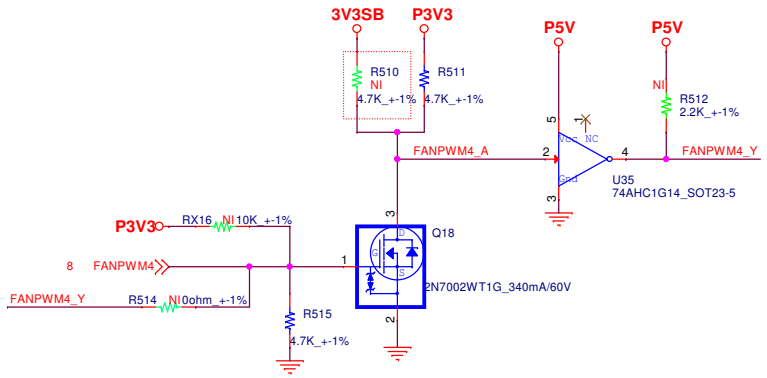
LID BTN

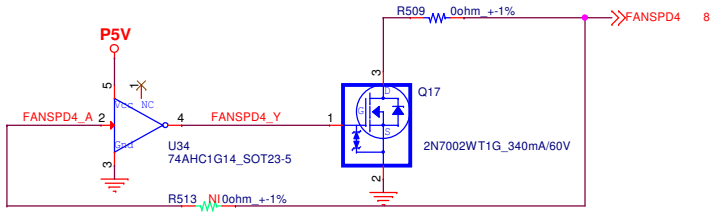
Type 6 Add



FAN(from module)







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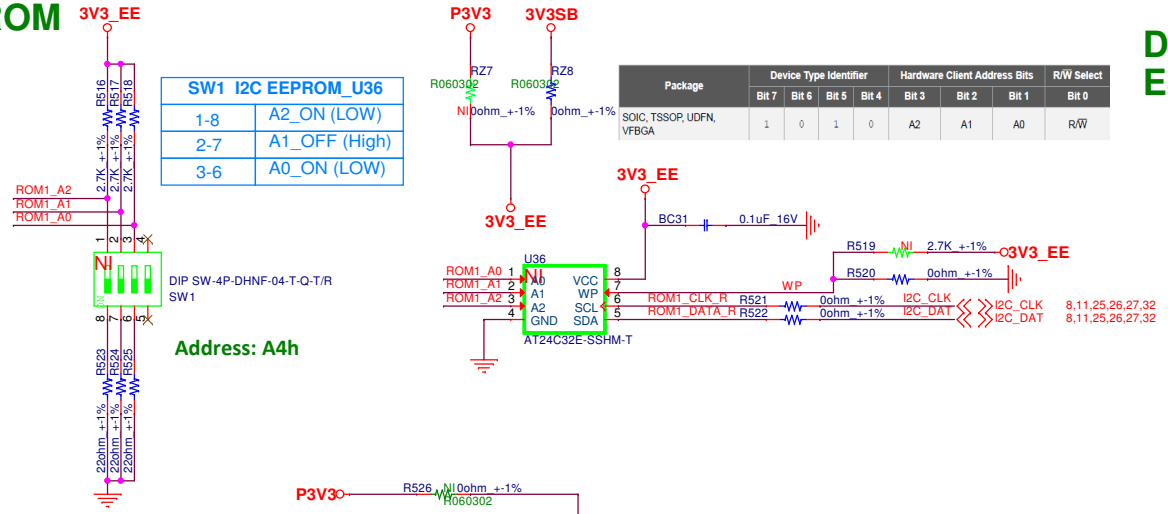
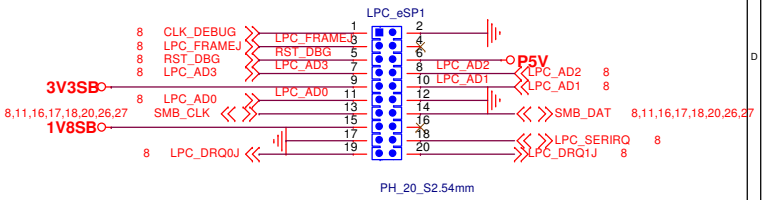
Title	Module FAN	
Size A3	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 24 of 39	

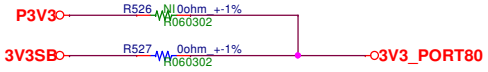
I2C EEPROM

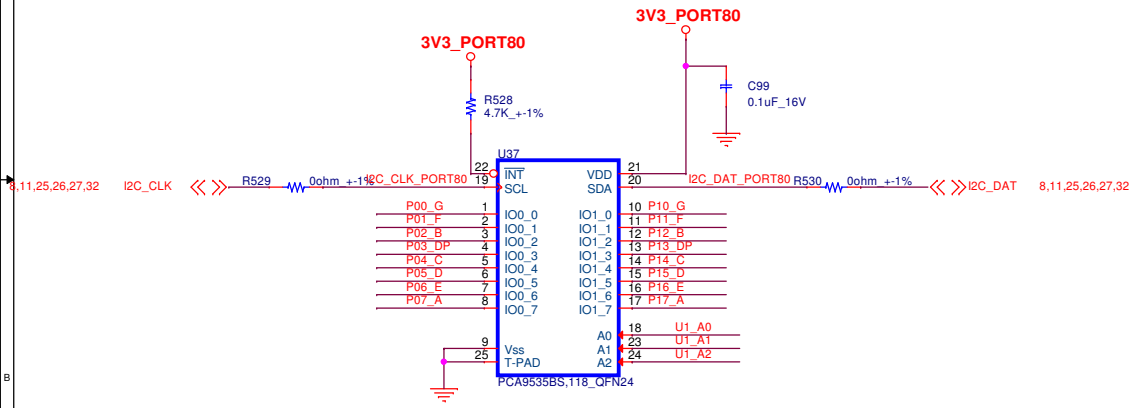


Debug Header (LPC / ESPI)

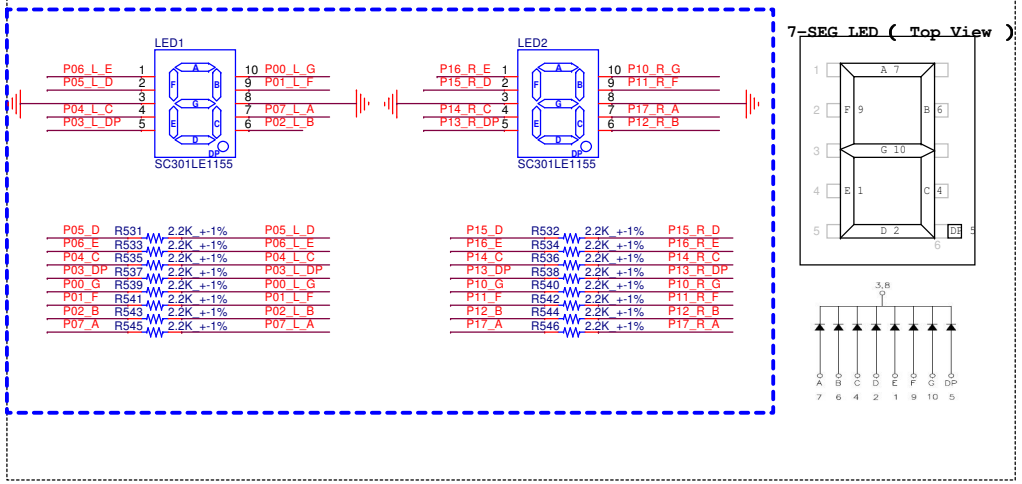
Reference Spec.
Installable LPC Debug Module Design Guide

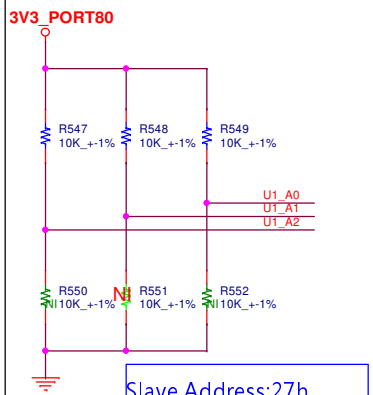






1st : PARA 83-30111-0700 (13.5NT)
2nd: LIGITEK 83-31541-0700 (14NT)





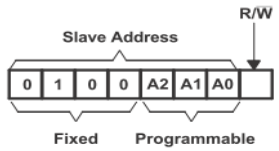


Figure 22. Pca9535 Address

Table 2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

Renew table

N O	P07	P06	P05	P04	P03	P02	P01	P00	HEX
0	1	1	1	1	0	1	1	0	F6
1	0	0	0	1	0	1	0	0	14
2	1	1	1	0	0	1	0	1	E5
3	1	0	1	1	0	1	0	1	B5
4	0	0	0	1	0	1	1	1	17
5	1	0	1	1	0	0	1	1	B3
6	1	1	1	1	0	0	1	1	F3
7	1	0	0	1	0	1	0	0	94
8	1	1	1	1	0	1	1	1	F7
9	1	0	1	1	0	1	1	1	B7
A	1	1	0	1	0	1	1	1	D7
b	0	1	1	1	0	0	1	1	73
c	1	1	1	0	0	0	1	0	E2
d	0	1	1	1	0	1	0	1	75
E	1	1	1	0	0	0	1	1	E3
F	1	1	0	0	0	0	1	1	C3
N O	P07	P06	P05	P04	P03	P02	P01	P00	HEX

2.Each I/O must be limited externally to a maximum of 25 mA, and each octal (P07 - P00 and P17 - P10) must be limited
to a maximum current of 100 mA, for a device total of 200 mA.

3. The total current sourced by all I/Os must be limited to 160
mA (80 mA for P07 - P00 and 80 mA for P17 - P10).

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Title: I2C Eeprom,LPC,Post Code LED
Size: A3
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Rev: A1
Date: Monday, December 30, 2024
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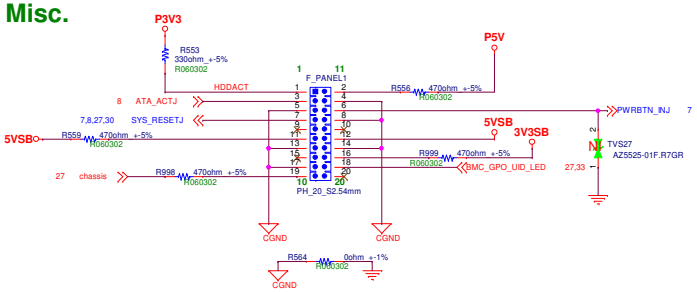
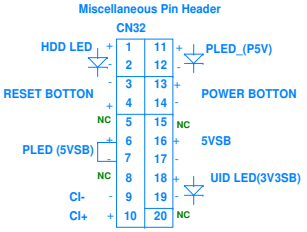
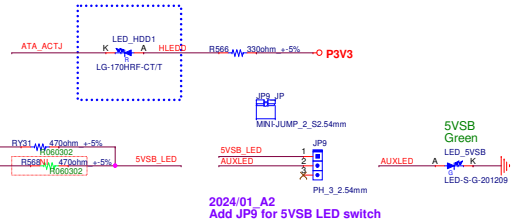
Misc.

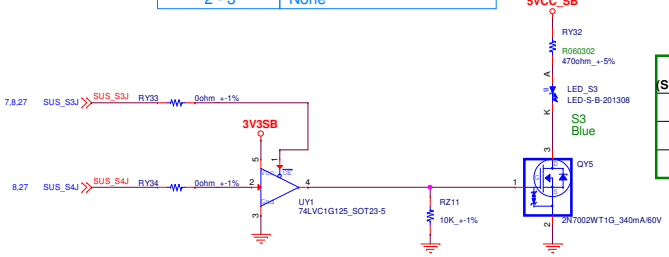




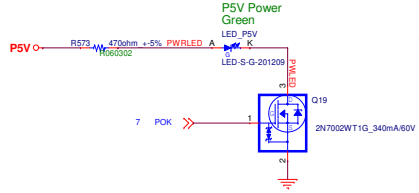


2024/01_A2
Add JP9 for 5VSB LED switch

JP9	5VSB LED
1 - 2	ATX 5VSB
2 - 3	None

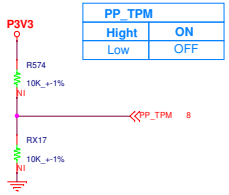


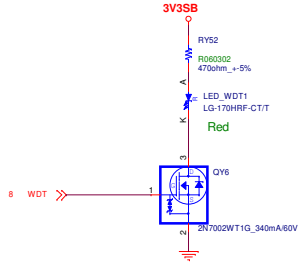
OE# (SUS_S3J)	A (SUS_S4J)	Output Y
L	H	H
L	L	L
H	X	Z



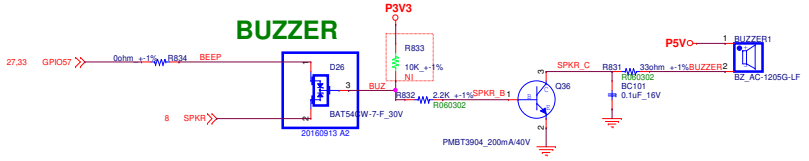
PP_TPM

PP_TPM	
Hight	ON
Low	OFF



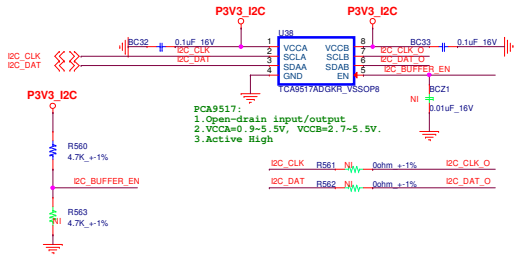


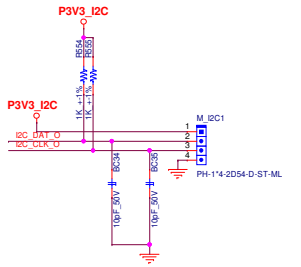
BUZZER



I2C

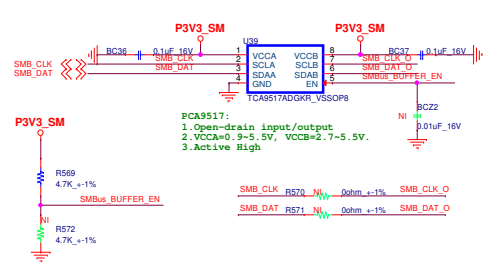
I2C BUFFER

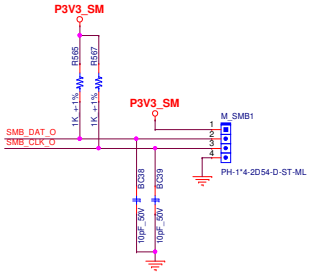




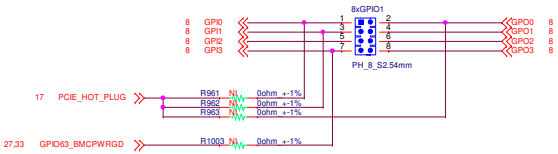
SMBus

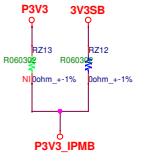
SMBus BUFFER

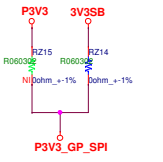


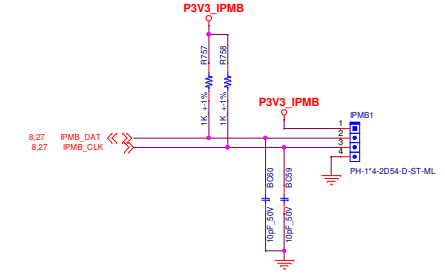


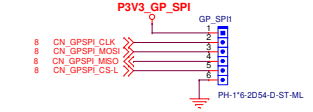
Module GPIOs











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Title	Misc. & GPIOs &SD CARD	
Size: A2	Document Number: Express-BASE7 R3.1	Rev: A1
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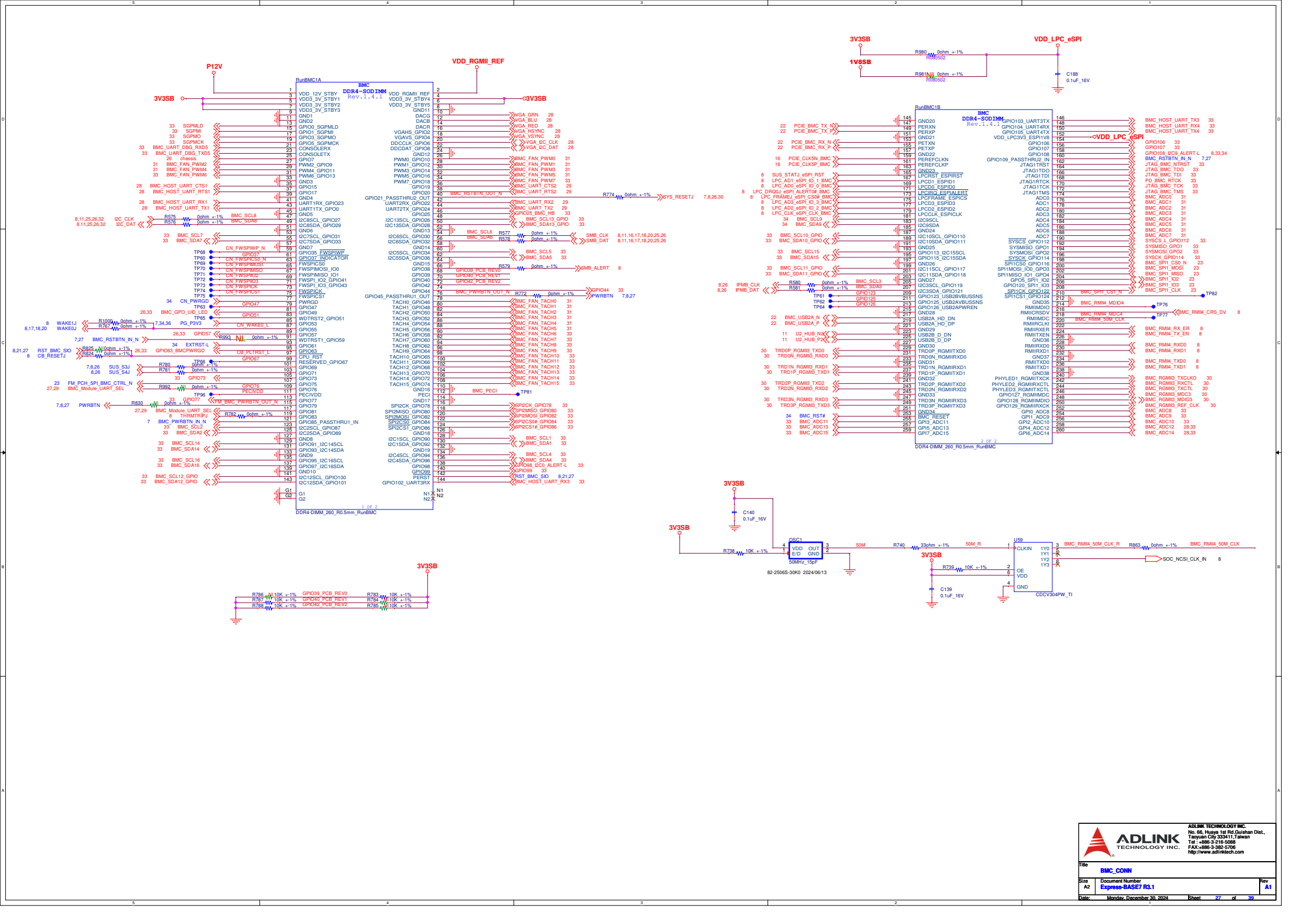
P12V
3V3SB
VDD_RGMII_REF
RunBMC1A
BMC
DDR4-SODIMM
Rev.1.4.1
VDD_12V_STBY
VDD3_3V_STBY1
VDD3_3V_STBY2
VDD3_3V_STBY3
GND1
GND2
GPIO0_SGPMLD
GPIO1_SGPMI
GPIO3_SGPMO
GPIO5_SGPMCK
CONSOLERX
CONSOLETX
GPIO7
PWM2_GPIO9
PWM4_GPIO11
PWM6_GPIO13
GND3
GPIO15
GPIO17
GND4
UART1RX_GPIO23
UART1TX_GPO0
GND5
I2C8SCL_GPIO27
I2C8SDA_GPIO29
GND6
I2C7SCL_GPIO31
I2C7SDA_GPIO33
GND7
GPIO35_FWSPIWP
GPIO37_INDICATOR
FWSPICS0
FWSPIMOSI_IO0
FWSPIMISO_IO1
FWSPI_IO2_GPIO41
FWSPI_IO3_GPIO43
FWSPICK
FWSPICS1
PWRGD
GPIO47
GPIO49
WDTRST2_GPIO51
GPIO53
GPIO55
GPIO57
WDTRST1_GPIO59
GPIO61
GPIO63
CPU_RST
RESERVED_GPIO67
GPIO69
GPIO71
GPIO73
GPIO75
GPIO76
PECIVDD
GPIO77
GPIO79
GPIO81
GPIO83
GPIO85_PASSTHRU1_IN
I2C2SCL_GPIO87
I2C2SDA_GPIO89
GND8
GPIO91_I2C14SCL
GPIO93_I2C14SDA
GND9
GPIO95_I2C16SCL
GPIO97_I2C16SDA
GND10
I2C12SCL_GPIO100
I2C12SDA_GPIO101
G1
G2
VDD_RGMII_REF
VDD3_3V_STBY4
VDD3_3V_STBY5
GND11
DACG
DACB
DACR
VGAHS_GPIO2
VGAVS_GPIO4
DDCCLK_GPIO6
DDCDAT_GPIO8
GND12
PWM0_GPIO10
PWM1_GPIO12
PWM3_GPIO14
PWM5_GPIO16
PWM7_GPIO18
GPIO19
GPIO20
GPIO21_PASSTHRU2_OUT
UART2RX_GPIO22
UART2TX_GPIO24
GPIO25
I2C13SCL_GPIO26
I2C13SDA_GPIO28
GND13
I2C6SCL_GPIO30
I2C6SDA_GPIO32
GND14
I2C5SCL_GPIO34
I2C5SDA_GPIO36
GND15
GPIO38
GPIO39
GPIO40
GPIO42
GPIO45_PASSTHRU1_OUT
TACH0_GPIO46
TACH1_GPIO48
TACH2_GPIO50
TACH3_GPIO52
TACH4_GPIO54
TACH5_GPIO56
TACH6_GPIO58
TACH7_GPIO60
TACH8_GPIO62
TACH9_GPIO64
TACH10_GPIO65
TACH11_GPIO66
TACH12_GPIO68
TACH13_GPIO70
TACH14_GPIO72
TACH15_GPIO74
GND16
PECI
GND17
SPI2CK_GPIO78
SPI2MISO_GPIO80
SPI2MOSI_GPIO82
SPI2CS0_GPIO84
SPI2CS1_GPIO86
GND18
I2C1SCL_GPIO90
I2C1SDA_GPIO92
GND19
I2C4SCL_GPIO94
I2C4SDA_GPIO96
GPIO98
GPIO99
PERST
GPIO102_UART3RX
N1
N2
DDR4-DIMM_260_R0.5mm_RunBMC
1_OF_2
VGA_GRN
VGA_BLU
VGA_RED
VGA_HSYNC
VGA_VSYNC
VGA_I2C_CLK
VGA_I2C_DAT
BMC_FAN_PWM0
BMC_FAN_PWM1
BMC_FAN_PWM3
BMC_FAN_PWM5
BMC_FAN_PWM7
BMC_UART_CTS2
BMC_UART_RTS2
BMC_RSTBTN_OUT_N
R774 0ohm +-1%
SYS_RESETJ
BMC_UART_RX2
BMC_UART_TX2
GPIO25_BMC_HB
BMC_SCL13_GPIO
BMC_SDA13_GPIO
BMC_SCL6
BMC_SDA6
R577 0ohm +-1%
R578 0ohm +-1%
SMB_CLK
SMB_DAT
BMC_SCL5
BMC_SDA5
R579 0ohm +-1%
SMB_ALERT
BMC_PWRBTN_OUT_N
R772 0ohm +-1%
GPIO44
PWRBTN
BMC_FAN_TACH0
BMC_FAN_TACH1
BMC_FAN_TACH2
BMC_FAN_TACH3
BMC_FAN_TACH4
BMC_FAN_TACH5
BMC_FAN_TACH6
BMC_FAN_TACH7
BMC_FAN_TACH8
BMC_FAN_TACH9
BMC_FAN_TACH10
BMC_FAN_TACH11
BMC_FAN_TACH12
BMC_FAN_TACH13
BMC_FAN_TACH14
BMC_FAN_TACH15
BMC_PECI
TP81
SPI2CK_GPIO78
SPI2MISO_GPIO80
SPI2MOSI_GPIO82
SPI2CS0# GPIO84
SPI2CS1#_GPIO86
BMC_SCL1
BMC_SDA1
BMC_SCL4
BMC_SDA4
GPIO98_I2C0_ALERT-L
GPIO99
RST_BMC_SIO
BMC_HOST_UART_RX3
8,21,27
33
R786 10K +-1% GPIO39_PCB_REV0
R787 10K +-1% GPIO40_PCB_REV1
R788 10K +-1% GPIO42_PCB_REV2
R783 10K +-1%
R784 10K +-1%
R785 10K +-1%
R575 0ohm +-1% BMC_SCL8
R576 0ohm +-1% BMC_SDA8
I2C_CLK
I2C_DAT
8,11,25,26,32
BMC_SCL7
BMC_SDA7
CN_FWSPIWP_N
CN_FWSPICS0_N
CN_FWSPIMOSI
CN_FWSPIMISO
CN_FWSPICK
CN_FWSPIIO3
CN_FWSPICK
CN_FWSPICS1
CN_PWRGD
BMC_GPO_UID_LED
WAKE1J
WAKE0J
R1099 0ohm +-1%
R767 0ohm +-1%
7,34,36
PG_P3V3
CN_WAKE0_L
GPIO57
R993 NI 0ohm +-1%
EXTRST-L
RST_BMC_SIO
CB_RESETJ
R825 NI 0ohm +-1%
R824 0ohm +-1%
26,33
GPIO63_BMCPWRGD
CB_PLTRST_L
GPIO67
SUS_S3J
SUS_S4J
R780 0ohm +-1%
R781 0ohm +-1%
FM_PCH_SPI_BMC_CTRL_N
BMC_Module_UART_SEL
R992 NI 0ohm +-1%
GPIO76
GPIO73
GPIO77
PWRBTN
R830 NI 0ohm +-1%
FM_BMC_PWRBTN_OUT_N
BMC_Module_UART_SEL
R782 0ohm +-1%
THRMTRPJ
BMC_PWRBTN_IN_N
BMC_SCL2
BMC_SDA2
BMC_SCL14
BMC_SDA14
BMC_SCL16
BMC_SDA16
BMC_SCL12_GPIO
BMC_SDA12_GPIO
BMC_HOST_UART_CTS1
BMC_HOST_UART_RTS1
BMC_HOST_UART_RX1
BMC_HOST_UART_TX1
BMC_UART_DBG_RXD5
BMC_UART_DBG_TXD5
chassis
BMC_FAN_PWM2
BMC_FAN_PWM4
BMC_FAN_PWM6
SGPMLD
SGPMI
SGPMO
SGPMCK
TP68
TP60
TP69
TP70
TP71
TP72
TP73
TP74
TP75
TP63
TP65
TP66
TP96
3V3SB
VDD_LPC_eSPI
R980 0ohm +-1%
R981 0ohm +-1%
R980502
C188
0.1uF_16V
RunBMC1B
BMC
DDR4-SODIMM
Rev.1.4.1
GND20
PERXN
PERXP
GND21
PETXN
PETXP
GND22
PEREFCLKN
PEREFCLKP
GND23
LPCRST_ESPIRST
LPCD1_ESPID1
LPCD0_ESPID0
LPCIRQ_ESPIALERT
LPCFRAME_ESPICS
LPCD3_ESPID3
LPCD2_ESPID2
LPCCLK_ESPICLK
I2C9SCL
I2C9SDA
GND24
I2C10SCL_GPIO110
I2C10SDA_GPIO111
GND25
GPIO113_I2C15SCL
GPIO115_I2C15SDA
GND26
I2C11SCL_GPIO117
I2C11SDA_GPIO118
GND27
I2C3SCL_GPIO119
I2C3SDA_GPIO121
GPIO123_USB2BVBUSSNS
GPIO125_USB2AVBUSSNS
GPIO126_USB2AWREN
GND28
USB2A_HD_DN
USB2A_HD_DP
GND29
USB2B_D_DN
USB2B_D_DP
GND30
TRD0P_RGMII3_TXD0
TRD0N_RGMII3_RXD0
GND31
TRD1N_RGMII3_RXD1
TRD1P_RGMII3_TXD1
GND32
TRD2P_RGMII3_TXD2
TRD2N_RGMII3_RXD2
GND33
TRD3N_RGMII3_RXD3
TRD3P_RGMII3_TXD3
GND34
BMC_RESET#
GPI3_ADC11
GPI5_ADC13
GPI7_ADC15
GPIO103_UART3TX
GPIO104_UART4RX
GPIO105_UART4TX
VDD_LPC3V3_ESPI1V8
GPIO106
GPIO107
GPIO108
GPIO109_PASSTHRU2_IN
JTAG1TRST
JTAG1TDO
JTAG1TDI
JTAG1TCK
JTAG1TMS
ADC0
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
SYSCS_GPIO112
SYSMISO_GPO1
SYSMOSI_GPO2
SYSCK_GPIO114
SPI1CS0_GPIO116
SPI1MOSI_IO0_GPO3
SPI1MISO_IO1_GPO4
GPO5_SPI1_IO2
GPIO120_SPI1_IO3
SPI1CK_GPIO122
SPI1CS1_GPIO124
GND35
RMIIMDIO
RMIIICRSDV
RMIIMDC
RMIIIRCLKI
RMIIIRXER
RMIIITXEN
GND36
RMIIIRXD0
RMIIIRXD1
GND37
RMIIITXD0
RMIIITXD1
GND38
PHYLED1_RGMIITXCK
PHYLED2_RGMIIRXCTL
PHYLED3_RGMIITXCTL
GPIO127_RGMIIMDC
GPIO128_RGMIIMDIO
GPIO129_RGMIIRXCK
GPI0_ADC8
GPI1_ADC9
GPI2_ADC10
GPI4_ADC12
GPI6_ADC14
2_OF_2
DDR4-DIMM_260_R0.5mm_RunBMC
PCIE_BMC_TX_N
PCIE_BMC_TX_P
PCIE_BMC_RX_N
PCIE_BMC_RX_P
PCIE_CLK5N_BMC
PCIE_CLK5P_BMC
SUS_STAT_eSPI_RST
LPC_AD1_eSPI_IO_1_BMC
LPC_AD0_eSPI_IO_0_BMC
LPC_DRQ0_eSPI_ALERT0#_BMC
LPC_FRAME_eSPI_CS0#_BMC
LPC_AD3_eSPI_IO_3_BMC
LPC_AD2_eSPI_IO_2_BMC
LPC_CLK_eSPI_CLK_BMC
BMC_SCL9
BMC_SDA9
BMC_SCL10_GPIO
BMC_SDA10_GPIO
BMC_SCL15
BMC_SDA15
BMC_SCL11_GPIO
BMC_SDA11_GPIO
IPMB_CLK
IPMB_DAT
R580 0ohm +-1%
R581 0ohm +-1%
BMC_SCL3
BMC_SDA3
GPIO123
GPIO125
GPIO126
TP61
TP62
TP64
BMC_USB2A_N
BMC_USB2A_P
U2_HUB_N3
U2_HUB_P2
TRD0P_RGMII3_TXD0
TRD0N_RGMII3_RXD0
TRD1N_RGMII3_RXD1
TRD1P_RGMII3_TXD1
TRD2P_RGMII3_TXD2
TRD2N_RGMII3_RXD2
TRD3N_RGMII3_RXD3
TRD3P_RGMII3_TXD3
BMC_RST#
BMC_ADC11
BMC_ADC13
BMC_ADC15
GPIO103_UART3TX
GPIO104_UART4RX
GPIO105_UART4TX
GPIO106
GPIO107
GPIO108
GPIO108_I2C9_ALERT-L
BMC_RSTBTN_IN_N
JTAG_BMC_NTRST
JTAG_BMC_TDO
JTAG_BMC_TDI
PD_BMC_RTCK
JTAG_BMC_TCK
JTAG_BMC_TMS
BMC_ADC0
BMC_ADC1
BMC_ADC2
BMC_ADC3
BMC_ADC4
BMC_ADC5
BMC_ADC6
BMC_ADC7
SYSCS_L_GPIO112
SYSMISO_GPO1
SYSMOSI_GPO2
SYSCK_GPIO114
BMC_SPI1_CS0_N
BMC_SPI1_MOSI
BMC_SPI1_MISO
BMC_SPI1_IO2
BMC_SPI1_IO3
BMC_SPI1_CLK
BMC_SPI1_CS1_N
TP82
BMC_RMII4_MDIO4
TP76
BMC_RMII4_CRS_DV
TP77
BMC_RMII4_MDC4
BMC_RMII4_50M_CLK
BMC_RMII4_RX_ER
BMC_RMII4_TX_EN
BMC_RMII4_RXD0
BMC_RMII4_RXD1
BMC_RMII4_TXD0
BMC_RMII4_TXD1
BMC_RGMII3_TXCLKO
BMC_RGMII3_RXCTL
BMC_RGMII3_TXCTL
BMC_RGMII3_MDC3
BMC_RGMII3_MDIO3
BMC_RGMII3_REF_CLK
BMC_ADC8
BMC_ADC9
BMC_ADC10
BMC_ADC12
BMC_ADC14
28,33
C140
0.1uF_16V
OSC1
VDD
E/D
OUT
GND
50MHz_15pF
82-2506S-30K0 2024/06/13
R738 10K +-1%
50M
R740 33ohm +-1%
50M_R
U59
CLKIN
1Y0
1Y1
1Y2
1Y3
OE
VDD
GND
CDCV304PW_TI
R739 10K +-1%
C139
0.1uF_16V
BMC_RMII4_50M_CLK_R
R863 0ohm +-1%
BMC_RMII4_50M_CLK
SOC_NCSI_CLK_IN
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Title
BMC_CONN
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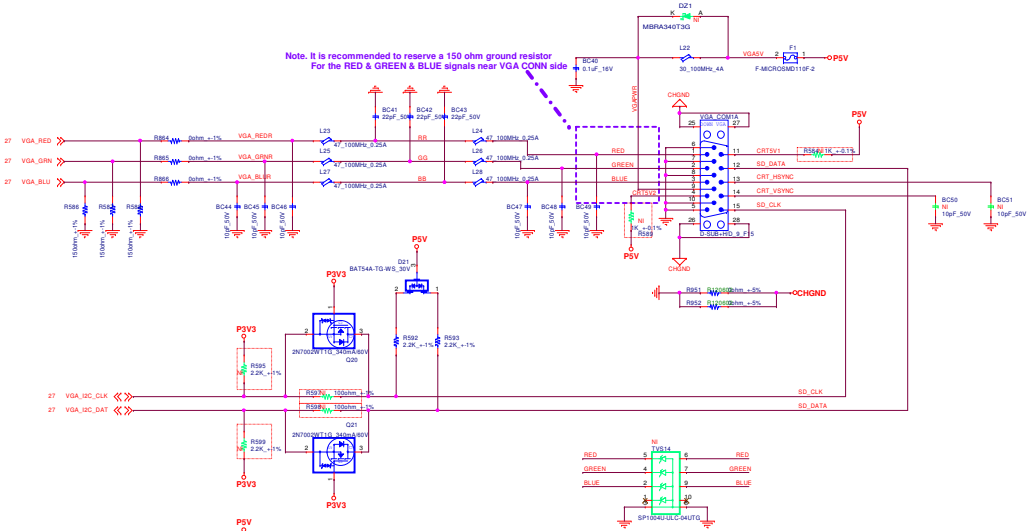
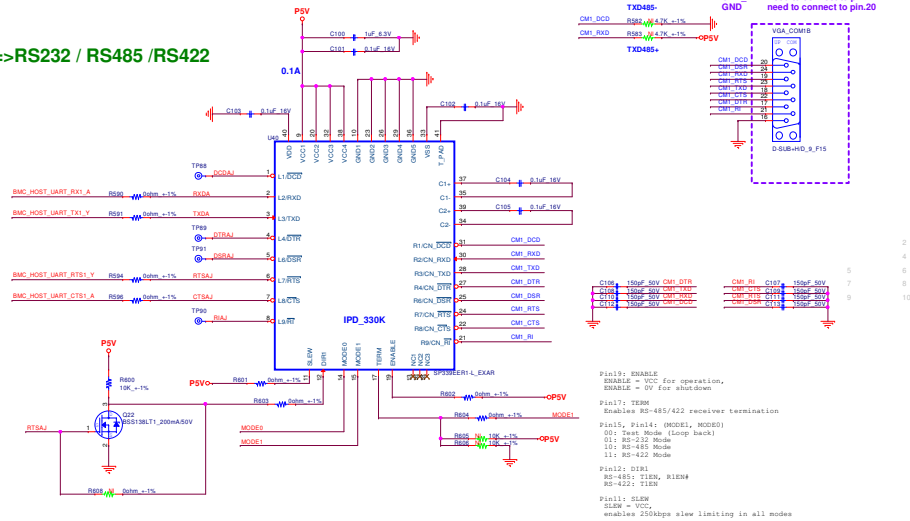
VGA

Note. It is recommended to reserve a 150 ohm ground resistor
For the RED & GREEN & BLUE signals near VGA CONN side



BMC_COM1 =>RS232 / RS485 /RS422



Pin19: ENABLE
ENABLE = VCC for operation,
ENABLE = 0V for shutdown

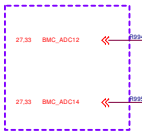
Pin17: TERM
Enables RS-485/422 receiver termination

Pin15, Pin14: (MODE1, MODE0)
00: Test Mode (Loop back)
01: RS-232 Mode
10: RS-485 Mode
11: RS-422 Mode

Pin12: DIR1
RS-485: T1EN, R1EN#
RS-422: T1EN

Pin11: SLEW
SLEW = VCC,
enables 250kbps slew limiting in all modes

Note. The pins MODE0 , MODE1 of SP339 is 5V level signal.
And GPIO signal of BMC is 3.3V level.
If you want to control the working mode of SP339 by BMC GPIO.
Adding signals level shift circuit is necessary.

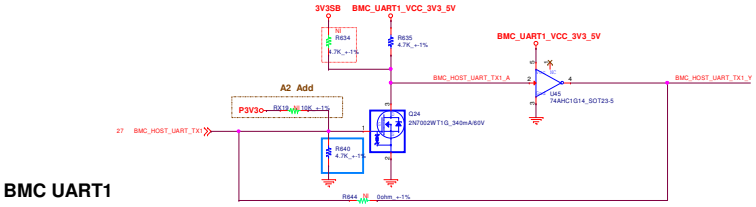


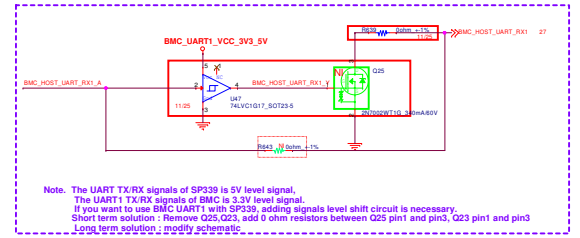
RS232/RS422/RS485 Select

	MODE1	MODE0
RS-232	0	1
RS-485	1	0
RS-422	1	1

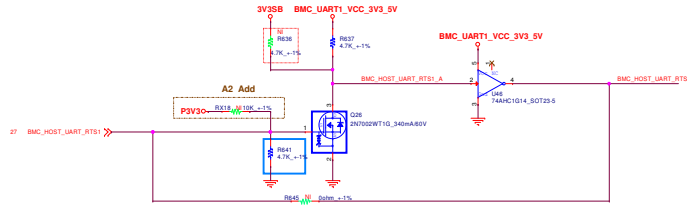
JP10 & JP11	RS232/RS422/RS485 Select	
	JP10	JP11
RS-232	1-2	2-3
RS-485	2-3	1-2
RS-422	1-2	1-2

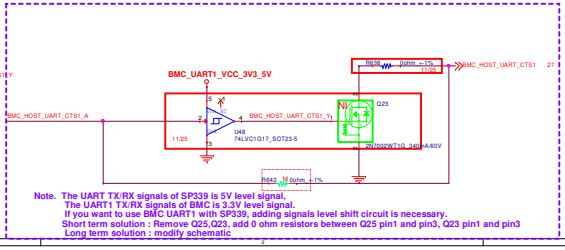
BMC UART1



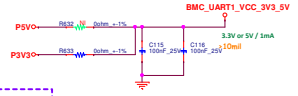


Note. The UART TX/RX signals of SP339 is 5V level signal,
The UART1 TX/RX signals of BMC is 3.3V level signal.
If you want to use BMC UART1 with SP339, adding signals level shift circuit is necessary.
Short term solution : Remove Q25,Q23, add 0 ohm resistors between Q25 pin1 and pin3, Q23 pin1 and pin3
Long term solution : modify schematic





Note. The UART TX/RX signals of SP339 is 5V level signal,
The UART1 TX/RX signals of BMC is 3.3V level signal.
If you want to use BMC UART1 with SP339, adding signals level shift circuit is necessary.
Short term solution : Remove Q25,Q23, add 0 ohm resistors between Q25 pin1 and pin3, Q23 pin1 and pin3
Long term solution : modify schematic



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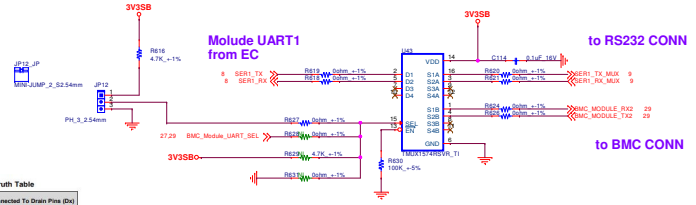
JP12 & JP13 UART SOL Select		
	JP12	JP13
SOL Function default	1-2	1-2
Module RS232	2-3	2-3

1-2 SOL Function default
2-3 Module RS232



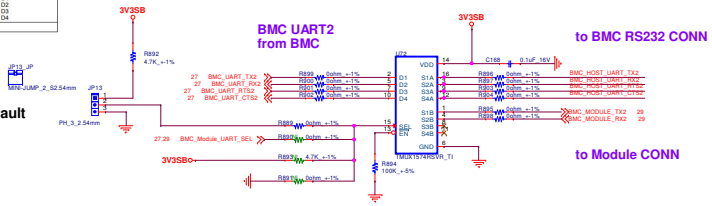
8.5 Truth Tables

Table 1. TMUX1574 Truth Table

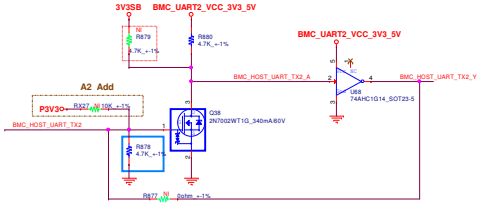
INPUTS		Selected Source Pins Connected To Drain Pins (Dx)
EN	SEL	
0	0	S1A connected to D1 S2A connected to D2 S3A connected to D3 S4A connected to D4
0	1	S1B connected to D1 S2B connected to D2 S3B connected to D3 S4B connected to D4
1	X(1)	Hi-Z (OFF)

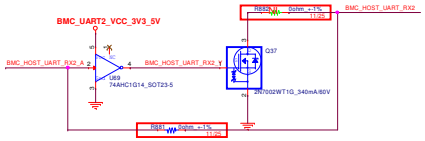
(1) X denotes don't care.

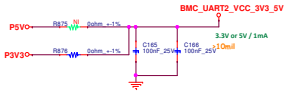
1-2 SOL Function default
2-3 BMC RS232



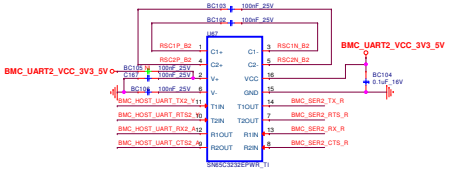
BMC UART2





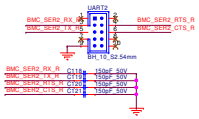


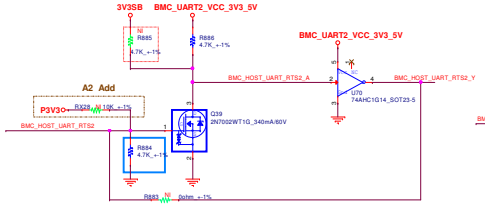
RS232 from BMC UART2

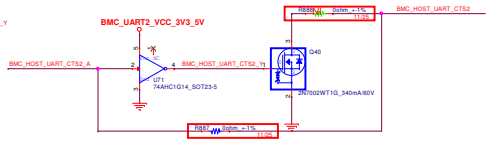


PCB Text => COM1

Port 0







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Title	BMC_COM2	
Size: D	Document Number: Express-BASE7 R5.1	Rev: A1
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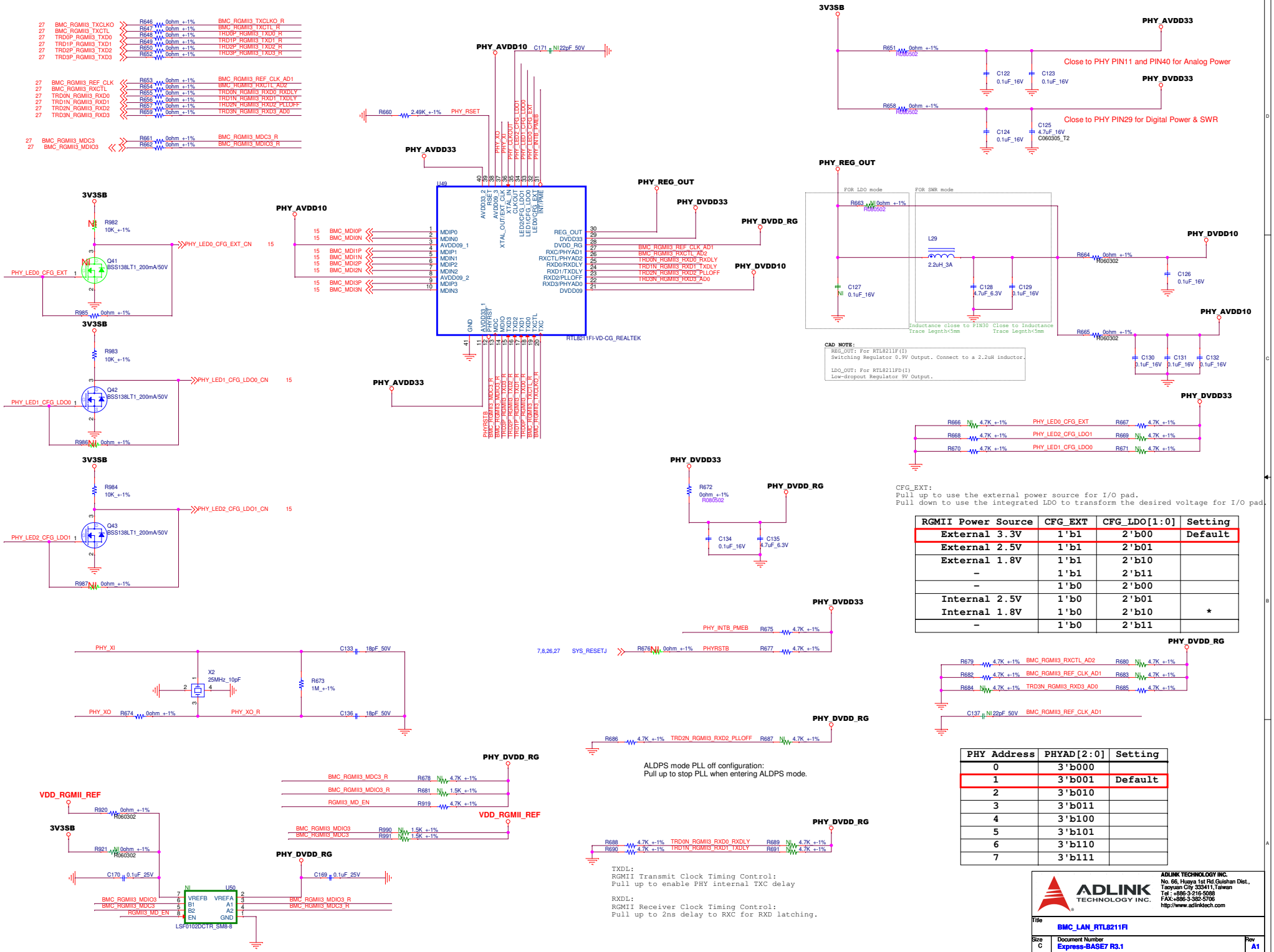
27 BMC_RGMII3_TXCLKO
27 BMC_RGMII3_TXCTL
27 TRD0P_RGMII3_TXD0
27 TRD1P_RGMII3_TXD1
27 TRD2P_RGMII3_TXD2
27 TRD3P_RGMII3_TXD3
R646 0ohm +-1%
R647 0ohm +-1%
R648 0ohm +-1%
R649 0ohm +-1%
R650 0ohm +-1%
R652 0ohm +-1%
BMC_RGMII3_TXCLKO_R
BMC_RGMII3_TXCTL_R
TRD0P_RGMII3_TXD0_R
TRD1P_RGMII3_TXD1_R
TRD2P_RGMII3_TXD2_R
TRD3P_RGMII3_TXD3_R
27 BMC_RGMII3_REF_CLK
27 BMC_RGMII3_RXCTL
27 TRD0N_RGMII3_RXD0
27 TRD1N_RGMII3_RXD1
27 TRD2N_RGMII3_RXD2
27 TRD3N_RGMII3_RXD3
R653 0ohm +-1%
R654 0ohm +-1%
R655 0ohm +-1%
R656 0ohm +-1%
R657 0ohm +-1%
R659 0ohm +-1%
BMC_RGMII3_REF_CLK_AD1
BMC_RGMII3_RXCTL_AD2
TRD0N_RGMII3_RXD0_RXDLY
TRD1N_RGMII3_RXD1_TXDLY
TRD2N_RGMII3_RXD2_PLLOFF
TRD3N_RGMII3_RXD3_AD0
27 BMC_RGMII3_MDC3
27 BMC_RGMII3_MDIO3
R661 0ohm +-1%
R662 0ohm +-1%
BMC_RGMII3_MDC3_R
BMC_RGMII3_MDIO3_R
3V3SB
PHY_AVDD10
PHY_AVDD33
PHY_DVDD33
PHY_DVDD_RG
PHY_DVDD10
PHY_REG_OUT
R660 2.49K +-1% PHY_RSET
C171 NI 22pF 50V
U49
RTL8211FI-VD-CG_REALTEK
MDIP0
MDIN0
AVDD09_1
MDIP1
MDIN1
MDIP2
MDIN2
AVDD09_2
MDIP3
MDIN3
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD09
BMC_RGMII3_REF_CLK_AD1
BMC_RGMII3_RXCTL_AD2
TRD0N_RGMII3_RXD0_RXDLY
TRD1N_RGMII3_RXD1_TXDLY
TRD2N_RGMII3_RXD2_PLLOFF
TRD3N_RGMII3_RXD3_AD0
15 BMC_MDI0P
15 BMC_MDI0N
15 BMC_MDI1P
15 BMC_MDI1N
15 BMC_MDI2P
15 BMC_MDI2N
15 BMC_MDI3P
15 BMC_MDI3N
PHY_XO
PHY_XI
PHY_CLKOUT
PHY_LED2/CFG_LDO1
PHY_LED1/CFG_LDO0
PHY_LED0/CFG_EXT
PHY_INTB_PMEB
PHYRSTB
BMC_RGMII3_MDC3_R
BMC_RGMII3_MDIO3_R
TRD0P_RGMII3_TXD0_R
TRD1P_RGMII3_TXD1_R
TRD2P_RGMII3_TXD2_R
TRD3P_RGMII3_TXD3_R
BMC_RGMII3_TXCTL_R
BMC_RGMII3_TXCLKO_R
R982 10K_+-1%
Q41 BSS138LT1_200mA/50V
PHY_LED0_CFG_EXT_CN 15
PHY_LED0_CFG_EXT 1
R985 0ohm +-1%
R983 10K_+-1%
Q42 BSS138LT1_200mA/50V
PHY_LED1_CFG_LDO0_CN 15
PHY_LED1_CFG_LDO0 1
R986 NI 0ohm +-1%
R984 10K_+-1%
Q43 BSS138LT1_200mA/50V
PHY_LED2_CFG_LDO1_CN 15
PHY_LED2_CFG_LDO1 1
R987 NI 0ohm +-1%
R651 0ohm +-1% RM00502
R658 0ohm +-1% RM00502
C122 0.1uF_16V
C123 0.1uF_16V
C124 0.1uF_16V
C125 4.7uF_16V C060305_T2
Close to PHY PIN11 and PIN40 for Analog Power
Close to PHY PIN29 for Digital Power & SWR
R663 NI 0ohm +-1% RM00502
FOR LDO mode
FOR SWR mode
L29 2.2uH_3A
C127 NI 0.1uF_16V
C128 4.7uF_6.3V
C129 0.1uF_16V
R664 0ohm +-1% R060302
C126 0.1uF_16V
R665 0ohm +-1% R060302
C130 0.1uF_16V
C131 0.1uF_16V
C132 0.1uF_16V
Inductance Close to PIN30 Trace Legnth<5mm
Inductance Close to Inductance Trace Legnth<5mm
CAD NOTE:
REG_OUT: For RTL8211F(I)
Switching Regulator 0.9V Output. Connect to a 2.2uH inductor.
LDO_OUT: For RTL8211FD(I)
Low-dropout Regulator 9V Output.
R666 NI 4.7K +-1% PHY_LED0_CFG_EXT R667 4.7K +-1%
R668 4.7K +-1% PHY_LED2_CFG_LDO1 R669 NI 4.7K +-1%
R670 4.7K +-1% PHY_LED1_CFG_LDO0 R671 NI 4.7K +-1%
R672 0ohm +-1% R080502
C134 0.1uF_16V
C135 4.7uF_6.3V
CFG_EXT:
Pull up to use the external power source for I/O pad.
Pull down to use the integrated LDO to transform the desired voltage for I/O pad.
RGMII Power Source | CFG_EXT | CFG_LDO[1:0] | Setting
External 3.3V | 1'b1 | 2'b00 | Default
External 2.5V | 1'b1 | 2'b01 |
External 1.8V | 1'b1 | 2'b10 |
- | 1'b1 | 2'b11 |
- | 1'b0 | 2'b00 |
Internal 2.5V | 1'b0 | 2'b01 |
Internal 1.8V | 1'b0 | 2'b10 | *
- | 1'b0 | 2'b11 |
PHY_INTB_PMEB R675 4.7K +-1%
7,8,26,27 SYS_RESETJ R676 NI 0ohm +-1% PHYRSTB R677 4.7K +-1%
R679 4.7K +-1% BMC_RGMII3_RXCTL_AD2 R680 NI 4.7K +-1%
R682 4.7K +-1% BMC_RGMII3_REF_CLK_AD1 R683 NI 4.7K +-1%
R684 NI 4.7K +-1% TRD3N_RGMII3_RXD3_AD0 R685 4.7K +-1%
C137 NI 22pF 50V BMC_RGMII3_REF_CLK_AD1
PHY_XI
C133 18pF_50V
X2 25MHz_10pF
R673 1M_+-1%
PHY_XO R674 0ohm +-1% PHY_XO_R
C136 18pF_50V
R686 4.7K +-1% TRD2N_RGMII3_RXD2_PLLOFF R687 NI 4.7K +-1%
ALDPS mode PLL off configuration:
Pull up to stop PLL when entering ALDPS mode.
R688 4.7K +-1% TRD0N_RGMII3_RXD0_RXDLY R689 NI 4.7K +-1%
R690 4.7K +-1% TRD1N_RGMII3_RXD1_TXDLY R691 NI 4.7K +-1%
TXDL:
RGMII Transmit Clock Timing Control:
Pull up to enable PHY internal TXC delay
RXDL:
RGMII Receiver Clock Timing Control:
Pull up to 2ns delay to RXC for RXD latching.
PHY Address | PHYAD[2:0] | Setting
0 | 3'b000 |
1 | 3'b001 | Default
2 | 3'b010 |
3 | 3'b011 |
4 | 3'b100 |
5 | 3'b101 |
6 | 3'b110 |
7 | 3'b111 |
VDD_RGMII_REF
R920 0ohm +-1% R060302
R921 NI 0ohm +-1% R060302
C170 0.1uF_25V
C169 0.1uF_25V
U50
LSF0102DCTR_SM8-8
VREFB VREFA
B1 A1
B2 A2
EN GND
BMC_RGMII3_MDIO3_R
BMC_RGMII3_MDC3_R
RGMII3_MD_EN
R678 NI 4.7K +-1%
R681 NI 1.5K +-1%
R919 4.7K +-1%
R990 NI 1.5K +-1%
R991 NI 1.5K +-1%
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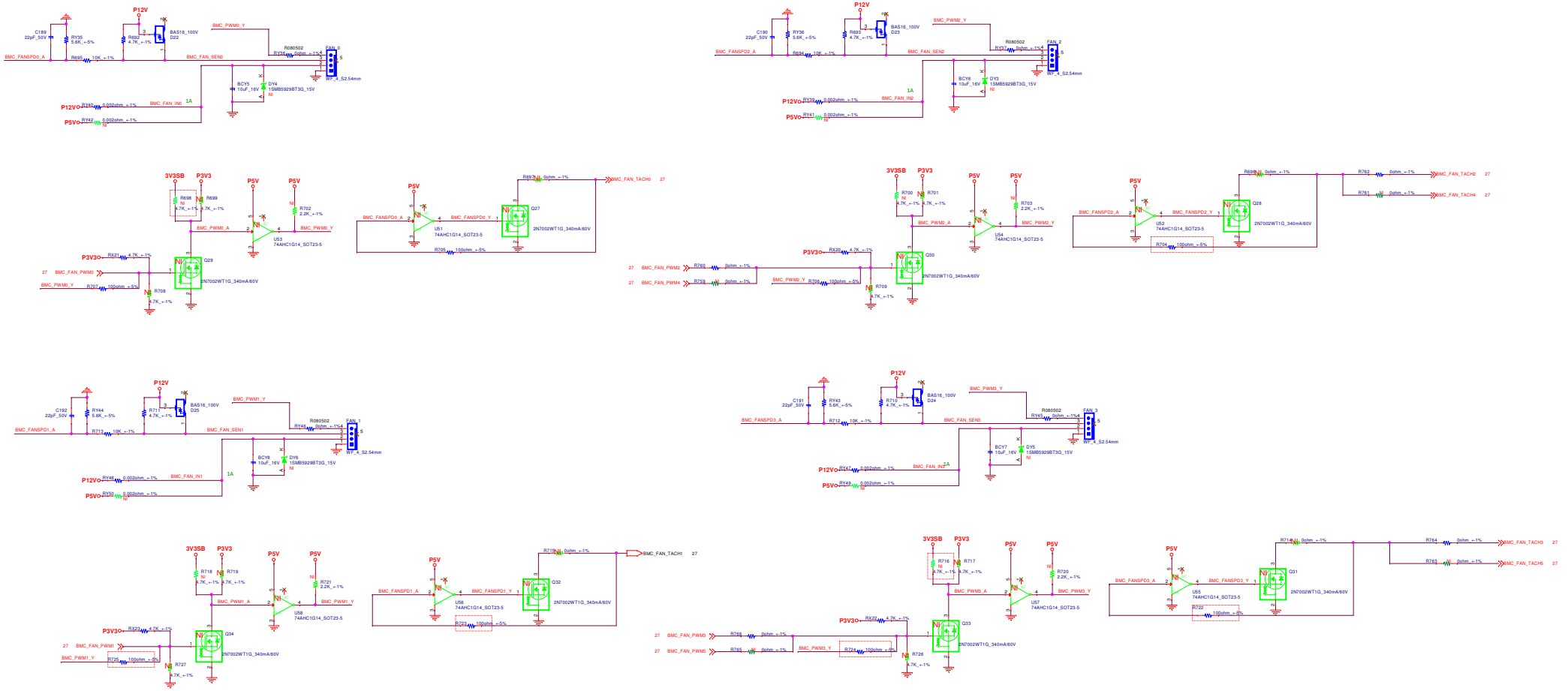
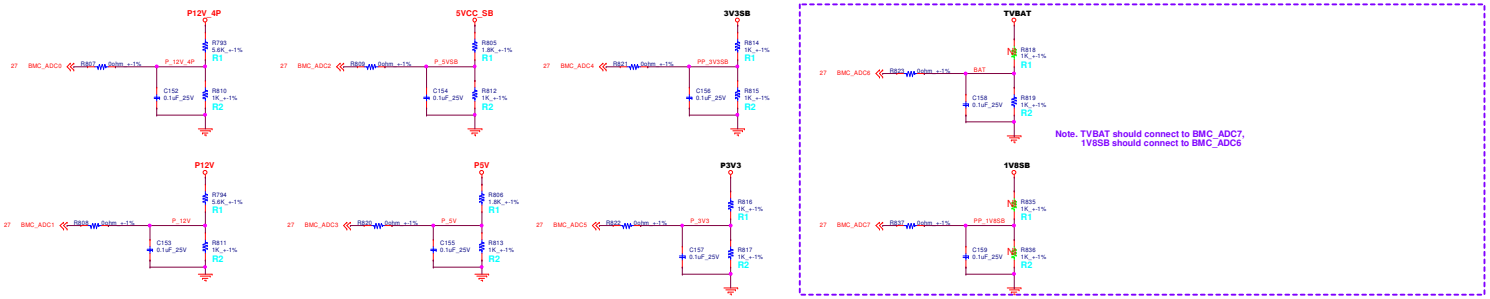
Title
BMC_LAN_RTL8211FI
Size C
Document Number Express-BASE7 R3.1
Rev A1
Date: Monday, December 30, 2024
Sheet 30 of 39



(ADC_Value/1023)*2.5 = V- + (V+-V-)*R2/(R1+R2)



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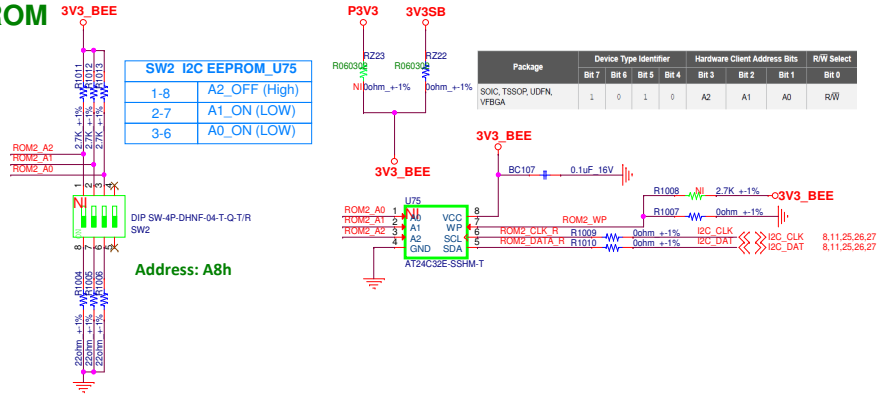
Title: BMC_ADC & FAN

Size: D | Document Number: Express-BASE7 R5.1 | Rev: A1

Date: Monday, December 30, 2024 | Sheet 31 of 39

I2C EEPROM



SW2 I2C EEPROM_U75	
1-8	A2_OFF (High)
2-7	A1_ON (LOW)
3-6	A0_ON (LOW)

Address: A8h

Package	Device Type Identifier				Hardware Client Address Bits			R/W Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, UDFN, VFBGA	1	0	1	0	A2	A1	A0	R/$\overline{W}$

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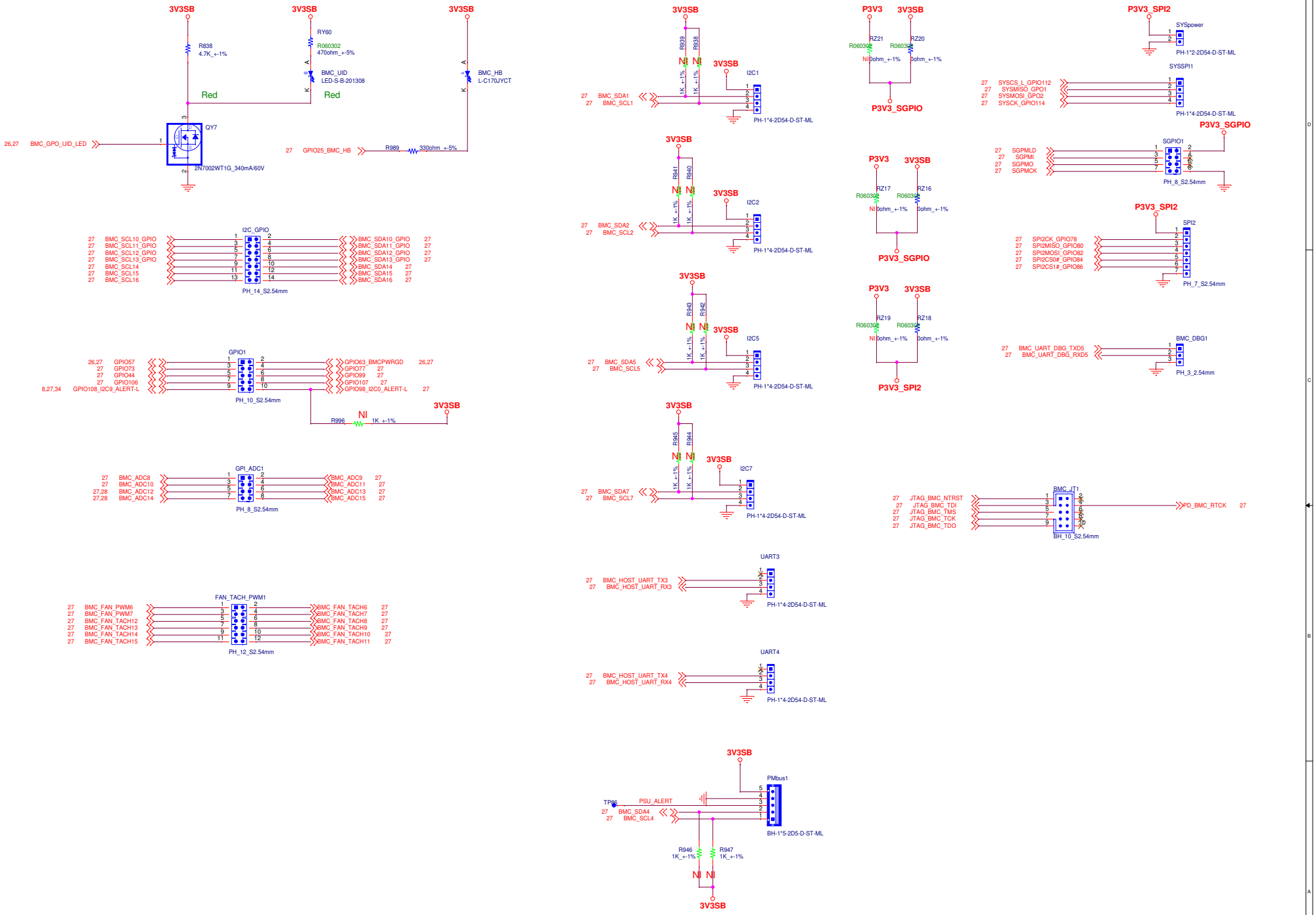
Title	BMC_SPI ROM & I2C EEPROM	
Size C	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 32 of 39	



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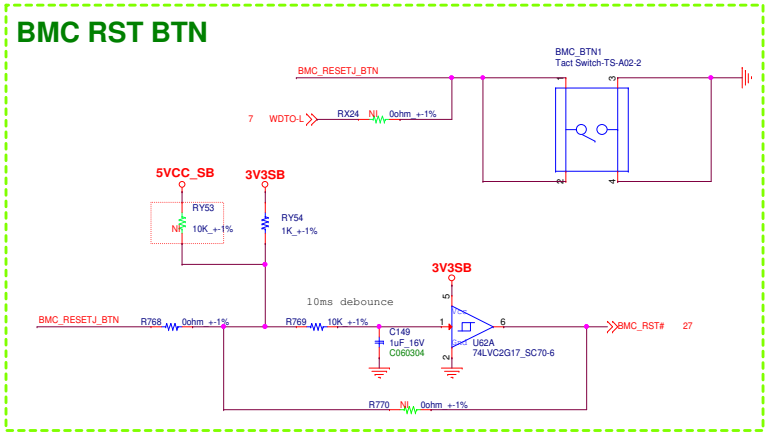
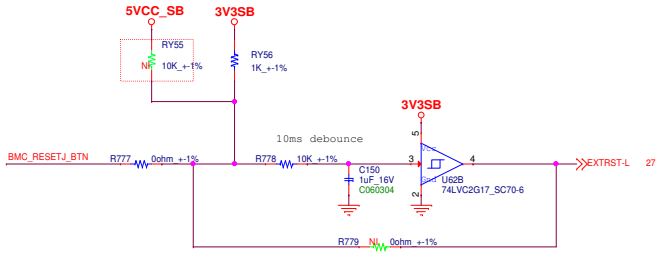
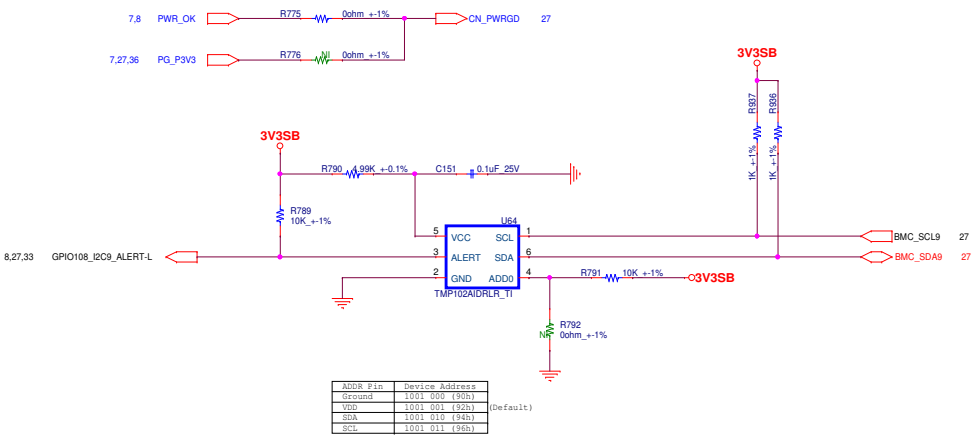
Title	BMC_Misc	
Size C	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 33 of 39	







ADDR Pin	Device Address
Ground	1001 000 (90h)
VDD	1001 001 (92h) (Default)
SDA	1001 010 (94h)
SCL	1001 011 (96h)

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Title	BMC_RSTBTN & Thermal IC	
Size C	Document Number Express-BASE7 R3.1	Rev A1
Date: Monday, December 30, 2024	Sheet 34 of 39	

Power Source

Input -------->
8.5V~19V
23.53A@Vin=8.5V, eff90%
10.53A@Vin=19V, eff90%

ATX_12V — PL1 Cyntec CMMS063T-R10MS 0.1uH_33A 0.1uH/33A/70A/0.8mohm/1mohm 7.2*6.8*3mm — P_+12V_A_VINFLT

VDD/Vdrv/Vbias -------->

P12V — PR1 R060302 0ohm — P_+12V_A_VBIAS_12V
High current jump <0.2mohm
Bias abs 40V

Output <--------

P12V — P12V_

EN

LM5176 POWER SEQUENCE
1.VIN
2.VCC (internal LDO)
3.EN
4.Output
5.PG

7 12V_EN — PR105 0ohm +-1% — EN_P_+12V_A_RS

ATX_12V
PR5 80.6K_+-1%
EN_P_+12V_A_RS — PR8 0ohm +-1% — P_+12V_A_EN
PR11 14.7K_+-1%
PC25 0.1uF_50V C060305

RUN_Pin
Absolute Value:60V to -0.3V
On-Threshold:1.22V(VIN=7.9V)

GND_A_P_+12V_A

PG

P_+12V_A_VCC7V35
PR19 100K_+-1%
36 PG_P12V — PR21 0ohm +-1% — P_+12V_A_PG
PR23 80.6K_+-1%
PD7 MMSZ5231C-TP_5.1V
PC39 10nF_50V

7.35V*(80.6K/(100K+80.6K))
=3.28V

P12V (LM5176)

P12V VR Schematic Description
Vin Range = 8.5~19 V
Vout = 12V
Imax = 15A
Istep= 7.5A
OCP=20A
Soft-Start Time = 7.5mS
Switching Frequecny =277kHZ

SUNCON 25FVF470M+P
Aluminum Electrolytic Capacitors with Hybrid Conductive Polymer
470uF/25V ESR : 14mohm 10*12.5H
Ripple Current : 4700mA@100kHz, 125degC
3400mA@100kHz, 135degC
1800mA@100kHz, 150degC

PC1 470uF_25V SECAP_10X12D8
PC2 470uF_25V SECAP_10X12D8
PC3 470uF_25V SECAP_10X12D8
PC4 470uF_25V SECAP_10X12D8

VIN — P_+12V_A_VINFLT

PC5 10uF_25V C080506_T2
PC6 10uF_25V C080506_T2
PC7 10uF_25V C080506_T2
PC8 10uF_25V C080506_T2
PC9 10uF_25V C080506_T2

PD1 PMEG4010CEJ_40V
PC10 2200pF_50V C060303 Close to MOSFET
PC11 0.1uF_50V C060305
PC12 10uF_25V C080506_T2
PC13 10uF_25V C080506_T2
PC14 10uF_25V C080506_T2
PC15 10uF_25V C080506_T2
PC16 10uF_25V C080506_T2

Ilim=80mV/2.5mOhm=32A

P_+12V_A_VBIAS_12V
P_+12V_A_VIN_R — PR2 10ohm_+-1% R060302 — P_+12V_A_VIN
P_+12V_A_BIAS
PC20 1uF_16V C060304
PC21 1uF_50V C080506_T2

PU1 LM5176PWPR_TI

Pin	Name	Net
24	BIAS	
2	VIN	
9	COMP	P_+12V_A_COMP
4	MODE	P_+12V_A_MODE
6	RT/SYNC	P_+12V_A_RT/SYNC
1	EN/UVLO	P_+12V_A_EN
7	SLOPE	P_+12V_A_SLOPE
5	DITH	P_+12V_A_DITH
8	SS	P_+12V_A_SS
3	VISNS	P_+12V_A_VINSNS
12	VOSNS	P_+12V_A_VOUTSNS
14	ISNS+	P_+12V_A_ISNS+
13	ISNS-	P_+12V_A_ISNS-
16	CS	P_+12V_A_SENSE_P_R
15	CSG	P_+12V_A_SENSE_N_R
11	FB	P_+12V_A_FB
17	PGOOD	P_+12V_A_PG
27	HDRV1	P_+12V_A_TG1
26	BOOT1	P_+12V_A_BST1
28	SW1	P_+12V_A_SW1
25	LDRV1	P_+12V_A_BG1
23	VCC	P_+12V_A_VCC7V35
20	BOOT2	P_+12V_A_BST2
18	SW2	P_+12V_A_SW2
21	LDRV2	P_+12V_A_BG2
19	HDRV2	P_+12V_A_TG2
29	PWPAD	
10	AGND	
22	PGND	

PC23 560pF_50V
PC24 47nF_25V — P_+12V_A_COMP_RC — PR6 7.15K_+-1%
PR10 93.1K_+-1%
PR12 29.4K_+-1%
Mode = 1.85 V, CCM, Hiccup Enabled
Fsw=277K
EN — P_+12V_A_EN
PC29 330pF_50V
PR15 0ohm_+-1%
PC31 47nF_25V
Tss=7.5ms
PC32 100pF_50V
NIPC33 100pF_50V
GND_A_P_+12V_A
P_+12V_A_VINFLT — PR17 2K_+-1%
P12V — PR20 0ohm_+-1% — P_+12V_A_VOUTSNS
P_+12V_A_ISNS+
PC37 0.33uF_25V
P_+12V_A_ISNS-
P_+12V_A_SENSE_P — PR24 100ohm_+-1% — PC40 47pF_50V — P_+12V_A_SENSE_N_R
P_+12V_A_SENSE_N — PR25 100ohm_+-1%
P12V
PR26 0ohm_+-1%
Vout =0.8(1+Ra/Rb) =0.8*(1+280k/20k) =12V
P_+12V_A_FB_R
PR27 280K_+-1%
PR30 20K_+-1%
PG
PR31 R060302 0ohm_+-1%
GND_A_P_+12V_A

P_+12V_A_TG1 — PR13 R060302 0ohm_+-1% — P_+12V_A_TG1_R
P_+12V_A_BST1 — PR14 R060302 2.2ohm_+-1% — P_+12V_A_BST1_RC — PC28 220nF_16V
P_+12V_A_SW1
PD2 PMEG4010CEJ_40V
P_+12V_A_BG1
PC30 C080506_T2 2.2uF_25V
Internal LDO
P_+12V_A_VCC7V35
VCC=7.5V (8V < BIAS < 40V)
PMEG4010CEJ_40V PD3
P_+12V_A_BST2 — PR22 R060302 0ohm_+-1% — P_+12V_A_BST2_RC — PC38 220nF_16V
P_+12V_A_SW2
P_+12V_A_SW2

PQ2 BSC0906NS_63A/30V
PQ1 BSC0901NS_100A/30V
PL2 Cyntec CMMB177T-2R2MS 2.2uH_37A 2.2uH/37A/38A/2.1mohm/2.5mohm 17.4*17.15*7mm
PQ3 BSC0901NS_100A/30V
PQ4 BSC0901NS_100A/30V
P_+12V_A_SENSE_MOS
PR18 5mohm_+-1% R251204_PA_5D29
PR16 5mohm_+-1% R251204_PA_5D29
2W
P_+12V_A_SENSE_P — PSP3 R0402_SHT_PAD
P_+12V_A_SENSE_N — PSP4 R0402_SHT_PAD

2W
PR3 5mohm_+-1% R251204_PA_5D29
PR4 5mohm_+-1% R251204_PA_5D29
PSP1 R0402_SHT_PAD
PSP2 R0402_SHT_PAD
P_+12V_A_IOSENSE_P_R
Vout — P12V

PR7 100ohm_+-1% — P_+12V_A_ISNS-
PR9 100ohm_+-1% — P_+12V_A_ISNS+

Vout cap
Panasonic 16SVP6270M
Aluminum Solid Capacitor Conductive Polymer
270uF/16V ESR : 6mohm 6.3*9.9H
Ripple Current : 5800mA@100kHz @105degC
P12V
PC34 270uF_16V SECAP_6D3X10
PC35 270uF_16V SECAP_6D3X10
PC36 270uF_16V SECAP_6D3X10

PC41 10uF_25V C080506_T2
PC42 10uF_25V C080506_T2
PC43 10uF_25V C080506_T2
PC44 10uF_25V C080506_T2
PC47 10uF_25V C080506_T2
PC48 10uF_25V C080506_T2
PC49 10uF_25V C080506_T2
PC50 10uF_25V C080506_T2

P_+12V_A_SW1 — PR28 1.5ohm_+-1% R251203 — P_+12V_A_SW1_SNUB — PC45 1000pF_100V C060304
P_+12V_A_SW2 — PR29 1ohm_+-1% R120602 — P_+12V_A_SW2_SNUB — PC46 1000pF_100V C060304

P_+12V_A_VINFLT
P_+12V_A_IOSENSE_P_R
PQ5 BSC0906NS_63A/30V
PQ6 BSC0901NS_100A/30V
P_+12V_A_TG1_R
P_+12V_A_SW1
P_+12V_A_TG2
P_+12V_A_SW2
PQ7 BSC0901NS_100A/30V
PD4 VS-30BQ060-M3/9AT_60V
P_+12V_A_BG2
P_+12V_A_SENSE_MOS

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Title	P_+12V_A(LM5176)	
Size: A2	Document Number: Express-BASE7 R3.1	Rev: A1
Date: Monday, December 30, 2024	Sheet 35 of 39	

Power Source

Input --------->
8.5V-19V
5V
7.355A@Vin=8.5V, eff96.23%,PD_H=0.799W,PD_L=0.387W
3.297A@Vin=19V, eff96.02%,PD_H=0.764W,PD_L=0.546W
3V3
7.378A@Vin=8.5V, eff95.11%,PD_H=0.523W,PD_L=0.351W
3.358A@Vin=19V, eff94.43%,PD_H=0.734W,PD_L=0.423W

P5VSB_B/ P3V3 (LM25143)

P5VSB_B Specification:
Vout: 5.00V
Imax: 11A
Istep: 5.5A
Slew Rate: 2.5A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 266.7kHZ

P3V3 Specification:
Vout: 3.30V
Imax: 18A
Istep: 9A
Slew Rate: 2.5A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 266.7kHZ

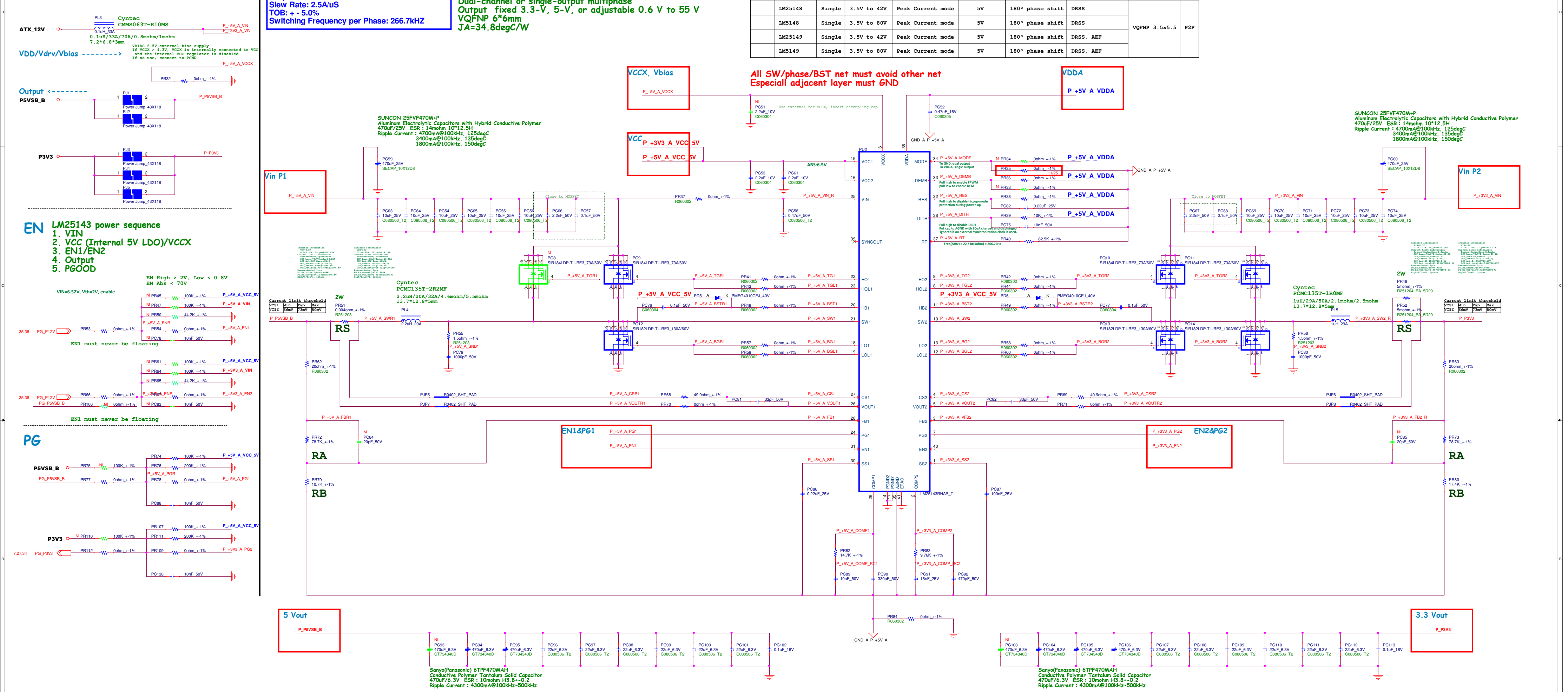
LM25143
Dual Synchronous Buck Controller With Low IQ
VIN range 3.5~42V
Dual-channel or single-output multiphase
Output fixed 3.3-V, 5-V, or adjustable 0.6V to 36V
VQFNP 6*6mm
JA=34.8degC/W

LM5143
Dual Synchronous Buck Controller With Low IQ
VIN range 3.5~65V
Dual-channel or single-output multiphase
Output fixed 3.3-V, 5-V, or adjustable 0.6 V to 55 V
VQFNP 6*6mm
JA=34.8degC/W

LM Buck series

No.	Controller	Phase	Vin Range	Control Method	Gate Driver	Sync Output	EMI Mitigation	SIZE	
	LM25141	Single	3.8V to 42V	Peak Current mode	5V	N/A	SR Control, TRSS	VQFN 4x4	P2P
	LM5141	Single	3.8V to 65V	Peak Current mode	5V	N/A	SR Control, TRSS		
*	LM25143	Dual	3.5V to 42V	Peak Current mode	5V	90° phase shift	SR Control, TRSS	VQFNP 6x6	P2P
	LM5143	Dual	3.5V to 65V	Peak Current mode	5V	90° phase shift	SR Control, TRSS		
	LM25145	Single	6V to 42V	Voltage mode	7.5V	180° phase shift	N/A	VQFNP 3.5x4.5	P2P
	LM5145	Single	5.5V to 75V	Voltage mode	7.5V	180° phase shift	N/A		
	LM5146	Single	5.5V to 100V	Voltage mode	7.5V	180° phase shift	N/A		
	LM25148	Single	3.5V to 42V	Peak Current mode	5V	180° phase shift	DRSS	VQFNP 3.5x5.5	P2P
	LM5148	Single	3.5V to 80V	Peak Current mode	5V	180° phase shift	DRSS		
	LM25149	Single	3.5V to 42V	Peak Current mode	5V	180° phase shift	DRSS, AEF		
	LM5149	Single	3.5V to 80V	Peak Current mode	5V	180° phase shift	DRSS, AEF		

LM25143 TI WEB US$1.32
LM5143 TI WEB US$1.65
LM25148 TI WEB US$0.526
LM5148 TI WEB US$0.605
LM25149 TI WEB US$1.204
LM5149 TI WEB US$1.65



Frequency Settings
Freq(KHz) = 22000/ Rt(kohm)

No.	Freq setting	Rt select	Freq actual
	200kHz	110k	200.0kHz
	220kHz	100k	220.0kHz
	225kHz	97.6k	225.4kHz
	250kHz	88.7k	248.0kHz
*	270kHz	82.5k	266.7kHz
	300kHz	73.2k	300.6kHz
	310kHz	71.5k	307.7kHz
	350kHz	63.4k	347.0kHz
	360kHz	60.4k	364.2kHz
	400kHz	54.9k	400.7kHz
	440kHz	49.9k	440.9kHz
	450kHz	48.7k	451.8kHz
	470kHz	46.4k	474.1kHz
	500kHz	44.2k	497.7kHz

Dual Vout Setting configurations

No.	VOUT1	VOUT2	MODE	FB1	FB2	EA gm
	5V	5V	AGND	AGND	AGND	1200uS
	3.3V	3.3V	AGND	VDDA	VDDA	1200uS
	3.3V	5V	AGND	VDDA	AGND	1200uS
	5V	3.3V	AGND	AGND	VDDA	1200uS
*	Adjust	Adjust	AGND	Adjust	Adjust	1200uS
	5V	5V	10k to AGND	AGND	AGND	60uS
	3.3V	3.3V	10k to AGND	VDDA	VDDA	60uS
	3.3V	5V	10k to AGND	VDDA	AGND	60uS
	5V	3.3V	10k to AGND	AGND	VDDA	60uS
	Adjust	Adjust	10k to AGND	Adjust	Adjust	60uS

Single Vout Interleaved Setting

No.	VOUT	MODE	FB1	FB2
	5V	VDDA	AGND	AGND
	3.3V	VDDA	VDDA	AGND
	Adjust	VDDA	Adjust	AGND

Single Vout Multiphase Setting

No.	VOUT	MODE	FB1(Salve)	FB2(Salve)	
	5V	VDDA	GND	VDDA	DEM
	3.3V	VDDA	VDDA	VDDA	FPWM

DEMB Settings

No.	DEMB	FPWM/DEM
*	VDDA	FPWM
	AGND	DEM
	External clock	FPWM

Vout Setting — Vout = Vvfb(0.6V) * [1+ (Ra / Rb)] — Soft Start recommend Tss(ms) = Css(nF) / 35

No.	Rail	Ra	Rb	Vout	Css	Tss
	0.90V	16.2k	32.4k	0.900V	33nF	0.94mS
	1.00V	16.0k	24.0k	1.000V	33nF	0.94mS
	1.05V	16.2k	21.5k	1.052V	47nF	1.34mS
	1.20V	16.2k	16.0k	1.208V	47nF	1.34mS
	1.50V	16.2k	10.7k	1.508V	56nF	1.60mS
	1.80V	16.2k	8.06k	1.806V	68nF	1.94mS
	2.50V	30.9k	9.76k	2.500V	82nF	2.34mS
*	3.30V	78.7k	17.4k	3.314V	100nF	2.86mS
*	5.00V	78.7k	10.7k	5.013V	220nF	6.29mS
	9.00V	105k	7.50k	9.000V	330nF	9.43mS
	12.0V	150k	7.87k	12.04V	330nF	9.43mS
	15.0V	165k	6.81k	15.14V	470nF	13.43mS
	20.0V	221k	6.81k	20.07V	560nF	16.00mS
	24.0V	249k	6.34k	24.17V	680nF	19.43mS
	30.0V	332k	6.65k	30.56V	680nF	19.43mS

No suitable 330nF for application,
need new apply or use 220nF for 6.29mS

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Title: P_+5V_A/P_+3V3_A (LM25143)
Size: A1 | Document Number: Express-BASE7 R3.1 | Rev: A1
Date: Monday, December 30, 2024 | Sheet 36 of 39

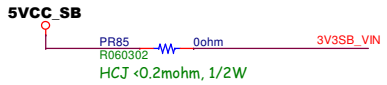
Power Source

Input -------->

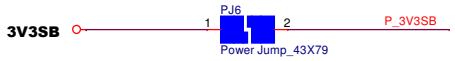
5V

PD calculation deduct DCR loss (Io*Io*DCR 16mohm)

2.806A@Vin=5.0V, eff94.5%,PD=0.516W

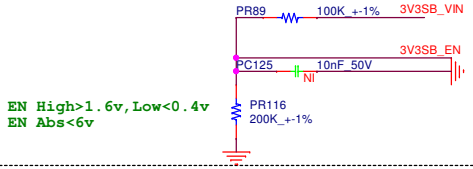


Output <--------

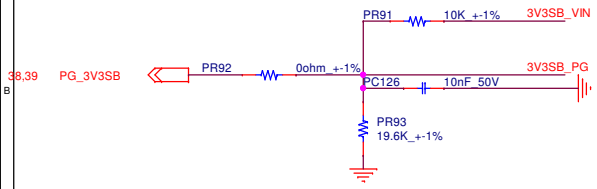


EN

MP2145 power sequence
1. VIN
2. EN
3. Output



PG



MP2145 Pin5, PG internal pull high 500kohm
from VIN
Parallel external 10k, Rth=9.8kohm
If Vin = 5V0, insert 19.6kohm for Vpg=3.33V
If Vin = 3V3, No insert 19.6kohm for Vpg =Vin

PG notes
1. Do loading PG
2. Recommend insert 10k, increase sink cability
3. If PG sink cability not enough,
please adjust divider resistance

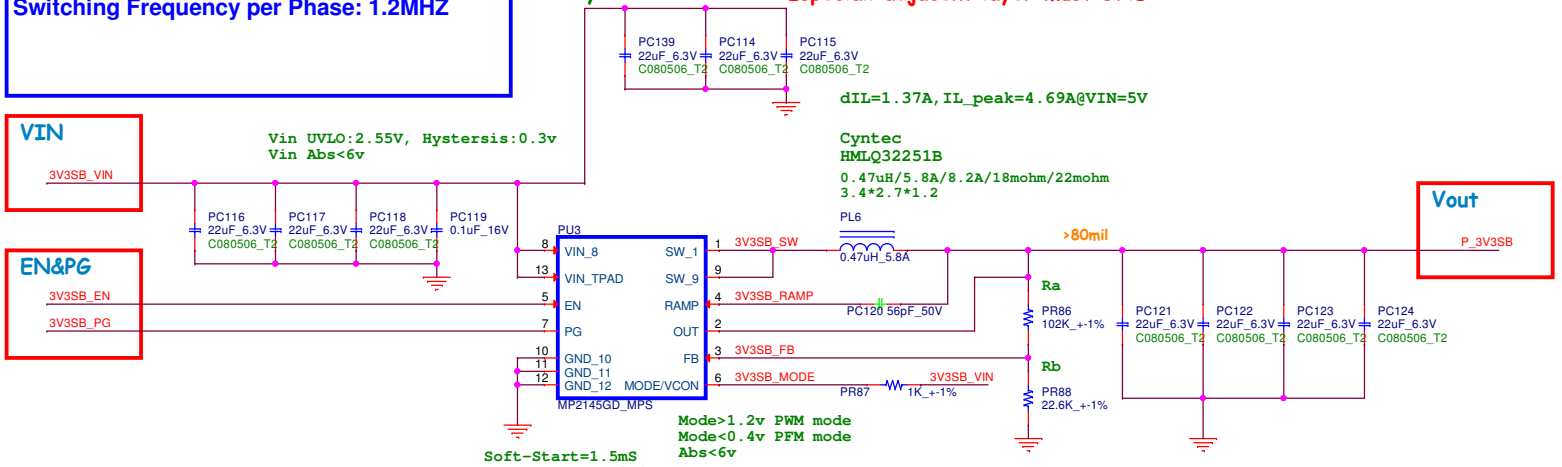
3V3SB (MP2145)

3V3SB Specification:
Vout: 3.3V
Imax: 4.0A
Istep: 2.0A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 1.2MHZ

MP2145
VIN range 2.8~5.5V
Io maximum 6A
QFN 2mm x 3mm
JA=70degC/W

Co-layout : MT3196

All SW/phase/BST net must avoid other net
Especiall adjacent layer must GND



Vout = Vvfb(0.6V) * [1 + (Ra / Rb)]

No.	Rail	Ra	Rb	Vout
	0.90V	100k	200k	0.900V
	0.95V	105k	180k	0.950V
	1.00V	100k	150k	1.000V
	1.05V	100k	133k	1.051V
	1.10V	100k	120k	1.100V
	1.15V	110k	120k	1.150V
	1.20V	100k	100k	1.200V
	1.24V	102k	95.3k	1.242V
	1.35V	200k	160k	1.350V
	1.50V	200k	133k	1.502V
	1.70V	187k	102k	1.700V
	1.80V	200k	100k	1.800V
	2.50V	105k	33k	2.509V
	2.56V	52.3k	16k	2.561V
*	3.30V	102k	22.6k	3.308V

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Title: P_+3V3_A (MP2145)

Size: A3 | Document Number: Express-BASE7 R3.1 | Rev: A1

Date: Monday, December 30, 2024 | Sheet 37 of 39

Power Source

Input -------->

5V

0.395A@Vin=5V, eff91.2%,PD=0.156W

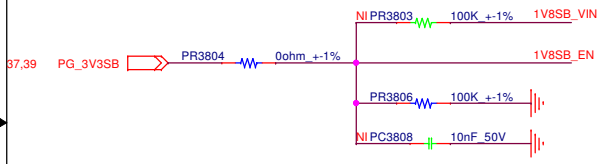
Current below 0.94A, can use normal 0603 resistor
But side effect is voltage drop maximum=Io*50mohm&OCP damage

Output <--------

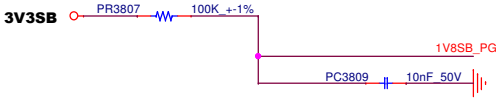
EN

TPS62A02A power sequence
1. VIN
2. EN
3. Output

EN High>1.2V,Low<0.4V
EN ABS<6V
Do not leave the pin floating



PG



1V8SB (TPS62A02A)

1V8SB Specification:
Vout: 1.80V
Imax: 1.0A
Istep: 0.5A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 2.4MHZ

TPS62A02A
VIN range 2.5~5.5V
Io maximum 2.0A
SOT563 1.6mm x 1.6mm
JA=157.3degC/W
JA top=92.2degC/W
WEB Bench JA=90degC/W
EVM JA(TPS62A06A) = 78.5degC

100%duty, HS Rds(on) = 100mohm
Vo = Vin - Io*(RL+Rds(on))
Ex, 3.3Vin/1A -->Vo=3.3-1*(0.1+0.018)=3.182V

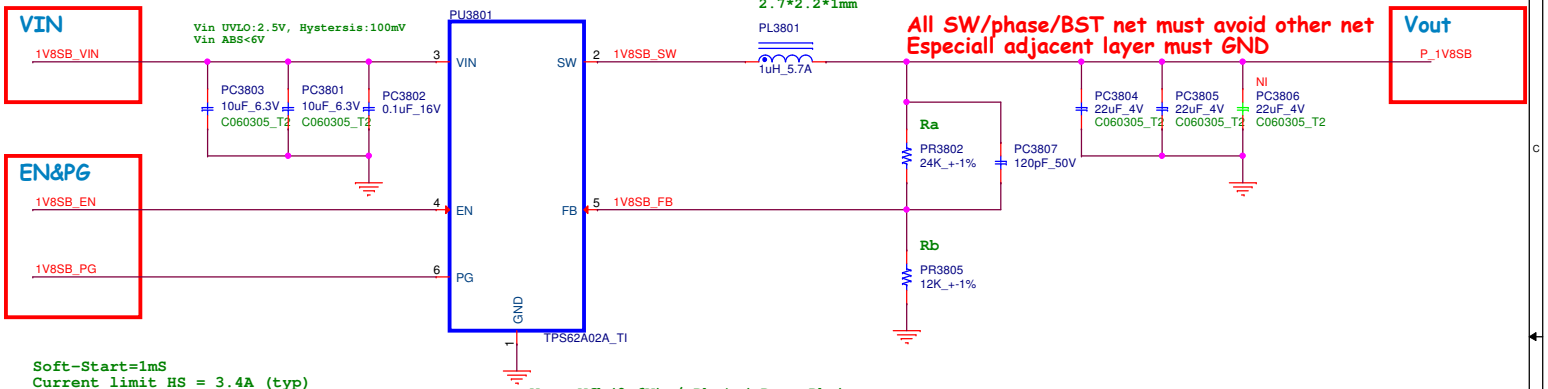
dIL=0.48A, IL_peak=1.24A@VIN=5V

Cyntec
HTQP25201T-1R0MSR
1uH/5.7A/5.5A/18mohm/25mohm
2.7*2.2*1mm

P2P table

No.	PN	Io max	Mode	L
	TPS62A01	1A	PSM/PWM	1uH
	TPS62A01A	1A	FPWM	1uH
	TPS62A02	2A	PSM/PWM	1uH
*	TPS62A02A	2A	FPWM	1uH
	TPS62A06	6A	PSM/PWM	0.22uH
	TPS62A06A	6A	FPWM	0.22uH
	MP2152D	2A	PSM/PWM	1uH
	MP2153D	3A	PSM/PWM	1uH

TPS62A02A P2P/B2B MP2152D
But light load DCM



Soft-Start=1mS
Current limit HS = 3.4A (typ)
Current limit LS = 4.2A (typ)

Vo = Vfb(0.6V) / Rb * (Ra + Rb)

No.	Rail	Ra	Rb	Vout
	0.80V	24k	71.5k	0.8014V
	0.85V	19.6k	47k	0.8502V
	0.90V	21.5k	43k	0.9000V
	0.95V	16k	27.4k	0.9504V
	1.00V	22k	33k	1.0000V
	1.05V	21k	28k	1.0500V
	1.10V	20k	24k	1.1000V
	1.15V	22k	24k	1.1500V
	1.20V	22k	22k	1.2000V
	1.24V	16k	15k	1.2400V
	1.35V	20k	16k	1.3500V
	1.50V	24k	16k	1.5000V
*	1.80V	24k	12k	1.8000V
	2.50V	34k	10.7k	2.5065V
	2.56V	39.2k	12k	2.5600V
	3.30V	45.3k	10k	3.3180V

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Title: P_+1V8_A (TPS62A02A)
Size: A3
Document Number: Express-BASE7 R3.1
Rev: A1
Date: Monday, December 30, 2024
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Power Source

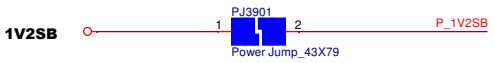
Input -------->

5V

0.273A@Vin=5V, eff87.9%,PD=0.147W

Current below 0.94A, can use normal 0603 resistor
But side effect is voltage drop maximum=Io*50mohm&OCP damage

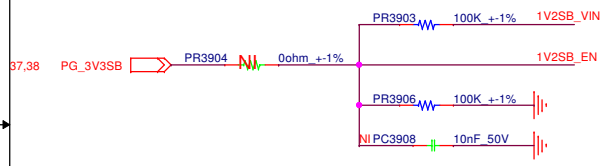
Output <--------



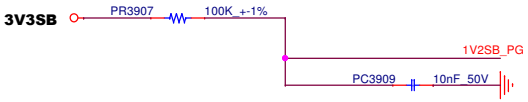
EN

TPS62A02A power sequence
1. VIN
2. EN
3. Output

EN High>1.2V,Low<0.4V
EN ABS<6V
Do not leave the pin floating



PG



1V2SB (TPS62A02A)

1V2SB Specification:
Vout: 1.20V
Imax: 1.0A
Istep: 0.5A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 2.4MHZ

TPS62A02A
VIN range 2.5~5.5V
Io maximum 2.0A
SOT563 1.6mm x 1.6mm
JA=157.3degC/W
JA top=92.2degC/W
WEB Bench JA=90degC/W
EVM JA(TPS62A06A) = 78.5degC

100%duty, HS Rds(on) = 100mohm
Vo = Vin - Io*(RL+Rds(on))
Ex, 3.3Vin/1A -->Vo=3.3-1*(0.1+0.018)=3.182V

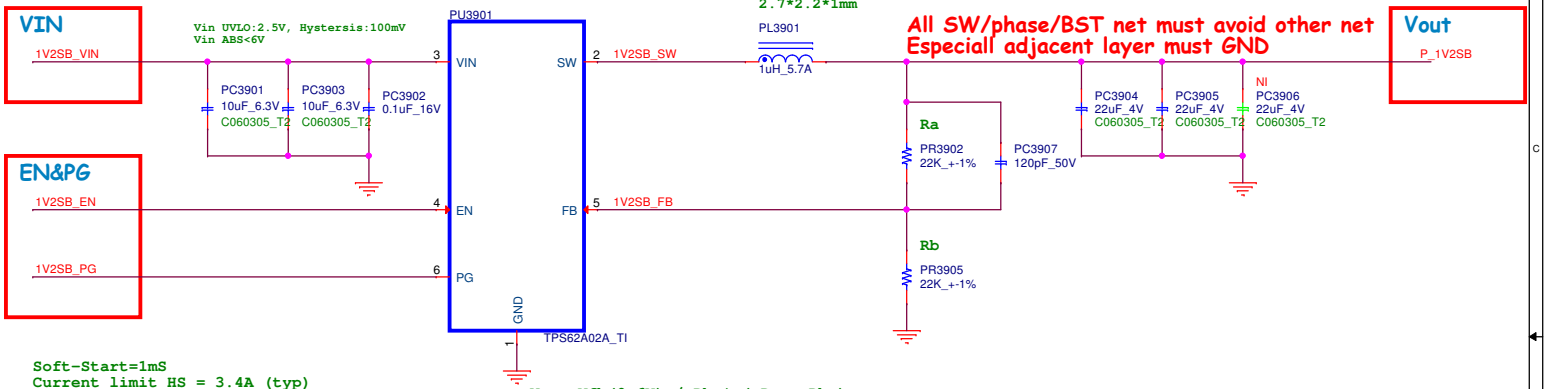
dIL=0.38A, IL_peak=1.19A@VIN=5V

Cyntec
HTQP25201T-1R0MSR
1uH/5.7A/5.5A/18mohm/25mohm
2.7*2.2*1mm

P2P table

No.	PN	Io max	Mode	L
	TPS62A01	1A	PSM/PWM	1uH
	TPS62A01A	1A	FPWM	1uH
	TPS62A02	2A	PSM/PWM	1uH
*	TPS62A02A	2A	FPWM	1uH
	TPS62A06	6A	PSM/PWM	0.22uH
	TPS62A06A	6A	FPWM	0.22uH
	MP2152D	2A	PSM/PWM	1uH
	MP2153D	3A	PSM/PWM	1uH

TPS62A02A P2P/B2B MP2152D
But light load DCM



Soft-Start=1mS
Current limit HS = 3.4A (typ)
Current limit LS = 4.2A (typ)

Vo = Vfb(0.6V) / Rb * (Ra + Rb)

No.	Rail	Ra	Rb	Vout
	0.80V	24k	71.5k	0.8014V
	0.85V	19.6k	47k	0.8502V
	0.90V	21.5k	43k	0.9000V
	0.95V	16k	27.4k	0.9504V
	1.00V	22k	33k	1.0000V
	1.05V	21k	28k	1.0500V
	1.10V	20k	24k	1.1000V
	1.15V	22k	24k	1.1500V
*	1.20V	22k	22k	1.2000V
	1.24V	16k	15k	1.2400V
	1.35V	20k	16k	1.3500V
	1.50V	24k	16k	1.5000V
	1.80V	24k	12k	1.8000V
	2.50V	34k	10.7k	2.5065V
	2.56V	39.2k	12k	2.5600V
	3.30V	45.3k	10k	3.3180V

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Title: P_+1V2_A (TPS62A02A)
Size: A3
Document Number: Express-BASE7 R3.1
Rev: A1
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Application note

Date	Page	Descriptions
20241218	8	a. LPC signals recommended to reserve 8.2pf ground capacitors for EMI b. For VR7 10G BaseT LAN function, Please connect MDIO1 & MDC1 signals to 10G CONN 1.short-circuit TP121 and TP110 2.short-circuit TP120 and TP109 c. LPC SERIRQ need to connect to AST2600 CONN Pin 171 (LPCIRQ_ESPIALERT)
20241218	21	a. For VR7 10G BaseT LAN function, Please connect MDIO1 & MDC1 signals to 10G CONN 1.short-circuit TP121 and TP110 2.short-circuit TP120 and TP109
20241218	28	a. It is recommended to reserve a 150 ohm ground resistor For the RED & GREEN & BLUE signals near VGA CONN side b. The pins MODE0 , MODE1 of SP339 is 5V level signal. And GPIO signal of BMC is 3.3V level. if you want to control the working mode of SP339 by BMC GPIO. Adding signals level shift circuit is necessary. c. The UART TX/RX signals of SP339 is 5V level signal, The UART1 TX/RX signals of BMC is 3.3V level signal. if you want to use BMC UART1 with SP339, adding signals level shift circuit is necessary. short term solution : Remove Q25,Q23, add 0 ohm resistors between Q25 pin1 and pin3, Q23 pin1 and pin3 Long term solution : modify schematic d. CM1_DCD need to connect to pin.16 CM1_DSR need to connect to pin.21 CM1_RXD need to connect to pin.17 CM1_RTS need to connect to pin.22 CM1_TXD need to connect to pin.18 CM1_CTS need to connect to pin.23 CM1_DTR need to connect to pin.19 CM1_RI need to connect to pin.24 GND need to connect to pin.20
20241218	31	a. TVBAT should connect to BMC_ADC7, 1V8SB should connect to BMC_ADC6

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