#ifndef \_pru\_HP\_

#define \_pru\_HP\_

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// \* Global Macro definitions \*

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Refer to this mapping in the file - \prussdrv\include\pruss\_intc\_mapping.h

#define PRU0\_PRU1\_INTERRUPT 17

#define PRU1\_PRU0\_INTERRUPT 18

#define PRU0\_ARM\_INTERRUPT 19

#define PRU1\_ARM\_INTERRUPT 20

#define ARM\_PRU0\_INTERRUPT 21

#define ARM\_PRU1\_INTERRUPT 22

#define CONST\_PRUSSINTC C0

#define CONST\_PRUCFG C4

#define CONST\_PRUDRAM C24

#define CONST\_PRUSHAREDRAM C28

#define CONST\_L3RAM C30

#define CONST\_DDR C31

#define PRU\_ICSS\_BASE 0x4a300000

#define CTRL\_CONTROL 0x22000

#define CTRL\_STATUS 0x22004

#define CTRL\_WAKEUP\_EN 0x22008

#define CTRL\_CYCLE 0x2200c

#define CTRL\_STALL 0x22010

// Address for the Constant table Programmable Pointer Register 0(CTPPR\_0)

#define CTBIR\_0 0x22020

// Address for the Constant table Programmable Pointer Register 0(CTPPR\_0)

#define CTBIR\_1 0x22024

// Address for the Constant table Programmable Pointer Register 0(CTPPR\_0)

#define CTPPR\_0 0x22028

// Address for the Constant table Programmable Pointer Register 1(CTPPR\_1)

#define CTPPR\_1 0x2202C

#define GER\_OFFSET 0x10

#define HIESR\_OFFSET 0x34

#define SICR\_OFFSET 0x24

#define EISR\_OFFSET 0x28

#define INTC\_CHNMAP\_REGS\_OFFSET 0x0400

#define INTC\_HOSTMAP\_REGS\_OFFSET 0x0800

#define INTC\_HOSTINTPRIO\_REGS\_OFFSET 0x0900

#define INTC\_HOSTNEST\_REGS\_OFFSET 0x1100

// Bit 5: 1 - Input, 0 - Output

// Bit 4: 1 - Pull up, 0 - Pull down

// Bit 3: 1 - Pull disabled, 0 - Pull enabled

// Bit 2 \\_

// Bit 1 |- Mode

// Bit 0 /

// MODE0 - Mux Mode 0

// MODE1 - Mux Mode 1

// MODE2 - Mux Mode 2

// MODE3 - Mux Mode 3

// MODE4 - Mux Mode 4

// MODE5 - Mux Mode 5

// MODE6 - Mux Mode 6

// MODE7 - Mux Mode 7

// IDIS - Receiver disabled

// IEN - Receiver enabled

// PD - Internal pull-down

// PU - Internal pull-up

// OFF - Internal pull disabled

#define MODE0 0

#define MODE1 1

#define MODE2 2

#define MODE3 3

#define MODE4 4

#define MODE5 5

#define MODE6 6

#define MODE7 7

#define IDIS (0 << 5)

#define IEN (1 << 5)

#define PD (0 << 3)

#define PU (2 << 3)

#define OFF (1 << 3)

// To get the physical address the offset has

// to be added to AM335X\_CTRL\_BASE

#define CONTROL\_PADCONF\_GPMC\_AD0 0x0800

#define CONTROL\_PADCONF\_GPMC\_AD1 0x0804

#define CONTROL\_PADCONF\_GPMC\_AD2 0x0808

#define CONTROL\_PADCONF\_GPMC\_AD3 0x080C

#define CONTROL\_PADCONF\_GPMC\_AD4 0x0810

#define CONTROL\_PADCONF\_GPMC\_AD5 0x0814

#define CONTROL\_PADCONF\_GPMC\_AD6 0x0818

#define CONTROL\_PADCONF\_GPMC\_AD7 0x081C

#define CONTROL\_PADCONF\_GPMC\_AD8 0x0820

#define CONTROL\_PADCONF\_GPMC\_AD9 0x0824

#define CONTROL\_PADCONF\_GPMC\_AD10 0x0828

#define CONTROL\_PADCONF\_GPMC\_AD11 0x082C

#define CONTROL\_PADCONF\_GPMC\_AD12 0x0830

#define CONTROL\_PADCONF\_GPMC\_AD13 0x0834

#define CONTROL\_PADCONF\_GPMC\_AD14 0x0838

#define CONTROL\_PADCONF\_GPMC\_AD15 0x083C

#define CONTROL\_PADCONF\_GPMC\_A0 0x0840

#define CONTROL\_PADCONF\_GPMC\_A1 0x0844

#define CONTROL\_PADCONF\_GPMC\_A2 0x0848

#define CONTROL\_PADCONF\_GPMC\_A3 0x084C

#define CONTROL\_PADCONF\_GPMC\_A4 0x0850

#define CONTROL\_PADCONF\_GPMC\_A5 0x0854

#define CONTROL\_PADCONF\_GPMC\_A6 0x0858

#define CONTROL\_PADCONF\_GPMC\_A7 0x085C

#define CONTROL\_PADCONF\_GPMC\_A8 0x0860

#define CONTROL\_PADCONF\_GPMC\_A9 0x0864

#define CONTROL\_PADCONF\_GPMC\_A10 0x0868

#define CONTROL\_PADCONF\_GPMC\_A11 0x086C

#define CONTROL\_PADCONF\_GPMC\_WAIT0 0x0870

#define CONTROL\_PADCONF\_GPMC\_WPN 0x0874

#define CONTROL\_PADCONF\_GPMC\_BEN1 0x0878

#define CONTROL\_PADCONF\_GPMC\_CSN0 0x087C

#define CONTROL\_PADCONF\_GPMC\_CSN1 0x0880

#define CONTROL\_PADCONF\_GPMC\_CSN2 0x0884

#define CONTROL\_PADCONF\_GPMC\_CSN3 0x0888

#define CONTROL\_PADCONF\_GPMC\_CLK 0x088C

#define CONTROL\_PADCONF\_GPMC\_ADVN\_ALE 0x0890

#define CONTROL\_PADCONF\_GPMC\_OEN\_REN 0x0894

#define CONTROL\_PADCONF\_GPMC\_WEN 0x0898

#define CONTROL\_PADCONF\_GPMC\_BEN0\_CLE 0x089C

#define CONTROL\_PADCONF\_LCD\_DATA0 0x08A0

#define CONTROL\_PADCONF\_LCD\_DATA1 0x08A4

#define CONTROL\_PADCONF\_LCD\_DATA2 0x08A8

#define CONTROL\_PADCONF\_LCD\_DATA3 0x08AC

#define CONTROL\_PADCONF\_LCD\_DATA4 0x08B0

#define CONTROL\_PADCONF\_LCD\_DATA5 0x08B4

#define CONTROL\_PADCONF\_LCD\_DATA6 0x08B8

#define CONTROL\_PADCONF\_LCD\_DATA7 0x08BC

#define CONTROL\_PADCONF\_LCD\_DATA8 0x08C0

#define CONTROL\_PADCONF\_LCD\_DATA9 0x08C4

#define CONTROL\_PADCONF\_LCD\_DATA10 0x08C8

#define CONTROL\_PADCONF\_LCD\_DATA11 0x08CC

#define CONTROL\_PADCONF\_LCD\_DATA12 0x08D0

#define CONTROL\_PADCONF\_LCD\_DATA13 0x08D4

#define CONTROL\_PADCONF\_LCD\_DATA14 0x08D8

#define CONTROL\_PADCONF\_LCD\_DATA15 0x08DC

#define CONTROL\_PADCONF\_LCD\_VSYNC 0x08E0

#define CONTROL\_PADCONF\_LCD\_HSYNC 0x08E4

#define CONTROL\_PADCONF\_LCD\_PCLK 0x08E8

#define CONTROL\_PADCONF\_LCD\_AC\_BIAS\_EN 0x08EC

#define CONTROL\_PADCONF\_MMC0\_DAT3 0x08F0

#define CONTROL\_PADCONF\_MMC0\_DAT2 0x08F4

#define CONTROL\_PADCONF\_MMC0\_DAT1 0x08F8

#define CONTROL\_PADCONF\_MMC0\_DAT0 0x08FC

#define CONTROL\_PADCONF\_MMC0\_CLK 0x0900

#define CONTROL\_PADCONF\_MMC0\_CMD 0x0904

#define CONTROL\_PADCONF\_MII1\_COL 0x0908

#define CONTROL\_PADCONF\_MII1\_CRS 0x090C

#define CONTROL\_PADCONF\_MII1\_RX\_ER 0x0910

#define CONTROL\_PADCONF\_MII1\_TX\_EN 0x0914

#define CONTROL\_PADCONF\_MII1\_RX\_DV 0x0918

#define CONTROL\_PADCONF\_MII1\_TXD3 0x091C

#define CONTROL\_PADCONF\_MII1\_TXD2 0x0920

#define CONTROL\_PADCONF\_MII1\_TXD1 0x0924

#define CONTROL\_PADCONF\_MII1\_TXD0 0x0928

#define CONTROL\_PADCONF\_MII1\_TX\_CLK 0x092C

#define CONTROL\_PADCONF\_MII1\_RX\_CLK 0x0930

#define CONTROL\_PADCONF\_MII1\_RXD3 0x0934

#define CONTROL\_PADCONF\_MII1\_RXD2 0x0938

#define CONTROL\_PADCONF\_MII1\_RXD1 0x093C

#define CONTROL\_PADCONF\_MII1\_RXD0 0x0940

#define CONTROL\_PADCONF\_RMII1\_REF\_CLK 0x0944

#define CONTROL\_PADCONF\_MDIO 0x0948

#define CONTROL\_PADCONF\_MDC 0x094C

#define CONTROL\_PADCONF\_SPI0\_SCLK 0x0950

#define CONTROL\_PADCONF\_SPI0\_D0 0x0954

#define CONTROL\_PADCONF\_SPI0\_D1 0x0958

#define CONTROL\_PADCONF\_SPI0\_CS0 0x095C

#define CONTROL\_PADCONF\_SPI0\_CS1 0x0960

#define CONTROL\_PADCONF\_ECAP0\_IN\_PWM0\_OUT 0x0964

#define CONTROL\_PADCONF\_UART0\_CTSN 0x0968

#define CONTROL\_PADCONF\_UART0\_RTSN 0x096C

#define CONTROL\_PADCONF\_UART0\_RXD 0x0970

#define CONTROL\_PADCONF\_UART0\_TXD 0x0974

#define CONTROL\_PADCONF\_UART1\_CTSN 0x0978

#define CONTROL\_PADCONF\_UART1\_RTSN 0x097C

#define CONTROL\_PADCONF\_UART1\_RXD 0x0980

#define CONTROL\_PADCONF\_UART1\_TXD 0x0984

#define CONTROL\_PADCONF\_I2C0\_SDA 0x0988

#define CONTROL\_PADCONF\_I2C0\_SCL 0x098C

#define CONTROL\_PADCONF\_MCASP0\_ACLKX 0x0990

#define CONTROL\_PADCONF\_MCASP0\_FSX 0x0994

#define CONTROL\_PADCONF\_MCASP0\_AXR0 0x0998

#define CONTROL\_PADCONF\_MCASP0\_AHCLKR 0x099C

#define CONTROL\_PADCONF\_MCASP0\_ACLKR 0x09A0

#define CONTROL\_PADCONF\_MCASP0\_FSR 0x09A4

#define CONTROL\_PADCONF\_MCASP0\_AXR1 0x09A8

#define CONTROL\_PADCONF\_MCASP0\_AHCLKX 0x09AC

#define CONTROL\_PADCONF\_XDMA\_EVENT\_INTR0 0x09B0

#define CONTROL\_PADCONF\_XDMA\_EVENT\_INTR1 0x09B4

#define CONTROL\_PADCONF\_WARMRSTN 0x09B8

#define CONTROL\_PADCONF\_PWRONRSTN 0x09BC

#define CONTROL\_PADCONF\_EXTINTN 0x09C0

#define CONTROL\_PADCONF\_XTALIN 0x09C4

#define CONTROL\_PADCONF\_XTALOUT 0x09C8

#define CONTROL\_PADCONF\_TMS 0x09D0

#define CONTROL\_PADCONF\_TDI 0x09D4

#define CONTROL\_PADCONF\_TDO 0x09D8

#define CONTROL\_PADCONF\_TCK 0x09DC

#define CONTROL\_PADCONF\_TRSTN 0x09E0

#define CONTROL\_PADCONF\_EMU0 0x09E4

#define CONTROL\_PADCONF\_EMU1 0x09E8

#define CONTROL\_PADCONF\_RTC\_XTALIN 0x09EC

#define CONTROL\_PADCONF\_RTC\_XTALOUT 0x09F0

#define CONTROL\_PADCONF\_RTC\_PWRONRSTN 0x09F8

#define CONTROL\_PADCONF\_PMIC\_POWER\_EN 0x09FC

#define CONTROL\_PADCONF\_EXT\_WAKEUP 0x0A00

#define CONTROL\_PADCONF\_RTC\_KALDO\_ENN 0x0A04

#define CONTROL\_PADCONF\_USB0\_DM 0x0A08

#define CONTROL\_PADCONF\_USB0\_DP 0x0A0C

#define CONTROL\_PADCONF\_USB0\_CE 0x0A10

#define CONTROL\_PADCONF\_USB0\_ID 0x0A14

#define CONTROL\_PADCONF\_USB0\_VBUS 0x0A18

#define CONTROL\_PADCONF\_USB0\_DRVVBUS 0x0A1C

#define CONTROL\_PADCONF\_USB1\_DM 0x0A20

#define CONTROL\_PADCONF\_USB1\_DP 0x0A24

#define CONTROL\_PADCONF\_USB1\_CE 0x0A28

#define CONTROL\_PADCONF\_USB1\_ID 0x0A2C

#define CONTROL\_PADCONF\_USB1\_VBUS 0x0A30

#define CONTROL\_PADCONF\_USB1\_DRVVBUS 0x0A34

#define CONTROL\_PADCONF\_DDR\_RESETN 0x0A38

#define CONTROL\_PADCONF\_DDR\_CSN0 0x0A3C

#define CONTROL\_PADCONF\_DDR\_CKE 0x0A40

#define CONTROL\_PADCONF\_DDR\_CK 0x0A44

#define CONTROL\_PADCONF\_DDR\_CKN 0x0A48

#define CONTROL\_PADCONF\_DDR\_CASN 0x0A4C

#define CONTROL\_PADCONF\_DDR\_RASN 0x0A50

#define CONTROL\_PADCONF\_DDR\_WEN 0x0A54

#define CONTROL\_PADCONF\_DDR\_BA0 0x0A58

#define CONTROL\_PADCONF\_DDR\_BA1 0x0A5C

#define CONTROL\_PADCONF\_DDR\_BA2 0x0A60

#define CONTROL\_PADCONF\_DDR\_A0 0x0A64

#define CONTROL\_PADCONF\_DDR\_A1 0x0A68

#define CONTROL\_PADCONF\_DDR\_A2 0x0A6C

#define CONTROL\_PADCONF\_DDR\_A3 0x0A70

#define CONTROL\_PADCONF\_DDR\_A4 0x0A74

#define CONTROL\_PADCONF\_DDR\_A5 0x0A78

#define CONTROL\_PADCONF\_DDR\_A6 0x0A7C

#define CONTROL\_PADCONF\_DDR\_A7 0x0A80

#define CONTROL\_PADCONF\_DDR\_A8 0x0A84

#define CONTROL\_PADCONF\_DDR\_A9 0x0A88

#define CONTROL\_PADCONF\_DDR\_A10 0x0A8C

#define CONTROL\_PADCONF\_DDR\_A11 0x0A90

#define CONTROL\_PADCONF\_DDR\_A12 0x0A94

#define CONTROL\_PADCONF\_DDR\_A13 0x0A98

#define CONTROL\_PADCONF\_DDR\_A14 0x0A9C

#define CONTROL\_PADCONF\_DDR\_A15 0x0AA0

#define CONTROL\_PADCONF\_DDR\_ODT 0x0AA4

#define CONTROL\_PADCONF\_DDR\_D0 0x0AA8

#define CONTROL\_PADCONF\_DDR\_D1 0x0AAC

#define CONTROL\_PADCONF\_DDR\_D2 0x0AB0

#define CONTROL\_PADCONF\_DDR\_D3 0x0AB4

#define CONTROL\_PADCONF\_DDR\_D4 0x0AB8

#define CONTROL\_PADCONF\_DDR\_D5 0x0ABC

#define CONTROL\_PADCONF\_DDR\_D6 0x0AC0

#define CONTROL\_PADCONF\_DDR\_D7 0x0AC4

#define CONTROL\_PADCONF\_DDR\_D8 0x0AC8

#define CONTROL\_PADCONF\_DDR\_D9 0x0ACC

#define CONTROL\_PADCONF\_DDR\_D10 0x0AD0

#define CONTROL\_PADCONF\_DDR\_D11 0x0AD4

#define CONTROL\_PADCONF\_DDR\_D12 0x0AD8

#define CONTROL\_PADCONF\_DDR\_D13 0x0ADC

#define CONTROL\_PADCONF\_DDR\_D14 0x0AE0

#define CONTROL\_PADCONF\_DDR\_D15 0x0AE4

#define CONTROL\_PADCONF\_DDR\_DQM0 0x0AE8

#define CONTROL\_PADCONF\_DDR\_DQM1 0x0AEC

#define CONTROL\_PADCONF\_DDR\_DQS0 0x0AF0

#define CONTROL\_PADCONF\_DDR\_DQSN0 0x0AF4

#define CONTROL\_PADCONF\_DDR\_DQS1 0x0AF8

#define CONTROL\_PADCONF\_DDR\_DQSN1 0x0AFC

#define CONTROL\_PADCONF\_DDR\_VREF 0x0B00

#define CONTROL\_PADCONF\_DDR\_VTP 0x0B04

#define CONTROL\_PADCONF\_AIN7 0x0B10

#define CONTROL\_PADCONF\_AIN6 0x0B14

#define CONTROL\_PADCONF\_AIN5 0x0B18

#define CONTROL\_PADCONF\_AIN4 0x0B1C

#define CONTROL\_PADCONF\_AIN3 0x0B20

#define CONTROL\_PADCONF\_AIN2 0x0B24

#define CONTROL\_PADCONF\_AIN1 0x0B28

#define CONTROL\_PADCONF\_AIN0 0x0B2C

#define CONTROL\_PADCONF\_VREFP 0x0B30

#define CONTROL\_PADCONF\_VREFN 0x0B34

#define AM335X\_CTRL\_BASE 0x44E10000

.macro MUX

.mparam dst, src

    MOV r28, AM335X\_CTRL\_BASE + dst

    MOV r29, src

    ST32 r28, r29

.endm

.macro LD32

.mparam dst,src

    LBBO dst,src,#0x00,4

.endm

.macro LD16

.mparam dst,src

    LBBO dst,src,#0x00,2

.endm

.macro LD8

.mparam dst,src

    LBBO dst,src,#0x00,1

.endm

.macro ST32

.mparam src,dst

    SBBO src,dst,#0x00,4

.endm

.macro ST16

.mparam src,dst

    SBBO src,dst,#0x00,2

.endm

.macro ST8

.mparam src,dst

    SBBO src,dst,#0x00,1

.endm

.macro POKE

.mparam addr, value

    mov r0, value

    mov r1, addr

    sbbo r0, r1, 0, 4

.endm

.macro PEEK

.mparam addr

    mov r1, addr

    lbbo r0, r1, 0, 4

.endm

.macro BLE

.mparam dest, arg1, arg2

    qbge dest, arg1, arg2

.endm

.macro BLT

.mparam dest, arg1, arg2

    qbgt dest, arg1, arg2

.endm

.macro BGE

.mparam dest, arg1, arg2

    qble dest, arg1, arg2

.endm

.macro BGT

.mparam dest, arg1, arg2

    qblt dest, arg1, arg2

.endm

#define GPIO0 0x44e07000

#define GPIO1 0x4804c000

#define GPIO2 0x481ac000

#define GPIO3 0x481ae000

#define GPIO\_REVISION 0x0

#define GPIO\_SYSCONFIG 0x10

#define GPIO\_IRQSTATUS\_RAW\_0 0x24

#define GPIO\_IRQSTATUS\_RAW\_1 0x28

#define GPIO\_IRQSTATUS\_0 0x2C

#define GPIO\_IRQSTATUS\_1 0x30

#define GPIO\_IRQSTATUS\_SET\_0 0x34

#define GPIO\_IRQSTATUS\_SET\_1 0x38

#define GPIO\_IRQSTATUS\_CLR\_0 0x3C

#define GPIO\_IRQSTATUS\_CLR\_1 0x40

#define GPIO\_IRQWAKEN\_0 0x44

#define GPIO\_IRQWAKEN\_1 0x48

#define GPIO\_SYSSTATUS 0x114

#define GPIO\_CTRL 0x130

#define GPIO\_OE 0x134

#define GPIO\_DATAIN 0x138

#define GPIO\_DATAOUT 0x13C

#define GPIO\_LEVELDETECT0 0x140

#define GPIO\_LEVELDETECT1 0x144

#define GPIO\_RISINGDETECT 0x148

#define GPIO\_FALLINGDETECT 0x14C

#define GPIO\_DEBOUNCENABLE 0x150

#define GPIO\_DEBOUNCINGTIME 0x154

#define GPIO\_CLEARDATAOUT 0x190

#define GPIO\_SETDATAOUT 0x194

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// \* Global Structure Definitions \*

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.struct Global

    .u32 regPointer

    .u32 regVal

.ends

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// \* Global Register Assignments \*

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.assign Global, r2, \*, global

#endif // \_pru\_HP\_