CDA 3103 Computer Organization Module 6 Assignment

Part I: Problems

1. [20 points] Suppose a computer has 2^{32} bytes of byte-addressable main memory and a cache size of 2^{15} bytes, and each cache block contains 64 bytes.

    a) How many blocks of main memory are there? (___**2^{26} Blocks**___)

    b) How many blocks of cache memory are there? (___**2^{9} Blocks**___)

    c) If this cache is direct-mapped, what is the format of a memory address as seen by the cache; that is, the size of the tag field__**17**__, the size of block field__**9**__, and the size of the offset field__**6**__.

    d) If this cache is fully associative, what is the format of a memory address as seen by the cache; that is, the size of the tag field__**26**__, and the size of the offset field__**6**__.

    e) If this cache is 4-way set associative, what is the format of a memory address as seen by the cache; that is, the size of the tag field__**19**__, the size of set field__**7**__, and the size of the offset field__**6**__.

2. [24 points] Suppose we have a memory and a direct-mapped cache with the following characteristics.
    - Memory is byte addressable
    - Memory addresses are 16 bits
    - The cache has 8 blocks
    - Each cache block holds 16 bytes of data

a) [6 points] In the spaces below, indicate how the 16 address bits are allocated to the offset, index, and tag parts of the address used to reference the cache:__**4**__offset bits __**3**__tag bits __**9**__ index bits.

b) [12 points] Below is a sequence of four binary memory addresses in the order they are used to reference memory. Assume that the cache is initially empty. For each reference, write down the tag and index bits and circle either hit or miss to indicate whether that reference is a hit or a miss.

Memory address	Tag	Index	Hit / Miss (circle)
0010 1101 1011 0011	**0010 1101 1**	**011**	**Miss**
0000 0110 1111 1100	**0000 0110 1**	**111**	**Miss**
0010 1101 1011 1000	**0010 1101 1**	**011**	**Hit**
1010 1010 1010 1011	**1010 1010 1**	**010**	**Miss**

c) [6 points] Suppose the cache access time is 15ns, main memory access time is 220ns, and the cache hit rate is 95%. Assuming non-overlapped access, what is the

average access time for the processor to access an item?

(.95)(15ns) +(.05)(220ns + 15ns)

3. [20 points] Assuming a cache of 4096 blocks, a four-word block size, each word contains 4 bytes, and a 64-bits memory address. Memory is byte addressable, and random block replacement policy and write back policy are implemented. Find the total number of tag bits for caches that are
    a) direct-mapped
    Tap = 48 bit
    b) 2-way set associative
    Tag = 49 bit
    c) 4-way set associative
    Tag = 50 bit
    d) Fully associative
    Tag = 60 bit

4. [30 points] Suppose you have a byte-addressable virtual address memory system with 8 virtual pages of 64 bytes each, and 4 page frames. Assuming the following page table, answer the questions below:

Page #	Frame #	Valid Bit
0	1	1
1	3	1
2	-	0
3	0	1
4	2	1
5	-	0
6	-	0
7	-	0

    a) [2 points] How many bits are in a virtual address?
    9 bits
    b) [2 points] How many bits are in a physical address?
    8 bits
    c) [2 points] How many bits are virtual page number?
    3 bits
    d) [2 points] How many bits are page frame number?
    2 bits
    e) [2 points] How many bits are page offset?
    6 bits
    f) [20 points] What physical address corresponds to the following virtual addresses (if the address causes a page fault, simply indicate this is the case)?
        1) 0x00
        01 00 0000, Hit
        2) 0x44
        11 00 0100, Hit

3) 0xC2

00 00 0010, Hit

4) 0x80

Page fault.

5. [6 points] Suppose we have 2^{10} bytes of virtual memory and 2^8 bytes of physical main memory. Suppose the page size is 2^4 bytes.

   a) [2 points] How many pages are there in virtual memory?

   2^6 pages

   b) [2 points] How many page frames are there in main memory?

   2^4 pages

   c) [2 points] How many entries are in the page table for a process that uses all of virtual memory?

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Part II: Submission Requirements