# Audio Mini: Terasic DE10-Nano Expansion Card

- --- Description:
- Intel Cyclone V SE 5CSEBA6U23I7NDK
- AD1939 Audio Codec
- Audio Output: Line Out TPA6120
- Audio Input: Digital Microphones INMP621 Not Populated by Default
- Audio Output: Headphone Out TPA6130
- User Switches and LEDs
- ---Frrata:
- 1. June 2018 First release, production-level prototype. Rev: 1P0
- 2. September 2020 Updated Schematics, PCB to AudioLogic Rev 1P1

Title: Audio Mini

Errata and Table of Contents

Sheet: 1 of 11 Size: 11 x 8.5 Inches

Table of Contents

Date: 9/10/2020 Time: 1:46:28 PM

System Architecture Engineer: Connor Dack

Connection Diagram File: Description+Errata.SchDoc

THE HARDWARE IS PROVIDED 'AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABUTY, FITNESS FOR A PARTICULAR PURPOSE AND NOMINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPPRIGHT HOLDER'S BE LIBILE FOR ANY CLAIM, DAMAGES OR OTHER LIBILITY, WEITHER IN AN ACTION OF CONTRACT, TONT OR OTHERWIS SHOWNED FROM OUT OF OR IN COMMECTION WITH THE HARDWARE OR THE USES OF OTHER DELAWING IN THE HARDWARE.

.

4

### Table of Contents

- Sheet 1. Description & Errata
- Sheet 2. Table of Contents
- Sheet 3. System Architecture
- Sheet 4. Top Level Hierarchy
- Sheet 5. Audio Codec AD1939
- Sheet 6. FPGA Connectors
- Sheet 7. Power
- Sheet 8. Support
- Sheet 9. Audio Inputs: Microphone In
- Sheet 10. Audio Inputs: MEMS Microphones
- Sheet 11. Audio Outputs: Headphone Out

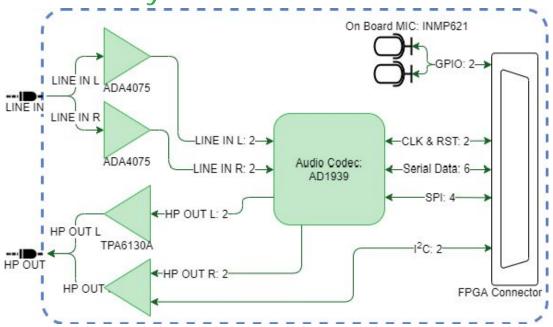
Title: Audio Mini Rev: 1P1 **Table of Contents** Sheet: 2 of 11 Size: 11 x 8.5 Inches Date: 9/10/2020 Time: 1:46:28 PM AudioLogic <sub>D</sub> Engineer: Connor Dack

File: ToC.SchDoc

Copyright 2020 Audio Logic Inc

COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE ARISING FROM, OUT OF OR IN CONNECTION WITH THE HARDWARE OR THE USE OR OTHER DEALINGS IN THE HARDWARE.





Title: Audio Mini	Rev: 1P1	
System Architect	6	
Sheet: 3 of 11	Size: 11 x 8.5 Inches	(C.V-
Date: 9/10/2020	Time: 1:46:28 PM	<b>Audio</b> Logic
Engineer: Connor Dack		AddioLogic

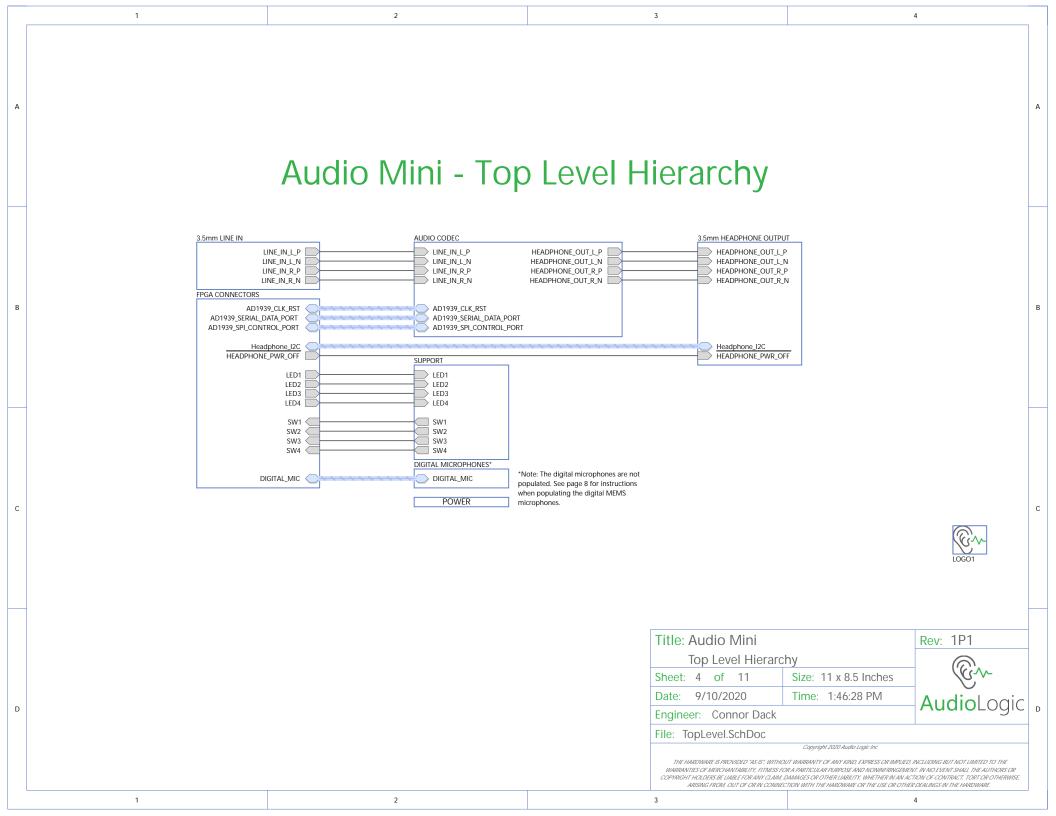
Engineer: Connor Dad

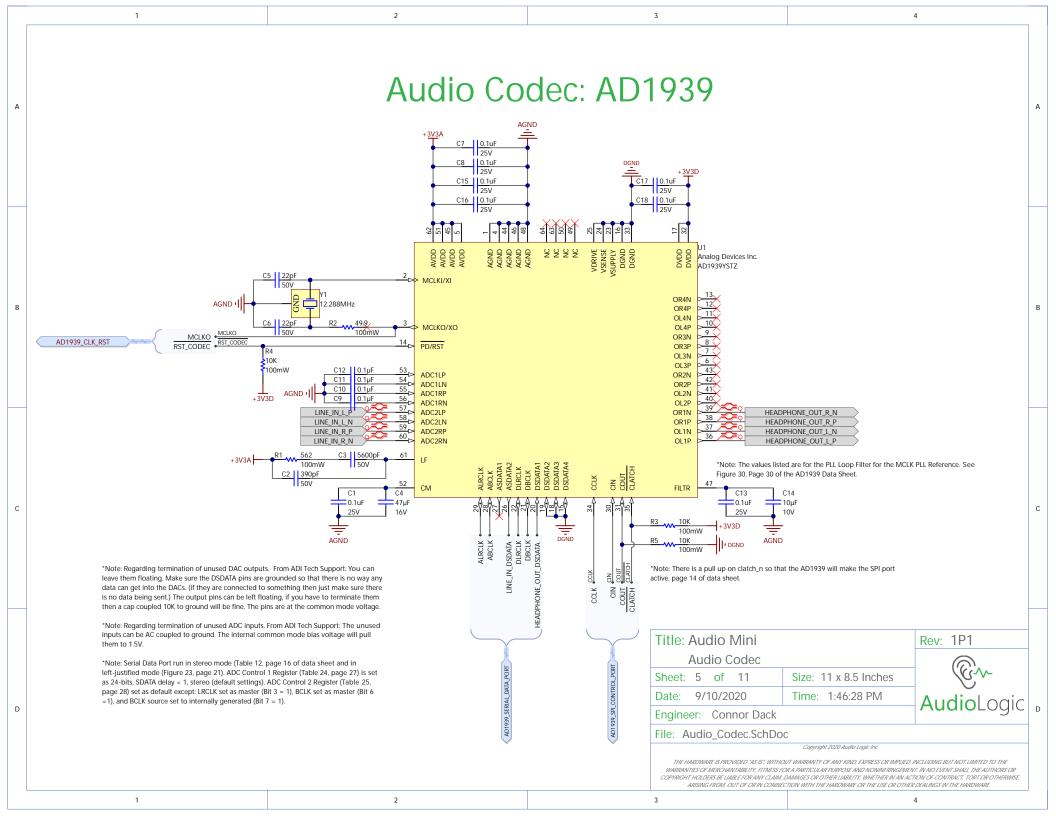
File: System\_Architecture.SchDoc

Copyright 2020 Audio Logic Inc

THE HARDWARE IS PROVIDED 'AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABUTY, FITNESS FOR A PARTICULAR PURPOSE AND NONWERWEGHENT, IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONSTRUTE, TORT OR OTHERWISE, ARSING FROM, OUT OF OR IN CONNECTION WITH THE HARDWARE OR THE USE OR OTHER DELINIS IN THE HARDWARE.

1 2 3

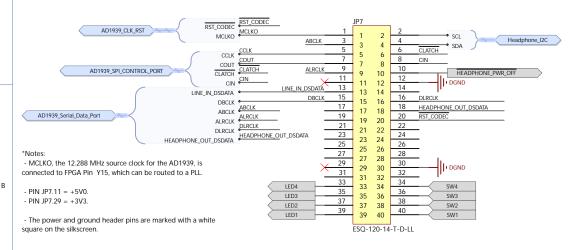


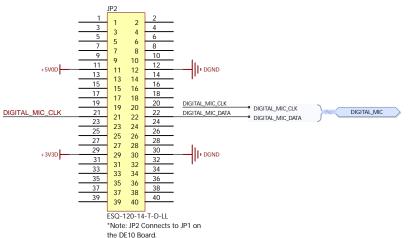




### **FPGA Headers**

Quartus Top Lovel Signal





### FPGA Pin Assignment Table

Schematic Signal Group	Schematic Net Name	Device Signal Name	Device / Part Number	/ Pin Number	FPGA Pin	Quartus Top Level Signal Name
AD1939_SPI_CONTROL_PORT	CIN	CIN	AD1939 / 30	JP7 / 8	AF27	AD1939_spi_CIN
	CLATCH_n	CLATCH_n	AD1939 / 35	JP7 / 6	AF28	AD1939_spi_CLATCH_n
	CCLK	CCLK	AD1939 / 34	JP7 / 5	AG28	AD1939_spi_CCLK
	COUT	COUT	AD1939 / 31	JP7 / 7	AE25	AD1939_spi_COUT
	ABCLK	ABCLK	AD1939 / 28	JP7 / 3	AA15	AD1939_ADC_ABCLK
AD1939_SERIAL_DATA_PORT	ALRCLK	ALRCLK	AD1939 / 29	JP7 / 9	AG26	AD1939_ADC_ALRCLK
	LINE_IN_DSDATA	ASDATA2	AD1939 / 26	JP7 / 13	AG25	AD1939_ADC_ASDATA2
AD1939_SERIAL_DATA_FORT	DBCLK	DBCLK	AD1939 / 21	JP7 / 15	AH24	AD1939_DAC_DBCLK
	DLRCLK	DLRCLK	AD1939 / 22	JP7 / 16	AF25	AD1939_DAC_DLRCLK
	HEADPHONE_OUT_DSDATA	DSDATA1	AD1939 / 20	JP7 / 18	AF23	AD1939_DAC_DSDATA1
AD1939 CLK RST	MCLK0	MCLK0	AD1939 / 3	JP7 / 1	Y15	AD1939_MCLK
AD1939_CLK_K31	RST_CODEC_n	PD/RST_n	AD1939 / 14	JP7 / 20	AH22	AD1939_RST_CODEC_n
HEADPHONE_I2C	SCL	SCL	TPA6130A2 / 8	JP7 / 2	AC24	TPA6130_i2c_SCL
	SDA	SDA	TPA6130A2 / 7	JP7 / 4	AD26	TPA6130_i2c_SDA
HEADPHONE_PWR_OFF	HEADPHONE_PWR_OFF_n	SD_n	TPA6130A2 /6	JP7 / 10	AH27	TPA6130_power_off
DIGITAL_MIC	DIGITAL_MIC_CLK	CLK	INMP621 / 1	JP1 / 21	C12	INMP621_mic_CLK
	DIGITAL_MIC_DATA	DATA	INMP621 / 5	JP1 / 22	AG21	INMP621_mic_DATA
LEDS	LED1			JP7 / 39	AE19	Audio_Mini_LEDs[0]
	LED2			JP7 / 37	AG15	Audio_Mini_LEDs[1]
	LED3			JP7 / 35	AF18	Audio_Mini_LEDs[2]
	LED4			JP7 / 33	AG18	Audio_Mini_LEDs[3]
SWITCHES	SW1			JP7 / 40	AE17	Audio_Mini_SWITCHES[0]
	SW2			JP7 / 38	AE20	Audio_Mini_SWITCHES[1]
	SW3			JP7 / 36	AF20	Audio_Mini_SWITCHES[2]
	SW4			JP7 / 34	AH18	Audio_Mini_SWITCHES[3]

Title: Audio Mini Rev: 1P1 **FPGA Connectors** Sheet: 6 of 11 Size: 11 x 8.5 Inches AudioLogic . Date: 9/10/2020 Time: 1:46:28 PM Engineer: Connor Dack

File: FPGA\_Connectors.SchDoc

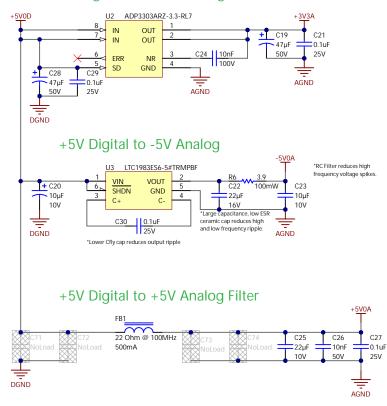
Copyright 2020 Audio Logic Inc

THE HARDWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE HARDWARE OR THE USE OR OTHER DEALINGS IN THE HARDWARE.

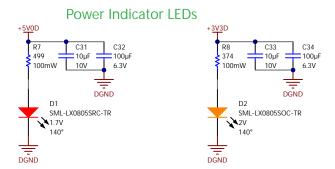
3

## Power Regulation & Indicator LEDs

#### +5V Digital to +3.3V Analog







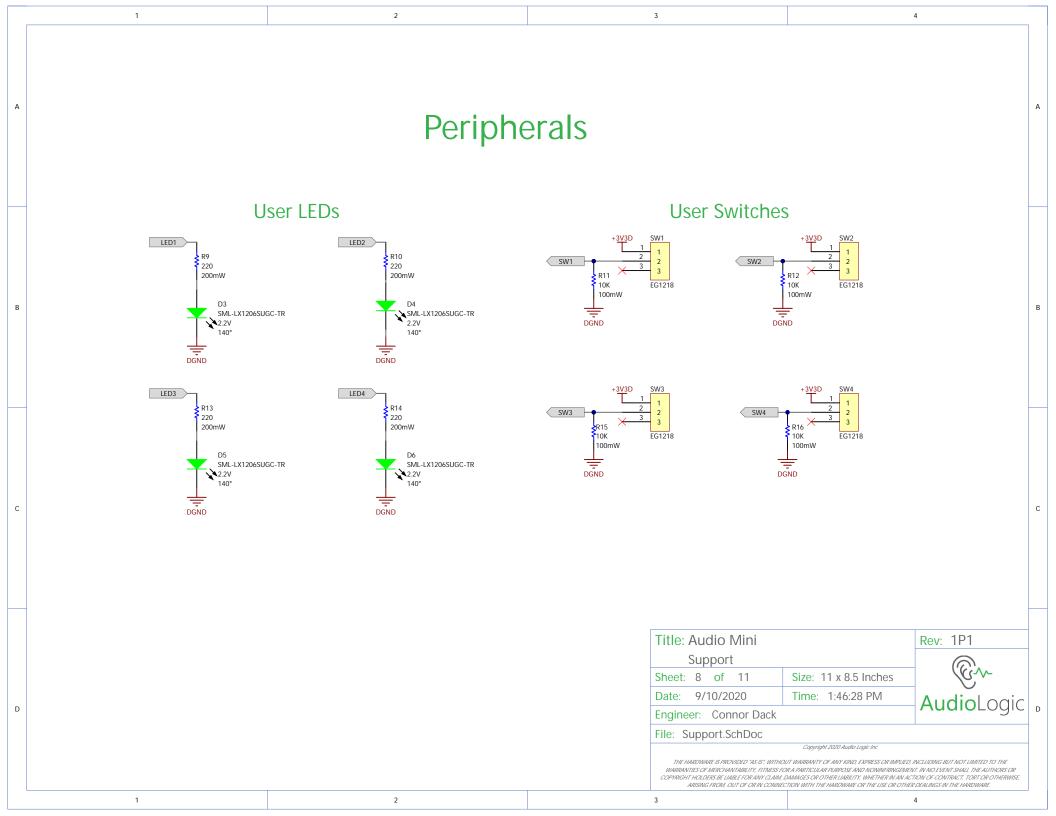
Title: Audio Mini	Rev: 1P1				
Power Regulation					
Sheet: 7 of 11	Size: 11 x 8.5 Inches	(C.V-			
Date: 9/10/2020	Time: 1:46:28 PM	<b>Audio</b> Logic			
Engineer: Connor Dack		AddioLogic	D		

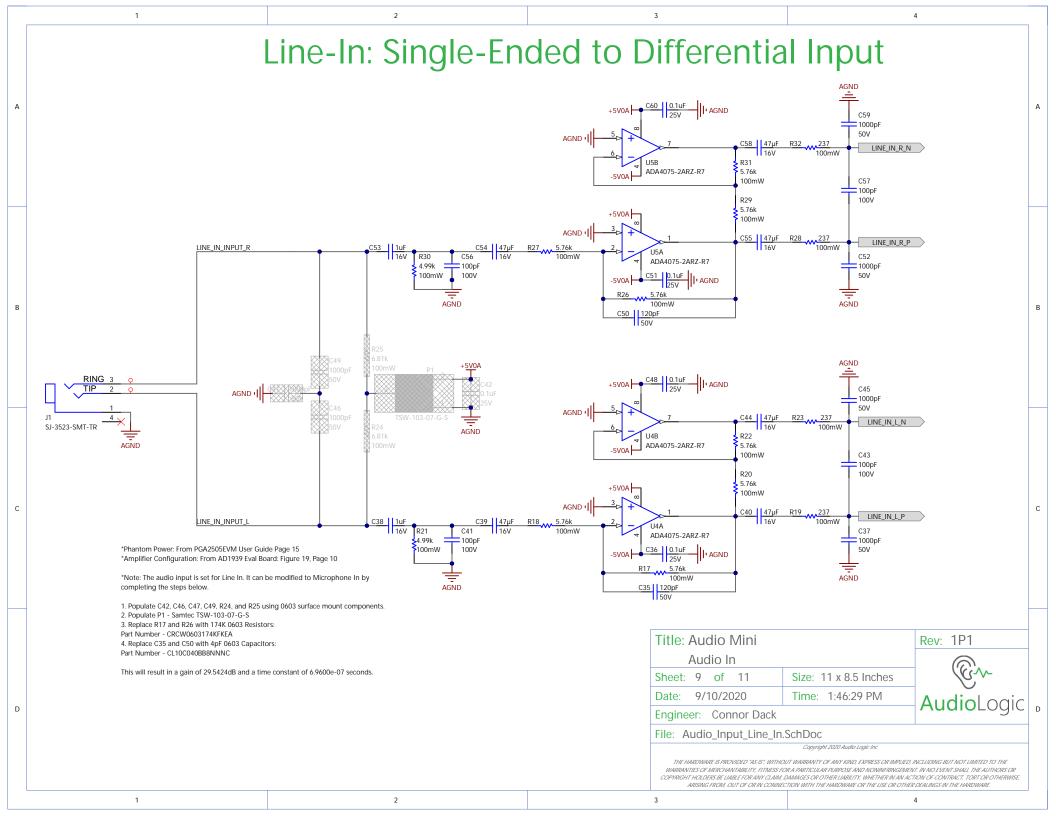
File: Power.SchDoc

Copyright 2020 Audio Logic Inc

THE HARDWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND INCOMVERINGEMENT, IN VIND EVENT SHALL THE AUTHORS OR COPPRIGHT HOLDERS BE LIBBLE FOR ANY CLAIM, DAMAGES OR OTHER HIBLE!!! WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM OUT OF ORINI COMMECTION WITH THE HARDWARE OR THE USE OR OTHER DEALINGS IN THE HARDWARE.

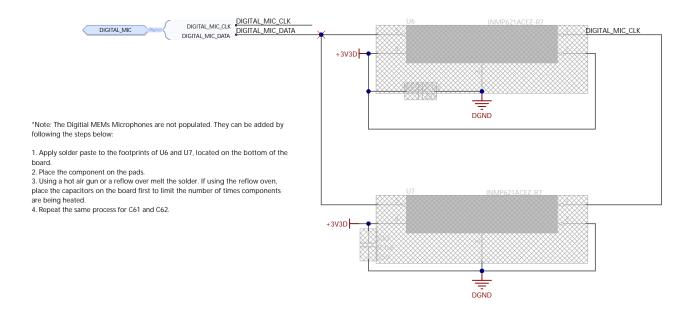
2 3







# Digital Microphones: INMP621



Title: Audio Mini

MEMS Microphones

Sheet: 10 of 11 Size: 11 x 8.5 Inches

Date: 9/10/2020 Time: 1:46:29 PM

Engineer: Coppor Dack

Engineer: Connor Dack

File: Audio\_Input\_Digitial\_Mic.SchDoc

Copyright 2020 Audio Logic Inc

THE HARDWARE IS PROVIDED 'AS IS', WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABUTY, FITNESS FOR A PARTICULAR PURPOSE AND INCOMPRINGEMENT, IN WIG EVENT SHALL THE AUTHORS OR COPPRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER HABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE ARISING FROM, OUT OF OR IN CONNECTION WITH THE HARDWARE OR THE USE OR OTHER DEALWISS IN THE HARDWARE.

1 2 3 4

