



STD2NB60 STD2NB60-1

N-CHANNEL 600V - 3.3 Ω - 2.6A DPAK/IPAK
PowerMESH™ MOSFET

Table 1. General Features

Type	V _{DSS}	R _{DS(on)}	I _D
STD2NB60	600 V	< 3.6 Ω	2.6 A
STD2NB60-1	600 V	< 3.6 Ω	2.6 A

FEATURES SUMMARY

- TYPICAL R_{DS(on)} = 3.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

Figure 1. Package

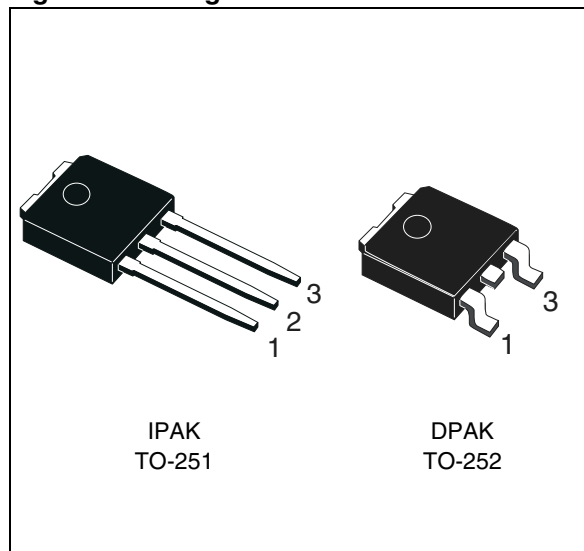


Figure 2. Internal Schematic Diagram

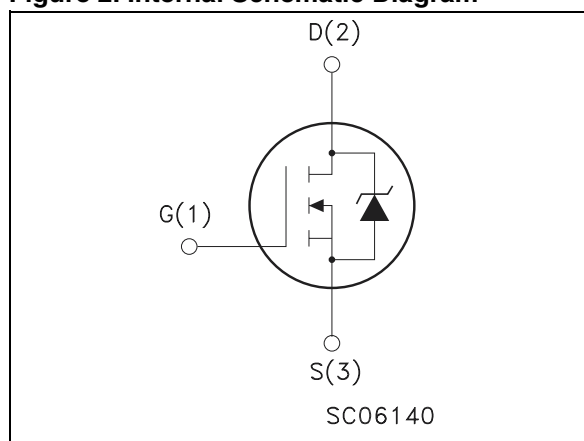


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STD2NB60T4	D2NB60	DPAK	TAPE & REEL
STD2NB60-1	D2NB60	IPAK	TUBE

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain- gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	600	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (cont.) at $T_C = 25\text{ }^\circ\text{C}$	2.6	A
I_D	Drain Current (cont.) at $T_C = 100\text{ }^\circ\text{C}$	1.6	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	10.4	A
P_{tot}	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
	Derating Factor	0.4	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak Diode Recovery voltage slope	4.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature	150	$^\circ\text{C}$

Note: 1. Pulse width limited by safe operating area

2. $I_{SD} \leq 2.6\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$ **Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	275	$^\circ\text{C}$

Table 5. Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	2.6	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$; $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	80	mJ

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)**Table 6. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{\text{GS}} = 0$	600			V
I_{DSS}	Zero Gate Voltage	$V_{\text{DS}} = \text{Max Rating}$			1	μA
	Drain Current ($V_{\text{GS}} = 0$)	$V_{\text{DS}} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			50	μA
I_{GSS}	Gate-body Leakage Current ($V_{\text{DS}} = 0$)	$V_{\text{GS}} = \pm 30\ \text{V}$			± 100	nA

Table 7. On ⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$; $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10\text{V}$; $I_D = 1.6\ \text{A}$		3.3	3.6	Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %**Table 8. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}^{(1)}$	Forward Transconductance	$V_{\text{DS}} > I_{\text{D(on)}} \times R_{\text{DS(on)max}}$; $I_D = 1.6\ \text{A}$	1.2	2		S
C_{iSS}	Input Capacitance	$V_{\text{DS}} = 25\ \text{V}$; $f = 1\ \text{MHz}$; $V_{\text{GS}} = 0$		400	520	pF
C_{oSS}	Output Capacitance			57	77	pF
C_{rSS}	Reverse Transfer Capacitance			7	9	pF

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %**Table 9. Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on Time	$V_{\text{DD}} = 300\ \text{V}$; $I_D = 1.6\ \text{A}$; $R_G = 4.7\ \Omega$		11	17	ns
t_r	Rise Time	$V_{\text{GS}} = 10\ \text{V}$ (see test circuit, Figure 16)		7	11	ns
Q_g	Total Gate Charge	$V_{\text{DD}} = 480\ \text{V}$; $I_D = 3.3\ \text{A}$; $V_{\text{GS}} = 10\ \text{V}$		15	22	nC
Q_{gs}	Gate-Source Charge			6.2		nC
Q_{gd}	Gate-Drain Charge			5.6		nC

Table 10. Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{r(Voff)}}$	Off-voltage Rise Time	$V_{\text{DD}} = 480\ \text{V}$; $I_D = 3.3\ \text{A}$; $R_G = 4.7\ \Omega$		11	16	ns
t_f	Fall Time	$V_{\text{GS}} = 10\ \text{V}$ (see test circuit, Figure 18)		13	18	ns
t_c	Cross-over Time			18	25	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3.3	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				13.2	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 3.3 \text{ A}; V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3.3 \text{ A}; di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}; T_j = 150^\circ\text{C}$ (see test circuit, Figure 18)		500		ns
Q_{rr}	Reverse RecoveryCharge			2.1		μC
I_{RRAM}	Reverse RecoveryCharge			8.5		A

Note: 1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Figure 3. Safe Operating Area

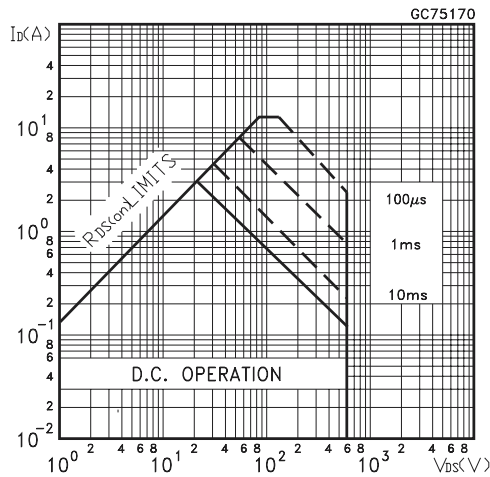


Figure 4. Thermal Impedance

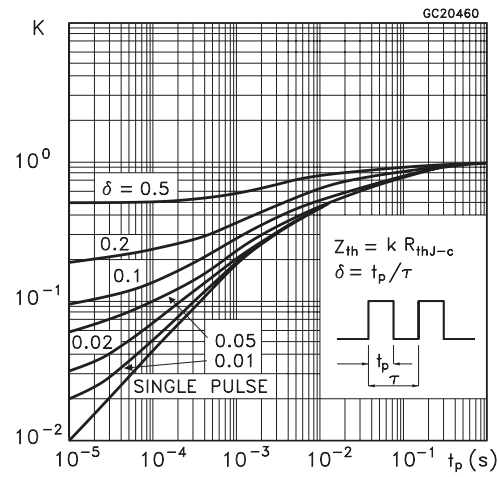


Figure 5. Output Characteristics

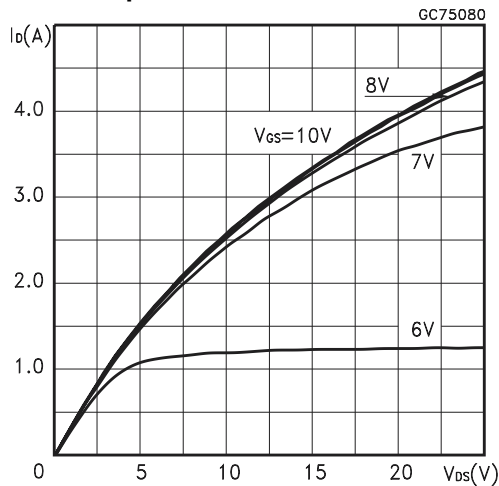


Figure 6. Transfer Characteristics

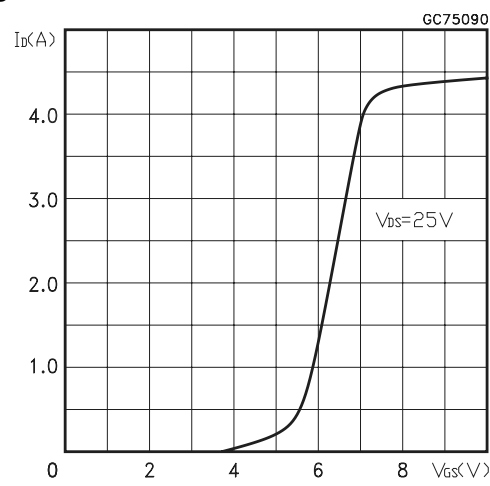


Figure 7. Transconductance

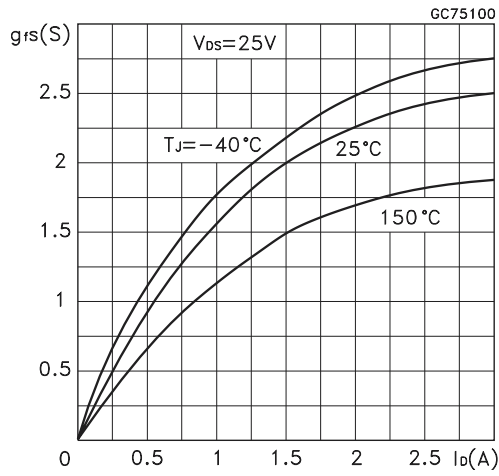


Figure 8. Gate Charge vs Gate-source Voltage

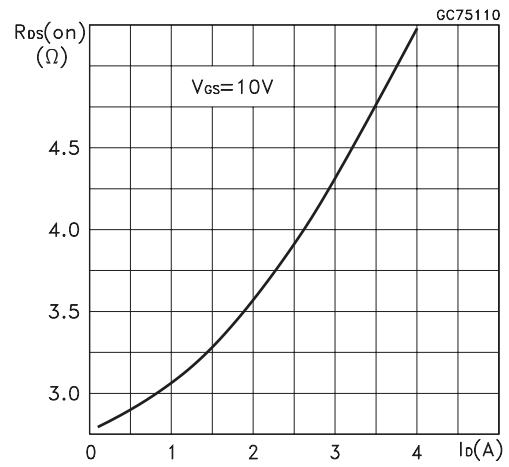


Figure 9. Static Drain-source On Resistance

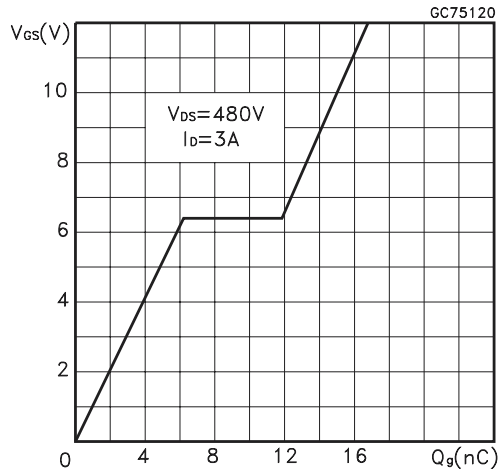


Figure 10. Capacitance Variations

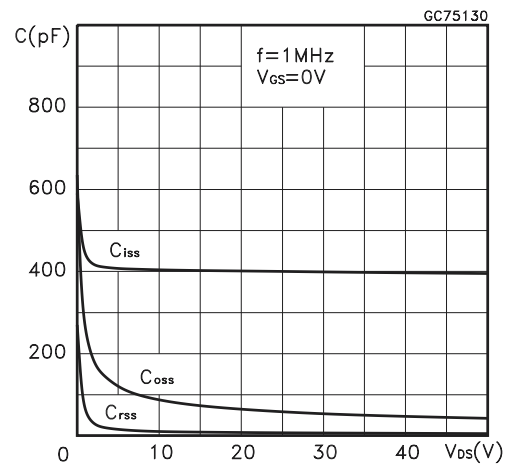


Figure 11. Normalized Gate Threshold Voltage vs Temperature

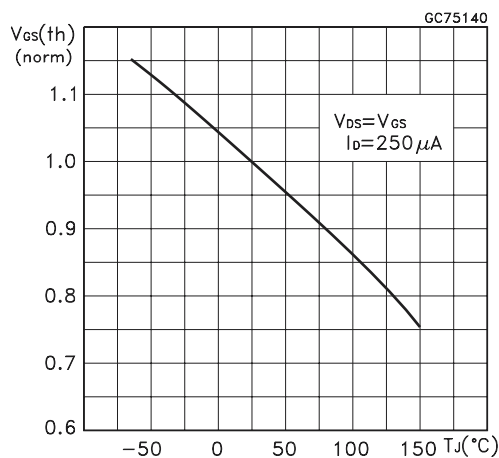


Figure 12. Normalized On Resistance vs Temperature

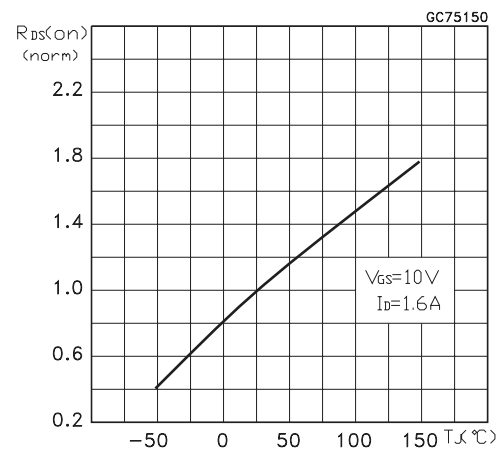


Figure 13. Source-drain Diode Forward Characteristics

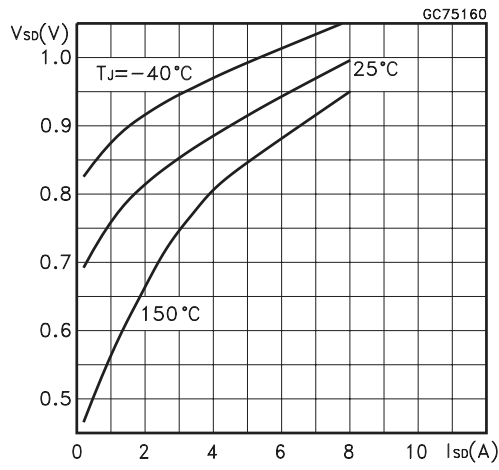


Figure 14. Unclamped Inductive Load Test Circuit

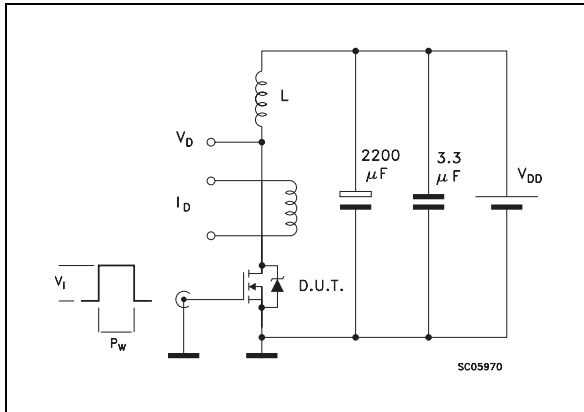


Figure 15. Unclamped Inductive Waveforms

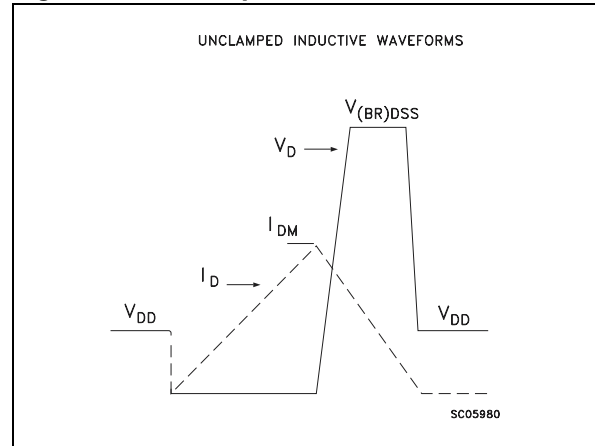


Figure 16. Switching Times Test Circuits For Resistive Load

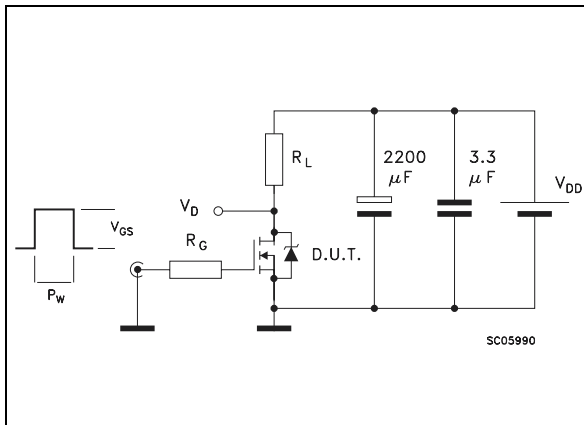


Figure 17. Gate Charge Test Circuit

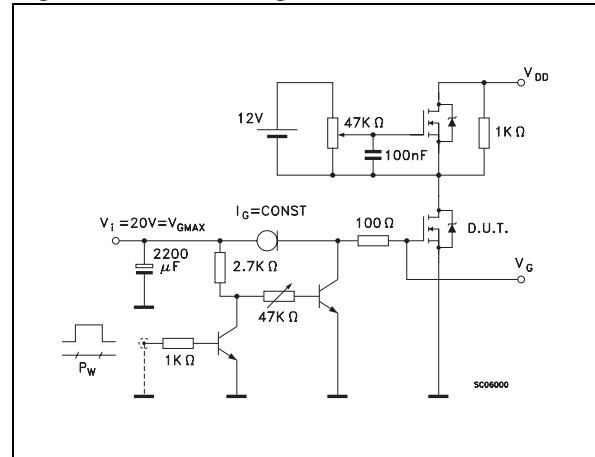
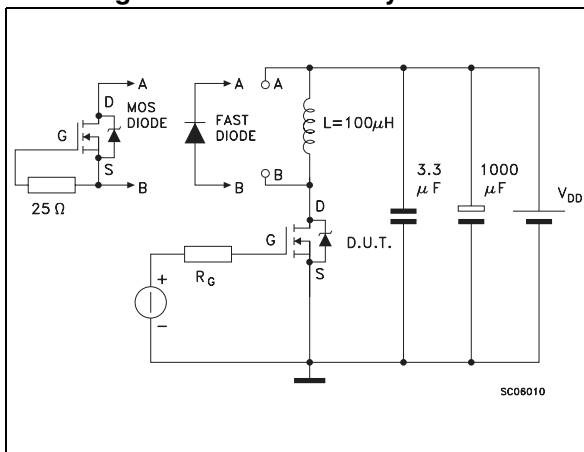
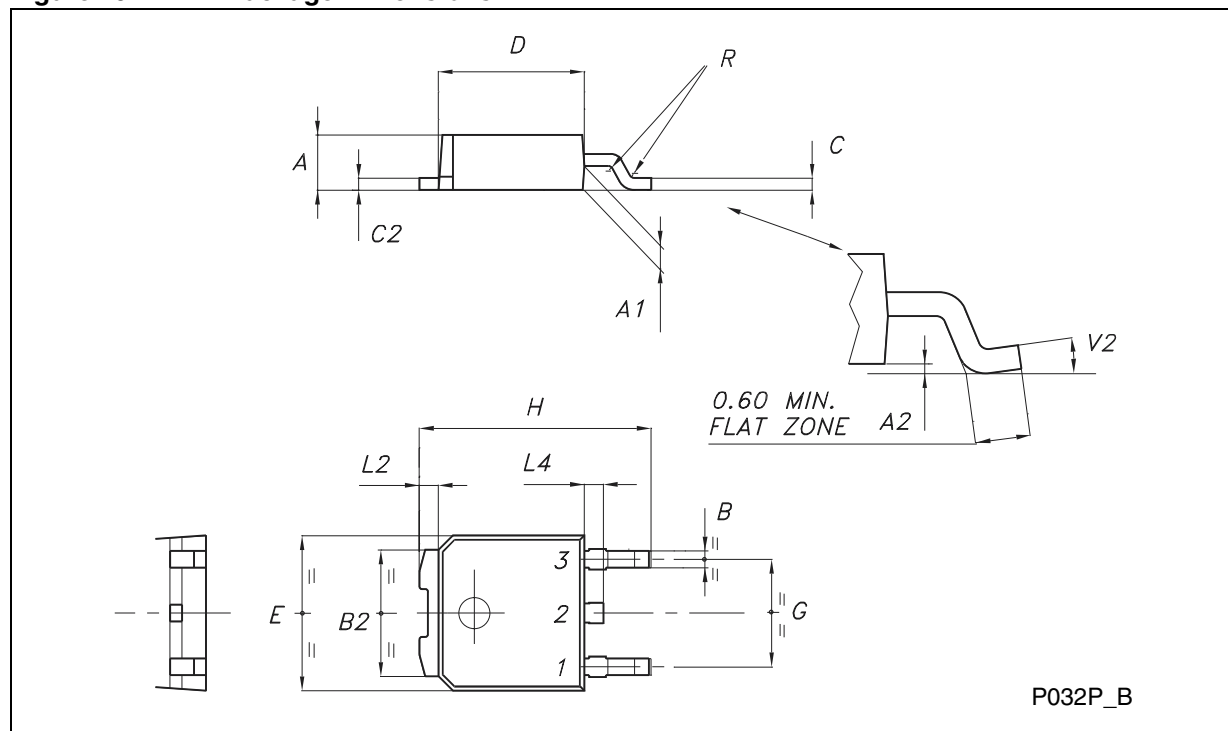


Figure 18. Test Circuit For Inductive Load Switching And Diode Recovery Times



PACKAGE MECHANICAL
Table 12. DPAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018	0.024	
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

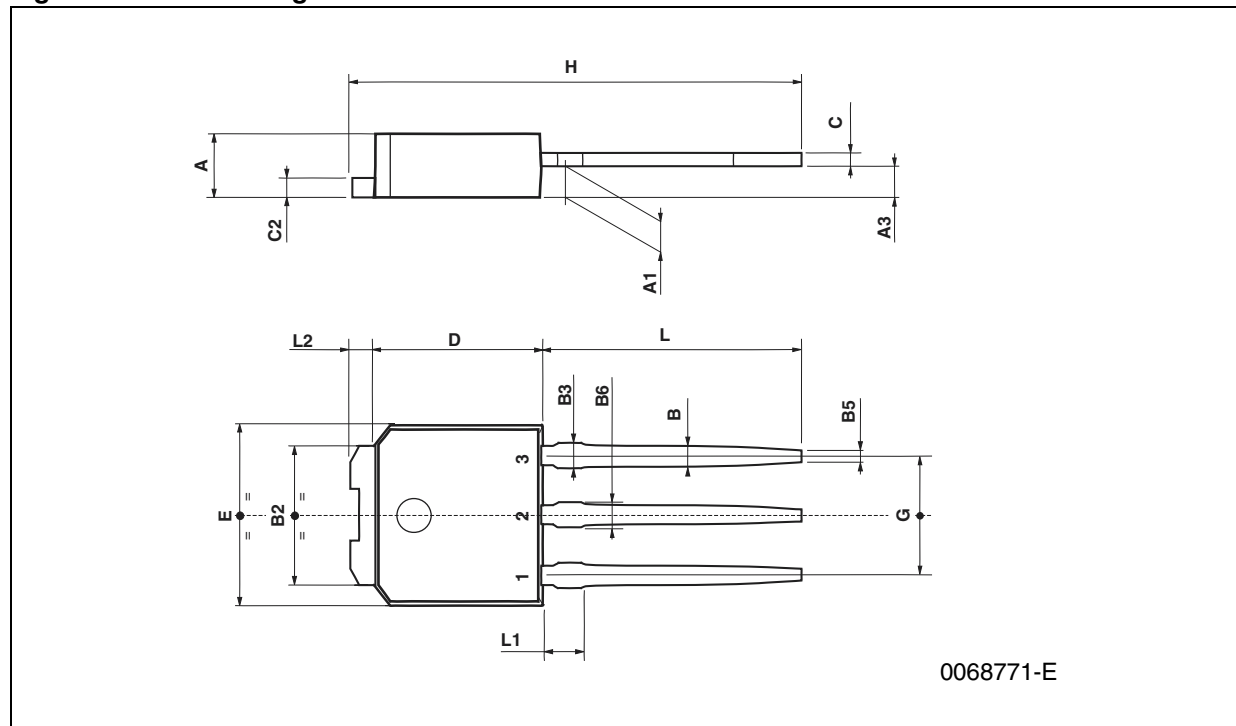
Figure 19. DPAK Package Dimensions


Note: Drawing is not to scale.

Table 13. IPAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.63			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

Figure 20. IPAK Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY**Table 14. Revision History**

Date	Revision	Description of Changes
March-1998	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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