## **Advanced Power MOSFET**

### **FEATURES**

■ Avalanche Rugged Technology

■ Rugged Gate Oxide Technology

■ Lower Input Capacitance

■ Improved Gate Charge

■ Extended Safe Operating Area

■ Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = 100V$ 

■ Lower  $R_{DS(ON)}$  : 0.155  $\Omega(Typ.)$ 

 $BV_{DSS} = 100 V$ 

 $R_{DS(on)} = 0.2\Omega$ 

 $I_D = 8.4 A$ 

**D-PAK** 

2





I-PAK

. ..

## **Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units	
$V_{ exttt{DSS}}$	Drain-to-Source Voltage	100	V	
	Continuous Drain Current (T <sub>C</sub> =25 °C)	8.4	^	
I <sub>D</sub>	Continuous Drain Current (T <sub>C</sub> =100 °C)	5.3	A	
I <sub>DM</sub>	Drain Current-Pulsed ①	34	Α	
$V_{GS}$	Gate-to-Source Voltage	<u>+</u> <b>2</b> 0	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy 2	141	mJ	
I <sub>AR</sub>	Avalanche Current ①	8.4	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy	3.2	mJ	
dv/dt	Peak Diode Recovery dv/dt 3	6.5	V/ns	
	Total Power Dissipation (T <sub>A</sub> =25°C) *	2.5	W	
P <sub>D</sub>	Total Power Dissipation (T <sub>C</sub> =25°C)	32	W	
	Linear Derating Factor	0.26	W/°C	
т т	Operating Junction and	55 to 1450		
$T_J$ , $T_STG$	Storage Temperature Range	- 55 to +150		
	Maximum Lead Temp. for Soldering	200	°C	
T <sub>L</sub>	Purposes, 1/8" from case for 5-seconds	300		

### **Thermal Resistance**

Symbol	Characteristic	Тур.	Max.	Units
$R_{ hetaJC}$	Junction-to-Case		3.9	
$R_{ hetaJA}$	Junction-to-Ambient *		50	°C/W
$R_{ heta JA}$	Junction-to-Ambient		110	

<sup>\*</sup> When mounted on the minimum pad size recommended (PCB Mount).



# **Electrical Characteristics** (T<sub>€</sub>=25 °C unless otherwise specified)

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	100	-		٧	$V_{GS}$ =0 $V$ , $I_{D}$ =250 $\mu$ A	
$\Delta$ BV/ $\Delta$ T $_{ m J}$	Breakdown Voltage Temp. Coeff.		0.12		V/°C	I <sub>D</sub> =250μA <b>See Fig 7</b>	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	$V_{DS}$ =5 $V$ , $I_{D}$ =250 $\mu$ A	
1	Gate-Source Leakage, Forward			100	nA	V <sub>GS</sub> =20V	
I <sub>GSS</sub>	Gate-Source Leakage, Reverse			-100	ПА	V <sub>GS</sub> =-20V	
<sub>1</sub>	Drain to Source Leekage Current			10		V <sub>DS</sub> =100V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current		-	100	μΑ	V <sub>DS</sub> =80V,T <sub>C</sub> =125°C	
	Static Drain-Source				0	V <sub>cs</sub> =10V,I <sub>p</sub> =4.2A <b>4</b>	
R <sub>DS(on)</sub>	On-State Resistance			0.2	Ω	$V_{GS} = 10V, I_{D} = 4.2A$ <b>4</b>	
g <sub>fs</sub>	Forward Transconductance		6.29		Ω	$V_{DS} = 40V, I_{D} = 4.2A$ <b>4</b>	
C <sub>iss</sub>	Input Capacitance		370	480		\/ _0\/\/ _25\/f_1MH>	
C <sub>oss</sub>	Output Capacitance		95	110	рF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	
C <sub>rss</sub>	Reverse Transfer Capacitance		38	45		See Fig 5	
t <sub>d(on)</sub>	Turn-On Delay Time		14	40		V <sub>DD</sub> =50V,I <sub>D</sub> =9.2A,	
t <sub>r</sub>	Rise Time		14	40			
t <sub>d(off)</sub>	Turn-Off Delay Time		36	90	ns	$R_G=18\Omega$	
t <sub>f</sub>	Fall Time		28	70		See Fig 13 ④⑤	
$Q_g$	Total Gate Charge		16	22		$V_{DS} = 80V, V_{GS} = 10V,$	
$Q_gs$	Gate-Source Charge		2.7		nC	I <sub>D</sub> =9.2A	
$Q_{gd}$	Gate-Drain("Miller") Charge		7.8			See Fig 6 & Fig 12 <sup>@</sup> ⑤	

# Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	I	Min.	Тур.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current				8.4	^	Integral reverse pn-diode
I <sub>SM</sub>	Pulsed-Source Current	D			34	Α	in the MOSFET
V <sub>SD</sub>	Diode Forward Voltage	Ð			1.5	V	$T_J = 25$ °C, $I_S = 8.4$ A, $V_{GS} = 0$ V
t <sub>rr</sub>	Reverse Recovery Time			98		ns	T <sub>J</sub> =25°C,I <sub>F</sub> =9.2A
Q <sub>rr</sub>	Reverse Recovery Charge			0.34		μС	di <sub>F</sub> /dt=100A/μs

#### Notes

- 1 Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- 2 L=3mH, I  $_{\rm AS}$ =8.4A, V  $_{\rm DD}$ =25V, R  $_{\rm G}$ =27 $\Omega$  , Starting T  $_{\rm J}$  =25°C
- $\begin{tabular}{l} \begin{tabular}{l} \begin{tab$
- 4 Pulse Test : Pulse Width = 250 µs, Duty Cycle ≤2%
- **(5)** Essentially Independent of Operating Temperature



Fig 1. Output Characteristics

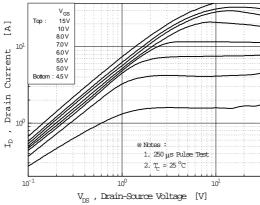


Fig 2. Transfer Characteristics

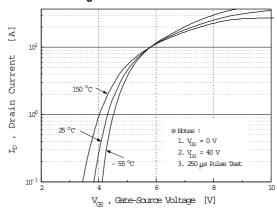


Fig 3. On-Resistance vs. Drain Current

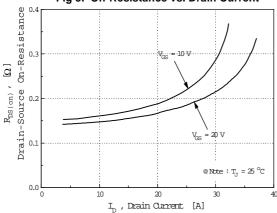


Fig 4. Source-Drain Diode Forward Voltage

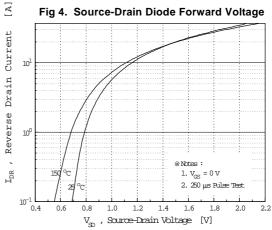


Fig 5. Capacitance vs. Drain-Source Voltage

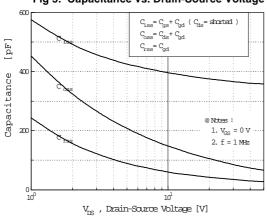
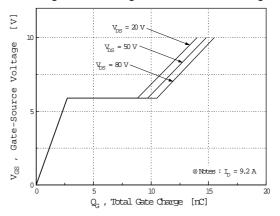
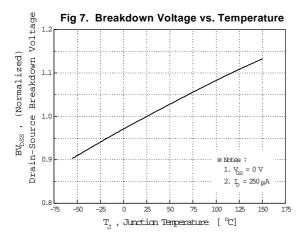


Fig 6. Gate Charge vs. Gate-Source Voltage







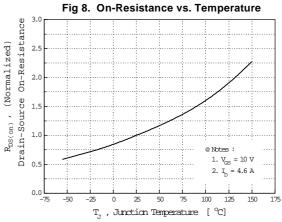
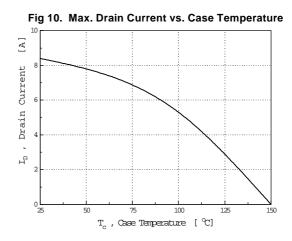


Fig 9. Max. Safe Operating Area

The state of the state o



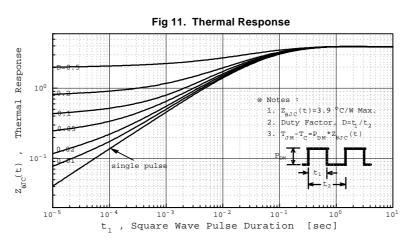




Fig 12. Gate Charge Test Circuit & Waveform

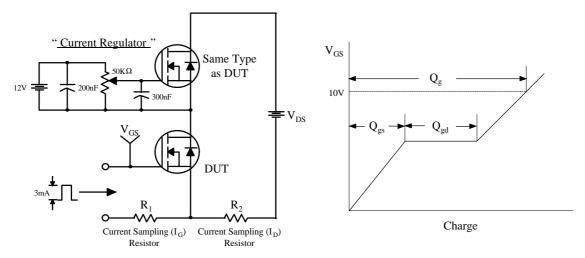


Fig 13. Resistive Switching Test Circuit & Waveforms

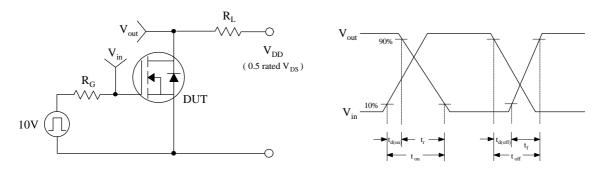


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

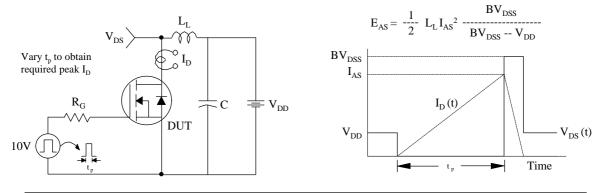
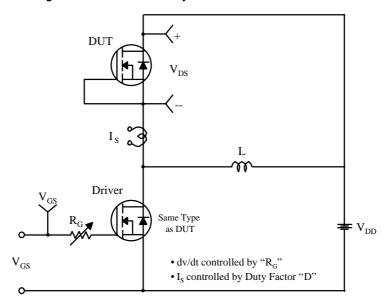
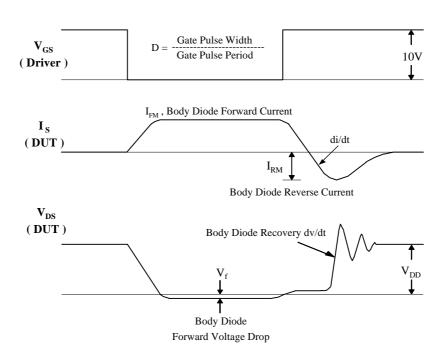




Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms







#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

 $\begin{array}{lll} \mathsf{FACT} \ \mathsf{Quiet} \ \mathsf{Series^{\mathsf{TM}}} & \mathsf{Quiet} \ \mathsf{Series^{\mathsf{TM}}} \\ \mathsf{FAST}^{\otimes} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}3 \\ \mathsf{FASTr^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}6 \\ \mathsf{GTO^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}8 \\ \mathsf{HiSeC^{\mathsf{TM}}} & \mathsf{TinyLogic^{\mathsf{TM}}} \\ \end{array}$ 

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### PRODUCT STATUS DEFINITIONS

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.