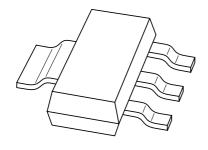
DISCRETE SEMICONDUCTORS

DATA SHEET



BSP89

N-channel enhancement mode vertical D-MOS transistor

Product specification Supersedes data of 1997 Jun 23 2001 May 18





N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- · No secondary breakdown.

DESCRIPTION

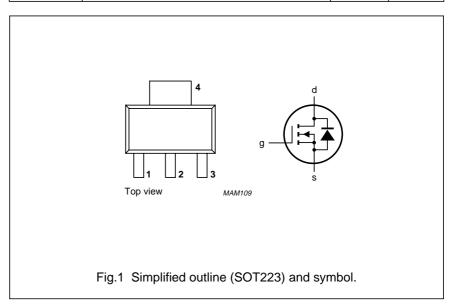
N-channel enhancement mode vertical D-MOS transistor in a SOT223 package, intended for use as a surface-mounted device in line current interrupters in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

| PIN | PIN DESCRIPTION | | | |
|-----|-----------------|--|--|--|
| | Code: BSP89 | | | |
| 1 | gate | | | |
| 2 | drain | | | |
| 3 | source | | | |
| 4 | drain | | | |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|-------------------|----------------------------------|------|------|
| V _{DS} | drain-source voltage (DC) | 240 | V |
| V_{GSth} | gate-source threshold voltage | 2 | V |
| I _D | drain current (DC) | 375 | mA |
| R _{DSon} | drain-source on-state resistance | 5 | Ω |



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|---------------------------|----------------------------------|------|------|------|
| V _{DS} | drain-source voltage (DC) | | _ | 240 | V |
| V_{GSO} | gate-source voltage (DC) | open drain | _ | ±20 | V |
| I _D | drain current (DC) | | _ | 375 | mA |
| I _{DM} | peak drain current | | _ | 1.5 | Α |
| P _{tot} | total power dissipation | T _{amb} ≤ 25 °C; note 1 | _ | 1.5 | W |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| Tj | junction temperature | | _ | 150 | °C |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

Philips Semiconductors Product specification

N-channel enhancement mode vertical D-MOS transistor

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THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------------|---|-------|------|
| R _{th j-a} | thermal resistance from junction to ambient; note 1 | 83.3 | K/W |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

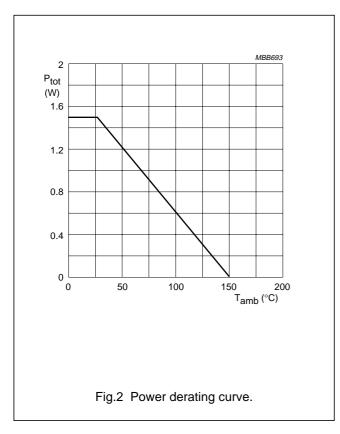
CHARACTERISTICS

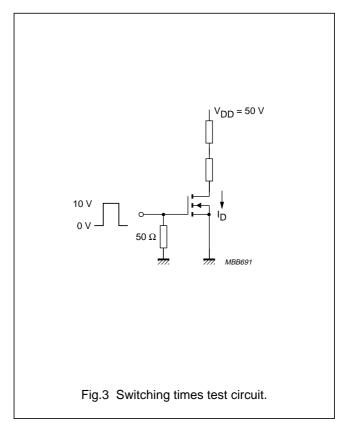
 $T_i = 25$ °C unless otherwise specified.

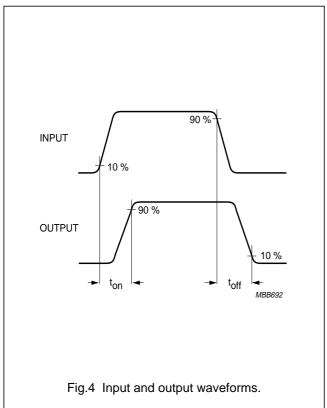
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|----------------------------------|--|------|------|------|------|
| V _{(BR)DSS} | drain-source breakdown voltage | $I_D = 10 \mu A; V_{GS} = 0$ | 240 | _ | _ | V |
| I _{DSS} | drain-source leakage current | V _{DS} = 60 V; V _{GS} = 0 | _ | _ | 200 | nA |
| I _{GSS} | gate-source leakage current | $V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$ | _ | _ | 100 | nA |
| V _{GSth} | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{GS} = V_{DS}$ | 0.8 | _ | 2 | V |
| R _{DSon} | drain-source on-state resistance | $I_D = 340 \text{ mA}; V_{GS} = 10 \text{ V}$ | _ | 2.8 | 5 | Ω |
| | | I _D = 340 mA; V _{GS} = 4.5 V | _ | _ | 7.5 | Ω |
| Y _{fs} | transfer admittance | I _D = 340 mA; V _{DS} = 25 V | 140 | 600 | _ | mS |
| C _{iss} | input capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | _ | 100 | 120 | pF |
| C _{oss} | output capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | _ | 20 | 30 | pF |
| C _{rss} | reverse transfer capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | _ | 10 | 15 | pF |
| Switching times (see Figs 3 and 4) | | | | | | |
| t _{on} | turn-on time | I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V | _ | 6 | 10 | ns |
| t _{off} | turn-off time | I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V | _ | 47 | 60 | ns |

N-channel enhancement mode vertical D-MOS transistor

BSP89







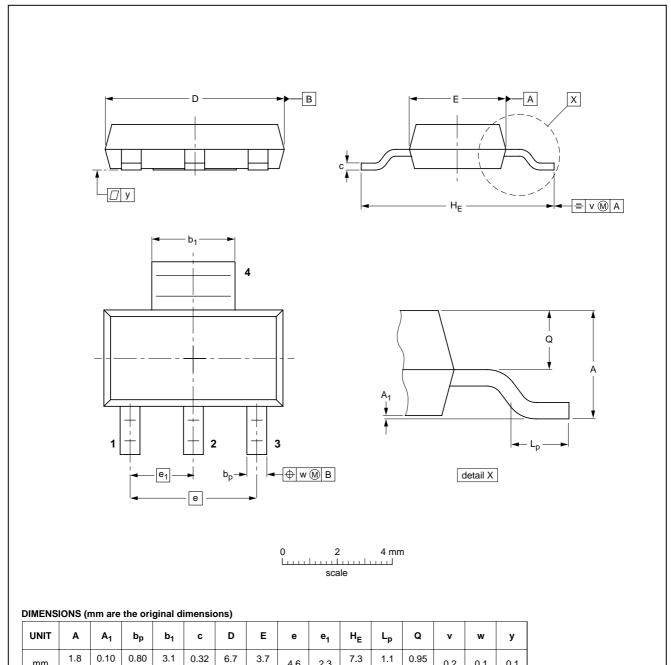
N-channel enhancement mode vertical D-MOS transistor

BSP89

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



| OUTLINE | RE | | REFERENCES | | EUROPEAN | ISSUE DATE |
|---------|-----|-------|------------|--|------------|---------------------------------|
| VERSION | IEC | JEDEC | EIAJ | | PROJECTION | 1350E DATE |
| SOT223 | | | SC-73 | | | 97-02-28 99-09-13 |

2.3

0.1

2001 May 18 5

mm

1.5

0.01

0.60

2.9

0.22

Philips Semiconductors Product specification

N-channel enhancement mode vertical D-MOS transistor

BSP89

DATA SHEET STATUS

| DATA SHEET STATUS(1) | PRODUCT STATUS ⁽²⁾ | DEFINITIONS |
|----------------------|----------------------------------|--|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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N-channel enhancement mode vertical D-MOS transistor

BSP89

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