Preliminary Specification

128XRGBX162 OUTPUT LCD DRIVER IC with built-in RAM

■ INSTRUCTION

HM17CM4096 is a dot-Matrix LCD drive IC with 162 commons and 384 segments (128 X RGB) drive ports for 4,096 colors driving.

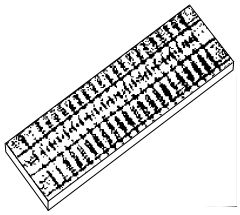
This IC stores the serial or parallel BIT data transferred by the microcomputer on the built-in RAM (248,832 bits for graphic) and generates the signals to drive LCD panel.

Color graphic display is achieved by selecting 16 gray (16R × 16G × 16B = 4,096 color or 256 color mode) levels out of 32 gray palettes independently.

This IC is suitable for battery-operated system, hand-carrying information equipment by ensuring low power consumption, low power supply (1.7V ~) and a wide range of operating voltage.

And 162 x 128 display is possible with just one chip.

- **EXTERNAL SHAPE**

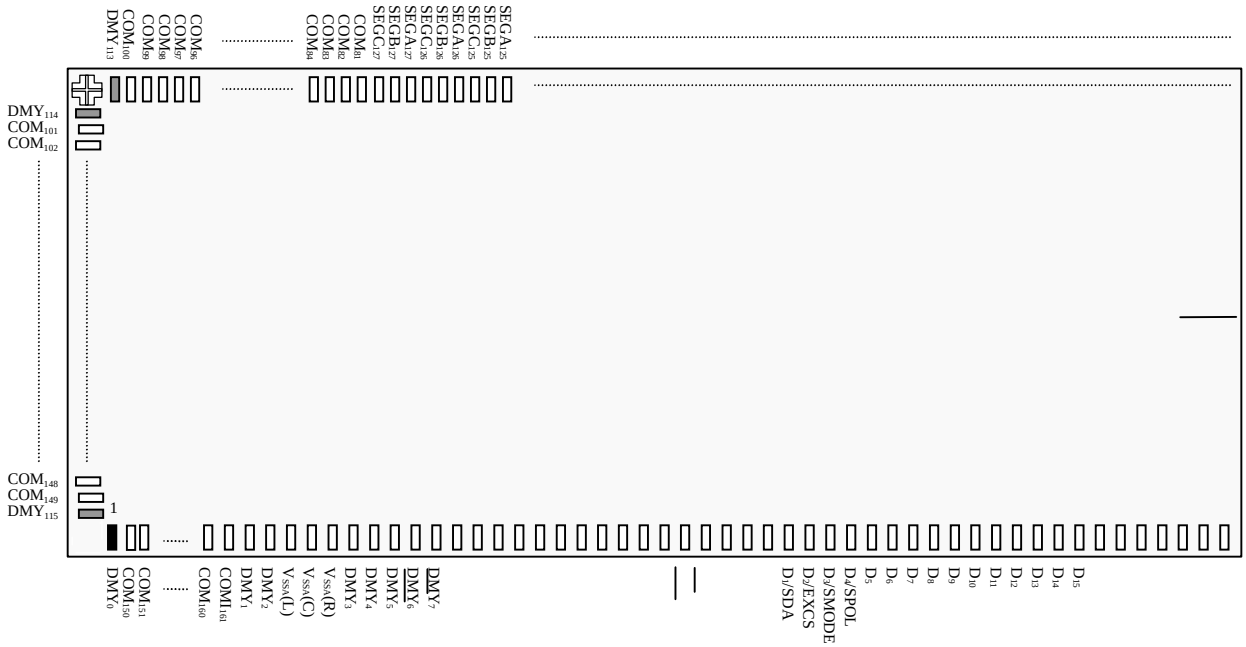


HM17CM4096

■ FEATURES

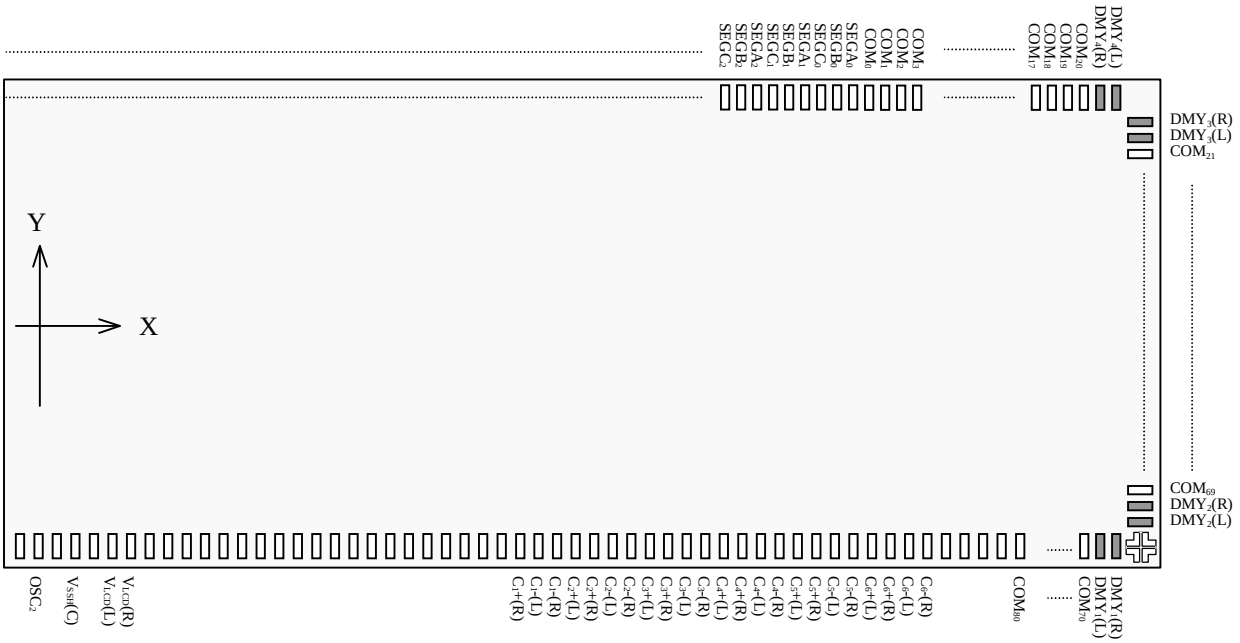
- 4,096 color bitmap LCD driver
- LCD drive outputs 128×RGB segments, 162 commons for graphic
- Display RAM capacity 248,832 bits (for graphic usage)
- Gradation display 16 gradations can be selected from 32 gradations by PWM control
- Black/White display 162 × (128 × 3) bits display is possible
- 8 bit BUS interface directly connectable with 68 / 80 series CPU
- RAM data length 8 BIT / 16 BIT selectable
- Serial interface available 3 or 4 line interface is selectable
- Programmable duty / bias ratio with command
- Various instruction set
  display data read/write, display ON/OFF, positive/negative display, page address set
  display start line address set, partial display, bias select,
  column address set, all display ON/OFF, boosting selection, n line inversion mode
  read modified write, power save …
- Built-in voltage booster (programmable) : 7 × boosting
- Built-in voltage regulator
- Controllable contrast with built-in electric volume (128 steps)
- Low current consumption
- Logic supply 1.7V ~ 3.3V
- LCD drive supply 5.0V ~ 18.0V
- C-MOS silicon process
- Package TCP/ bumped chip / bare chip and so on

PAD LAYOUT

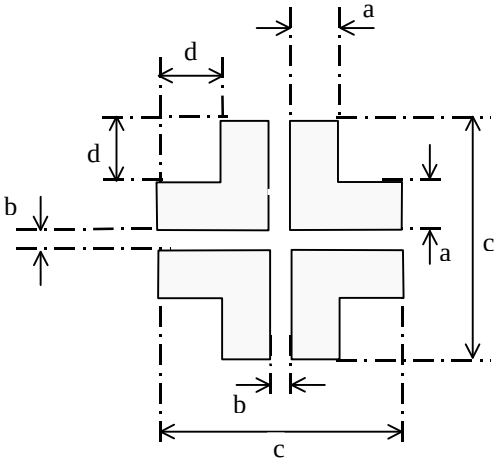


note 1) The (L) (R) (C) mark after port name is internally shorted.
note 2) DMYport is opened electrically.

chip center	**:**	**X= 0μm, Y= 0μm**
chip size	**:**	**with scribe lane : 19.84 × 2.97mm ,**
		main chip : 19.83mm × 2.96mm
chip thickness	**:**	**525μm ± 25μm**
bump size	**:**	**68μm × 33μm, 68μm × 80μm**
bump pitch	**:**	**45μm(Min)**
bump height	**:**	**18 ± 3μm**
bump material	**:**	**Au**



align mark appearance and size



a : 30μm
b : 6μm
c : 120μm
d : 27μm

coordinates of align marks

(X= TBD μm, Y= TBD μm)
(X= TBD μm, Y= TBD μm)

■ PAD coordinates 1

chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
1	DMY0	-9581	-1396	52	VSS(R)	-6510	-1396	103	DMY55	-2250	-1396
2	COM150	-9518	-1396	53	DMY27	-6330	-1396	104	D8	-2130	-1396
3	COM151	-9473	-1396	54	DMY28	-6270	-1396	105	DMY56	-2010	-1396
4	COM152	-9428	-1396	55	TEST2	-6210	-1396	106	D9	-1890	-1396
5	COM153	-9383	-1396	56	DMY29	-6150	-1396	107	DMY57	-1770	-1396
6	COM154	-9338	-1396	57	DMY30	-6090	-1396	108	D10	-1650	-1396
7	COM155	-9293	-1396	58	VDDA(L)	-6030	-1396	109	DMY58	-1530	-1396
8	COM156	-9248	-1396	59	VDDA(C)	-5970	-1396	110	D11	-1410	-1396
9	COM157	-9203	-1396	60	VDDA(R)	-5910	-1396	111	DMY59	-1290	-1396
10	COM158	-9158	-1396	61	DMY31	-5850	-1396	112	D12	-1170	-1396
11	COM159	-9113	-1396	62	DMY32	-5790	-1396	113	DMY60	-1050	-1396
12	COM160	-9068	-1396	63	P/S	-5730	-1396	114	D13	-930	-1396
13	COM161	-9023	-1396	64	DMY33	-5670	-1396	115	DMY61	-810	-1396
14	DMY1	-8910	-1396	65	DMY34	-5610	-1396	116	D14	-690	-1396
15	DMY2	-8850	-1396	66	DMY35	-5550	-1396	117	DMY62	-570	-1396
16	VSSA(L)	-8790	-1396	67	SEL68	-5490	-1396	118	D15	-450	-1396
17	VSSA(C)	-8730	-1396	68	DMY36	-5430	-1396	119	DMY63	-330	-1396
18	VSSA(R)	-8670	-1396	69	DMY37	-5370	-1396	120	VSS(L)	-270	-1396
19	DMY3	-8610	-1396	70	VSSA(L)	-5310	-1396	121	VSS(C)	-210	-1396
20	DMY4	-8550	-1396	71	VSSA(C)	-5250	-1396	122	VSS(R)	-150	-1396
21	DMY5	-8490	-1396	72	VSSA(R)	-5190	-1396	123	DMY64	30	-1396
22	DMY6	-8430	-1396	73	DMY38	-5130	-1396	124	CL	150	-1396
23	DMY7	-8370	-1396	74	DMY39	-5070	-1396	125	DMY65	270	-1396
24	TEST1	-8310	-1396	75	WRB	-5010	-1396	126	DMY66	330	-1396
25	DMY8	-8250	-1396	76	DMY40	-4950	-1396	127	FLM	450	-1396
26	DMY9	-8190	-1396	77	DMY41	-4890	-1396	128	DMY67	570	-1396
27	DMY10	-8130	-1396	78	DMY42	-4830	-1396	129	DMY68	630	-1396
28	DMY11	-8070	-1396	79	RDB	-4770	-1396	130	FR	750	-1396
29	DMY12	-8010	-1396	80	DMY43	-4710	-1396	131	DMY69	870	-1396
30	VDD(L)	-7950	-1396	81	DMY44	-4650	-1396	132	DMY70	930	-1396
31	VDD(C)	-7890	-1396	82	DMY45	-4590	-1396	133	CLK	1050	-1396
32	VDD(R)	-7830	-1396	83	VDD(L)	-4530	-1396	134	DMY71	1170	-1396
33	DMY13	-7650	-1396	84	VDD(C)	-4470	-1396	135	DMY72	1230	-1396
34	DMY14	-7590	-1396	85	VDD(R)	-4410	-1396	136	DMY73	1290	-1396
35	DMY15	-7530	-1396	86	DMY46	-4230	-1396	137	OSC1	1350	-1396
36	DMY16	-7470	-1396	87	DMY47	-4170	-1396	138	DMY74	1410	-1396
37	DMY17	-7410	-1396	88	D0	-4050	-1396	139	DMY75	1470	-1396
38	DMY18	-7350	-1396	89	DMY48	-3930	-1396	140	OSC2	1650	-1396
39	RESB	-7290	-1396	90	D1	-3810	-1396	141	DMY76	1830	-1396
40	DMY19	-7230	-1396	91	DMY49	-3690	-1396	142	DMY77	1890	-1396
41	DMY20	-7170	-1396	92	D2	-3570	-1396	143	VSSH(L)	1950	-1396
42	DMY21	-7110	-1396	93	DMY50	-3450	-1396	144	VSSH(C)	2010	-1396
43	CSB	-7050	-1396	94	D3	-3330	-1396	145	VSSH(R)	2070	-1396
44	DMY22	-6990	-1396	95	DMY51	-3210	-1396	146	DMY78	2250	-1396
45	DMY23	-6930	-1396	96	D4	-3090	-1396	147	DMY79	2310	-1396
46	DMY24	-6870	-1396	97	DMY52	-2970	-1396	148	VLCD(L)	2370	-1396
47	RS	-6810	-1396	98	D5	-2850	-1396	149	VLCD(C)	2430	-1396
48	DMY25	-6750	-1396	99	DMY53	-2730	-1396	150	VLCD(R)	2490	-1396
49	DMY26	-6690	-1396	100	D6	-2610	-1396	151	V1(L)	2670	-1396
50	VSS(L)	-6630	-1396	101	DMY54	-2490	-1396	152	V1(C)	2730	-1396
51	VSS(C)	-6570	-1396	102	D7	-2370	-1396	153	V1(R)	2790	-1396

■ PAD coordinates 2

chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
154	DMY80	2850	-1396	205	DMY95	6390	-1396	256	COM70	9473	-1396
155	V2(L)	2910	-1396	206	C3+(L)	6450	-1396	257	COM69	9518	-1396
156	V2(C)	2970	-1396	207	C3+(C)	6510	-1396	258	DMY109	9581	-1396
157	V2(R)	3030	-1396	208	C3+(R)	6570	-1396	259	DMY110	9831	-1143
158	V3(L)	3210	-1396	209	DMY96	6630	-1396	260	COM68	9831	-1080
159	V3(C)	3270	-1396	210	C3-(L)	6690	-1396	261	COM67	9831	-1035
160	V3(R)	3330	-1396	211	C3-(C)	6750	-1396	262	COM66	9831	-990
161	DMY81	3390	-1396	212	C3-(R)	6810	-1396	263	COM65	9831	-945
162	V4(L)	3450	-1396	213	DMY97	6870	-1396	264	COM64	9831	-900
163	V4(C)	3510	-1396	214	C4+(L)	6930	-1396	265	COM63	9831	-855
164	V4(R)	3570	-1396	215	C4+(C)	6990	-1396	266	COM62	9831	-810
165	VREG(L)	3750	-1396	216	C4+(R)	7050	-1396	267	COM61	9831	-765
166	VREG(C)	3810	-1396	217	DMY98	7110	-1396	268	COM60	9831	-720
167	VREG(R)	3870	-1396	218	C4-(L)	7170	-1396	269	COM59	9831	-675
168	DMY82	3930	-1396	219	C4-(C)	7230	-1396	270	COM58	9831	-630
169	DMY83	3990	-1396	220	C4-(R)	7290	-1396	271	COM57	9831	-585
170	VREF(L)	4050	-1396	221	DMY99	7350	-1396	272	COM56	9831	-540
171	VREF(C)	4110	-1396	222	C5+(L)	7410	-1396	273	COM55	9831	-495
172	VREF(R)	4170	-1396	223	C5+(C)	7470	-1396	274	COM54	9831	-450
173	DMY84	4230	-1396	224	C5+(R)	7530	-1396	275	COM53	9831	-405
174	VBA(L)	4290	-1396	225	DMY100	7590	-1396	276	COM52	9831	-360
175	VBA(C)	4350	-1396	226	C5-(L)	7650	-1396	277	COM51	9831	-315
176	VBA(R)	4410	-1396	227	C5-(C)	7710	-1396	278	COM50	9831	-270
177	DMY85	4470	-1396	228	C5-(R)	7770	-1396	279	COM49	9831	-225
178	DMY86	4530	-1396	229	DMY101	7830	-1396	280	COM48	9831	-180
179	DMY87	4590	-1396	230	C6+(L)	7890	-1396	281	COM47	9831	-135
180	VEE(L)	4650	-1396	231	C6+(C)	7950	-1396	282	COM46	9831	-90
181	VEE(C)	4710	-1396	232	C6+(R)	8010	-1396	283	COM45	9831	-45
182	VEE(R)	4770	-1396	233	DMY102	8070	-1396	284	COM44	9831	0
183	DMY88	4950	-1396	234	C6-(L)	8130	-1396	285	COM43	9831	45
184	DMY89	5010	-1396	235	C6-(C)	8190	-1396	286	COM42	9831	90
185	VSSH(L)	5190	-1396	236	C6-(R)	8250	-1396	287	COM41	9831	135
186	VSSH(C)	5250	-1396	237	DMY103	8310	-1396	288	COM40	9831	180
187	VSSH(R)	5310	-1396	238	DMY104	8370	-1396	289	COM39	9831	225
188	DMY90	5370	-1396	239	DMY105	8430	-1396	290	COM38	9831	270
189	DMY91	5430	-1396	240	DMY106	8490	-1396	291	COM37	9831	315
190	C1+(L)	5490	-1396	241	DMY107	8550	-1396	292	COM36	9831	360
191	C1+(C)	5550	-1396	242	VOUT(L)	8610	-1396	293	COM35	9831	405
192	C1+(R)	5610	-1396	243	VOUT(C)	8670	-1396	294	COM34	9831	450
193	DMY92	5670	-1396	244	VOUT(R)	8730	-1396	295	COM33	9831	495
194	C1-(L)	5730	-1396	245	DMY108	8910	-1396	296	COM32	9831	540
195	C1-(C)	5790	-1396	246	COM80	9023	-1396	297	COM31	9831	585
196	C1-(R)	5850	-1396	247	COM79	9068	-1396	298	COM30	9831	630
197	DMY93	5910	-1396	248	COM78	9113	-1396	299	COM29	9831	675
198	C2+(L)	5970	-1396	249	COM77	9158	-1396	300	COM28	9831	720
199	C2+(C)	6030	-1396	250	COM76	9203	-1396	301	COM27	9831	765
200	C2+(R)	6090	-1396	251	COM75	9248	-1396	302	COM26	9831	810
201	DMY94	6150	-1396	252	COM74	9293	-1396	303	COM25	9831	855
202	C2-(L)	6210	-1396	253	COM73	9338	-1396	304	COM24	9831	900
203	C2-(C)	6270	-1396	254	COM72	9383	-1396	305	COM23	9831	945
204	C2-(R)	6330	-1396	255	COM71	9428	-1396	306	COM22	9831	990

PAD coordinates 3

chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
307	COM21	9831	1035	358	SEGA9	7403	1396	409	SEGA26	5108	1396
308	COM20	9831	1080	359	SEGB9	7358	1396	410	SEGB26	5063	1396
309	DMY111	9831	1144	360	SEGC9	7313	1396	411	SEGC26	5018	1396
310	DMY112	9581	1396	361	SEGA10	7268	1396	412	SEGA27	4973	1396
311	COM19	9518	1396	362	SEGB10	7223	1396	413	SEGB27	4928	1396
312	COM18	9473	1396	363	SEGC10	7178	1396	414	SEGC27	4883	1396
313	COM17	9428	1396	364	SEGA11	7133	1396	415	SEGA28	4838	1396
314	COM16	9383	1396	365	SEGB11	7088	1396	416	SEGB28	4793	1396
315	COM15	9338	1396	366	SEGC11	7043	1396	417	SEGC28	4748	1396
316	COM14	9293	1396	367	SEGA12	6998	1396	418	SEGA29	4703	1396
317	COM13	9248	1396	368	SEGB12	6953	1396	419	SEGB29	4658	1396
318	COM12	9203	1396	369	SEGC12	6908	1396	420	SEGC29	4613	1396
319	COM11	9158	1396	370	SEGA13	6863	1396	421	SEGA30	4568	1396
320	COM10	9113	1396	371	SEGB13	6818	1396	422	SEGB30	4523	1396
321	COM9	9068	1396	372	SEGC13	6773	1396	423	SEGC30	4478	1396
322	COM8	9023	1396	373	SEGA14	6728	1396	424	SEGA31	4433	1396
323	COM7	8978	1396	374	SEGB14	6683	1396	425	SEGB31	4388	1396
324	COM6	8933	1396	375	SEGC14	6638	1396	426	SEGC31	4343	1396
325	COM5	8888	1396	376	SEGA15	6593	1396	427	SEGA32	4298	1396
326	COM4	8843	1396	377	SEGB15	6548	1396	428	SEGB32	4253	1396
327	COM3	8798	1396	378	SEGC15	6503	1396	429	SEGC32	4208	1396
328	COM2	8753	1396	379	SEGA16	6458	1396	430	SEGA33	4163	1396
329	COM1	8708	1396	380	SEGB16	6413	1396	431	SEGB33	4118	1396
330	COM0	8663	1396	381	SEGC16	6368	1396	432	SEGC33	4073	1396
331	SEGA0	8618	1396	382	SEGA17	6323	1396	433	SEGA34	4028	1396
332	SEGB0	8573	1396	383	SEGB17	6278	1396	434	SEGB34	3983	1396
333	SEGC0	8528	1396	384	SEGC17	6233	1396	435	SEGC34	3938	1396
334	SEGA1	8483	1396	385	SEGA18	6188	1396	436	SEGA35	3893	1396
335	SEGB1	8438	1396	386	SEGB18	6143	1396	437	SEGB35	3848	1396
336	SEGC1	8393	1396	387	SEGC18	6098	1396	438	SEGC35	3803	1396
337	SEGA2	8348	1396	388	SEGA19	6053	1396	439	SEGA36	3758	1396
338	SEGB2	8303	1396	389	SEGB19	6008	1396	440	SEGB36	3713	1396
339	SEGC2	8258	1396	390	SEGC19	5963	1396	441	SEGC36	3668	1396
340	SEGA3	8213	1396	391	SEGA20	5918	1396	442	SEGA37	3623	1396
341	SEGB3	8168	1396	392	SEGB20	5873	1396	443	SEGB37	3578	1396
342	SEGC3	8123	1396	393	SEGC20	5828	1396	444	SEGC37	3533	1396
343	SEGA4	8078	1396	394	SEGA21	5783	1396	445	SEGA38	3488	1396
344	SEGB4	8033	1396	395	SEGB21	5738	1396	446	SEGB38	3443	1396
345	SEGC4	7988	1396	396	SEGC21	5693	1396	447	SEGC38	3398	1396
346	SEGA5	7943	1396	397	SEGA22	5648	1396	448	SEGA39	3353	1396
347	SEGB5	7898	1396	398	SEGB22	5603	1396	449	SEGB39	3308	1396
348	SEGC5	7853	1396	399	SEGC22	5558	1396	450	SEGC39	3263	1396
349	SEGA6	7808	1396	400	SEGA23	5513	1396	451	SEGA40	3218	1396
350	SEGB6	7763	1396	401	SEGB23	5468	1396	452	SEGB40	3173	1396
351	SEGC6	7718	1396	402	SEGC23	5423	1396	453	SEGC40	3128	1396
352	SEGA7	7673	1396	403	SEGA24	5378	1396	454	SEGA41	3083	1396
353	SEGB7	7628	1396	404	SEGB24	5333	1396	455	SEGB41	3038	1396
354	SEGC7	7583	1396	405	SEGC24	5288	1396	456	SEGC41	2993	1396
355	SEGA8	7538	1396	406	SEGA25	5243	1396	457	SEGA42	2948	1396
356	SEGB8	7493	1396	407	SEGB25	5198	1396	458	SEGB42	2903	1396
357	SEGC8	7448	1396	408	SEGC25	5153	1396	459	SEGC42	2858	1396

■ PAD coordinates 4

chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
460	SEGA43	2813	1396	511	SEGA60	518	1396	562	SEGA77	-1778	1396
461	SEGB43	2768	1396	512	SEGB60	473	1396	563	SEGB77	-1823	1396
462	SEGC43	2723	1396	513	SEGC60	428	1396	564	SEGC77	-1868	1396
463	SEGA44	2678	1396	514	SEGA61	383	1396	565	SEGA78	-1913	1396
464	SEGB44	2633	1396	515	SEGB61	338	1396	566	SEGB78	-1958	1396
465	SEGC44	2588	1396	516	SEGC61	293	1396	567	SEGC78	-2003	1396
466	SEGA45	2543	1396	517	SEGA62	248	1396	568	SEGA79	-2048	1396
467	SEGB45	2498	1396	518	SEGB62	203	1396	569	SEGB79	-2093	1396
468	SEGC45	2453	1396	519	SEGC62	158	1396	570	SEGC79	-2138	1396
469	SEGA46	2408	1396	520	SEGA63	113	1396	571	SEGA80	-2183	1396
470	SEGB46	2363	1396	521	SEGB63	68	1396	572	SEGB80	-2228	1396
471	SEGC46	2318	1396	522	SEGC63	23	1396	573	SEGC80	-2273	1396
472	SEGA47	2273	1396	523	SEGA64	-23	1396	574	SEGA81	-2318	1396
473	SEGB47	2228	1396	524	SEGB64	-68	1396	575	SEGB81	-2363	1396
474	SEGC47	2183	1396	525	SEGC64	-113	1396	576	SEGC81	-2408	1396
475	SEGA48	2138	1396	526	SEGA65	-158	1396	577	SEGA82	-2453	1396
476	SEGB48	2093	1396	527	SEGB65	-203	1396	578	SEGB82	-2498	1396
477	SEGC48	2048	1396	528	SEGC65	-248	1396	579	SEGC82	-2543	1396
478	SEGA49	2003	1396	529	SEGA66	-293	1396	580	SEGA83	-2588	1396
479	SEGB49	1958	1396	530	SEGB66	-338	1396	581	SEGB83	-2633	1396
480	SEGC49	1913	1396	531	SEGC66	-383	1396	582	SEGC83	-2678	1396
481	SEGA50	1868	1396	532	SEGA67	-428	1396	583	SEGA84	-2723	1396
482	SEGB50	1823	1396	533	SEGB67	-473	1396	584	SEGB84	-2768	1396
483	SEGC50	1778	1396	534	SEGC67	-518	1396	585	SEGC84	-2813	1396
484	SEGA51	1733	1396	535	SEGA68	-563	1396	586	SEGA85	-2858	1396
485	SEGB51	1688	1396	536	SEGB68	-608	1396	587	SEGB85	-2903	1396
486	SEGC51	1643	1396	537	SEGC68	-653	1396	588	SEGC85	-2948	1396
487	SEGA52	1598	1396	538	SEGA69	-698	1396	589	SEGA86	-2993	1396
488	SEGB52	1553	1396	539	SEGB69	-743	1396	590	SEGB86	-3038	1396
489	SEGC52	1508	1396	540	SEGC69	-788	1396	591	SEGC86	-3083	1396
490	SEGA53	1463	1396	541	SEGA70	-833	1396	592	SEGA87	-3128	1396
491	SEGB53	1418	1396	542	SEGB70	-878	1396	593	SEGB87	-3173	1396
492	SEGC53	1373	1396	543	SEGC70	-923	1396	594	SEGC87	-3218	1396
493	SEGA54	1328	1396	544	SEGA71	-968	1396	595	SEGA88	-3263	1396
494	SEGB54	1283	1396	545	SEGB71	-1013	1396	596	SEGB88	-3308	1396
495	SEGC54	1238	1396	546	SEGC71	-1058	1396	597	SEGC88	-3353	1396
496	SEGA55	1193	1396	547	SEGA72	-1103	1396	598	SEGA89	-3398	1396
497	SEGB55	1148	1396	548	SEGB72	-1148	1396	599	SEGB89	-3443	1396
498	SEGC55	1103	1396	549	SEGC72	-1193	1396	600	SEGC89	-3488	1396
499	SEGA56	1058	1396	550	SEGA73	-1238	1396	601	SEGA90	-3533	1396
500	SEGB56	1013	1396	551	SEGB73	-1283	1396	602	SEGB90	-3578	1396
501	SEGC56	968	1396	552	SEGC73	-1328	1396	603	SEGC90	-3623	1396
502	SEGA57	923	1396	553	SEGA74	-1373	1396	604	SEGA91	-3668	1396
503	SEGB57	878	1396	554	SEGB74	-1418	1396	605	SEGB91	-3713	1396
504	SEGC57	833	1396	555	SEGC74	-1463	1396	606	SEGC91	-3758	1396
505	SEGA58	788	1396	556	SEGA75	-1508	1396	607	SEGA92	-3803	1396
506	SEGB58	743	1396	557	SEGB75	-1553	1396	608	SEGB92	-3848	1396
507	SEGC58	698	1396	558	SEGC75	-1598	1396	609	SEGC92	-3893	1396
508	SEGA59	653	1396	559	SEGA76	-1643	1396	610	SEGA93	-3938	1396
509	SEGB59	608	1396	560	SEGB76	-1688	1396	611	SEGB93	-3983	1396
510	SEGC59	563	1396	561	SEGC76	-1733	1396	612	SEGC93	-4028	1396

PAD coordinates 5

chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

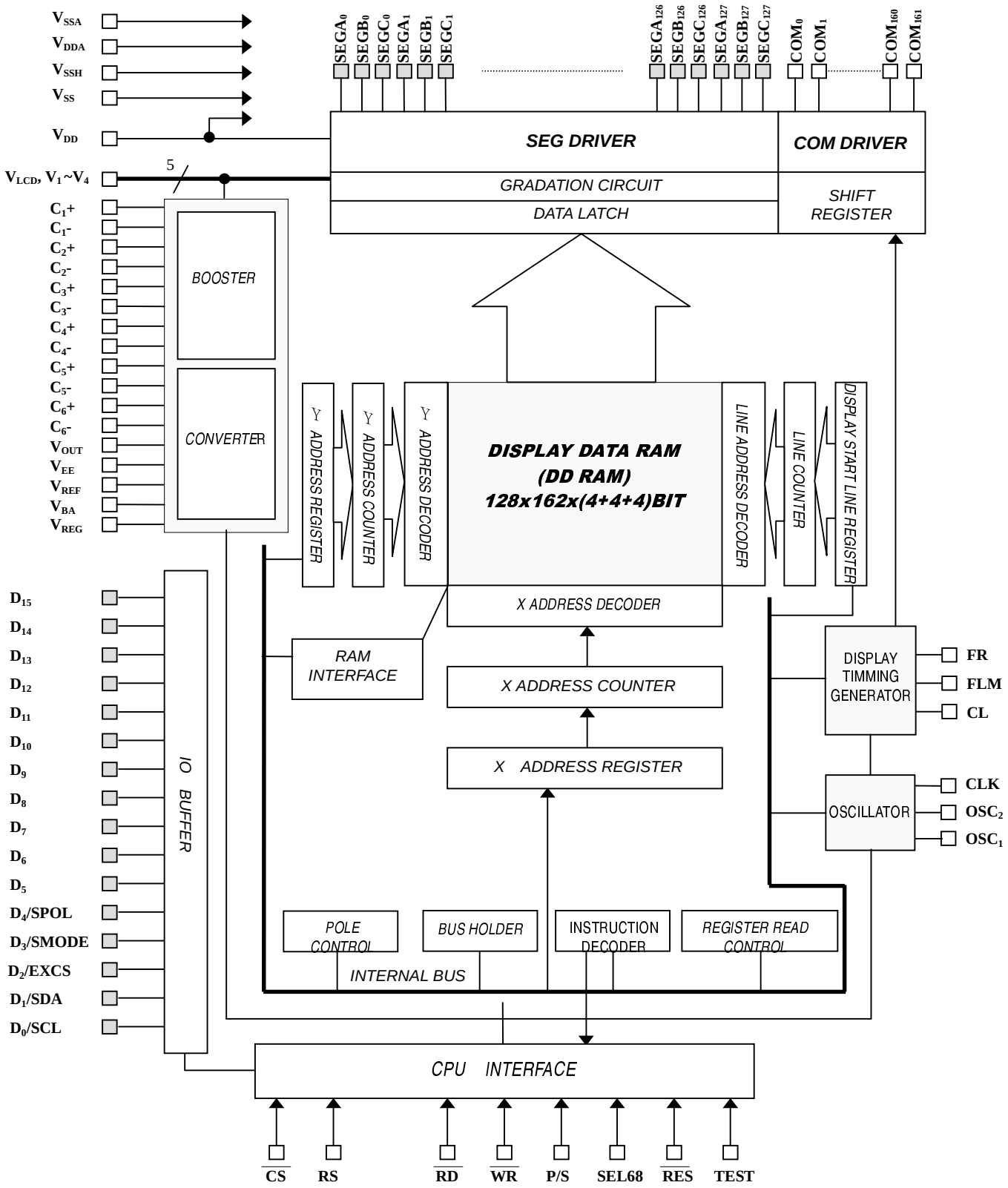
PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
613	SEGA94	-4073	1396	664	SEGA111	-6368	1396	715	COM81	-8663	1396
614	SEGB94	-4118	1396	665	SEGB111	-6413	1396	716	COM82	-8708	1396
615	SEGC94	-4163	1396	666	SEGC111	-6458	1396	717	COM83	-8753	1396
616	SEGA95	-4208	1396	667	SEGA112	-6503	1396	718	COM84	-8798	1396
617	SEGB95	-4253	1396	668	SEGB112	-6548	1396	719	COM85	-8843	1396
618	SEGC95	-4298	1396	669	SEGC112	-6593	1396	720	COM86	-8888	1396
619	SEGA96	-4343	1396	670	SEGA113	-6638	1396	721	COM87	-8933	1396
620	SEGB96	-4388	1396	671	SEGB113	-6683	1396	722	COM88	-8978	1396
621	SEGC96	-4433	1396	672	SEGC113	-6728	1396	723	COM89	-9023	1396
622	SEGA97	-4478	1396	673	SEGA114	-6773	1396	724	COM90	-9068	1396
623	SEGB97	-4523	1396	674	SEGB114	-6818	1396	725	COM91	-9113	1396
624	SEGC97	-4568	1396	675	SEGC114	-6863	1396	726	COM92	-9158	1396
625	SEGA98	-4613	1396	676	SEGA115	-6908	1396	727	COM93	-9203	1396
626	SEGB98	-4658	1396	677	SEGB115	-6953	1396	728	COM94	-9248	1396
627	SEGC98	-4703	1396	678	SEGC115	-6998	1396	729	COM95	-9293	1396
628	SEGA99	-4748	1396	679	SEGA116	-7043	1396	730	COM96	-9338	1396
629	SEGB99	-4793	1396	680	SEGB116	-7088	1396	731	COM97	-9383	1396
630	SEGC99	-4838	1396	681	SEGC116	-7133	1396	732	COM98	-9428	1396
631	SEGA100	-4883	1396	682	SEGA117	-7178	1396	733	COM99	-9473	1396
632	SEGB100	-4928	1396	683	SEGB117	-7223	1396	734	COM100	-9518	1396
633	SEGC100	-4973	1396	684	SEGC117	-7268	1396	735	DMY113	-9581	1396
634	SEGA101	-5018	1396	685	SEGA118	-7313	1396	736	DMY114	-9831	1143
635	SEGB101	-5063	1396	686	SEGB118	-7358	1396	737	COM101	-9831	1080
636	SEGC101	-5108	1396	687	SEGC118	-7403	1396	738	COM102	-9831	1035
637	SEGA102	-5153	1396	688	SEGA119	-7448	1396	739	COM103	-9831	990
638	SEGB102	-5198	1396	689	SEGB119	-7493	1396	740	COM104	-9831	945
639	SEGC102	-5243	1396	690	SEGC119	-7538	1396	741	COM105	-9831	900
640	SEGA103	-5288	1396	691	SEGA120	-7583	1396	742	COM106	-9831	855
641	SEGB103	-5333	1396	692	SEGB120	-7628	1396	743	COM107	-9831	810
642	SEGC103	-5378	1396	693	SEGC120	-7673	1396	744	COM108	-9831	765
643	SEGA104	-5423	1396	694	SEGA121	-7718	1396	745	COM109	-9831	720
644	SEGB104	-5468	1396	695	SEGB121	-7763	1396	746	COM110	-9831	675
645	SEGC104	-5513	1396	696	SEGC121	-7808	1396	747	COM111	-9831	630
646	SEGA105	-5558	1396	697	SEGA122	-7853	1396	748	COM112	-9831	585
647	SEGB105	-5603	1396	698	SEGB122	-7898	1396	749	COM113	-9831	540
648	SEGC105	-5648	1396	699	SEGC122	-7943	1396	750	COM114	-9831	495
649	SEGA106	-5693	1396	700	SEGA123	-7988	1396	751	COM115	-9831	450
650	SEGB106	-5738	1396	701	SEGB123	-8033	1396	752	COM116	-9831	405
651	SEGC106	-5783	1396	702	SEGC123	-8078	1396	753	COM117	-9831	360
652	SEGA107	-5828	1396	703	SEGA124	-8123	1396	754	COM118	-9831	315
653	SEGB107	-5873	1396	704	SEGB124	-8168	1396	755	COM119	-9831	270
654	SEGC107	-5918	1396	705	SEGC124	-8213	1396	756	COM120	-9831	225
655	SEGA108	-5963	1396	706	SEGA125	-8258	1396	757	COM121	-9831	180
656	SEGB108	-6008	1396	707	SEGB125	-8303	1396	758	COM122	-9831	135
657	SEGC108	-6053	1396	708	SEGC125	-8348	1396	759	COM123	-9831	90
658	SEGA109	-6098	1396	709	SEGA126	-8393	1396	760	COM124	-9831	45
659	SEGB109	-6143	1396	710	SEGB126	-8438	1396	761	COM125	-9831	0
660	SEGC109	-6188	1396	711	SEGC126	-8483	1396	762	COM126	-9831	-45
661	SEGA110	-6233	1396	712	SEGA127	-8528	1396	763	COM127	-9831	-90
662	SEGB110	-6278	1396	713	SEGB127	-8573	1396	764	COM128	-9831	-135
663	SEGC110	-6323	1396	714	SEGC127	-8618	1396	765	COM129	-9831	-180

PAD coordinates 6

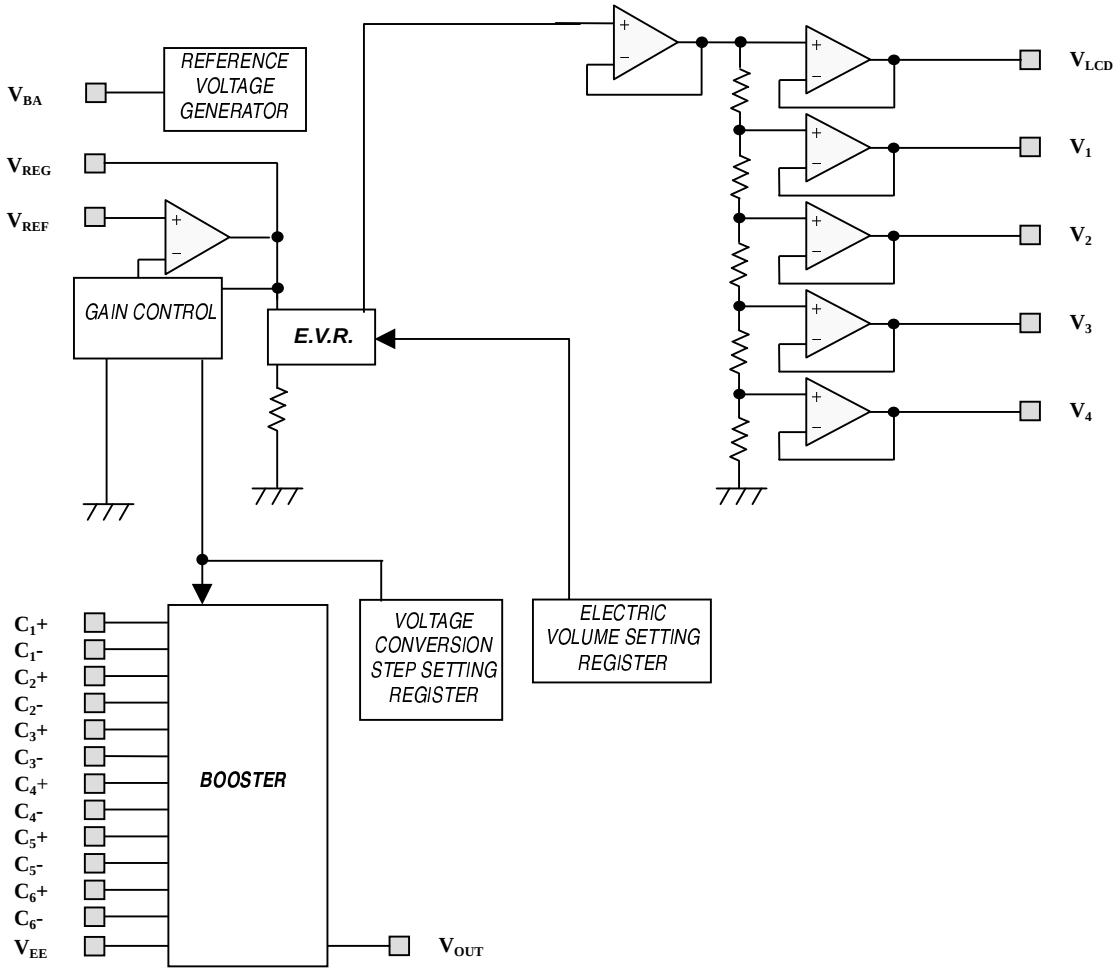
chip size 19840μm × 2390μm (chip center : 0μm × 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
766	COM130	-9831	-225								
767	COM131	-9831	-270								
768	COM132	-9831	-315								
769	COM133	-9831	-360								
770	COM134	-9831	-405								
771	COM135	-9831	-450								
772	COM136	-9831	-495								
773	COM137	-9831	-540								
774	COM138	-9831	-585								
775	COM139	-9831	-630								
776	COM140	-9831	-675								
777	COM141	-9831	-720								
778	COM142	-9831	-765								
779	COM143	-9831	-810								
780	COM144	-9831	-855								
781	COM145	-9831	-900								
782	COM146	-9831	-945								
783	COM147	-9831	-990								
784	COM148	-9831	-1035								
785	COM149	-9831	-1080								
786	DMY115	-9831	-1144								

BLOCK DIAGRAM



■ POWER CIRCUIT BLOCK DIAGRAM



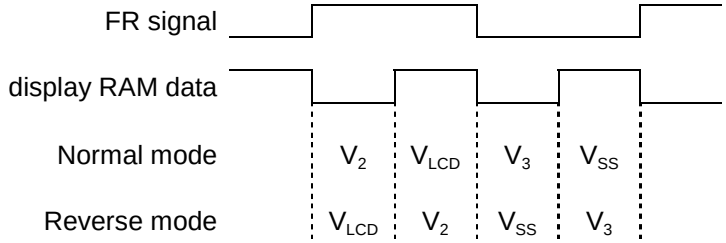
■ PIN DESCRIPTION 1

NAME	I/O	FUNCTION
V_{DD}	supply	Power pin for logic
V_{SS}	supply	GND pin for logic
V_{SSH}	supply	High voltage GND pin
V_{DDA}	supply	This pin is internally connected to V_{DD} pin. This pin is used when the voltage of each input pin is fixed to V_{DD} level. *caution) Do not use to main power pin.*
V_{SSA}	supply	This pin is internally connected to V_{SS} pin. This pin is used when the voltage of each input pin is fixed to V_{SS} level. *caution) Do not use to main power pin.*
V_{LCD} V_1 V_2 V_3 V_4	supply/O	LCD driver supply voltage • LCD driver power supply port when external power supply is used. When external power is used, voltages should have following relations. $V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}$ • V_{LCD}, V_1~V_4 voltages are generated by voltage booster under power circuit ON status. • When internal power supply is used, capacitors must be connected between V_{LCD}, V_1~V_4 and V_{SS}.
C_1+ C_1-	O	Capacitor connection pin for voltage converter
C_2+ C_2-	O	Capacitor connection pin for voltage converter
C_3+ C_3-	O	Capacitor connection pin for voltage converter
C_4+ C_4-	O	Capacitor connection pin for voltage converter
C_5+ C_5-	O	Capacitor connection pin for voltage converter
C_6+ C_6-	O	Capacitor connection pin for voltage converter
V_{BA}	O	Reference voltage output pin for voltage regulating.
V_{REF}	I	Reference voltage input pin for voltage regulating.
V_{EE}	supply	Voltage supply pin for boosted voltage generation. V_{DD} level at normal status.
V_{OUT}	supply/O	Internal DC/DC converter output pin.
V_{REG}	O	Voltage regulator output pin.
$\overline{RES}$	I	Reset pin Reset when RES= “L”
D_0/SCL	I/O	• When parallel interface is selected (P/S=”H”), data line is connected to MPU data bus with 8bit bi-directional bus • When serial interface is selected (P/S=”L”), D_0 and D_1(SCL, SDA) are used as serial interface pins and various sets are taken by serial interface use mode of D_2, D_3, D_4. SDA : serial data input pin SCL : data transfer clock EXCS : extension chip selection I/O pin SMODE : serial transfer mode setting input pin SPOL : RS polarity selection pin when 3 line serial interface is selected. SDA data is shifted at the rising edge of SCL Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL. Set to “L” after data transfer or during non-access time
D_1/SDA	I/O	
D_2/EXCS	I/O	
D_3/SMODE	I/O	
D_4/SPOL	I/O	
D_5,D_6,D_7	I/O	

■ PIN DESCRIPTION 2

<table>
<tr><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>D_8,D_9,D_{10},D_{11},
D_{12},D_{13},D_{14},D_{15}</td><td>I/O</td><td>Connect to data bus to MPU with 8bit bi-directional bus.
Used as MSB 8bit data bus in the 16bit data RAM transfer mode
Set to “L” or “H” when not used.</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip selection pin.
Data in-out is possible when CS = “L”.</td></tr>
<tr><td>RS</td><td>I</td><td>Input data selection pin.
Distinguish bus data from CPU whether instruction or display data.
<table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>class</td><td>instruction</td><td>display data</td></tr></table></td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td><80 series CPU interface (P/S=”H”,SEL68=”L”)>
RD signal connection port of 80 series CPU.
Data bus goes to output state at RD = “L”.
<68 series CPU interface (P/S=”H”,SEL68=”H”)>
Enable signal connection port of 68 series CPU.
Active status when this signal is at “H”.</td></tr>
<tr><td>$\overline{WR}$ (R/W)</td><td>I</td><td><80 series CPU interface (P/S=”H”,SEL68=”L”)>
WR signal connection port of 80 series CPU.
Active at “L” and data bus signal is taken at the rising edge of WR.
<68 series CPU interface (P/S=”H”,SEL68=”H”)>
Read write control signal , R/W connection port of 68-series MPU.
<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>status</td><td>read</td><td>write</td></tr></table></td></tr>
<tr><td>SEL68</td><td>I</td><td>CPU interface selection port
<table><tr><td>SEL68</td><td>H</td><td>L</td></tr><tr><td>status</td><td>68 series</td><td>80 series</td></tr></table></td></tr>
<tr><td>P/S</td><td>I</td><td>Serial / parallel interface selection port
<table><tr><td>P/S</td><td>chip select</td><td>data/ command</td><td>data</td><td>read/ write</td><td>serial clock</td></tr><tr><td>H</td><td>CS</td><td>RS</td><td>D_0~D_7</td><td>RD, WR</td><td>-</td></tr><tr><td>L</td><td>CS</td><td>RS</td><td>SDA(D_1)</td><td>write only</td><td>SCL (D_0)</td></tr></table>※ P/S = “L” :serial interface selection ,D15~D5 goes to Hi-Z state. Fix RD, WR to “H” or “L”.</td></tr>
<tr><td>TEST</td><td>I</td><td>Test port.
Fix to ”L”.</td></tr>
<tr><td>CL</td><td>I/O</td><td>Latching signal pin of display data.
Display line counter is counted up at the rising edge and LCD driving signal is generated at the falling edge</td></tr>
<tr><td>FLM</td><td>I/O</td><td>LCD synchronous signal (first line marker) I/O pin.
Display start address is loaded in the display line counter at FLM = “H”.</td></tr>
<tr><td>FR</td><td>I/O</td><td>Alternated display signal of LCD driver output I/O pin.</td></tr>
</table>

PIN DESCRIPTION 4

<table>
<tr><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>$SEGA_0$~$SEGA_{127}$,
$SEGB_0$~$SEGB_{127}$,
$SEGC_0$~$SEGC_{127}$</td><td>O</td><td>Segment drive port
Segment output from display RAM data
<table>
<tr><td>mode</td><td>Non-lighted</td><td>lighted</td></tr>
<tr><td>Normal</td><td>0</td><td>1</td></tr>
<tr><td>Reverse</td><td>1</td><td>0</td></tr>
</table>
The output level is selected among V_{LCD}, V_2, V_3, V_{SS} by the combination of FR signal and RAM data
(B/W mode)
 
</td></tr>
<tr><td>COM_0~COM_{162}</td><td>O</td><td>Common driver output
The output level is selected among V_{LCD}, V_1, V_4 and V_{SS} by the combination of FR and scan data.
<table>
<tr><td>data</td><td>FR</td><td>Output level</td></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>V_{LCD}</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
</table></td></tr>
<tr><td>OSC_1,
OSC_2</td><td>I
O</td><td>External reference clock input pin
Open or fix “L” when using internal oscillator clock .
In this case, OSC_1 goes to V_{SS} level.
Connect external oscillating source to OSC_1 port or connect resistor between OSC_1 and OSC_2 when using external oscillator.</td></tr>
<tr><td>CLK</td><td>I/O</td><td>Input / output pin for display timing clock
External clock is applied to chip through CLK pin when internal clock is not used.</td></tr>
</table>

■ FUNCTION DESCRIPTION

(1) CPU interface

(1-1) Selection of interface type

HM17CM4096 receives data through 8 bit parallel I/O(D_0~D_7)、16 bit parallel I/O(D_0~D_{15}) or divided into serial data input (SDA, SCL). Parallel or serial selection is decided by P/S pin setting.
Parallel or serial selection is possible as following table.
Reading out from internal register or RAM is not possible at serial interface mode.

TABLE

P/S	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68	SDA	SCL	data
H	Parallel input	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	SEL68			D_0~D_7 (D_0~D_{15})
L	Serial input	$\overline{CS}$	RS	-	-	-	SDA	SCL	-

caution 1) "-" mark item : Fix to "H" or "L"

(1-2) Parallel input

In the parallel interface mode selected by P/S port, parallel data is transferred from the 8bit/16bit MPU through data bus. SEL68 port setting makes 80-series or 68-series interface selection

TABLE

SEL68	CPU type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	data
H	68 series CPU	$\overline{CS}$	RS	E	R/W	D_0~D_7 (D_0~D_{15})
L	80 series CPU	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D_0~D_7 (D_0~D_{15})

(1-3) Data identification

Combinations of RS, $\overline{RD}$, and $\overline{WR}$ signals identify contents of 8bit data bus.

TABLE

RS	68 series	80 series		FUNCTION
	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read out from internal register
1	0	1	0	Write in to internal register
0	1	0	1	Read display data
0	0	1	0	Write display data

(1-4) Serial interface

2 types of serial interface (3 line type mode, 4 line type mode) are available by selecting SMODE pin.

TABEL

SMODE	Serial interface mode
H	3 line type
L	4 line type

(1-5) 4 line type serial interface

4 line serial interface by SDA and SCL is possible at chip selection state ($\overline{CS}$="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Serial input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of D_7, ⋯, D_1, D_0 and converted into 8-bit parallel data at the rising edge of 8th serial clock.

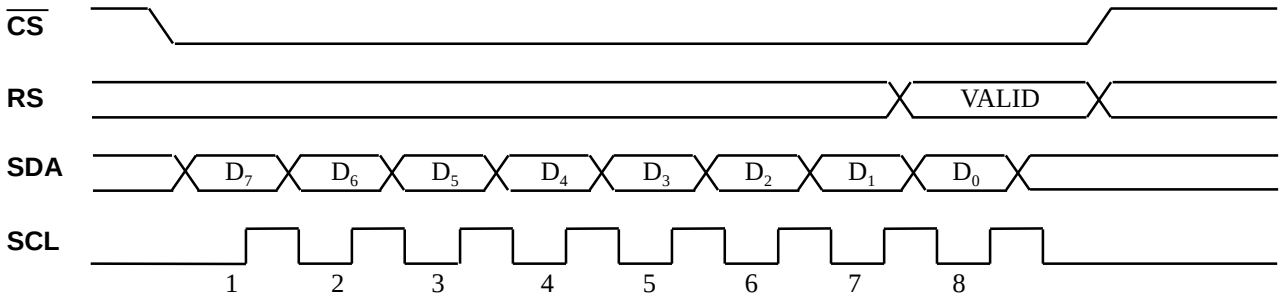
Serial data (SDA) are identified to display data or command by RS input.

TABLE

RS	Data contents
H	command
L	Display data

Make serial clock (SCL) "L" at the non-access period and after 8bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent mal-function, chip selector state should be released ($\overline{CS}$ = "H") after 8bit data transfer as shown in the following figure.



4 line serial interface

(1-6) 3 line type serial interface

3-line serial interface by SDA and SCL is possible at chip selection state ($\overline{CS}$="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of RS, D_7⋯, ,D_1, D_0, and converted to 8bit parallel data and handled at the rising edge of 9th serial clock.

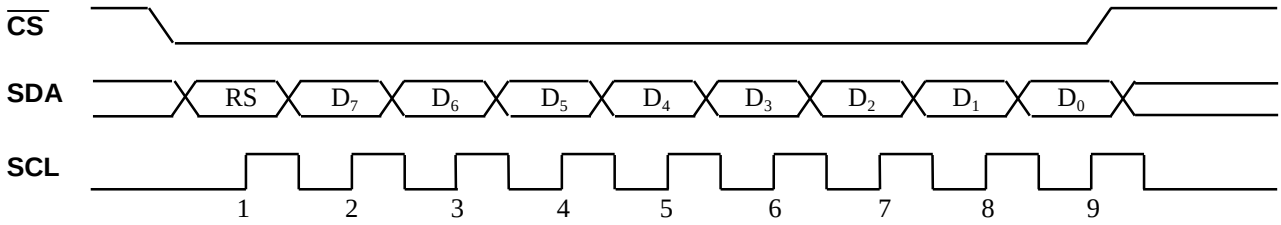
Serial data (SDA) are identified to display data or command by RS bit data at the rising of first serial clock (SCL) and state of command data bit polarity shift pin (SPOL).

TABLE

SPOL=L		SPOL=H	
RS	Data identify	RS	Data identify
L	Display data	L	command
H	command	H	Display data

Serial clock (SCL) should go to “L” at the non-access period and after 9bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent miss operation chip selector state should be released ($\overline{CS}$ = “H”) after 9bit data transfer as shown in the following figure.



3line serial interface

(1-7) One systematization of $\overline{CS}$ under some interface

In some operation mode, data interface control is possible.

Data in-out is possible under the condition, $\overline{CS}$ = “L”.

(2) DDRAM and internal register access

DDRAM and internal register are accessed by data bus D_0~D_7(D_0~D_{15}), chip select pin ($\overline{CS}$), DDRAM / register select pin (RS), read / write control pin ($\overline{RD}$) or $\overline{WR}$ pin.

When $\overline{CS}$=“H”, it is in non-selective state and DDRAM and internal register access is impossible.

During access, Set $\overline{CS}$=“L”.

Access selection to DDRAM or internal register is controlled by RS input.

TABLE

RS	Data contents
L	Display RAM data
H	Internal command register

Write process starts after address setting and then the data on the 8bit data bus D_0~D_7 or 16bit data bus D_0~D_{15} will be written in by CPU. The data is written at the rising edge of $\overline{WR}$ (80 series) or falling edge of E (68 series).

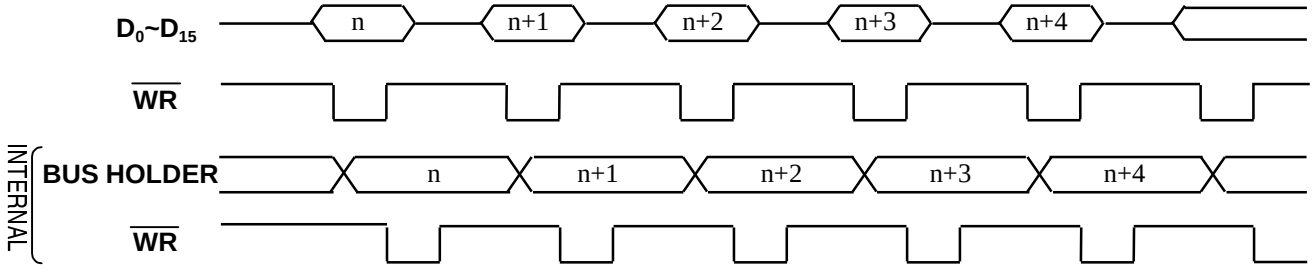
Internally, bus holder data is processed to data bus and data are written to bus holder from CPU until next cycle.

After address setting, data of assigned address are read at the 1st and 3rd clock, which means it needs dummy read at the 2nd clock.

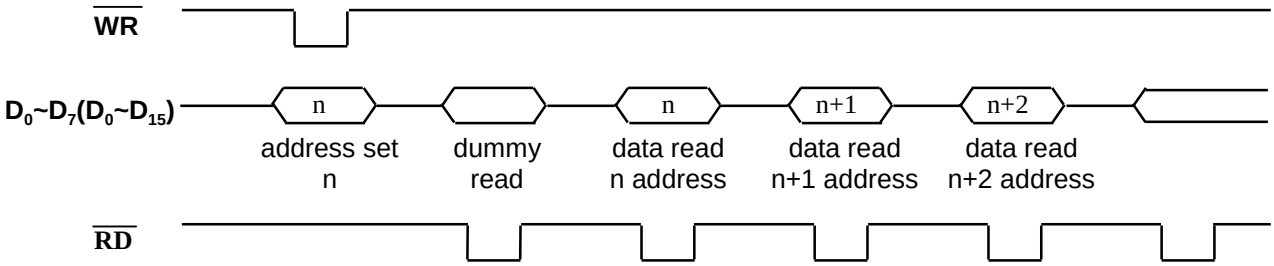
There are rules at reading data out of display RAM, after address setting, the data of assigned address is shown directly after the end of the read command, so pay attention that assigned data is available at 2nd timing step.

In other words, 1 cycle dummy read is needed after address setting and write cycle.

DATA WRITE IN OPERATION



DATA READ OUT OPERATION

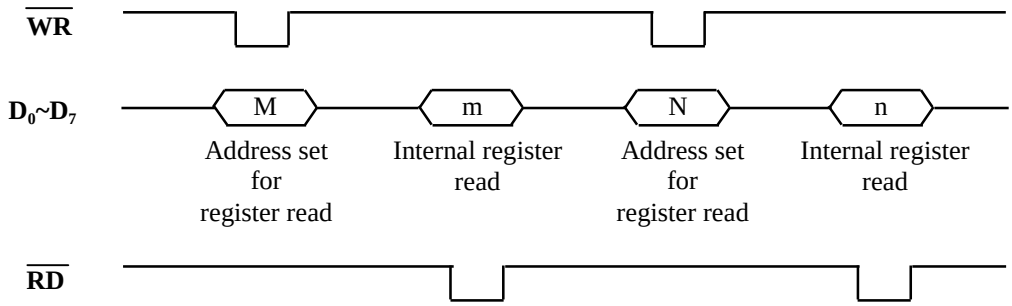


caution) When 16 bit mode, do write in and read out by 16 bit not only RAM access but also command setting.

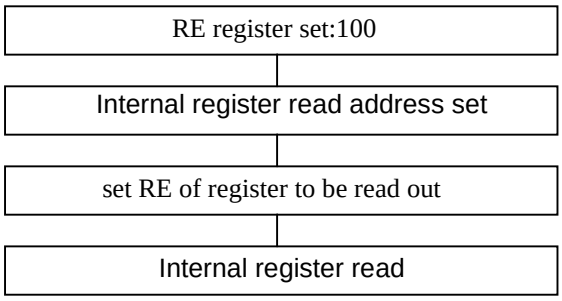
(3) Read out of internal register

Read out is possible not only from DDRAM, but also from the internal register. Addresses for read (0~F_H) are allocated in each register.

Read out is executed after writing read-out register address to internal register.



Internal register read out sequence



When register is read out, upper 4 bit data are “1111”.

Non-used bits of active registers are “0”.

When non-used registers are read out, upper 4 bits are “1111” and lower 4 bits are “0000”.

(4) 16 bit data access to DDRAM

It is possible to write in DDRAM by 16-bits access with the data of 16 bits data bus D_0~D_{15}.
16 bits data access mode is possible by setting the value of WLS register to "1".

TABEL

WLS	Access mode
L	8 bit
H	16 bit

Each command should be set to 8-bits(D_0~D_7) as well as to 16-bit access mode.
16-bit access is available at display RAM access.

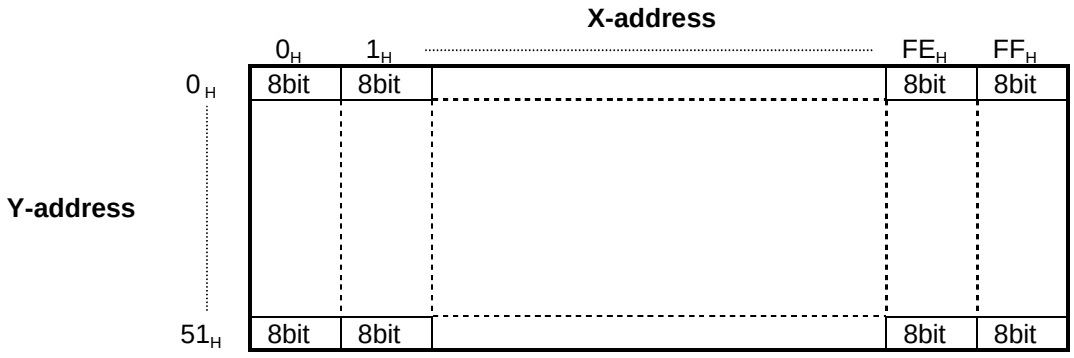
(5) Display start line register

When displaying the DDRAM data, it is the contents of Y address register that is corresponding to display start line.
The data of Y address is displayed on the display start line depending on the value of the shift command register and the display start line register.
The data of this register are preset to the display line counter per FLM signal transition.
Line counter is counted up in synchronization with CL input and generates line address that read out 384bit data from DDRAM to LCD driver circuit.

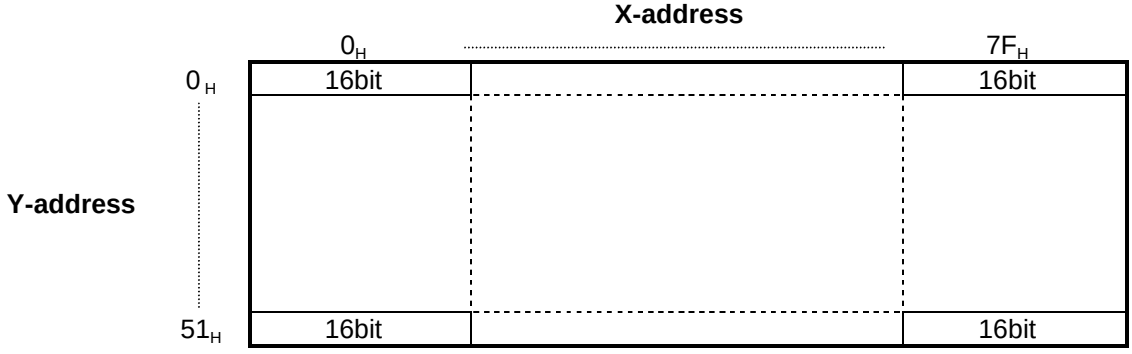
(6) DDRAM addressing

This IC includes display memory Bit mapped that is composed of 1,536 bit of X direction (12bit×128) and 162bit of Y direction.
In gray mode, neighboring 4-bit data are displayed by segment driver with 16 grays, respectively.
3 outputs of segment driver compose 1 pixel of RGB and 128×162 pixels are displayed with 4096 color (16gray×16gray×16gray).
Address area of X direction is varied according to accessed data length. The area of X direction is 0_H~FF_H at 8bit access mode and 0_H~$7F_H$ at 16bit access mode.

- **8BIT access**



- **16 BIT access**

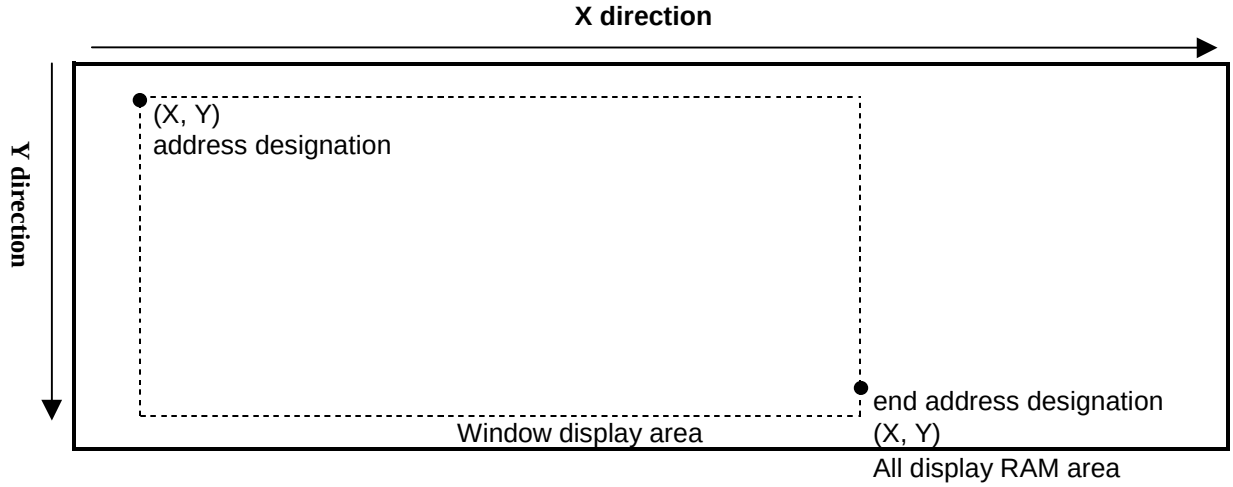


In the Black & white mode, the MSBs of 4 bit corresponding with RGB are used to display data. And so, 128x162 dot gray display or 384 × 162 B/W mode display is possible.

Display RAM is accessed with X address and Y address from CPU by 8 bit or 16 bit unit.
X address and Y address can be increased automatically by setting status of control register.
The address is increased per every read and write of display RAM by CPU. (Please see detail description at command function.)
X direction is selected by X address and Y direction is selected by Y address. Please do not set the address on non-effective area and it is forbidden to set address on outside area in each case.
384bit display data of Y direction are read out to display latch at rising edge of CL signal per 1 line cycle and this data comes out from display latch at falling edge of CL signal.
Display start line address register is preset to line counter at "H" state of FLM signal which changes per one frame cycle and the address is counted up with synchronized CL input.
Display line address counter is synchronized by timing signals of LCD driver, and it operates independently with X, Y address counters.

(7) Window address assign of display RAM

This IC can be accessed to display RAM by window area designation in addition to access to display RAM designated by X and Y address.
Through address space of all display address, specific area of RAM can be accessed by designated two points.
The start point of two point addresses is assigned by normal X address and Y address register and the end point of them is done by X end address and Y end address register value. Designated inner addresses depend on WLS bit.
Read modified write action can be taken by AIM="1".
In case of using window area accessing mode, you must set start point X address, Y address in sequence and end point X address, Y address in sequence after executing Win command (WIN="1", auto increase mode AXI="1", AYI="1") and then access to Display RAM.
And set start point and end point not to be designated to access the outside of available address area. Address set value should be taken to set AX ≤ EX (end point of X address) and AY≤EY (end point of Y address).



(8) display RAM data and LCD

Display RAM data related with one dot of LCD is dependent on REV register. Normal display and reverse display by REV register are set up as follows.

TABLE

REV	Display	RAM data
L	normal	0
		1
H	reverse	0
		1

(9) Segment display output order/reverse set up

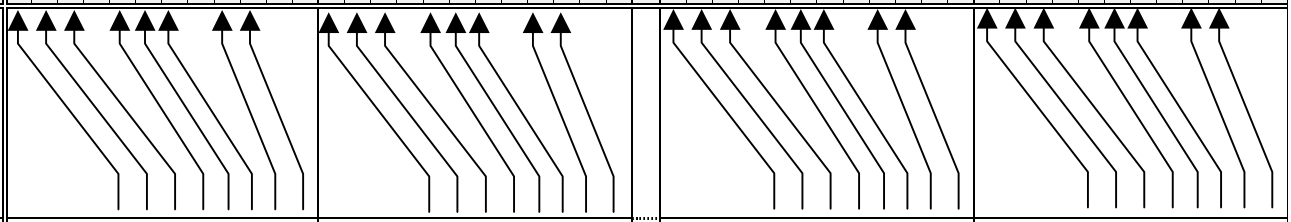
The order of display outputs, $SEGA_0$, $SEGB_0$, $SEGC_0$ to $SEGA_{127}$, $SEGB_{127}$, and can be reversed by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

(10) Relation between RAM X-address and Bit Assign

RAM X-Address / Bit Assign TABLE 1 (4096 color mode)

MODE	WLS	ABS	HSW	REF	SEG0												SEG1													SEG126												SEG127											
					Palette A				Palette B				Palette C				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
					R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0		R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
16 bit	1	0	X	0	X=00H												X=01H													X=7EH												X=7FH											
					D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1		D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	0	X	1	X=7FH												X=7EH													X=01H												X=00H											
					D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1		D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	1	X	0	X=00H												X=01H													X=7EH												X=7FH											
					D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	X	1	X=7FH												X=7EH													X=01H												X=00H											
					D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bit	0	0	0	0	X=00H							X=01H					X=02H							X=03H					X=FCH							X=FDH					X=FEH							X=FFH			
					D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1		D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	0	0	1	X=FEH							X=FFH					X=FCH							X=FDH					X=02H							X=03H					X=00H							X=01H			
					D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1		D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	1	0	0	X=00H				X=01H				X=02H				X=03H								X=FCH				X=FDH								X=FEH				X=FFH							
					D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	1	X=FEH				X=FFH				X=FCH				X=FDH								X=02H				X=03H								X=00H				X=01H							
					D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	1	0	X=00H							X=01H					X=02H								X=BDH					X=BEH								X=BFH											
					D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	1	1	X=BEH(L)				X=BFH				X=BDH				X=BEH(H)								X=01H(L)				X=02H								X=00H								X=01H(H)			
					D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4

RAM X-Address / Bit Assign TABLE 2 (256 color mode)

Mode	WLS	ABS	HSW	REF	C256	SEG0												SEG1												...	SEG126												SEG127											
						Palette R				Palette G				Palette B				Palette R				Palette G				Palette B					Palette R				Palette G				Palette B				Palette R				Palette G				Palette B			
						R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0		R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
assignment																																																								
8 bit	0	X	X	0	1	X=00H												X=01H													X=7EH												X=7FH											
						-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0		-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	X	1	1	X=7FH												X=7EH													X=01H												X=00H											
						-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0		-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

Remark 1) Under 256 color mode, the lowest vacant bits are filled with "1".
2) There are no relations between the wrote-in data when C256="0" and C256="1".

SWAP OPERATION TABLE

REF	SWAP	Palette A				Palette B				Palette C			
		R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
0	0	SEGAx				SEGBx				SEGCx			
1	1												
0	1	SEGCx				SEGBx				SEGAx			
1	0												

- **RAM DATA WRITE – IN TABLE**

WLS = 1, ABS = 0, HSW = *

Data Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Write 1	R3_0	R2_0	R1_0	R0_0	*	G3_0	G2_0	G1_0	G0_0	*	*	B3_0	B2_0	B1_0	B0_0	*
Data Write 2	R3_1	R2_1	R1_1	R0_1	*	G3_1	G2_1	G1_1	G0_1	*	*	B3_1	B2_1	B1_1	B0_1	*
.																
Data Write 127	R3_126	R2_126	R1_126	R0_126	*	G3_126	G2_126	G1_126	G0_126	*	*	B3_126	B2_126	B1_126	B0_126	*
Data Write 128	R3_127	R2_127	R1_127	R0_127	*	G3_127	G2_127	G1_127	G0_127	*	..					

WLS = 1, ABS = 1, HSW = *

Data Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Write 1	*	*	*	*	R3_0	R2_0	R1_0	R0_0	G3_0	G2_0	G1_0	G0_0	B3_0	B2_0	B1_0	B0_0
Data Write 2	*	*	*	*	R3_1	R2_1	R1_1	R0_1	G3_1	G2_1	G1_1	G0_1	B3_1	B2_1	B1_1	B0_1
.																
Data Write 127	*	*	*	*	R3_126	R2_126	R1_126	R0_126	G3_126	G2_126	G1_126	G0_126	B3_126	B2_126	B1_126	B0_126
Data Write 128	*	*	*	*	R3_127	R2_127	R1_127	R0_127	G3_127	G2_127	..					

WLS = 0, ABS = 0, HSW = 0

Data Write	D7	D6	D5	D4	D3	D2	D1	D0
Data Write 1	R3_0	R2_0	R1_0	R0_0	*	G3_0	G2_0	G1_0
Data Write 2	G0_0	*	*	B3_0	B2_0	B1_0	B0_0	*
Data Write 3	R3_1	R2_1	R1_1	R0_1	*	G3_1	G2_1	G1_1
Data Write 4	G0_1	*	*	B3_1	B2_1	B1_1	B0_1	*
.								
Data Write 153	R3_126	R2_126	R1_126	R0_126	*	G3_126	G2_126	G1_126
Data Write 254	G0_126	*	*	B3_126	B2_126	B1_126	B0_126	*
Data Write 255	R3_127	R2_127	R1_127	R0_127	*	G3_127	G2_127	G1_127
Data Write 256	G0_127	*	..					

WLS = 0, ABS = 1, HSW = 0

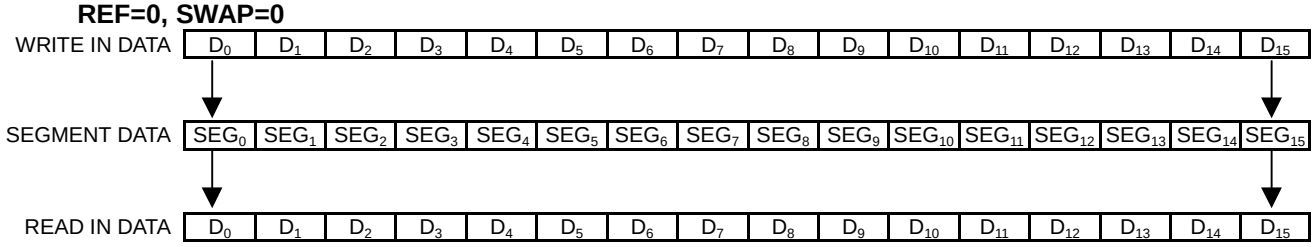
Data Write	D7	D6	D5	D4	D3	D2	D1	D0
Data Write 1	*	*	*	*	R3_0	R2_0	R1_0	R0_0
Data Write 2	G3_0	G2_0	G1_0	G0_0	B3_0	B2_0	B1_0	B0_0
Data Write 3	*	*	*	*	R3_1	R2_1	R1_1	R0_1
Data Write 4	G3_1	G2_1	G1_1	G0_1	B3_1	B2_1	B1_1	B0_1
.								
Data Write 153	*	*	*	*	R3_126	R2_126	R1_126	R0_126
Data Write 254	G3_126	G2_126	G1_126	G0_126	B3_126	B2_126	B1_126	B0_126
Data Write 255	*	*	*	*	R3_127	R2_127	R1_127	R0_127
Data Write 256	G3_127	G2_127	G1_127					

WLS = 0, ABS = *, HSW = 1

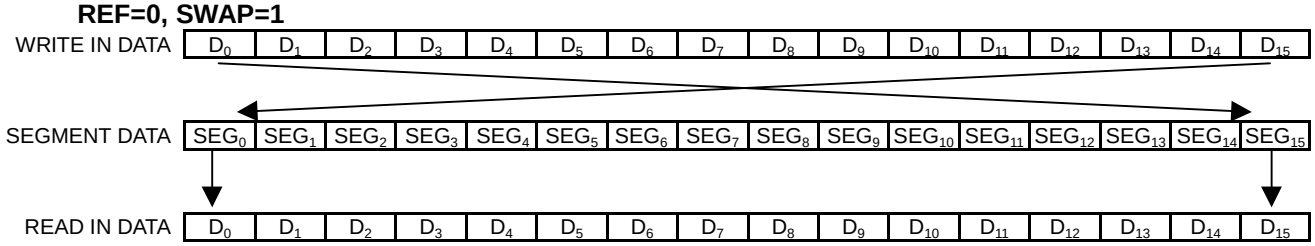
Data Write	D7	D6	D5	D4	D3	D2	D1	D0
Data Write 1	R3_0	R2_0	R1_0	R0_0	G3_0	G2_0	G1_0	G0_0
Data Write 2	B3_0	B2_0	B1_0	B0_0	R3_1	R2_1	R1_1	R0_1
Data Write 3	G3_1	G2_1	G1_1	G0_1	B3_1	B2_1	B1_1	B0_1
....								
Data Write 190	R3_126	R2_126	R1_126	R0_126	G3_126	G2_126	G1_126	G0_126
Data Write 191	B3_126	B2_126	B1_126	B0_126	R3_127	R2_127	R1_127	R0_127
Data Write 192	G3_127	G2_127	..					

. WRITE IN / READ IN BITMAP (16 BIT MODE)

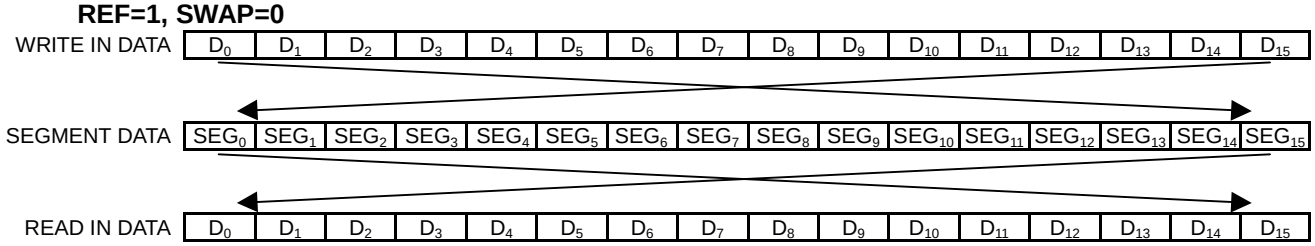
REF=0, SWAP=0



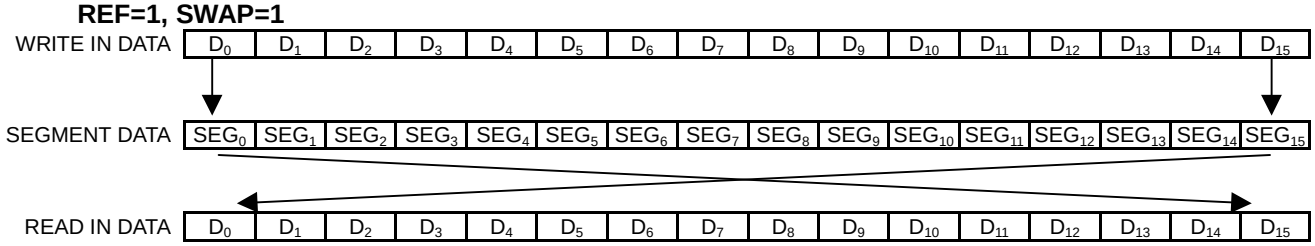
REF=0, SWAP=1



REF=1, SWAP=0

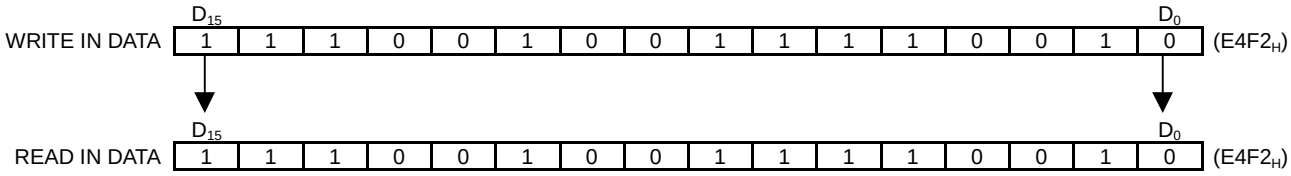


REF=1, SWAP=1

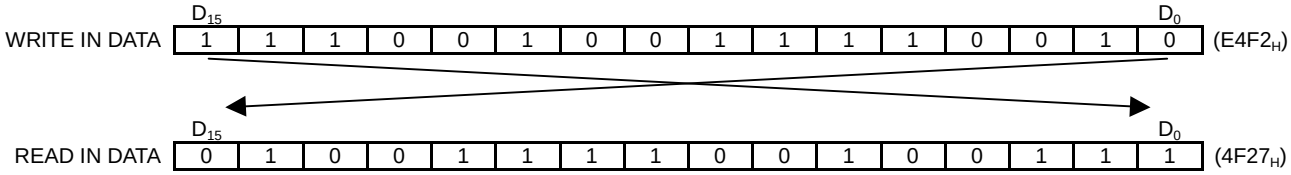


. READ OUT AFTER WROTE IN DATA (16 BIT MODE)

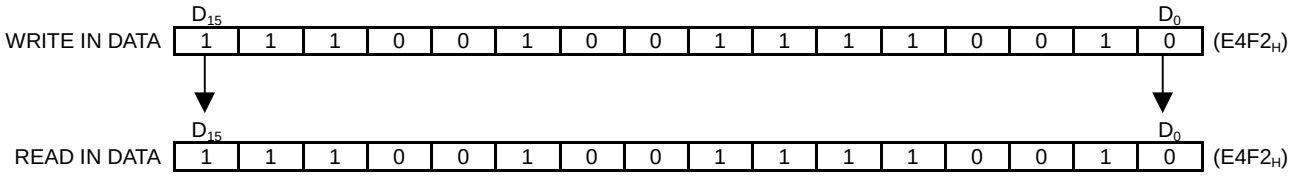
REF=0, SWAP=0



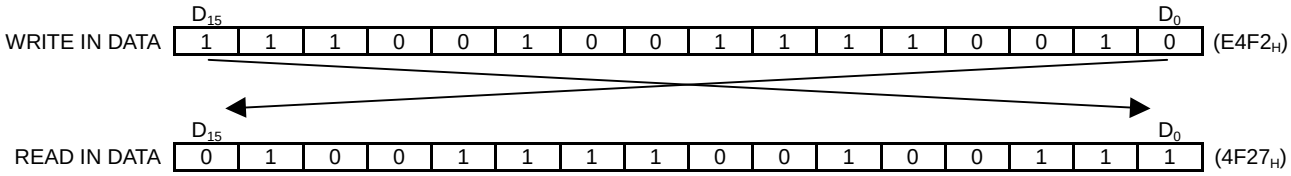
REF=0, SWAP=1



REF=1, SWAP=0

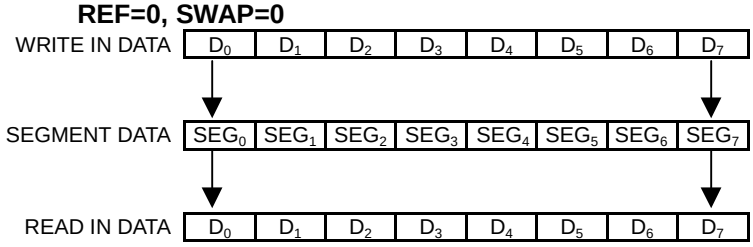


REF=1, SWAP=1

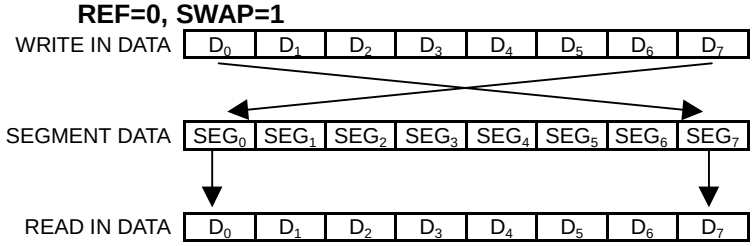


. WRITE IN / READ IN BITMAP (8 BIT MODE)

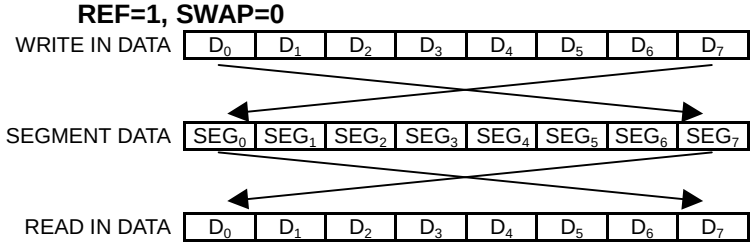
REF=0, SWAP=0



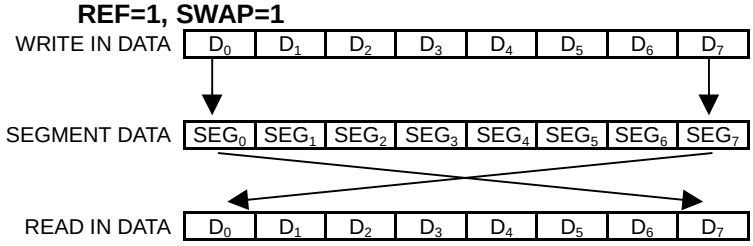
REF=0, SWAP=1



REF=1, SWAP=0

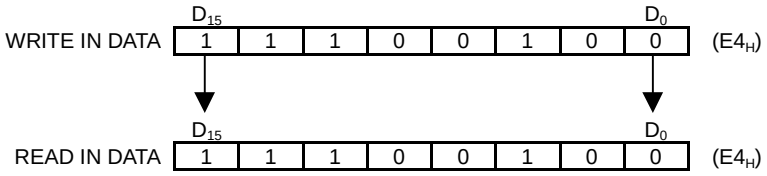


REF=1, SWAP=1

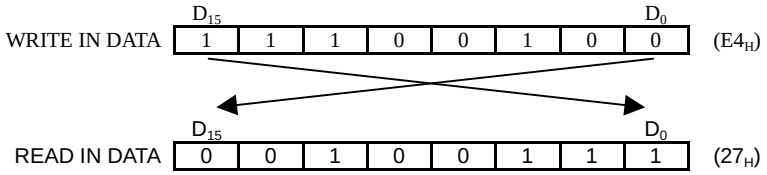


. READ OUT AFTER WROTE IN DATA (8 BIT MODE)

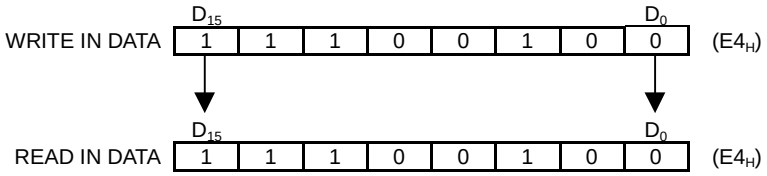
REF=0, SWAP=0



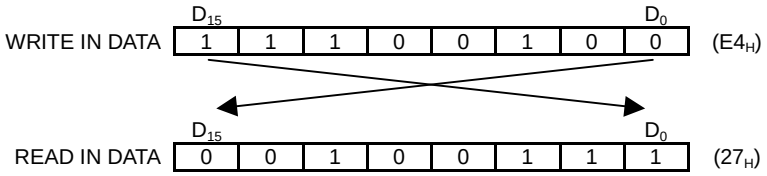
REF=0, SWAP=1



REF=1, SWAP=0



REF=1, SWAP=1



(11) display data structure and gradation control

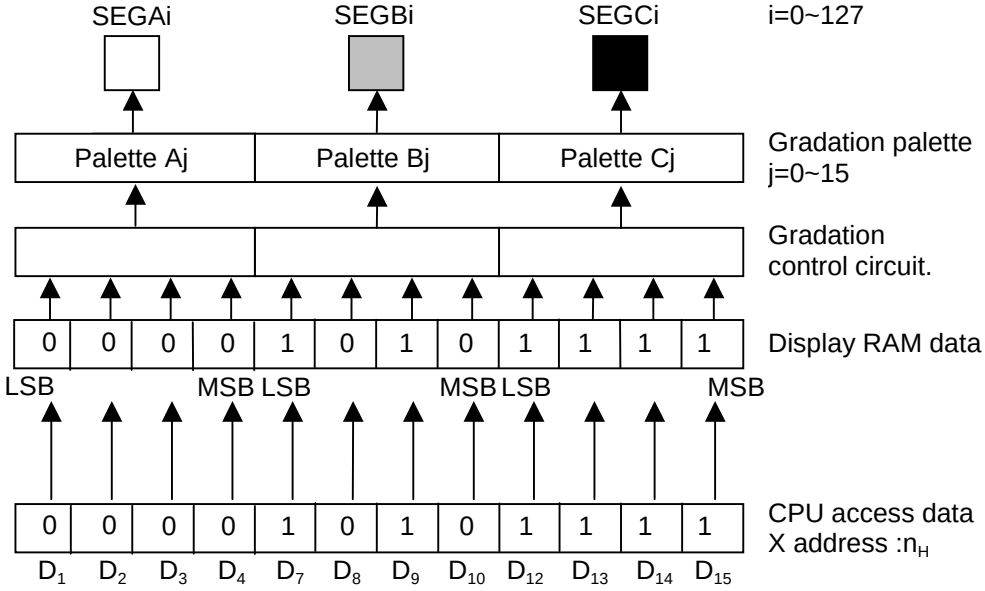
For the purpose of gradation control, information per pixel requires multiple bits. This IC has 4 bit per output to achieve the gradation display.

This IC is connected to an STN color LCD panel by three segment port units and one pixel consists of three outputs of segment driver, and so 4096 color (4 bits x 4 bits x 4 bits) display on 128 x 162 pixels is realized.

Since one pixel data can be processed by one time access to memory, the data can be rewritten fast and naturally.

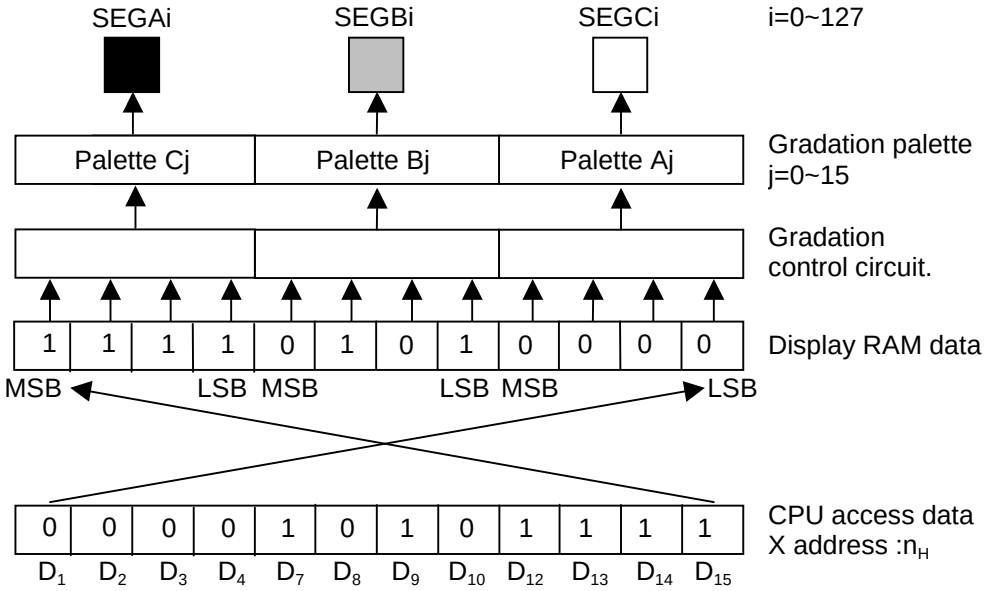
The weight of each data bit is dependent on the status of SWAP register bit and REF register when data is written to the display RAM.

- **ACCESS when (REF, SWAP)=(0, 0) or (1, 1)**



notice) internal access X address :n_H~$7F_H$ (access when REF="0")
:$7F_H$~n_H (access when REF="1")

- **ACCESS when (REF, SWAP)=(0, 1) or (1, 0)**



notice) internal access X address :n_H~$7F_H$ (access when REF="0")
:$7F_H$~n_H (access when REF="1")

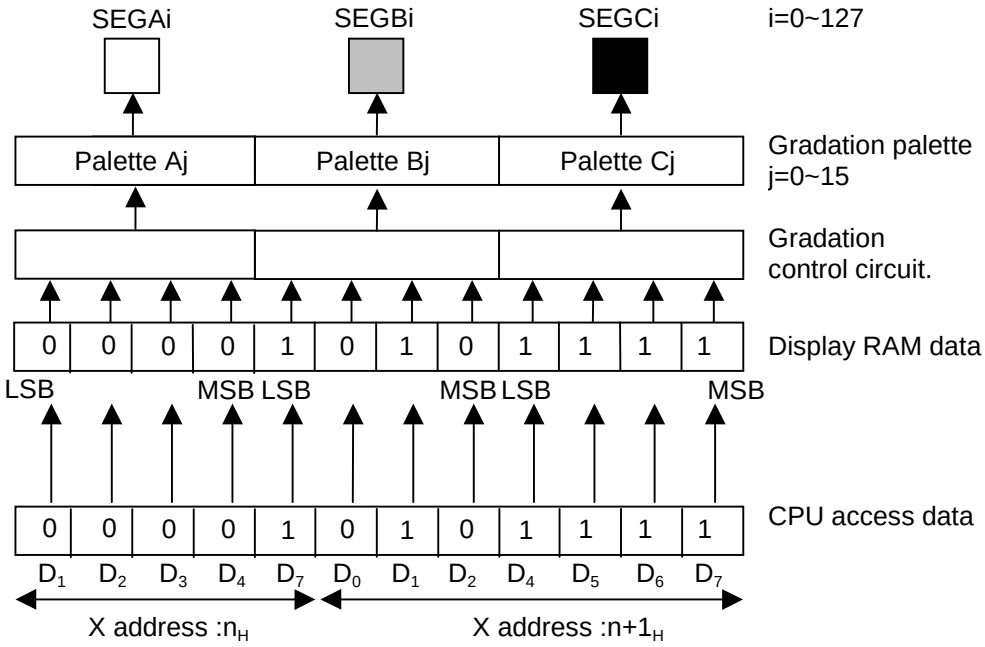
When display RAM is accessed by 16 bit data width, the weight of each data bit is dependent on the status of SWAP register and REF register, the same method as 8 bit access.

12 bit data are extracted from 16 bit address, and then transmitted to gradation palettes.

At 8 bit – 4096 gradation mode , two 8 bit address map is used at display.

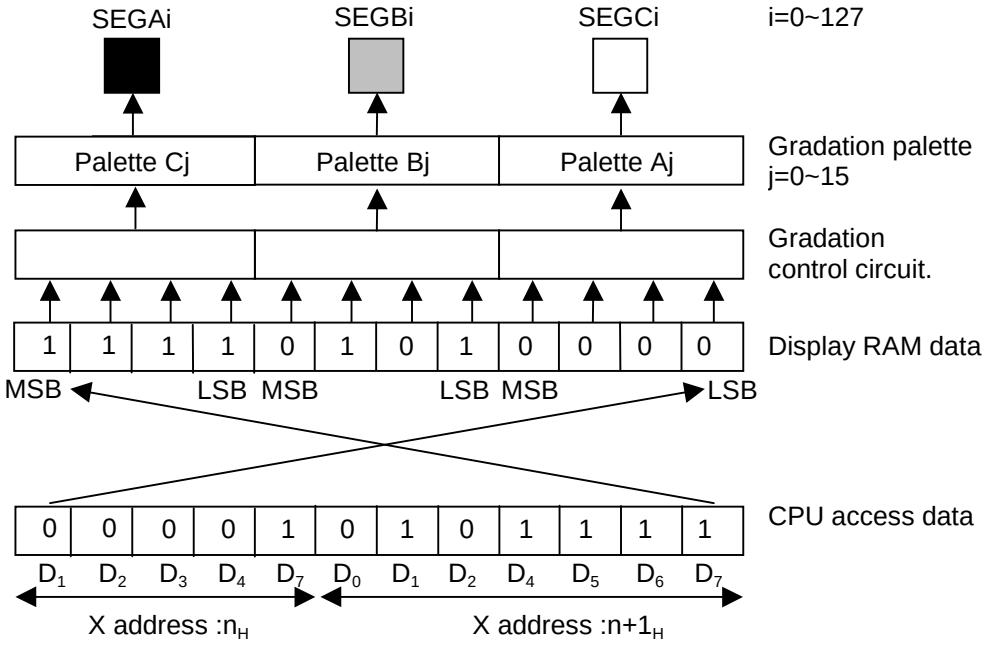
More detail information, please refer to bit assign table.

- **ACCESS when (REF, SWAP)=(0, 0) or (1, 1)**



notice) internal access X address :n_H~FF_H (access when REF="0")
:FF_H~n_H (access when REF="1")

- **ACCESS when (REF, SWAP)=(0, 1) or (1, 0)**



notice) internal access X address :n_H~FF_H (access when REF="0")
:FF_H~n_H (access when REF="1")

■ DUTY RATIO SETTING

DS3	DS2	DS1	DS0	Dot width in Y-direction	Duty setting	f_{FLM} (Frame Frequency)		
						Variable 16 gradation (fosc=763kHz)	Fixed 8 gradation (fosc=172kHz)	BW(fosc=25kHz)
0	0	0	0	162	1/163Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	0	0	1	160	1/160Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	0	1	0	144	1/144Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	0	1	1	133	1/133Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	1	0	0	128	1/128Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	1	0	1	112	1/112Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	1	1	0	96	1/96Duty	fosc/(62*D)	fosc/(14*D)	fosc/(2*D)
0	1	1	1	80	1/80Duty	fosc/(62*D*2)	fosc/(14*D*2)	fosc/(2*D*2)
1	0	0	0	72	1/72Duty	fosc/(62*D*2)	fosc/(14*D*2)	fosc/(2*D*2)
1	0	0	1	64	1/64Duty	fosc/(62*D*2)	fosc/(14*D*2)	fosc/(2*D*2)
1	0	1	0	56	1/56Duty	fosc/(62*D*2)	fosc/(14*D*2)	fosc/(2*D*2)
1	0	1	1	48	1/48Duty	fosc/(62*D*4)	fosc/(14*D*4)	fosc/(2*D*4)
1	1	0	0	40	1/40Duty	fosc/(62*D*4)	fosc/(14*D*4)	fosc/(2*D*4)
1	1	0	1	32	1/32Duty	fosc/(62*D*4)	fosc/(14*D*4)	fosc/(2*D*4)
1	1	1	0	24	1/24Duty	fosc/(62*D*8)	fosc/(14*D*8)	fosc/(2*D*8)
1	1	1	1	16	1/16Duty	fosc/(62*D*8)	fosc/(14*D*8)	fosc/(2*D*8)

■ COMMON START LINE SET

SC3	SC2	SC1	SC0	SHIFT="0"	SHIFT="1"
0	0	0	0	COM0 ~	COM161 ~
0	0	0	1	COM1 ~	COM160 ~
0	0	1	0	COM9 ~	COM152 ~
0	0	1	1	COM14 ~	COM146 ~
0	1	0	0	COM17 ~	COM144 ~
0	1	0	1	COM25 ~	COM136 ~
0	1	1	0	COM33 ~	COM128 ~
0	1	1	1	COM41 ~	COM120 ~
1	0	0	0	COM49 ~	COM112 ~
1	0	0	1	COM57 ~	COM104 ~
1	0	1	0	COM65 ~	COM96 ~
1	0	1	1	COM73 ~	COM88 ~
1	1	0	0	COM122 ~	COM39 ~
1	1	0	1	COM130 ~	COM31 ~
1	1	1	0	COM138 ~	COM23 ~
1	1	1	1	COM146 ~	COM15 ~

■ BIAS SETTING

B2	B1	B0	Bias setting
0	0	0	1/9Bias
0	0	1	1/8Bias
0	1	0	1/7Bias
0	1	1	1/6Bias
1	0	0	1/5Bias
1	0	1	1/10Bias
1	1	0	1/11Bias
1	1	1	1/12Bias

■ GRADATION MODE SETTING

MON	PWM	C256	Gradation mode	1 pixel RAM data												Palette setting
				R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	
0	0	0	Variable 16 gradation mode (variable 4096 color display)	E	E	E	E	E	E	E	E	E	E	E	E	E（variable）
0	1	*	Fixed 8 gradation mode (fixed 256 color display)	E	E	E	X	E	E	E	X	E	E	X	X	X（fixed）
1	*	*	BW mode (8 color display)	E	X	X	X	E	X	X	X	E	X	X	X	X（fixed）
*	*	1	256 color mode	D7	D6	D5	“1’	D4	D3	D2	“1”	D1	D0	“1”	“1”	E (variable)

Remark) X means non-effective data

■ 16 BIT RAM ACCESS SETTING (WLS = “1”)

ABS	Access mode	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Normal access mode 1	R3	R2	R1	R0	X	G3	G2	G1	G0	X	X	B3	B2	B1	B0	X
1	Normal access mode 2	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

Remark) X means non-effective data

■ 8 BIT RAM ACCESS SETTING (WLS = “0”)

HSW	ABS	C256	Access mode		D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	Normal access mode 1 (1 frame data write in during 2 write cycle)	1	R3	R2	R1	R0	X	G3	G2	G1
				2	G0	X	X	B3	B2	B1	B0	X
0	1	0	Normal access mode 2 (1 frame data write in during 2 write cycle)	1	X	X	X	X	R3	R2	R1	R0
				2	G3	G2	G1	G0	B3	B2	B1	B0
1	*	0	High speed access mode (2 frame data write in during 3 write cycle)	1	R3	R2	R1	R0	G3	G2	G1	G0
				2	B3	B2	B1	B0	R3	R2	R1	R0
				3	G3	G2	G1	G0	B3	B2	B1	B0
*	*	1	256 Color Mode		R3	R2	R1	G3	G2	G1	B3	B2

Remark) X means non-effective data

■ GRADATION MODE SETTING (WLS = “1”)

FDC1	FDC2	Boosting clock
0	0	Normal speed
0	1	2 × normal speed
1	0	3 × normal speed
1	1	4 × normal speed

(12) GRADATION PALETTE

This IC has two gradation display modes, the fixed gradation display mode and the variable gradation display mode.

Select mode by setting the gradation display mode register (PWM command) to the purpose.

PWM="0" : variable gradation mode among 32-level gradations.
PWM="1" : fixed 16 gradation mode

To select the best gradation level suited to LCD panel at variable gradation display mode, use the gradation palette register among 32-level gradation palettes. Segment driver outputs are set by selected 8-level gradation palette.

The gradation palette register provides three registers (palette Aj, Bj, and Cj : j=0~15) for the segment driver outputs, SEGAi(0~127), SEGBi(0~127), and SEGCi(0~127) . Each register consists of a 5-bit register, selecting 16 gradations from the 32 gradation pattern.

GRADATION PALETTE INITIAL VALUE

(palette Aj, palette Bj, palette Cj ; j = 0 ~ 15)

RAM data				Register name	Initial value
0	0	0	0	Gradation palette 0	0/31
0	0	0	1	Gradation palette 1	3/31
0	0	1	0	Gradation palette 2	5/31
0	0	1	1	Gradation palette 3	7/31
0	1	0	0	Gradation palette 4	9/31
0	1	0	1	Gradation palette 5	11/31
0	1	1	0	Gradation palette 6	13/31
0	1	1	1	Gradation palette 7	15/31
1	0	0	0	Gradation palette 8	17/31
1	0	0	1	Gradation palette 9	19/31
1	0	1	0	Gradation palette 10	21/31
1	0	1	1	Gradation palette 11	23/31
1	1	0	0	Gradation palette 12	25/31
1	1	0	1	Gradation palette 13	27/31
1	1	1	0	Gradation palette 14	29/31
1	1	1	1	Gradation palette 15	31/31

GRADATION PALETTE TABLE (PWM = "1", MON = "0" ; fixed 8 gradation mode)

RAM data (R,G)				gradation
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

RAM data (B)				gradation
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

GRADATION PALETTE TABLE (PWM = “0”, MON = “0” ; variable 16 gradation mode)

(palette Aj, palette Bj, palette Cj ; j = 0 ~ 15)

palette					gradation	REMARK
0	0	0	0	0	0/31	Palette 0 initial value
0	0	0	0	1	1/31	
0	0	0	1	0	2/31	
0	0	0	1	1	3/31	Palette 1 initial value
0	0	1	0	0	4/31	
0	0	1	0	1	5/31	Palette 2 initial value
0	0	1	1	0	6/31	
0	0	1	1	1	7/31	Palette 3 initial value
0	1	0	0	0	8/31	
0	1	0	0	1	9/31	Palette 4 initial value
0	1	0	1	0	10/31	
0	1	0	1	1	11/31	Palette 5 initial value
0	1	1	0	0	12/31	
0	1	1	0	1	13/31	Palette 6 initial value
0	1	1	1	0	14/31	
0	1	1	1	1	15/31	Palette 7 initial value
1	0	0	0	0	16/31	
1	0	0	0	1	17/31	Palette 8 initial value
1	0	0	1	0	18/31	
1	0	0	1	1	19/31	Palette 9 initial value
1	0	1	0	0	20/31	
1	0	1	0	1	21/31	Palette 10 initial value
1	0	1	1	0	22/31	
1	0	1	1	1	23/31	Palette 11 initial value
1	1	0	0	0	24/31	
1	1	0	0	1	25/31	Palette 12 initial value
1	1	0	1	0	26/31	
1	1	0	1	1	27/31	Palette 13 initial value
1	1	1	0	0	28/31	
1	1	1	0	1	29/31	Palette 14 initial value
1	1	1	1	0	30/31	
1	1	1	1	1	31/31	Palette 15 initial value

GRADATION PALETTE TABLE (MON = “1” ; BW mode)

RAM data				gradation
0	*	*	*	0
1	*	*	*	1

(13) DISPLAY TIMMING GENERATOR

The display-timing generator makes a timing clock and timing pulses (CL, FLM, FR and CLK) for internal operation by inputting the original oscillating clock CK or by the oscillating circuit.

(14) SIGNAL GENERATION OF DISPLAY LINE COUNTER, DISPLAY DATA LATCH CIRCUIT.

The latch signal from line counter clock to display data latch circuit is generated from display clock (CL). Synchronized with the display clock, the line addresses of Display RAM are generated and 384-bit display data are latched to display-data latching circuit and then output to the LCD drive circuit (SEG output port).

Read-out of the display data to the LCD drive circuit is completely independent of MPU side and so MPU can access it with no relationship with the read-out operation of the display data.

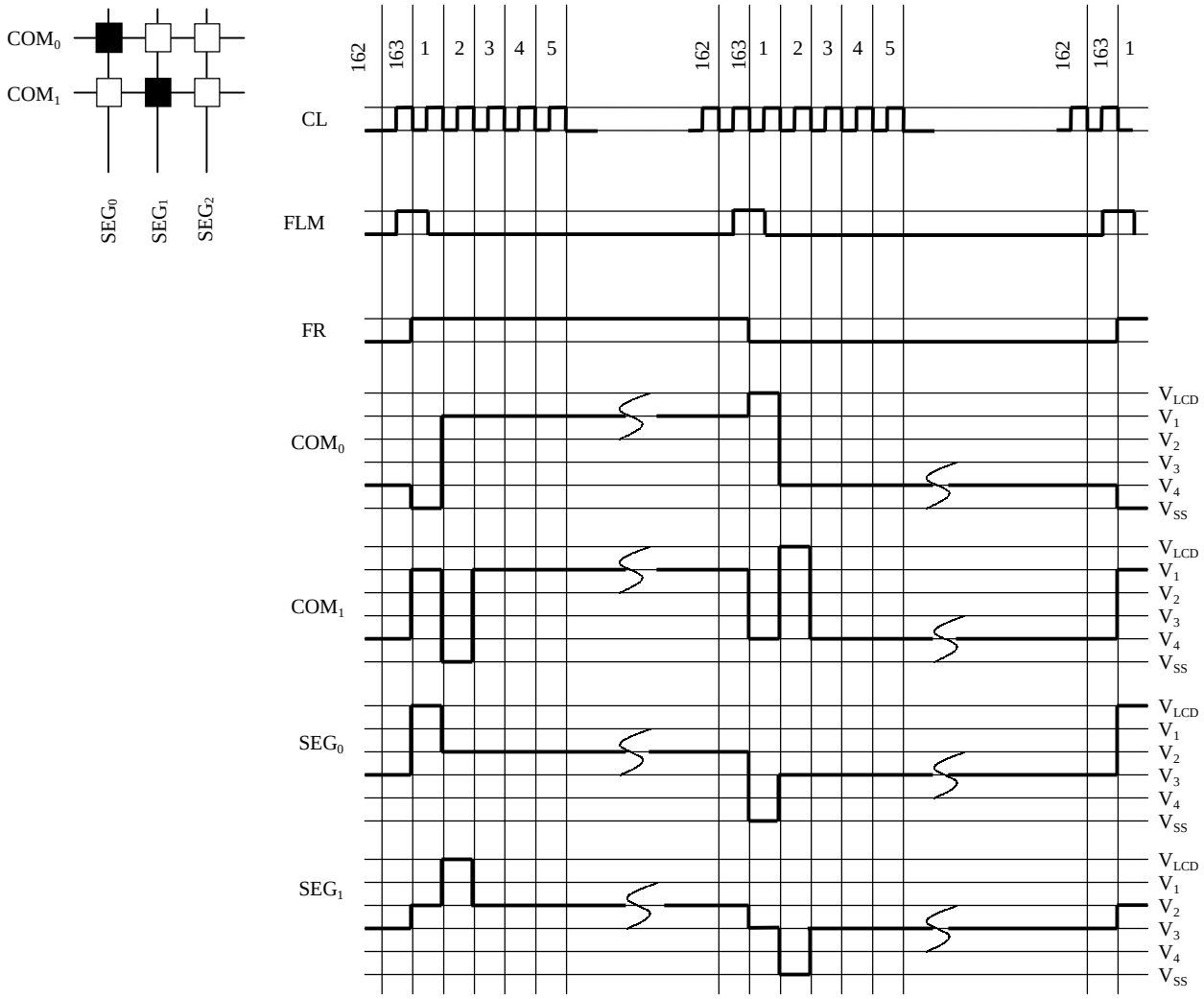
(15) GENERATION OF THE ALTERNATED SIGNAL(FR), SYNCHRONOUS SIGNAL(FLM).

The alternated signal (FR) and synchronous signal (FLM) are generated from the display clock (CL). The FLM generates alternated drive waveform to the LCD drive circuit per frame at normal state (inverse FR signal level per 1 frame). But by setting up data (n-1) on n-line inversion register and “1” on n-line alternated command (NLIN), n-line inverse waveform can be generated.

(16) DISPLAY DATA LATCH CIRCUIT

This circuit latches the display data from display RAM to LCD driver circuit temporarily per every common period. Normal / reverse display, display ON/OFF, and display all on command are done by controlling data in this latch. And no data within display RAM changes.

(17) EXAMPLE OF LCD DRIVING (NORMAL MODE, 1/163 DUTY, BLACK & WHITE DISPLAY MODE)



Remark) when 1/163 duty, the status of COM/SEG at 163rd driving sequence.
COM : all no selection
SEG : same with 162 line data output

(18) LCD DRIVER CIRCUIT

This drive circuit generates four levels of LCD drive voltage. The circuit has 384 segment outputs and 162 common outputs and outputs combined display data and FR signal.

The common drive circuit that has shift register and outputs common scan signals sequentially.

(19) OSCILLATOR CIRCUIT

HM17CM4096 has the CR oscillator. The output of oscillator is used as the timing signal source of display and boosting clock to the booster.

If external clock is used, feed the clock to OSC_1 pin or connect resistor between OSC_1 and OSC_2.

And feedback resistance with command can set the inner oscillator circuit of **HM17CM4096.**

The frame frequency can be altered by changed oscillator frequency according to feedback resistance length set value. To get optimum frame frequency, please check LCD and then set the frequency of oscillator.

(20) POWER SUPPLY CIRCUIT

This block generates the voltages necessary for driving LCD panel. The power supply circuit consists of voltage boosting circuit and voltage converting circuit and generates the voltages (V_{LCD}, V_1, V_2, V_3, V_4.) for LCD driving.

For large panel driving, it's preferable to use external voltage source rather than to use built-in power supply circuit for good image quality.

When using external voltage source, disable the built-in power supply circuit(AMPON, DCON='00'), supply the V_{LCD}, V_1, V_2, V_3, V_4 and V_{OUT} externally and open the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG}, V_{EE} terminals.

According to power supply circuit control command input, the power supply circuit can be enabled partially. External power supply and partial inner power circuit can be used together. Refer to the next table.

DCON	AMPON	Boosting circuit	Converting circuit	External voltage input	remark
0	0	Disable	disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4 common	※1,3
0	1	Disable	enable	V_{OUT} common	※2,3
1	1	Enable	enable	–	–

※1. All the built-in boosting circuit, converting circuit is not used. Open the ,C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG}, V_{EE} terminals, LCD driving voltage should be applied externally.

※2.Only the Boosting circuit is not used. Open the C_1+,C_1-,C_2+,C_2-,C_3+,C_3-,C_4+,C_4-,C_5+,C_5-,C_6+,C_6-, V_{OUT} terminals, The power for converting circuit must be supplied through V_{OUT} terminal and the reference voltage must be supplied by V_{REF} terminal.

※3.The conditions between V_{OUT}, V_{LCD}, V_1, V_2, V_3, and V_4 are $V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.

(21) VOLTAGE BOOSTING CIRCUIT

By connecting capacitor CA_1 between C_1+ and C_1-, C_2+ and C_2-, C_3+ and C_3-, C_4+ and C_4-, C_5+ and C_5- , C_6+ and C_6-, V_{OUT} and V_{SS} , n-time boosted voltage of V_{EE} - V_{SS} can be generated through V_{OUT} port. The boosting coefficient can be set by command and 2-times/ 3-times / 4-times/ 5-times/ 6-times/ 7-times boosted voltage is output through V_{OUT} port.

At application, specific boosting coefficient is used, refer to the following description.

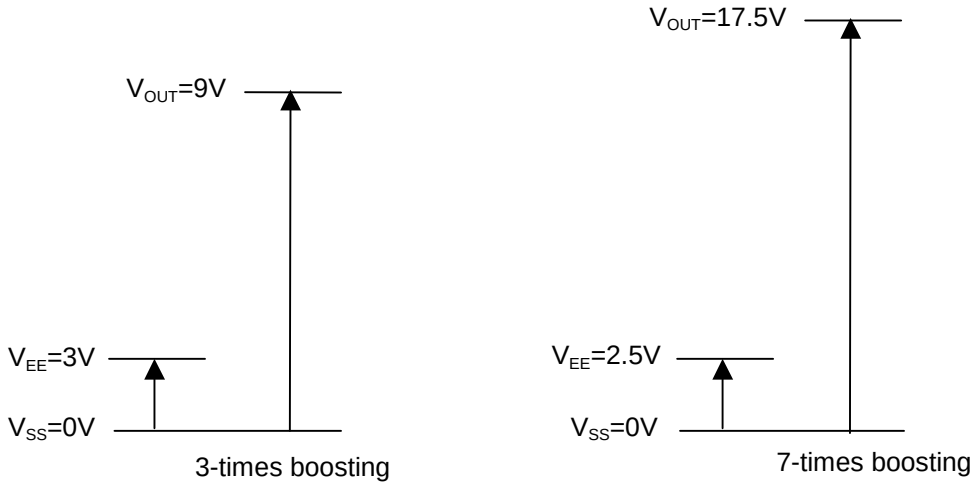
At 2-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , and open C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals.

At 3-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , C_2+ and C_2- , and open C_3+,C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals.

At 4-times boosting is designed, connect boosting capacitor CA_1 between C_1+ and C_1- , C_2+ and C_2- , C_3+ and C_3- , and open C_4+, C_4-, C_5+, C_5-, C_6+, C_6- terminals

At 5-times/ 6-times/ 7-times boosting are same structures with upper case.

Special care should be taken so that the voltage of VOUT would not exceed 18V MAX.
VOUT voltage exceeding 18V can cause malfunction and reliability problem.



(22) ELECTRIC VOLUME

The electric volume is within voltage converting circuit and the brightness of LCD can be controlled by adjusting V_{LCD} level with command.

The LCD driving voltage V_{LCD} is generated by selecting 1 level within 128 step electric volume controlled levels by setting 7 bit electric volume register.

(23) VOLTAGE REGULATOR CIRCUIT

The voltage regulator circuit is within voltage converting circuit and generates regulated voltage using V_{REF} input with magnification by adjusting internal resistor. The generated voltage by voltage regulator is output at V_{REG} terminal. Even though boosted voltage variation, generated regulator voltage is stable because boosting voltage level is higher than the amplified regulator voltage V_{REG} . And so, stable voltage level can be generated even if there is load variation.

V_{REG} is used as input voltage of electric volume circuit to generate LCD driving voltage.

(24) REFERENCE VOLTAGE GENERATION CIRCUIT

The reference voltage generation circuit is within voltage converting circuit.

This circuit generates reference voltage V_{BA} terminal for using at regulator circuit through. The output voltage level from V_{BA} terminal is as following description.

$$V_{BA} = V_{EE} \times 0.9$$

The LCD driving voltages can be made by applying reference voltage to reference voltage input terminal V_{REF}.

(25) LCD DRIVING VOLTAGE GENERATION CIRCUIT

The generation circuit of LCD driving voltage is within voltage converting circuit and generates voltages V_{LCD}, V_1, V_2, V_3, V_4 by resistively dividing V_{LCD} into 4 levels.

The bias ratio of LCD driving voltages can be one of 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12.

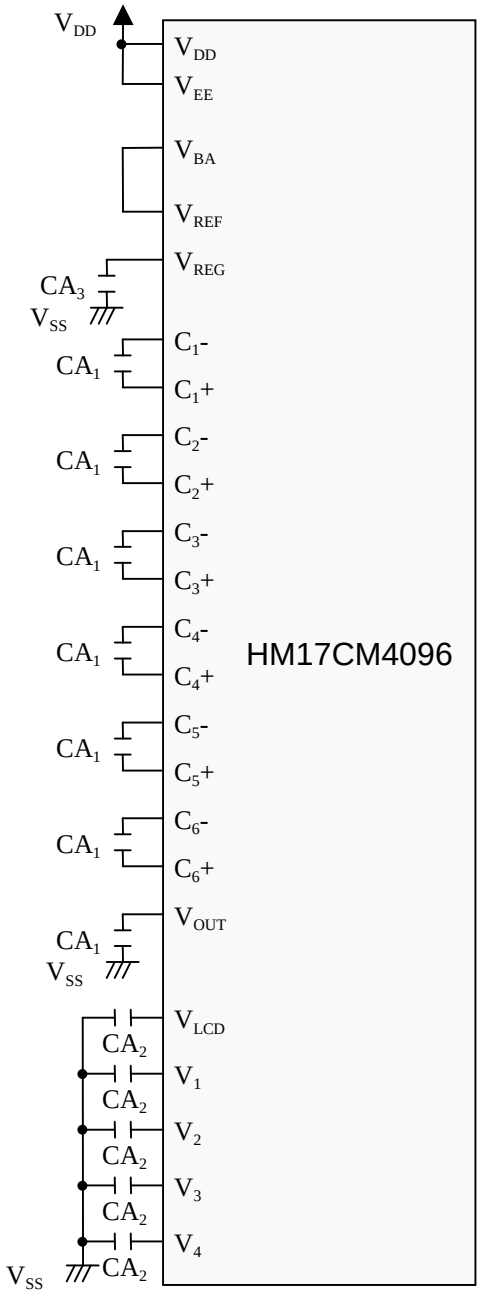
When using built-in power supply circuit, you should connect voltage stabilization capacitor CA_2 at each of LCD power terminals. There is need for selecting the coefficient of capacitor CA_2 after display the LCD.

When using external voltage supply, disable the built-in power supply circuit(AMPON, DCON='00'), supply the V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4 voltages externally and open the C_1+ , C_1- , C_2+ , C_2- , C_3+ , C_3- , C_4+ , C_4- , C_5+ , C_5- , C_6+ , C_6- , V_{EE} , V_{REF} , V_{REG} terminals.

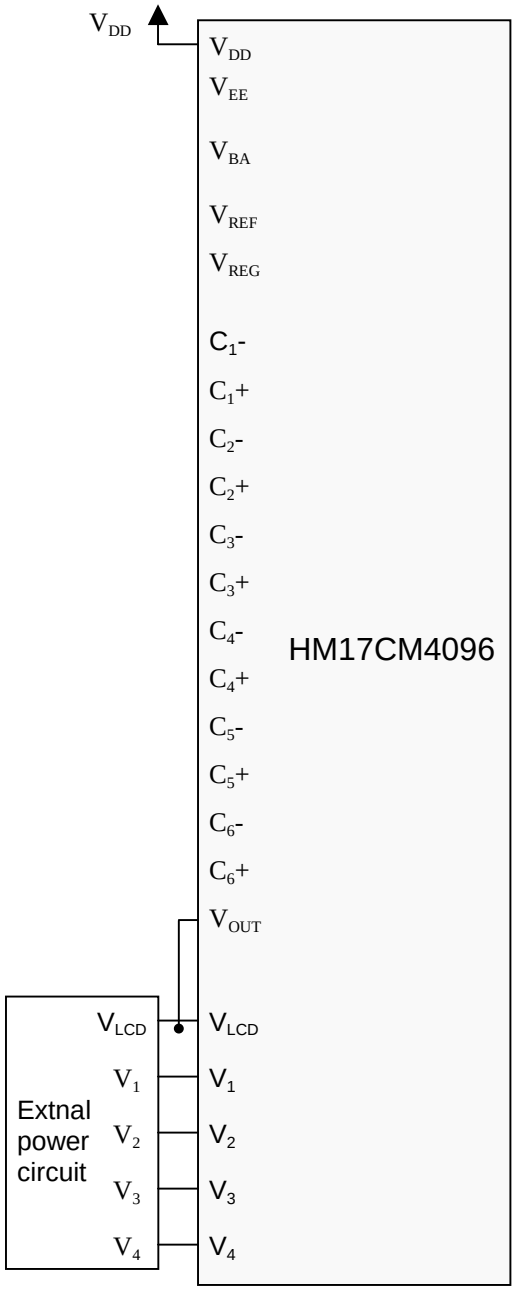
When using external voltage source and parts of built-in voltage converting circuit, the terminals of C_1+ , C_1- , C_2+ , C_2- , C_3+ , C_3- , C_4+ , C_4- , C_5+ , C_5- , C_6+ , C_6- should be open because boosting circuit is not activated, you should supply reference voltage through V_{REF} terminal and the voltage for voltage converting circuit at V_{OUT}.

Connecting stabilization capacitor CA_3 at V_{REG} terminal is recommended.

internal power circuit / internal reference voltage generating circuit are activated case.(7 times boosting)



internal power circuit is not used case

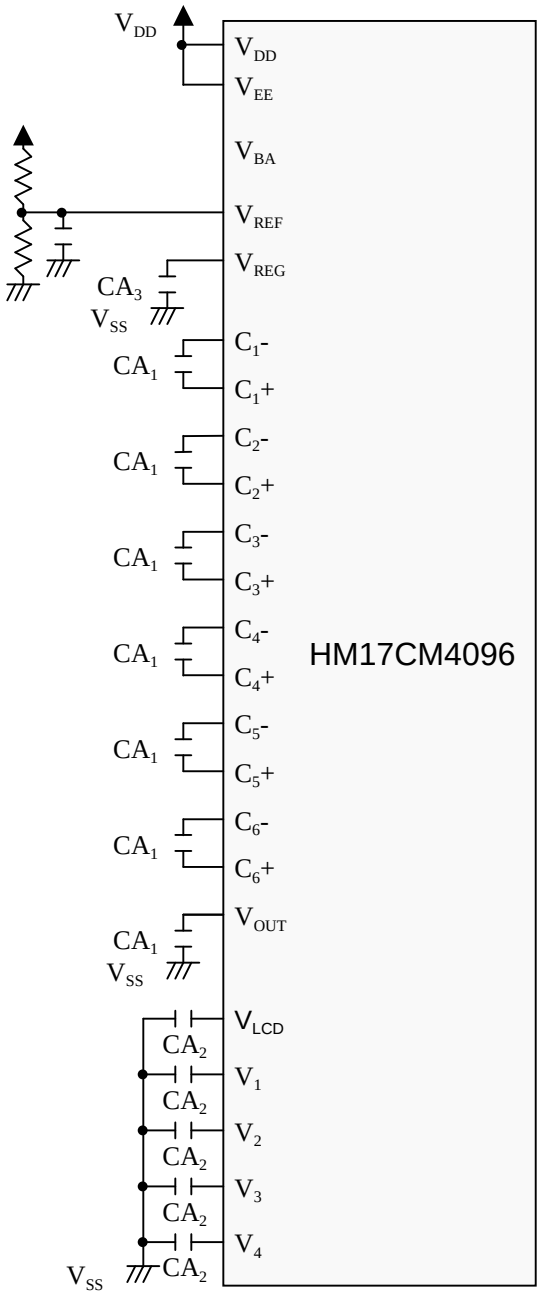


value

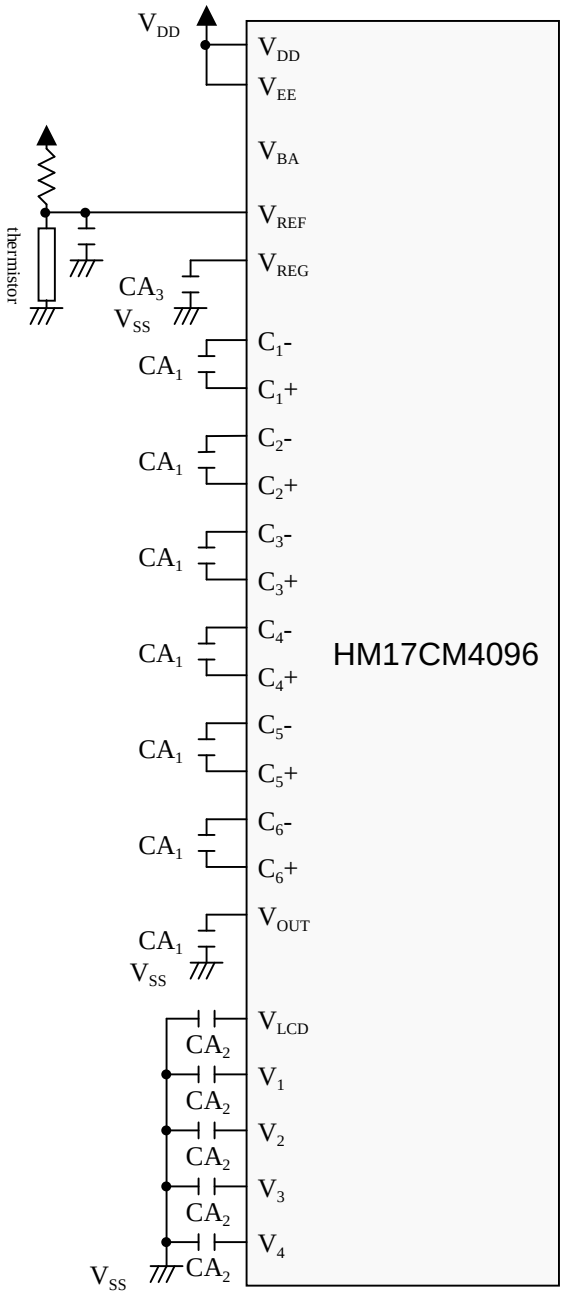
CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

Internal power circuit is used case. Reference voltage input from outside . (7 times boosting)



Internal power circuit is used case. Temperature compensation by external thermistor . (7 times boosting)

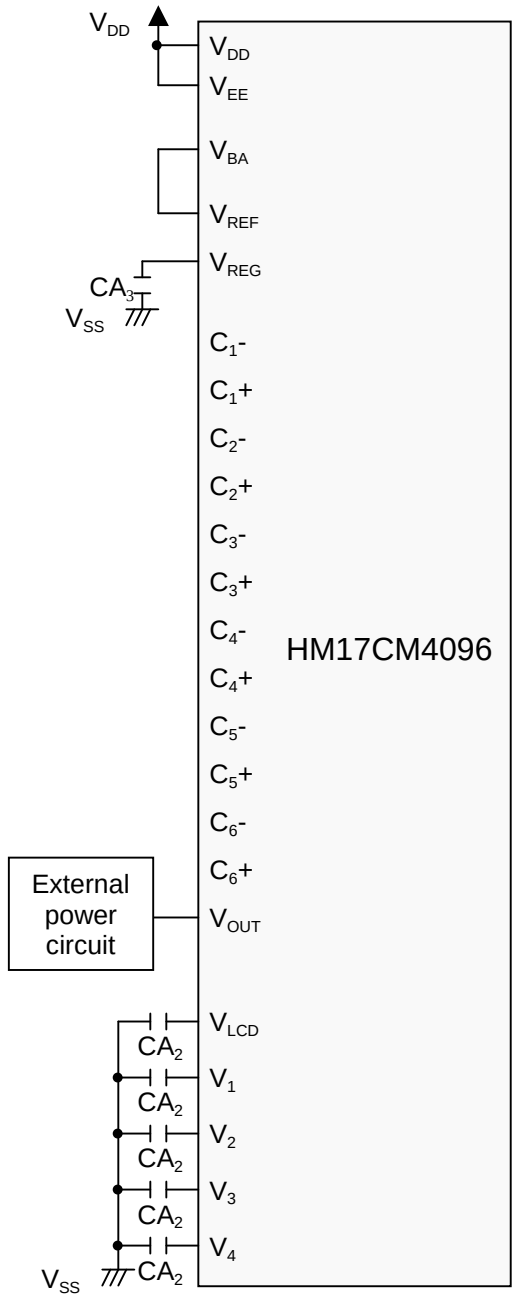


value

CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

Internal power circuit is used case. (boosting circuit is not used, V_{OUT} is supplied from outside)



value

CA_1	1.0 ~ 4.7μF
CA_2	1.0 ~ 2.2μF
CA_3	0.1μF

caution） Please use B grade capacitor.

PARTIAL DISPLAY FUNCTION

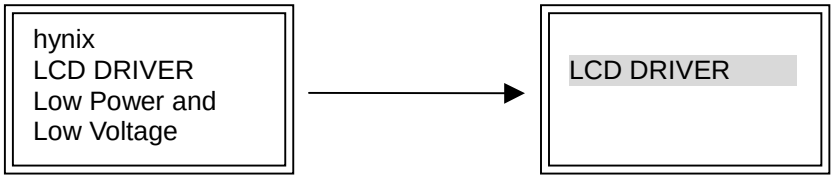
HM17CM4096 can realize the partial display at graphic display area on LCD panel.

Partial display is used with lower duty than normal state at driving.

And so, **HM17CM4096** can drive the LCD panel with lower bias ratio, lower boosting times and lower LCD driving voltages, and that can drive the LCD panel with lower power consumption.

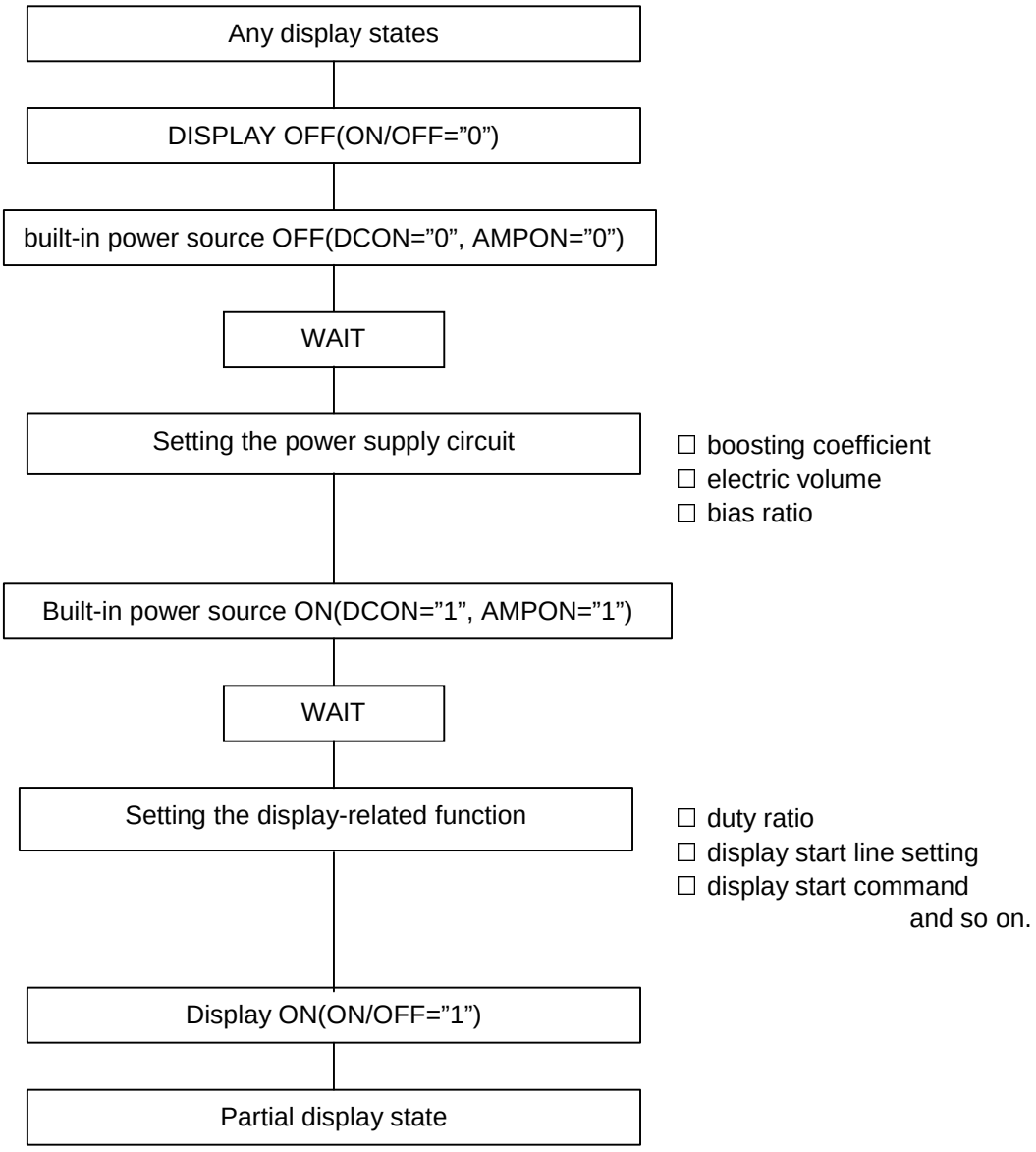
This function is suitable for calendar or clock display at mobile information apparatus.

PARTIAL DISPLAY IMAGE



Normal display　　partial display

The next sequence should be followed carefully to realize partial display function.



When using partial display function, the display duty can be selected among 1/16, 1/24, 1/32, 1/40, 1/48, 1/56, 1/64, 1/72, 1/80, 1/96, 1/112, 1/128, 1/133, 1/144, 1/160, 1/163 by setting the LCD duty set command.

The display states such as LCD driving bias ratio, LCD Driving voltage, electric volume setting value, boosting coefficient should be optimized to the selected LCD and display duty.

(26) DISCHARGE CIRCUIT

The discharge circuit of voltage(V_{LCD}, V_1~V_4) stabilization capacitor is built in the **HM17CM4096**.

To discharge the capacitors, set the DIS register to "1" or set the $\overline{RES}$ terminal to "0". When built-in power supply circuit is used, built-in power supply circuit should be disabled before discharging of the capacitor is executed. When external power supply(V_{LCD}, V_1~V_4, V_{OUT}) is used, external power supply should be turned off before discharging of the capacitor is executed. Do not turn on the internal power supply and external power supply (V_{LCD}, V_1~V_4, V_{OUT}) during discharging is executed.

(27) RESET CIRCUIT

HM17CM4096 is initialized as following description when $\overline{RES}$ terminal is set to "L".

INITIAL SETTING CONDITION (default setting)

1. display RAM :unknown
2. X address :00_H set
3. Y address :00_H set
4. display start line :1 line value 0_H
5. display ON/OFF :display OFF
6. positive/negative :positive
7. display duty ratio :1/163
8. n line inversion :n inversion disable
9. COM shift direction :$COM_0 \rightarrow COM_{161}$
10. increment mode :increment OFF
11. REF mode :positive
12. data SWAP mode :OFF
13. electric volume :(0, 0, 0, 0, 0, 0, 0)
14. power circuit :OFF
15. display mode:gradation display mode
16. bias ratio :1/9 bias
17. gradation palette 0 :(0, 0, 0, 0, 0)
18. gradation palette 1 :(0, 0, 1, 0, 1)
19. gradation palette 2 :(0, 1, 0, 1, 0)
20. gradation palette 3 :(0, 1, 1, 1, 0)
21. gradation palette 4 :(1, 0, 0, 0, 1)
22. gradation palette 5 :(1, 0, 1, 0, 1)
23. gradation palette 6 :(1, 1, 0, 1, 0)
24. gradation palette 7 :(1, 1, 1, 1, 1)
25. gradation mode :variable mode
26. GLSB :"0"
27. RAM data length :8 bit mode
28. discharge register :"0"

Usually $\overline{RES}$ terminal is connected reset terminal of CPU, so that the chip can be initialized simultaneously with CPU. **HM17CM4096** should be initialized when the power is on.

(28) SUPPLYING POWER AND ON/OFF SEQUENCE

Special care should be taken to the next notice. Supplying the power at LCD driving voltage terminal when the logic VDD is floating can cause over-current and damage the IC

(28-1) WHEN USING EXTERNAL POWER SUPPLY

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal, and then turn on the LCD driving voltage at the terminals (V_{LCD}, V_1, V_2, V_3, V_4).

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

- power OFF sequence

Execute HALT command or reset the IC to turn off the outputs of LCD driving output port, and then turn off the LCD driving voltage after logic power OFF.

Inserting series resistor of 50 ~100Ω or fuse at V_{LCD} or V_{OUT} terminal (when only internal voltage converting circuit is used) is recommended to prevent over-current.

This series resistor should be selected carefully because image quality can be dependent on.

(28-2) WHEN USING BUILT-IN POWER SUPPLY CIRCUIT

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal or after supplying power through voltage common port (V_{EE}) of boosting voltage generation and then operate internal power circuit by command.

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

You should turn on the display after the output level of internal power module is set.

If you do not keep this sequence, LCD can display wrong data.

- power OFF sequence

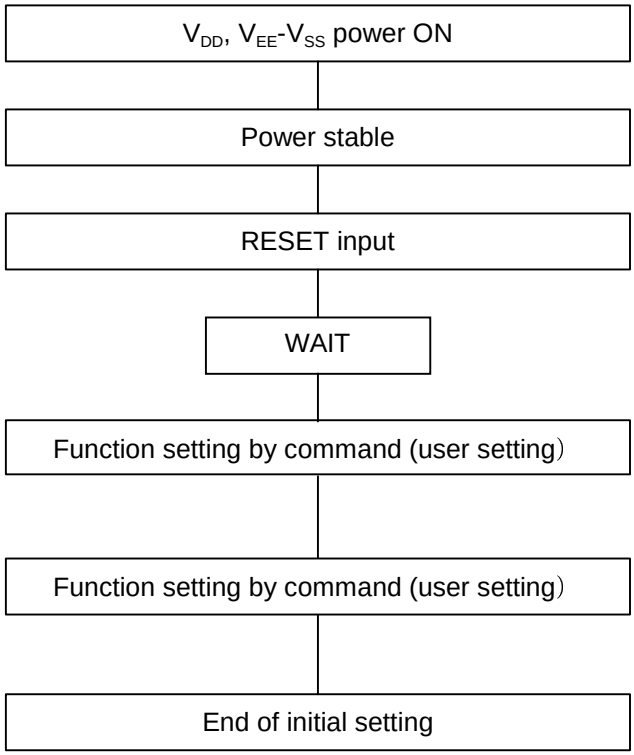
To make off state of LCD driving output, cut the source to voltage common port (V_{EE}) of boosting voltage generation, the logic power at V_{DD} terminal after reset the IC by HALT command.

If V_{EE}, and V_{DD} are supplied from different power source, V_{EE} terminal should be turned on/off during V_{DD} terminal voltage maintain voltage level specified in specification sheet.

Specially, when turn off the power, after cut the source to voltage common port (V_{EE}), and then turn off the logic power at V_{DD} terminal after the voltage levels of V_{EE}, V_{OUT}, V_{LCD}, V_1~V_4 become under LCD on voltage(LCD threshold voltage)level.

(29) COMMAND SETTING EXAMPLE

(29-1) initial setting

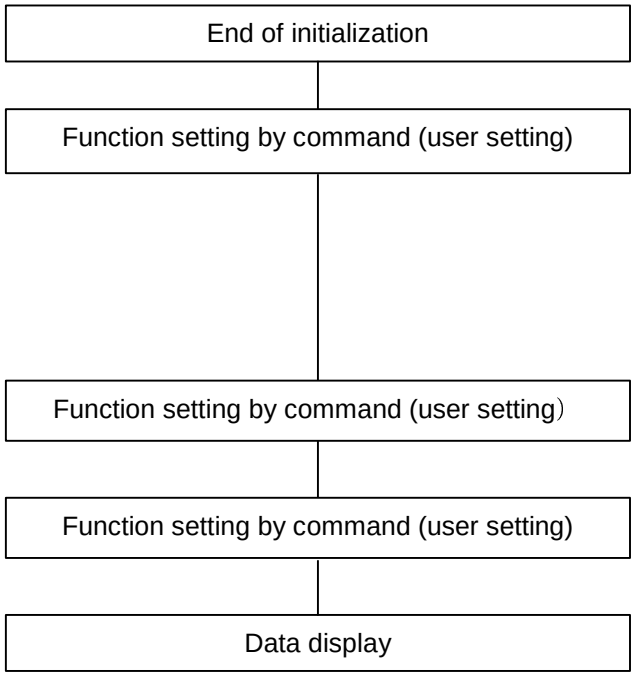


☐ electric volume code set
☐ bias ratio set

☐ power control set
(DCON="1", AMPON="1")

(notice) If the voltage level of VEE and VDD are different, VDD should be inputted first.

(29-2) DATA DISPLAY

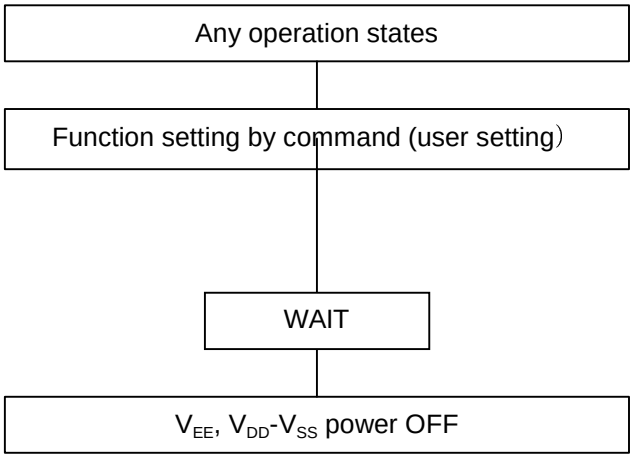


☐ display start line set
☐ increment mode set
☐ X address set
☐ Y address set

☐ display data write

☐ display ON/OFF command set(ON/OFF="1")

(29-3) POWER OFF



HALT command set or reset operation
(all LCD driver output is V_{SS} level)
Discharge command set
(discharge of V_{LCD}, V_1~V_4 capacitor)

Before turning off the power, be sure to execute HALT or RESET command to make LCD driver output OFF state.

Please, discharge the capacitors that connected to VLCD, V1, V2, V3,V4 before power OFF.

(30) INSTRUCTION

INSTRUCTION TABLE (1)

INSTRUCTION	CODE(80 series I/F)				RE flag			Register address				Control address				function
	CS	RS	RD	WR	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
X address(lower)	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Write in to display RAM
X address(upper)	0	1	1	0	0	0	0	0	0	0	1	*	AX6	AX5	AX4	
Y address(lower)	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	表示RAMのYｱﾄﾞﾚｽを□□□
Y address(upper)	0	1	1	0	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	
display start line set (lower)	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	RAM Y address setting corresponds to scan start line of common driver.
display start line set (upper)	0	1	1	0	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	
N line inversion set (lower)	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	quantity setting of line inversion
N line inversion set (upper)	0	1	1	0	0	0	0	0	1	1	1	N7	N6	N5	N4	
display control (1)	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: common shift direction set, MON: BW/gradation display, ALLON: all on , ON/OFF: display ON/OFF control
display control (2)	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: display positive / negative, NLIN: n line inversion ON/OFF, SWAP: display data swap, REF: segment positive / negative
increment control	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: window selection, AIM: increment timing selection, AYI:Y increment, AXI:X increment
power control	0	1	1	0	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: internal OP Amp. ON, HALT: power save DCON: boosting circuit ON, ACL: reset
LCD duty set	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	LCD driver duty ratio set
boosting coefficient set	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Boosting times set
bias ratio set	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	LCD drive bias set
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (2)

INSTRUCTION	CODE(80 series I/F)				RE flag			Register address				Control address				function
	CS	RS	RD	WR	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette R0/R8 set (lower)	0	1	1	0	0	0	1	0	0	0	0	PR03	PR02	PR01	PR00	Set gradation palette R0 or R8
Gradation palette R0/R8 set (upper)	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PR04	
Gradation palette R1/R9 set (lower)	0	1	1	0	0	0	1	0	0	1	0	PR13	PR12	PR11	PR10	Set gradation palette R1 or R9
Gradation palette R1/R9 set (upper)	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PR14	
Gradation palette R2/R10 set (lower)	0	1	1	0	0	0	1	0	1	0	0	PR23	PR22	PR21	PR20	Set gradation palette R2 or R10
Gradation palette R2/R10 set (upper)	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PR24	
Gradation palette R3/R11 set (lower)	0	1	1	0	0	0	1	0	1	1	0	PR33	PR32	PR31	PR30	Set gradation palette R3 or R11
Gradation palette R3/R11 set (upper)	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PR34	
Gradation palette R4/R12 set (lower)	0	1	1	0	0	0	1	1	0	0	0	PR43	PR42	PR41	PR40	Set gradation palette R4 or R12
Gradation palette R4/R12 set (upper)	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PR44	
Gradation palette R5/R13 set (lower)	0	1	1	0	0	0	1	1	0	1	0	PR53	PR52	PR51	PR50	Set gradation palette R5 or R13
Gradation palette R5/R13 set (upper)	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PR54	
Gradation palette R6/R14 set (lower)	0	1	1	0	0	0	1	1	1	0	0	PR63	PR62	PR61	PR60	Set gradation palette R6 or R14
Gradation palette R6/R14 set (upper)	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PR64	
Gradation palette R7/R15 set (lower)	0	1	1	0	0	1	0	0	0	0	0	PR73	PR72	PR71	PR70	Set gradation palette R7 or R15
Gradation palette R7/R15 set (upper)	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PR74	
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set
Gradation palette G0/G8 set (lower)	0	1	1	0	0	1	0	0	0	1	0	PG03	PG02	PG01	PG00	Set gradation palette G0 or G8
Gradation palette G0/G8 set (upper)	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PG04	
Gradation palette G1/G9 set (lower)	0	1	1	0	0	1	0	0	1	0	0	PG13	PG12	PG11	PG10	Set gradation palette G1 or G9
Gradation palette G1/G9 set (upper)	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PG14	
Gradation palette G2/G10 set (lower)	0	1	1	0	0	1	0	0	1	1	0	PG23	PG22	PG21	PG20	Set gradation palette G2 or G10
Gradation palette G2/G10 set (upper)	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PG24	
Gradation palette G3/G11 set (lower)	0	1	1	0	0	1	0	1	0	0	0	PG33	PG32	PG31	PG30	Set gradation palette G3 or G11
Gradation palette G3/G11 set (upper)	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PG34	
Gradation palette G4/G12 set (lower)	0	1	1	0	0	1	0	1	0	1	0	PG43	PG42	PG41	PG40	Set gradation palette G4 or G12
Gradation palette G4/G12 set (upper)	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PG44	
Gradation palette G5/G13 set (lower)	0	1	1	0	0	1	0	1	1	0	0	PG53	PG52	PG51	PG50	Set gradation palette G5 or G13
Gradation palette G5/G13 set (upper)	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PG54	
Gradation palette G6/G14 set (lower)	0	1	1	0	0	1	1	0	0	0	0	PG63	PG62	PG61	PG60	Set gradation palette G6 or G14
Gradation palette G6/G14 set (upper)	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PG64	
Gradation palette G7/G15 set (lower)	0	1	1	0	0	1	1	0	0	1	0	PG73	PG72	PG71	PG70	Set gradation palette G7 or G15
Gradation palette G7/G15 set (upper)	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PG74	
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) The commands that upper/lower register settings are demanded are effective at the point of commands input.

But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (3)

INSTRUCTION	CODE(80 series I/F)				RE flag			Register address				Control address				function
	CS	RS	RD	WR	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette B0/B8 set (lower)	0	1	1	0	0	1	1	0	1	0	0	PB03	PB02	PB01	PB00	Set gradation palette B0 or B8
Gradation palette B0/B8 set (upper)	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PB04	
Gradation palette B1/B9 set (lower)	0	1	1	0	0	1	1	0	1	1	0	PB13	PB12	PB11	PB10	Set gradation palette B1 or B9
Gradation palette B1/B9 set (upper)	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PB14	
Gradation palette B2/B10 set (lower)	0	1	1	0	0	1	1	1	0	0	0	PB23	PB22	PB21	PB20	Set gradation palette B2 or B10
Gradation palette B2/B10 set (upper)	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PB24	
Gradation palette B3/B11 set (lower)	0	1	1	0	0	1	1	1	0	1	0	PB33	PB32	PB31	PB30	Set gradation palette B3 or B11
Gradation palette B3/B11 set (upper)	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PB34	
Gradation palette B4/B12 set (lower)	0	1	1	0	0	1	1	1	1	0	0	PB43	PB42	PB41	PB40	Set gradation palette B4 or G12
Gradation palette B4/B12 set (upper)	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PB44	
Gradation palette B5/B13 set (lower)	0	1	1	0	1	0	0	0	0	0	0	PB53	PB52	PB51	PB50	Set gradation palette B5 or B13
Gradation palette B5/B13 set (upper)	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PB54	
Gradation palette B6/B14 set (lower)	0	1	1	0	1	0	0	0	0	1	0	PB63	PB62	PB61	PB60	Set gradation palette B6 or B14
Gradation palette B6/B14 set (upper)	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PB64	
Gradation palette B7/B15 set (lower)	0	1	1	0	1	0	0	0	1	0	0	PB73	PB72	PB71	PB70	Set gradation palette B7 or B15
Gradation palette B7/B15 set (upper)	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PB74	
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (4)

INSTRUCTION	CODE(80 series I/F)				RE flag			Register address				Control address				function
	CS	RS	RD	WR	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Display start command set	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Common driver scan start set
Display signal output set	0	1	1	0	1	0	0	0	1	1	1	*	*	*	SON	Control of outputs status of CKL, CL, FLM, FR 0CKL, CL, FLM, FR="L"(default) 1CKL, CL, FLM, FR="H"
Display selection control	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM：variable 16 /fixed 8 gray mode selection C256：256 color Mode ON/OFF(default : OFF) FDC：boost clock control
RAM data length	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW：high speed write in at 8 bit access mode ABS：effective 12 bit RAM selection CKS：oscillator selection WLS：RAM access length 8 /16 bit
Electric volume control (lower)	0	1	1	0	1	0	0	1	0	1	0	DV3				DV2
Electric volume control (upper)	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	
Address set for internal address reading	0	1	1	0	1	0	0	1	1	0	0	Address for register read				Internal register read out
Oscillator Rf control	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	RF：oscillator Rf selection
discharge	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Cap. Of VLCD, V1～V4 discharge
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set
Window end X address set (lower)	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	X end address under window mode
Window end X address set (upper)	0	1	1	0	1	0	1	0	0	0	1	*	EX6	EX5	EX4	
Window end Y address set (lower)	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Y end address under window mode
Window end Y address set (upper)	0	1	1	0	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	
Line inversion start address (lower)	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Start line address set under line inversion mode
Line inversion start address (upper)	0	1	1	0	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	
Line inversion end address (lower)	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	End line address set under line inversion mode
Line inversion end address (upper)	0	1	1	0	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	
Line inversion control	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT: blink type set LREV: line inversion ON/OFF
Gradation palette setting selection	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	Upper/lower 8 gradation palette
PWM mode control	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	PWM mode selection
RE register set	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST	RE2	RE1	RE0	RE flag set

*Notice 1) * mark is Don't Care*
Notice 2) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

■ RELATION BETWEEN PS REGISTER AND GRADATION PALETTE (1)

Gradation palette	Upper / lower	RE register			PS register	Setting register address	Gradation palette control register			
		RE2	RE1	RE0			D3	D2	D1	D0
R0	Lower	0	0	1	0	00h	PR03	PR02	PR01	PR00
	Upper	0	0	1	0	01h	*	*	*	PR04
R1	Lower	0	0	1	0	02h	PR13	PR12	PR11	PR10
	Upper	0	0	1	0	03h	*	*	*	PR14
R2	Lower	0	0	1	0	04h	PR23	PR22	PR21	PR20
	Upper	0	0	1	0	05h	*	*	*	PR24
R3	Lower	0	0	1	0	06h	PR33	PR32	PR31	PR30
	Upper	0	0	1	0	07h	*	*	*	PR34
R4	Lower	0	0	1	0	08h	PR43	PR42	PR41	PR40
	Upper	0	0	1	0	09h	*	*	*	PR44
R5	Lower	0	0	1	0	0Ah	PR53	PR52	PR51	PR50
	Upper	0	0	1	0	0Bh	*	*	*	PR54
R6	Lower	0	0	1	0	0Ch	PR63	PR62	PR61	PR60
	Upper	0	0	1	0	0Dh	*	*	*	PR64
R7	Lower	0	1	0	0	00h	PR73	PR72	PR71	PR70
	Upper	0	1	0	0	01h	*	*	*	PR74
R8	Lower	0	0	1	1	00h	PR03	PR02	PR01	PR00
	Upper	0	0	1	1	01h	*	*	*	PR04
R9	Lower	0	0	1	1	02h	PR13	PR12	PR11	PR10
	Upper	0	0	1	1	03h	*	*	*	PR14
R10	Lower	0	0	1	1	04h	PR23	PR22	PR21	PR20
	Upper	0	0	1	1	05h	*	*	*	PR24
R11	Lower	0	0	1	1	06h	PR33	PR32	PR31	PR30
	Upper	0	0	1	1	07h	*	*	*	PR34
R12	Lower	0	0	1	1	08h	PR43	PR42	PR41	PR40
	Upper	0	0	1	1	09h	*	*	*	PR44
R13	Lower	0	0	1	1	0Ah	PR53	PR52	PR51	PR50
	Upper	0	0	1	1	0Bh	*	*	*	PR54
R14	Lower	0	0	1	1	0Ch	PR63	PR62	PR61	PR60
	Upper	0	0	1	1	0Dh	*	*	*	PR64
R15	Lower	0	1	0	1	00h	PR73	PR72	PR71	PR70
	Upper	0	1	0	1	01h	*	*	*	PR74
G0	Lower	0	1	0	0	02h	PG03	PG02	PG01	PG00
	Upper	0	1	0	0	03h	*	*	*	PG04
G1	Lower	0	1	0	0	04h	PG13	PG12	PG11	PG10
	Upper	0	1	0	0	05h	*	*	*	PG14
G2	Lower	0	1	0	0	06h	PG23	PG22	PG21	PG20
	Upper	0	1	0	0	07h	*	*	*	PG24
G3	Lower	0	1	0	0	08h	PG33	PG32	PG31	PG30
	Upper	0	1	0	0	09h	*	*	*	PG34
G4	Lower	0	1	0	0	0Ah	PG43	PG42	PG41	PG40
	Upper	0	1	0	0	0Bh	*	*	*	PG44
G5	Lower	0	1	0	0	0Ch	PG53	PG52	PG51	PG50
	Upper	0	1	0	0	0Dh	*	*	*	PG54
G6	Lower	0	1	1	0	00h	PG63	PG62	PG61	PG60
	Upper	0	1	1	0	01h	*	*	*	PG64
G7	Lower	0	1	1	0	02h	PG73	PG72	PG71	PG70
	Upper	0	1	1	0	03h	*	*	*	PG74

■ RELATION BETWEEN PS REGISTER AND GRADATION PALETTE (2)

Gradation palette	Upper / lower	RE register			PS register	Setting register address	Gradation palette control register			
		RE2	RE1	RE0			D3	D2	D1	D0
G8	Lower	0	1	0	1	02h	PG03	PG02	PG01	PG00
	Upper	0	1	0	1	03h	*	*	*	PG04
G9	Lower	0	1	0	1	04h	PG13	PG12	PG11	PG10
	Upper	0	1	0	1	05h	*	*	*	PG14
G10	Lower	0	1	0	1	06h	PG23	PG22	PG21	PG20
	Upper	0	1	0	1	07h	*	*	*	PG24
G11	Lower	0	1	0	1	08h	PG33	PG32	PG31	PG30
	Upper	0	1	0	1	09h	*	*	*	PG34
G12	Lower	0	1	0	1	0Ah	PG43	PG42	PG41	PG40
	Upper	0	1	0	1	0Bh	*	*	*	PG44
G13	Lower	0	1	0	1	0Ch	PG53	PG52	PG51	PG50
	Upper	0	1	0	1	0Dh	*	*	*	PG54
G14	Lower	0	1	1	1	00h	PG63	PG62	PG61	PG60
	Upper	0	1	1	1	01h	*	*	*	PG64
G15	Lower	0	1	1	1	02h	PG73	PG72	PG71	PG70
	Upper	0	1	1	1	03h	*	*	*	PG74
B0	Lower	0	1	1	0	04h	PB03	PB02	PB01	PB00
	Upper	0	1	1	0	05h	*	*	*	PB04
B1	Lower	0	1	1	0	06h	PB13	PB12	PB11	PB10
	Upper	0	1	1	0	07h	*	*	*	PB14
B2	Lower	0	1	1	0	08h	PB23	PB22	PB21	PB20
	Upper	0	1	1	0	09h	*	*	*	PB24
B3	Lower	0	1	1	0	0Ah	PB33	PB32	PB31	PB30
	Upper	0	1	1	0	0Bh	*	*	*	PB34
B4	Lower	0	1	1	0	0Ch	PB43	PB42	PB41	PB40
	Upper	0	1	1	0	0Dh	*	*	*	PB44
B5	Lower	1	0	0	0	00h	PB53	PB52	PB51	PB50
	Upper	1	0	0	0	01h	*	*	*	PB54
B6	Lower	1	0	0	0	02h	PB63	PB62	PB61	PB60
	Upper	1	0	0	0	03h	*	*	*	PB64
B7	Lower	1	0	0	0	04h	PB73	PB72	PB71	PB70
	Upper	1	0	0	0	05h	*	*	*	PB74
B8	Lower	0	1	1	1	04h	PB03	PB02	PB01	PB00
	Upper	0	1	1	1	05h	*	*	*	PB04
B9	Lower	0	1	1	1	06h	PB13	PB12	PB11	PB10
	Upper	0	1	1	1	07h	*	*	*	PB14
B10	Lower	0	1	1	1	08h	PB23	PB22	PB21	PB20
	Upper	0	1	1	1	09h	*	*	*	PB24
B11	Lower	0	1	1	1	0Ah	PB33	PB32	PB31	PB30
	Upper	0	1	1	1	0Bh	*	*	*	PB34
B12	Lower	0	1	1	1	0Ch	PB43	PB42	PB41	PB40
	Upper	0	1	1	1	0Dh	*	*	*	PB44
B13	Lower	1	0	0	1	00h	PB53	PB52	PB51	PB50
	Upper	1	0	0	1	01h	*	*	*	PB54
B14	Lower	1	0	0	1	02h	PB63	PB62	PB61	PB60
	Upper	1	0	0	1	03h	*	*	*	PB64
B15	Lower	1	0	0	1	04h	PB73	PB72	PB71	PB70
	Upper	1	0	0	1	05h	*	*	*	PB74

■ ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	CONDITION	PORT	RATINGS	UNIT
supply voltage (1)	V_{DD}	V_{SS}(0V) reference Ta = +25°C	V_{DD}	-0.3 ~ +4.0	V
supply voltage (2)	V_{EE}		V_{EE}	-0.3 ~ +4.0	V
supply voltage (3)	V_{OUT}		V_{OUT}	-0.3 ~ +20.0	V
supply voltage (4)	V_{REG}		V_{REG}	-0.3 ~ +20.0	V
supply voltage (5)	V_{LCD}		V_{LCD}	-0.3 ~ +20.0	V
supply voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 ~ V_{LCD} + 0.3	V
input voltage	V_I		*1	-0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}			-45 ~ +125	°C

*1 D_0~D_{15}, $\overline{CS}$, RS, M/S, $\overline{RD}$, $\overline{WR}$, OSC_1, LP, FLM, FR, CLK, $\overline{RES}$, TEST port

■ RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	PORT	MIN	TYP	MAX	UNIT	REMARK
supply voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Recommended operating voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			V_{OUT} x 0.9	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operation temperature	T_{opr}		-30		85	°C	

*1 The case when internal reference voltage generation circuit (V_{BA} output) is not used.
The voltage compare to V_{SS} port.

*2 The case when internal reference voltage generation circuit (V_{BA} output) is used.
The voltage compare to V_{SS} port.

*3 When the boosting circuit is used, supply voltage V_{EE} should be used within the limit.
When driving LCD panel by use of internal boosting circuit, it is possible to short V_{DD} and V_{EE}.

*4 Please keep the relation, $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} \leq V_{OUT}$.

*5 When the internal voltage regulator circuit is used, reference voltage V_{REF} should be used within the limit. Please keep the relation $V_{REF} \leq V_{EE}$.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics 1

Unless otherwise noted V_{SS} = 0V, V_{DD} = +1.7~+3.3V, Ta = -30~+85°C

ITEM	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	PORT
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.22 V_{DD}	V	
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	
Input leakage current	IL_I	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	IL_O	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
LCD driver output ON resistance	R_{ON1}	|Δ V_{ON}| = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Static current	I_{STB}	$\overline{CS}$=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Oscillator frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C	FFL = "0" (normal mode)	625	763	900	kHz	*8
	f_{OSC2}			141	172	203		*9
	f_{OSC3}			20.5	25	29.5		*10
oscillator frequency by External resistor	fr_1	Rf=10kΩ			750		kHz	*11
	fr_2	Rf=51kΩ			185			
	fr_3	Rf=390kΩ			27.2			
Boosting output voltage	V_{OUT}	N x boosting (N=2~7) RL =500kΩ (between V_{OUT} ,V_{SS})		N * V_{EE} * 0.95			V	*12
Current consumption (1)	I_{DD1}	V_{DD} = 2.5V 7 x boosting (all ON)			870	1300	µA	*13
Current consumption (2)	I_{DD3}	V_{DD} = 2.5V 7x boosting (cross check)			1060	1590		
Current consumption (3)	I_{DD5}	V_{DD} = 3.0V 6 x boosting (all ON)			760	1140		
Current consumption (4)	I_{DD7}	V_{DD} = 3.0V 6x boosting (cross check)			930	1400		
Current consumption (5)	I_{DD9}	V_{DD} = 3.0V5 x boosting (all ON)			520	780		
Current consumption (6)	I_{DD11}	V_{DD} = 3.0V 5x boosting (cross check)			650	980		
Current consumption (7)	I_{DD13}	V_{DD} = 3.0V 4 x boosting (all ON)			360	540		
Current consumption (8)	I_{DD15}	V_{DD} = 3.0V 4x boosting (cross check)			450	680		
V_{BA} output voltage	V_{BA}	V_{EE} = 2.4~3.3V		(0.9 V_{EE}) × 0.98	0.9 V_{EE}	(0.9 V_{EE}) × 1.02	V	*14
V_{REG} output voltage	V_{REG}	V_{EE} = 2.4~3.3V V_{REF} = 0.9 × V_{EE} N × boosting (N=2~7)		(V_{REF} × N) × 0.97	(V_{REF} x N)	(V_{REF} × N) × 1.03	V	*15
Output voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100	mV	
	V_{D12}			-30	0	+30	mV	
	V_{D34}			-30	0	+30	mV	

Applied port (* Remark Solves)

*1 D_0~D_{15}, $\overline{CS}$, RS, M/S, $\overline{RD}$, $\overline{WR}$, P/S, SEL68, CLK, CL, FLM, FR, $\overline{RES}$ ports

*2 D_0~D_{15} ports

*3 CL, FLM, FR, CLK ports

*4 $\overline{CS}$, RS, M/S, SEL68, $\overline{RD}$, $\overline{WR}$, P/S, $\overline{RES}$, OSC_1 ports

*5 applicable at D_0~D_{15}, CL, FLM, FR, CLK = high impedance state

*6 $SEGA_0$~$SEGA_{127}$, $SEGB_0$~$SEGB_{127}$, $SEGC_0$~$SEGC_{127}$, COM_0~COM_{79}, $COMI_0$, $COMI_1$ ports
resistance when being supplied 0.5V between each output ports and power port ($V_{LCD,}$ $V_{1,}$ $V_{2,}$ $V_{3,}$ V_4)
applicable under bias ratio = 1/9

*7 V_{DD} ports
V_{DD} current when source clock is stopped, chip selection ($\overline{CS}$=V_{DD}) is non-selection state and no load.

*8 oscillator frequency when internal oscillator circuit is used (gradation display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*9 oscillator frequency when internal oscillator circuit is used (fixed gradation display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*10 oscillator frequency when internal oscillator circuit is used (BW display mode).
applicable under Rf register of oscillator circuit, {Rf_2, Rf_1, Rf_0} = “000”

*11 VDD＝3V、Ta＝25℃

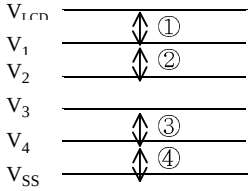
*12 V_{OUT} port
N x boosting (N=2~7). applicable under internal oscillator circuit and internal power circuit are ON state
V_{EE} = 2.4~3.3V, electric volume is MAX(“1111111”).
bias = 1/5~1/10, 1/82 duty, no load at LCD driver port.
RL = 500kΩ(between V_{OUT} ,V_{SS}), CA_1= CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”

*13 applicable under internal oscillator circuit and internal power circuit are ON state and no access from CPU.
electric volume is “1111111”.
Display is all ON and cross check pattern display (variable gradation display mode), and no load at LCD driver port.
Test condition : V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”, NLIN=”0”, 1/82 duty. Ta=25℃

*14 V_{REG} output voltage when V_{BA} output is connected to V_{REF} input, V_{REG} gain is N=1.
force VOUT=13.5V with DCON=”0”

*15 V_{REG} port
V_{EE}= 2.4~3.3V, V_{REF}= 0.9 V_{EE}, bias= 1/5~1/10, 1/82 duty, electric volume is “1111111”。
Cross check pattern state and no load at LCD driver port.
Boosting coefficient N is 2~7 times
Test condition : CA_1=CA_2=1.0μF, CA_3=0.1μF, DCON=“1”, AMPON=“1”, NLIN=”0”。

*16 V_{LCD}、V_1、V_2、V_3、V_4 port
V_{EE} = 3.0V, V_{REF} = 0.9 V_{EE}, Vout=13.5V, bias = 1/5~1/10, electric volume is “1111111”。
Display OFF and no load at LCD drive port.
Boosting coefficient N is 5 times.
Test condition : CA_2=1.0μF, CA_3=0.1μF, DCON=“0”, AMPON=“1”。

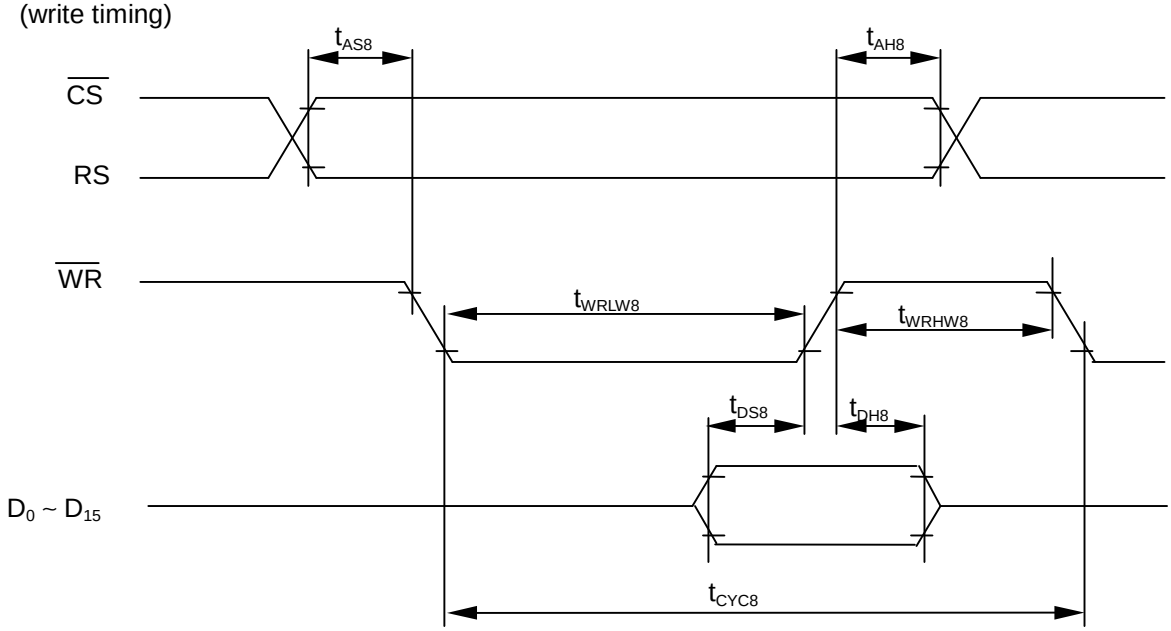


V_{D12} = ① - ②
V_{D34} = ③ - ④

■ AC CHARACTERISTICS

- SYSTEM BUS READ / WRITE TIMING (80 series CPU interface)

(write timing)



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		30 5		ns ns	D_0 ~ D_{15}

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

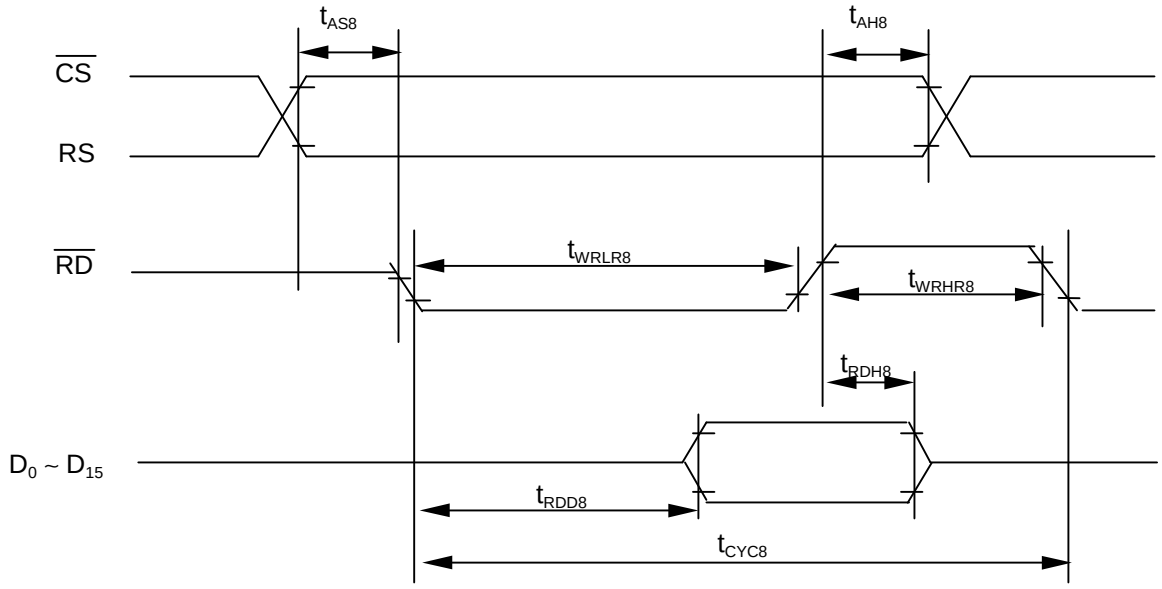
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		40 5		ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.2, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		70 10		ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

（read timing）



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write ”L” pulse width Write ”H” pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{RDD8} t_{RDH8}	C_L = 15 pF	 0	60	ns ns	D_0 ~ D_{15}

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write ”L” pulse width Write ”H” pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{RDD8} t_{RDH8}	C_L = 15 pF	 0	60	ns ns	D_0 ~ D_{15}

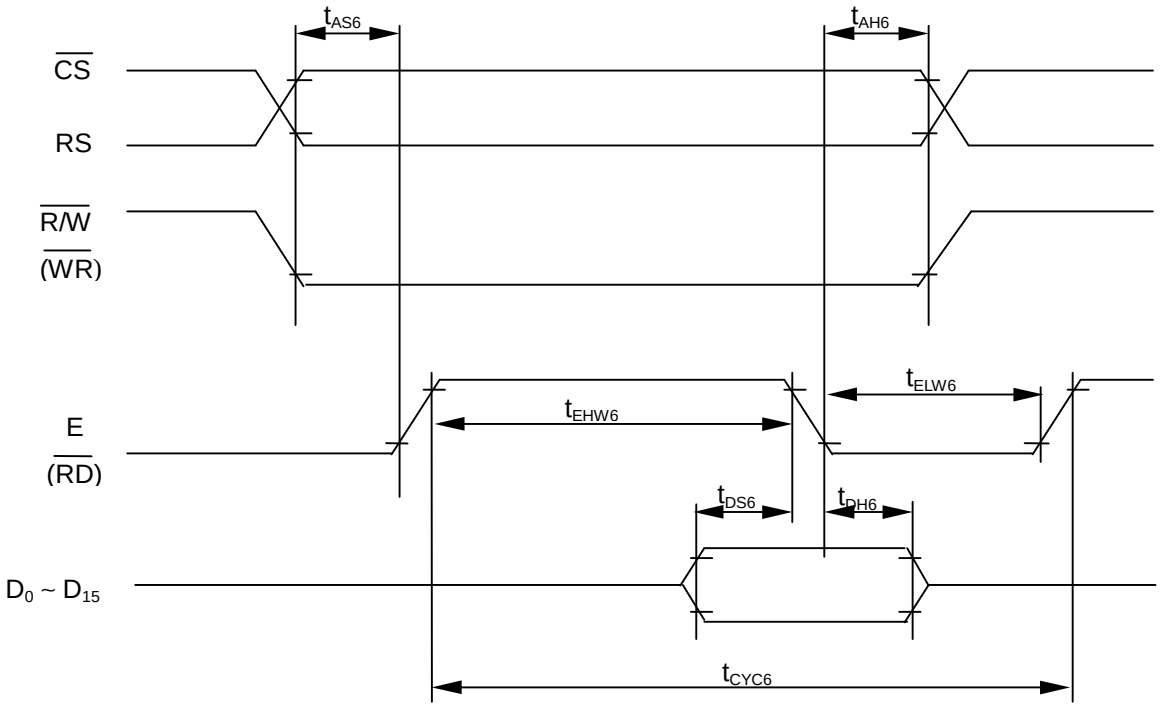
(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write ”L” pulse width Write ”H” pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	$\overline{RD}$
Data setup timing Data hold timing	t_{RDD8} t_{RDH8}	C_L = 15 pF	 0	110	ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SYSTEM BUS READ / WRITE TIMING (68 series CPU interface)

(write timing)



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup timing Data hold timing	t_{DS6} t_{DH6}		40 5		ns ns	D_0 ~ D_{15}

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

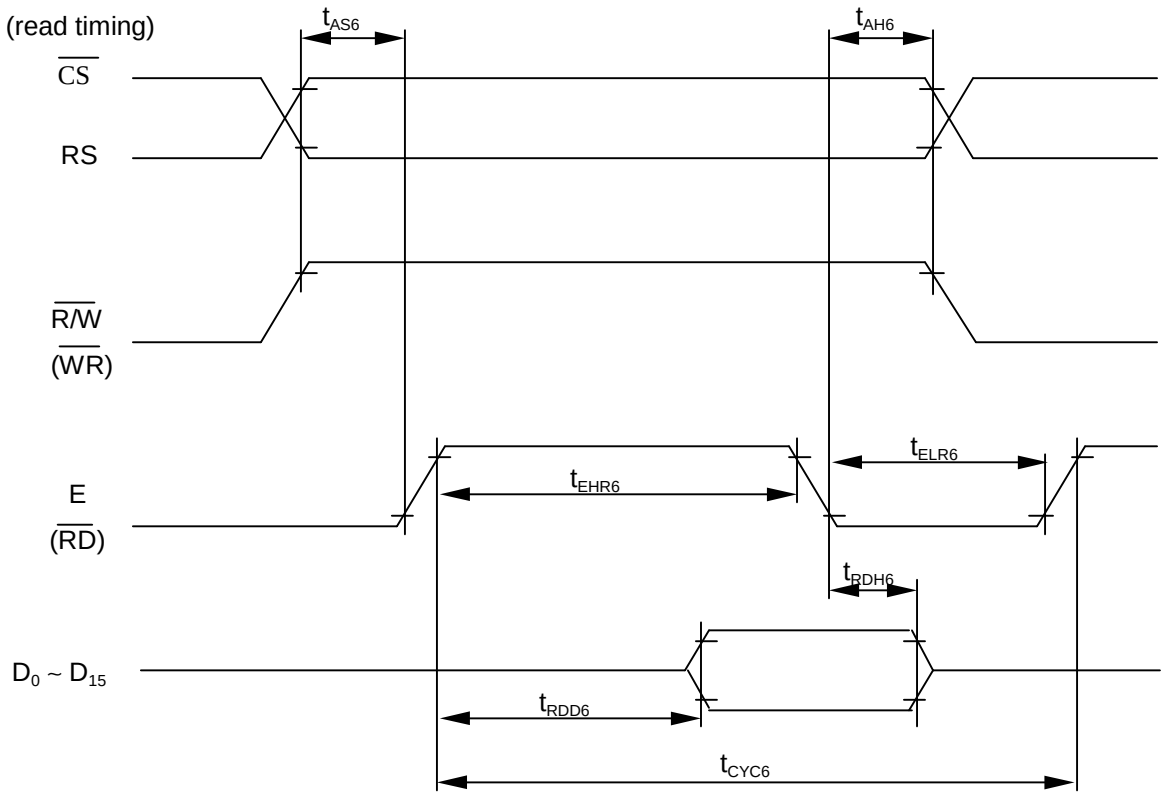
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW8}		160 70 70		ns ns ns	E
Data setup timing Data hold timing	t_{DS6} t_{DH6}		50 5		ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW8}		180 80 80		ns ns ns	E
Data setup timing Data hold timing	t_{DS6} t_{DH6}		70 10		ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

(read timing)



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Data setup timing Data hold timing	t_{RDD6} t_{RDH6}	C_L = 15 pF	 0	70	ns ns	D_0 ~ D_{15}

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

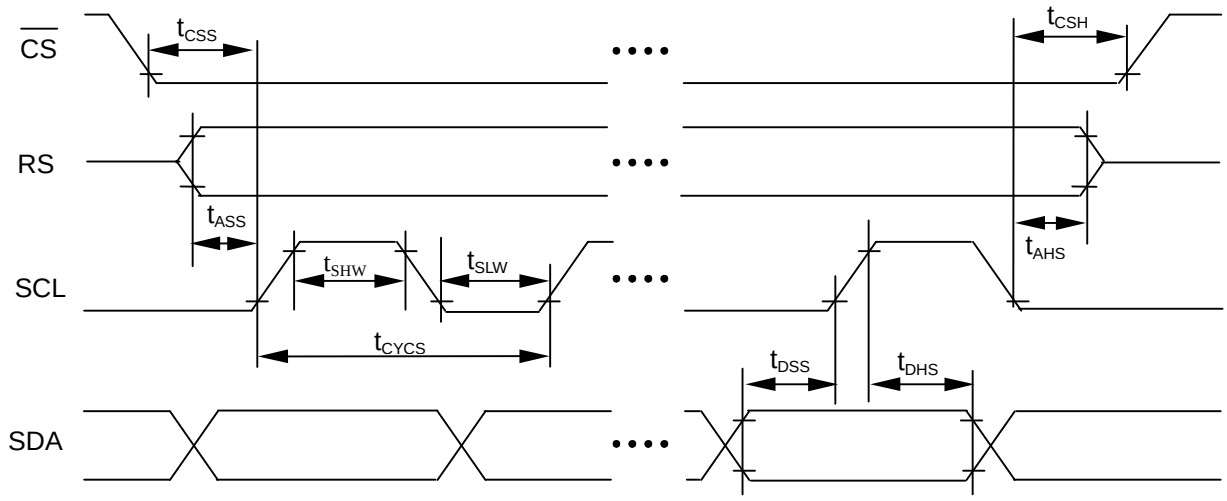
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR8}		180 80 80		ns ns ns	E
Data setup timing Data hold timing	t_{RDD6} t_{RDH6}	C_L = 15 pF	 0	70	ns ns	D_0 ~ D_{15}

(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Enable "L" pulse width Enable "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR8}		250 120 120		ns ns ns	E
Data setup timing Data hold timing	t_{RDD6} t_{RDH6}	C_L = 15 pF	 0	110	ns ns	D_0 ~ D_{15}

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SERIAL INTERFACE TIMING



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" pulse width	t_{SHW}		20		ns	
SCL "L" pulse width	t_{SLW}		20		ns	
Address setup timing	t_{ASS}		20		ns	RS
Address hold timing	t_{AHS}		20		ns	
Data setup timing	t_{DSS}		20		ns	SDA
Data hold timing	t_{DHS}		20		ns	
$\overline{CS}$ – SCL timing	t_{CSS}		20		ns	$\overline{CS}$
$\overline{CS}$ hold timing	t_{CSH}		20		ns	

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

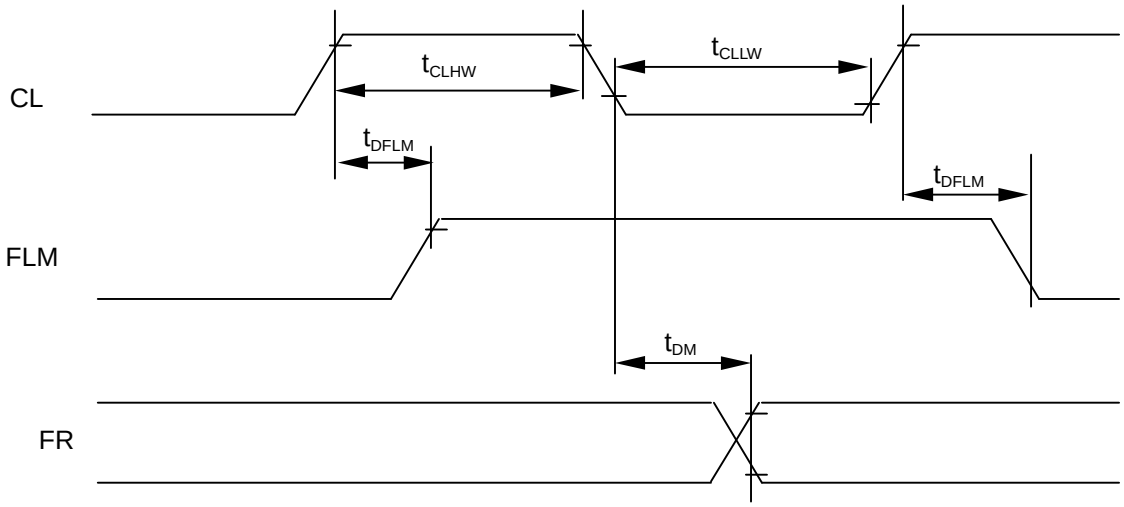
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" pulse width	t_{SHW}		20		ns	
SCL "L" pulse width	t_{SLW}		20		ns	
Address setup timing	t_{ASS}		20		ns	RS
Address hold timing	t_{AHS}		20		ns	
Data setup timing	t_{DSS}		20		ns	SDA
Data hold timing	t_{DHS}		20		ns	
$\overline{CS}$ – SCL timing	t_{CSS}		20		ns	$\overline{CS}$
$\overline{CS}$ hold timing	t_{CSH}		20		ns	

(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" pulse width	t_{SHW}		35		ns	
SCL "L" pulse width	t_{SLW}		35		ns	
Address setup timing	t_{ASS}		35		ns	RS
Address hold timing	t_{AHS}		35		ns	
Data setup timing	t_{DSS}		35		ns	SDA
Data hold timing	t_{DHS}		35		ns	
$\overline{CS}$ – SCL timing	t_{CSS}		35		ns	$\overline{CS}$
$\overline{CS}$ hold timing	t_{CSH}		35		ns	

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- DISPLAY CONTROL TIMING (normal speed , FFL=0)



OUTPUT TIMING (V_{DD}=2.4~3.3V, Ta=-30~+85°C)

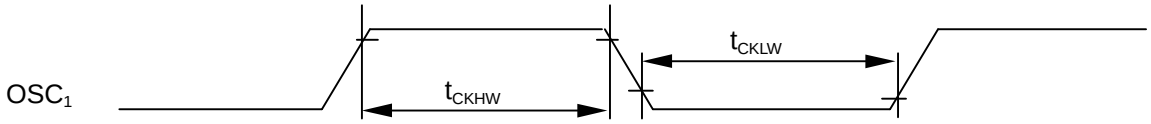
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	C_L=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR

OUTPUT TIMING (V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	C_L=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		10	1000	ns	FR

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- SOURCE CLOCK INPUT TIMING



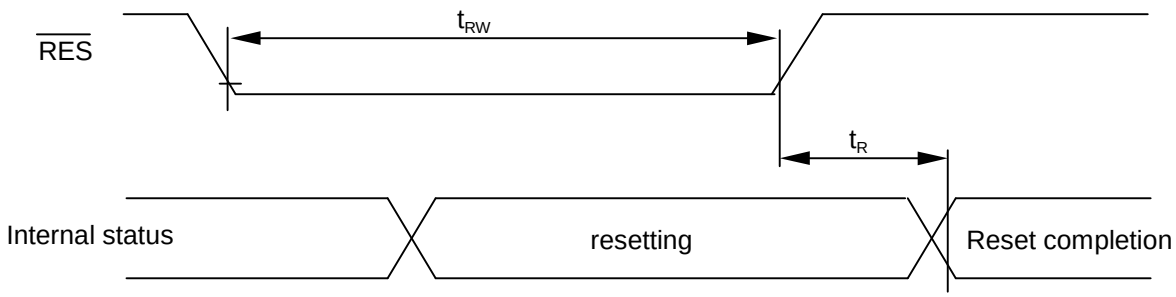
(V_{DD}=1.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC_1 "H" pulse width (1)	t_{CKHW1}		0.525	0.800	µs	OSC_1
OSC_1 "L" pulse width (1)	t_{CKLW1}		0.525	0.800	µs	∗1
OSC_1 "H" pulse width (2)	t_{CKHW2}		2.45	3.55	µs	OSC_1
OSC_1 "L" pulse width (2)	t_{CKLW2}		2.45	3.55	µs	∗2
OSC_1 "H" pulse width (3)	t_{CKHW3}		16.9	24.4	µs	OSC_1
OSC_1 "L" pulse width (3)	t_{CKLW3}		16.9	24.4	µs	∗3

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

∗1 applicable under gradation display , MON="0", PWM="0"
∗2 applicable under fixed gradation display , MON="0",PWM="1"
∗3 applicable under BW display , MON="1"

- RESET INPUT TIMING



(V_{DD}=2.4~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.0	µs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		µs	$\overline{RES}$

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

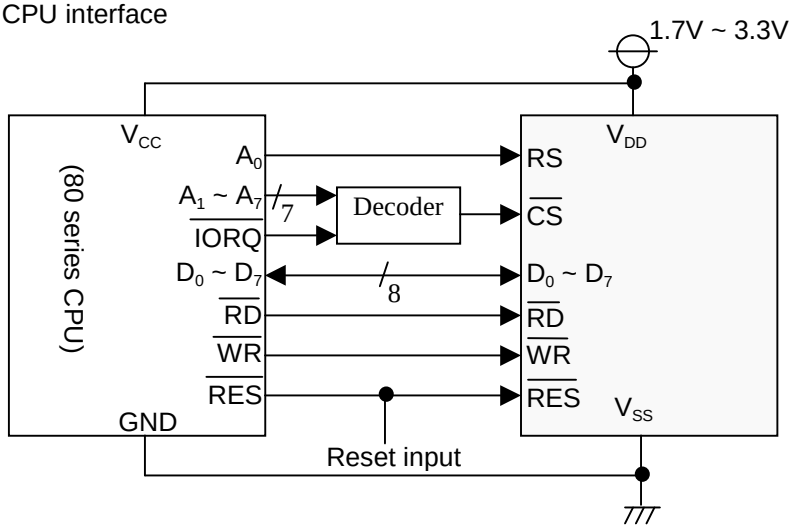
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.5	µs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		µs	$\overline{RES}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

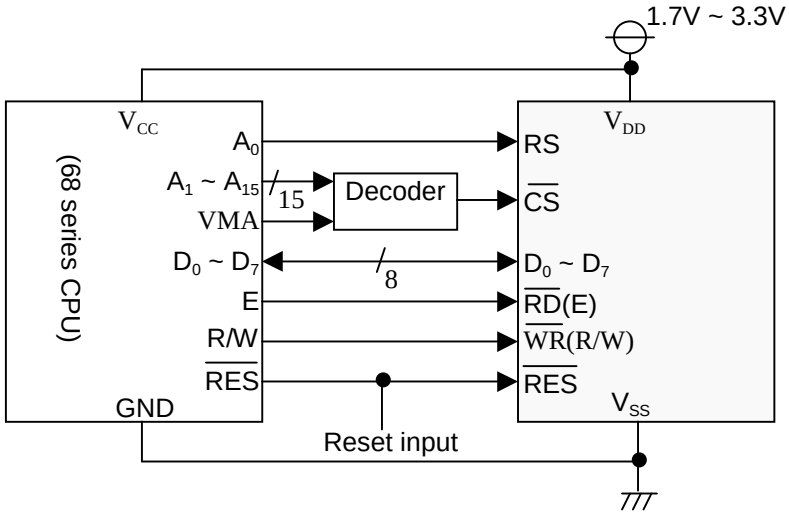
■ APPLICATION EXAMPLE（*reference*）

connection with CPU

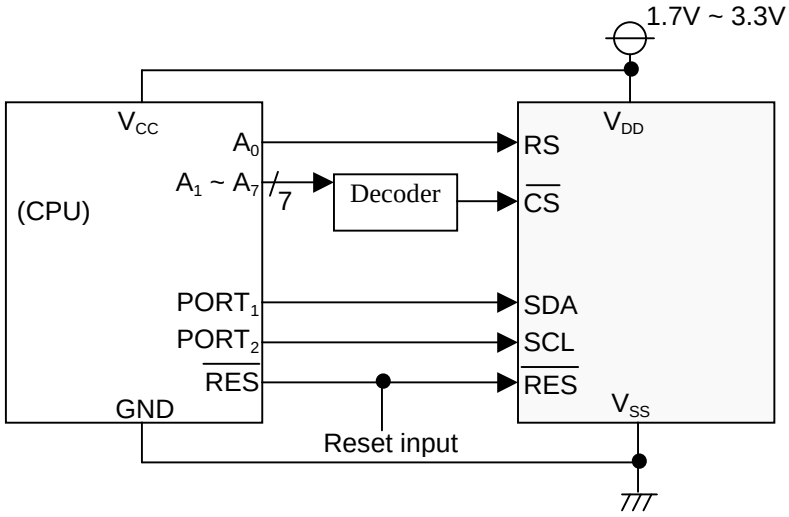
a) 80 series CPU interface



b) 68 series CPU interface



a) CPU connection with serial interface

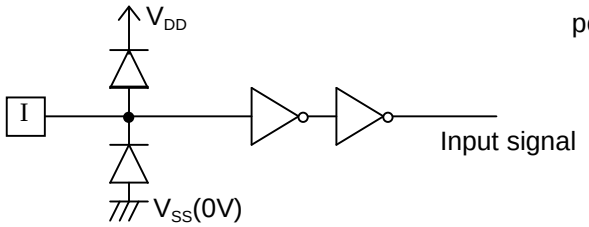


- Typical characteristic

ITEM	CONDITION	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

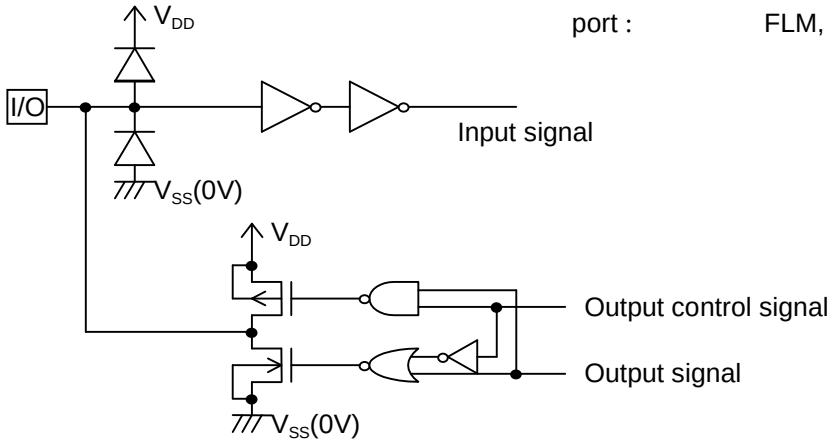
- IN/OUTPUT CIRCUIT STRUCTURE

(a) input circuit 1



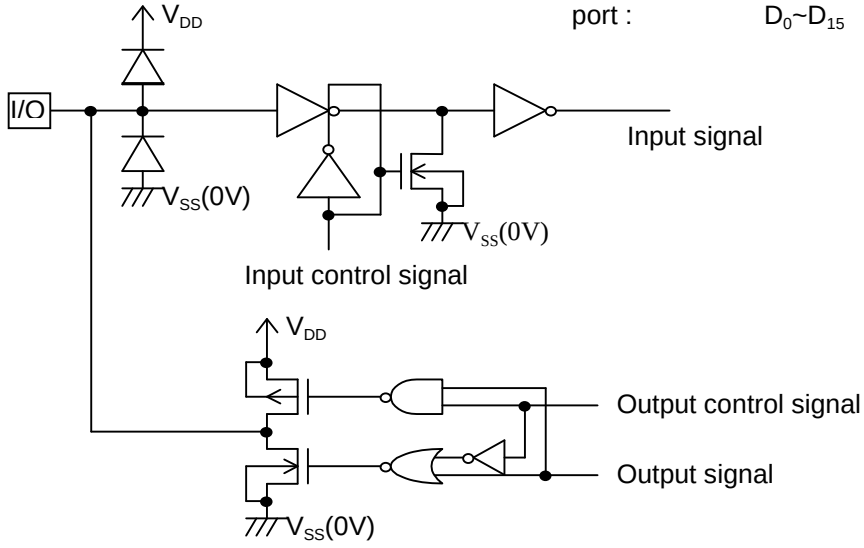
port : $\overline{CS}$, RS, $\overline{RD}$, $\overline{WR}$, SEL68
P/S, $\overline{RES}$

(b-1) in/out circuit 1



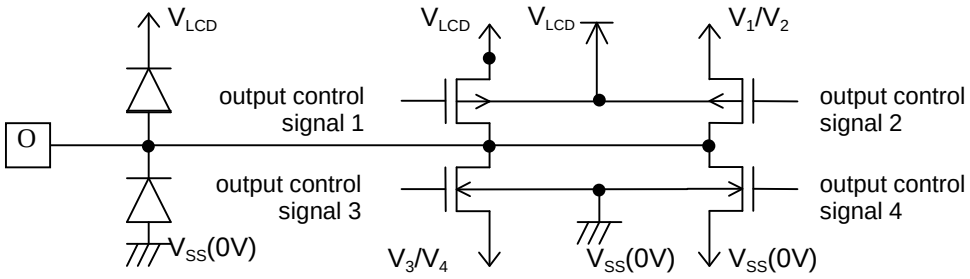
port : FLM, LP, FR, CLK

(b-2) in/out circuit 2



port : D_0~D_{15}

(c) LCD driver output circuit



Port : $SEGA_0$~$SEGA_{127}$
$SEGB_0$~$SEGB_{127}$
$SEGC_0$~$SEGC_{127}$
COM_0~COM_{162}

<precautions>

The details of this specification was written sincerely, but it is not a letter of guarantee of legal. Especially, the application circuit is just for reference.

This specification do not guarantee that we did not use others patent or intellectural property.