# Advik Bahadur Electronic and Computer Engineering Student

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## Profile

Final-year Electronic and Computer Engineering student specializing in **transistor-level design** and **RF/microwave device modeling**. Experienced in **extracting intrinsic and extrinsic parasitic parameters** for GaN FETs using MATLAB and Julia. Proficient in **Verilog/SystemVerilog** for FPGA-based convolution engines and **SoC integration**. Technical background includes developing **Hardware-in-the-Loop (HiL) testbenches**, sensor calibration rigs, and real-time embedded pipelines for high-performance automotive ECUs.

## Professional Experience

**Intern,** *Jaguar Land Rover (JLR)* 01/2025 – 09/2025 | Shannon, Ireland

- Built **real-time multi-sensor processing pipelines** on **NVIDIA embedded ECUs** under strict latency and safety constraints.
- Developed **simulation and visualisation tools** for LiDAR, radar, and camera streams to enable structured debugging and repeatable test scenarios.
- Trained, optimised and validated **ML modules** for resource-constrained ECUs, improving runtime stability through **profiling** and **constraint-driven optimisation.**

**Captain,** *Formula Trinity Autonomous* 2021 – 2025 | Dublin, Ireland

- Achieved award-winning autonomous driving performance by leading the **AI division** to secure **Best Design at Formula Student UK 2024**, demonstrating robust **end-to-end perception, control, and systems engineering** impact on a real-world **embedded platform**
- Delivered reliable, **low-latency closed-loop behaviour** by building **hardware-in-the-loop testbenches**, **sensor calibration rigs**, and **ROS/ROS2 Linux pipelines**, improving **validation coverage** and de-risking deployment of **safety-critical control stacks** for driverless operation
- Improved **real-time decision-making** and **embedded compute efficiency** by designing the **driverless system architecture** (**perception pipelines, MPC-based control, multi-sensor fusion**) and deploying **deep learning models** for **object detection** on **NVIDIA Jetson platforms**, enabling **synchronised perception–actuation** for autonomous vehicles

**FPGA Design Summer Intern,** *Radiona.org* 07/2024 – 09/2024 | Zagreb, Croatia

- **Designed and optimised Verilog-based 2D convolution engines on the Lattice ECP5**, enabling hardware-accelerated image processing under strict timing and resource constraints on the ULX3S FPGA.
- **Built a hybrid ML-acceleration pipeline combining a RISC-V soft core with custom FPGA logic**, where the CPU orchestrated model flow and the FPGA executed convolution workloads—delivering ~5 FPS super-resolution throughput on limited fabric.
- **Verified timing, functional correctness, and end-to-end behaviour** using simulation, synthesis, and waveform analysis, gaining practical experience in SoC integration, hardware–software co-design, and digital design optimisation.

**Software Engineer,** *RampInfoTech Ltd* 07/2023 – 09/2024 | Dublin, Ireland

- Worked as a **client-facing developer in the packaging and supply-chain industry**, analyzing business processes to design and implement end to end **automation solutions** using **APIs**, **Python**, and **Power Platform automation tools**.
- Managed and manipulated data from **SQL databases**, creating algorithms for **trend identification** and **predictive analytics** to support data-driven decision making.
- Led a team to design and develop a **Container Tracking automation** solution to provide real-time data insights for the clients in a short timeframe

## Education

**Masters in Electronic and Computer Engineering,** *Trinity College Dublin* 2021 – 05/2026 | Dublin, Ireland

Completed 4th Year with First Class Honours. Currently in the final year of the course.

## Projects

**Transistor Parasitic Model Extraction,** *MAI Research project* 09/2025 – Present

Developing MATLAB/Julia-based methods for extracting **intrinsic/extrinsic parasitic parameters** of **GaN FETs** to improve RF/microwave device modelling accuracy.

**Super-Resolution Deep Learning Model,** *Deep Learning Pytorch Network* 05/2024 – 07/2024

Worked with industry mentors to **train and optimise a lightweight super-resolution model** for **autonomous-driving camera enhancement**, developing the full **PyTorch** training pipeline in **Python** with data preprocessing, augmentation, and performance-driven tuning.

## Skills

**Hardware:** Verilog/SystemVerilog, FPGA (ECP5, ULX3S), digital design, test-benches, SoC integration

**Software:** Python, C/C++, Java, Linux, ROS/ROS2, Git, CI/CD, SQL

**AI/ML:** PyTorch, Keras, TensorFlow, Transformer Architectures, inference acceleration, model pruning.

**Tools:** Vivado, MATLAB/Simulink, Keysight ADS, SolidWorks, AutoCAD, waveform analysis, embedded profiling