

# Advik Bahadur

## Electronic and Computer Engineering Student

 advikbahadur@gmail.com

 +353 (0) 892325102

 Dublin, Ireland

 linkedin.com/in/advik-bahadur/

### Profile

Final-year Electronic and Computer Engineering student specializing in **AI hardware accelerators and high-performance embedded systems**. Expert in **C++ and Python** with a focus on optimizing **deep learning perception pipelines** for resource-constrained architectures. Experienced in developing **custom FPGA-based ML acceleration engines** and managing **heterogeneous hardware-software co-design** for real-time inference.

### Professional Experience

#### AI Intern, Jaguar Land Rover (JLR)

01/2025 – 09/2025 | Shannon, Ireland

- Engineered a ground-up **multi-sensor visualisation and simulation suite** for LiDAR, Radar, and Camera streams to generate synthetic datasets for niche ADAS features.
- Leveraged **AWS for scalable development and deployment**, enabling structured fine-tuning of ML models within a cloud-to-edge workflow.
- Developed **real-time processing pipelines** on NVIDIA embedded ECUs, utilising **profiling and constraint-driven optimisation** to ensure deterministic execution.
- Trained, Tested & Optimized ML modules for resource-constrained hardware, improving runtime stability and reducing latency through rigorous **performance analysis**.

#### Captain, Formula Trinity Autonomous

2021 – 2025 | Dublin, Ireland

- Architected an **award-winning autonomous driving stack**, deploying deep learning models for object detection on **NVIDIA Jetson GPU accelerators**.
- Developed **closed-loop control and perception pipelines (YOLO)** using **LINUX & ROS2**, achieving high-performance real-time decision-making.
- Built **Hardware-in-the-Loop (HiL)** testbenches and simulation environments to validate safety-critical software and sensor calibration rigs for driverless operation.

#### Software Engineer, RampInfoTech Ltd

07/2023 – 09/2024 | Dublin, Ireland

- Worked as a **client-facing developer in the packaging and supply-chain industry**, analyzing business processes to design and implement end to end **automation solutions** using **APIs, Python, and Power Platform automation tools**.
- Managed and manipulated data from **SQL databases**, creating algorithms for **trend identification and predictive analytics** to support data-driven decision making.
- Led a team to design and develop a **Container Tracking automation** solution to provide real-time data insights for the clients in a short timeframe.

#### FPGA Design Summer Intern, Radiona.org

07/2024 – 09/2024 | Zagreb, Croatia

- Designed **Verilog-based 2D convolution engines** for hardware-accelerated image processing, optimising for strict timing and resource constraints.
- Developed a **hybrid ML-acceleration pipeline** utilising a **RISC-V soft core** to orchestrate workloads executed on custom FPGA logic.
- Executed full-stack hardware-software co-design, including **SoC integration, synthesis, and waveform analysis** for timing verification.

### Education

#### Masters in Electronic and Computer Engineering, Trinity College Dublin

2021 – 05/2026 | Dublin, Ireland

Completed 4th Year with First Class Honours. Currently in the final year of the course.

### Projects

#### Transistor Parasitic Model Extraction, MAI Research project

09/2025 – Present

Developing MATLAB/Julia-based methods for extracting **intrinsic/extrinsic parasitic parameters** of GaN FETs to improve RF/microwave device modelling accuracy.

#### Super-Resolution Deep Learning Model, Deep Learning Pytorch Network

05/2024 – 07/2024

Worked with industry mentors to **train and optimise a lightweight super-resolution model for autonomous-driving camera enhancement**, developing the full PyTorch training pipeline in **Python** with data preprocessing, augmentation, and performance-driven tuning.

### Skills

**Software:** C/C++, Python, Java, Linux, ROS/ROS2, Git, CI/CD, SQL

**AI/ML:** PyTorch, Keras, TensorFlow, HuggingFace, Transformer Architectures, inference acceleration, model pruning.

**Hardware:** Verilog/SystemVerilog, FPGA (ECP5, ULX3S), digital design, test-benches, SoC integration

**Tools:** Vivado, MATLAB/Simulink, Keysight ADS, SolidWorks, AutoCAD, waveform analysis, embedded profiling