Contact

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Susan Kwan

Staff Layout Designer at Micron Technology
Santa Clara, California

Summary

Successful and driven team leader with 18 years of experience in Layout Design. Proven track record of success in leadership and project execution.

Specialties:
-Cadence Virtuoso and VXL
-Mentor Calibre LVS/DRC

Experience

Apple
Layout Designer

Micron Technology
Staff Layout Designer
January 2007 - August 2014 (7 years 8 months)

- Leading revision work of core array block. Responsibilities include signal planning, power planning,
block integration and physical verification with 3D 16nm nodes.
- Layout Lead of volgen block with charge pumps, regulators, low power and high power blocks for
revision and process migration from 21nm nodes to 3D 16nm nodes. Performed floor planning,
signal/power planning, revision work of charge pumps, block integration, IR/EM fix and physical
verification.
- Layout Lead of coredrv block. Responsibilities include signal/power planning, layout of word line
bias generating blocks, block integration, EM/IR fix and physical verification with 21nm nodes.
- Laid out IO pad/pad block, data path blocks and library cells for multiple projects.

Broadcom

Principal Layout Designer

2000 - 2006 (6 years)

- Integrated ALU datapath block for 64-bit microprocessor.
- Developed datapath library cells with TSMC 65nm nodes.
- Layout Lead of functional blocks, core integration, EM/IR fixes and clock balancing for quad core
embedded processor.
- Layout Lead for revision, shrinking and migration of the SB1 microprocessor core. Implemented
layout changes, core integration and verification.
- Integration of data-path and control blocks for PC box, and ownership of global repeaters for the
first tape-out of SB1 dual core embedded processor.

Philips

Senior Layout Designer

1999 - 2000 (1 year)

San Jose, California

- Built register file and bypass blocks from floor planning, cell layout, block integration and
verification.

Quality Semiconductor, Inc.

Layout Designer

1996 - 1999 (3 years)

San Jose, CA

Performed full custom layout of a variety of logic chips including Line Driver, Transceiver, Latch, Register and Multiplexer. Responsibilities included from floor planning, cell layout, integration, verification to tape-out of each chip

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Education

International Technological University

Technical Certificate (IC Mask Design) · (1996 - 1996)

RPI

Master's degree, Civil Engineering