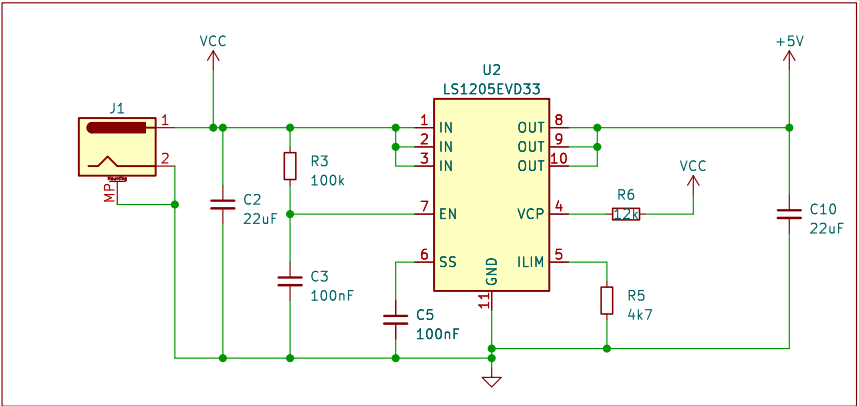


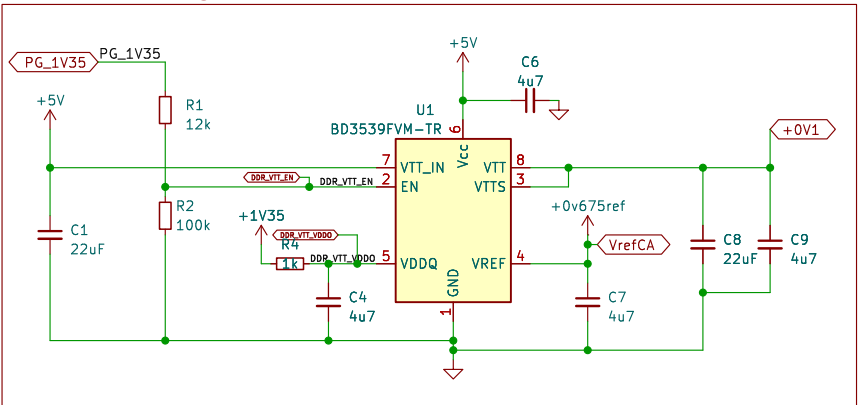
	1	2	3	4	5	6	7	8
A	<div>[01] – POWER</div> <div>File: [01] – Power.kicad_sch</div>	<div>[02] – Zync Power</div> <div>File: ZyncPower.kicad_sch</div>	<div>[03] – Programmable Logic (PL)</div> <div>File: PL.kicad_sch</div>	<div>[04] – Processing System (PS)</div> <div>File: PS.kicad_sch</div>	<div>[05] – JTAG</div> <div>File: JTAG.kicad_sch</div>			
B	<div>[06] – Zync DDR</div> <div>File: Memory.kicad_sch</div>	<div>[07] – DDR3</div> <div>File: DDR3.kicad_sch</div>	<div>[08] – Ethernet</div> <div>File: Ethernet.kicad_sch</div>	<div>[09] – High Speed (OTG)</div> <div>File: OTG.kicad_sch</div>	<div>[10] – Peripherals</div> <div>File: Peripherals.kicad_sch</div>			
C								
D								
E								
F								<div></div> <div>Sheet: / File: ZettBrett.kicad_sch</div> <div><div>Title:</div><div>Size: A3</div><div>KiCad E.D.A. 8.0.1</div></div> <div><div>Date:</div><div>Rev:</div><div>Id: 1/11</div></div>
	1	2	3	4	5	6	7	8

POWER

INPUT POWER

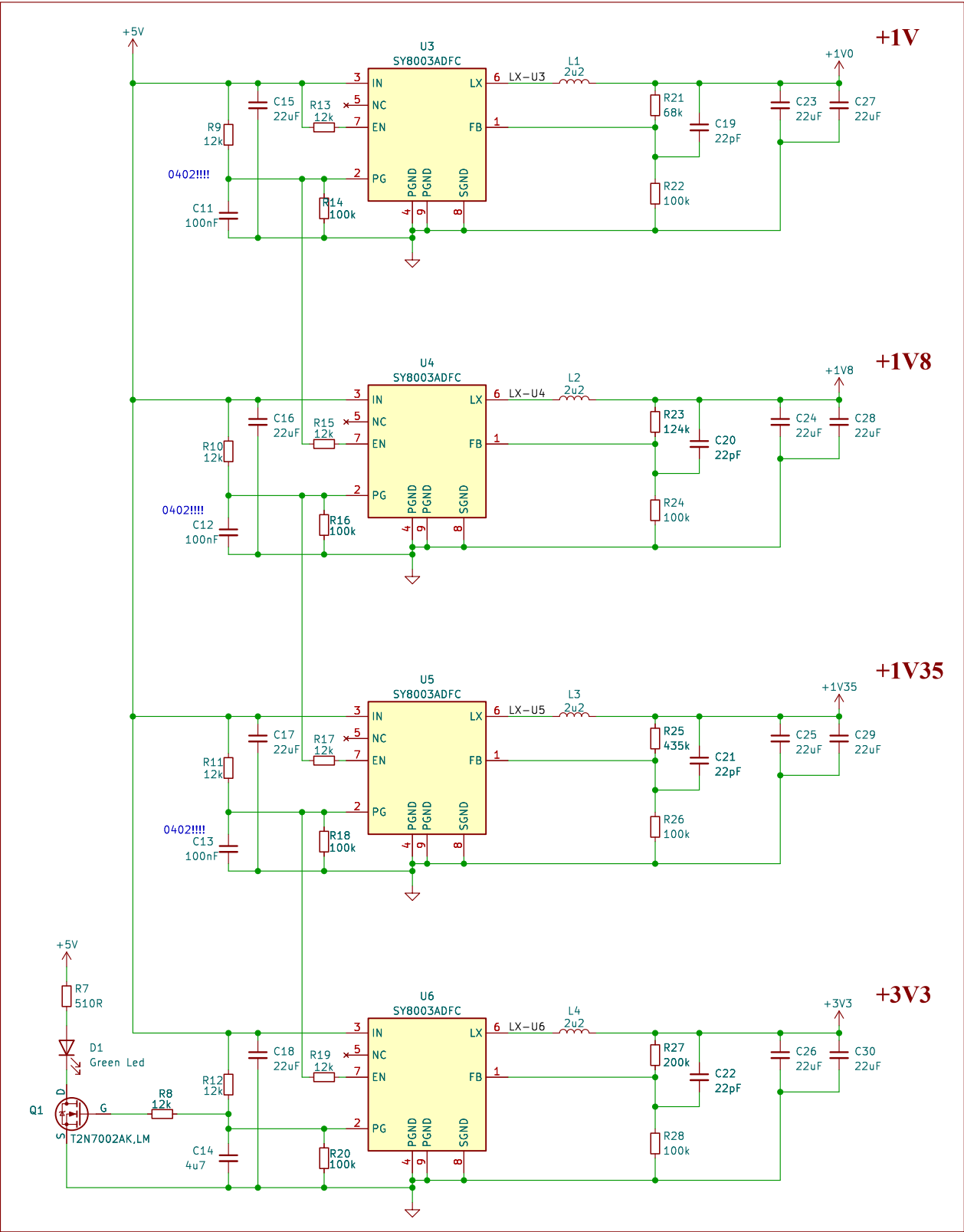


DDR3 VTT Reg



BUCK CONVERTERS

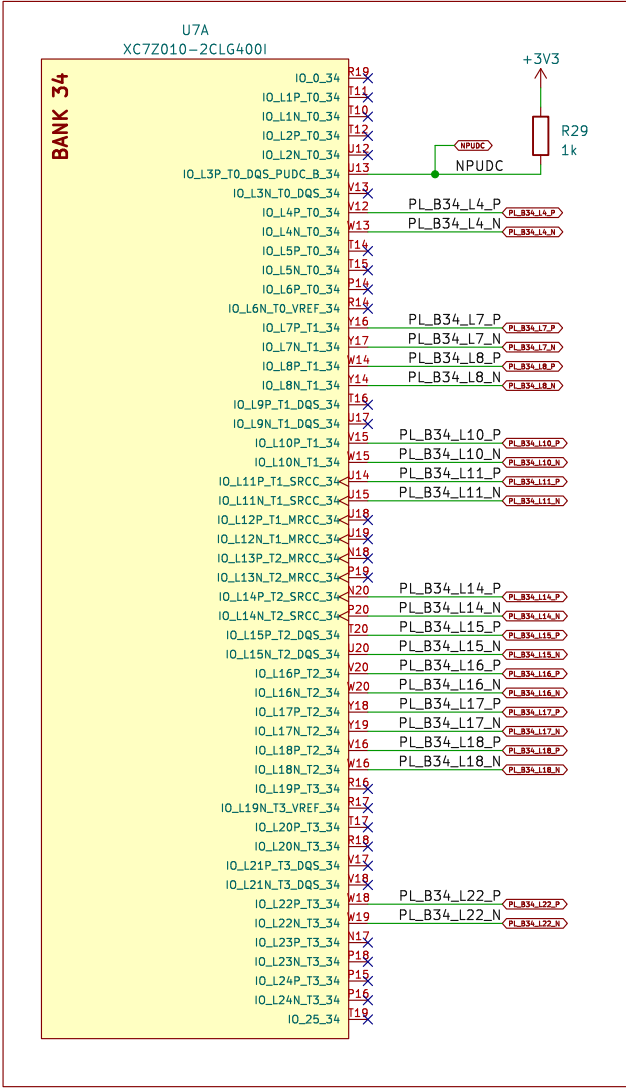
Power Sequence: +1V0 -> +1V8 -> +1V35 -> +3V3



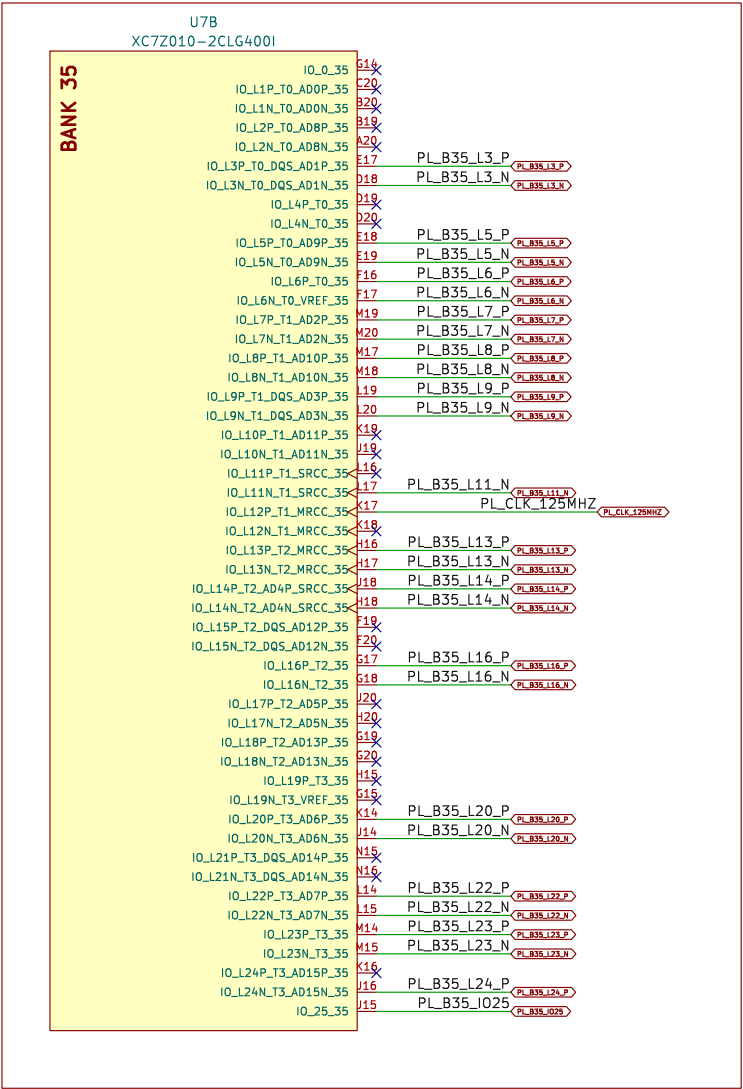
1	2	3	4	5	6	7	8
---	---	---	---	---	---	---	---

PROGRAMMABLE LOGIC (PL)

BANK 34



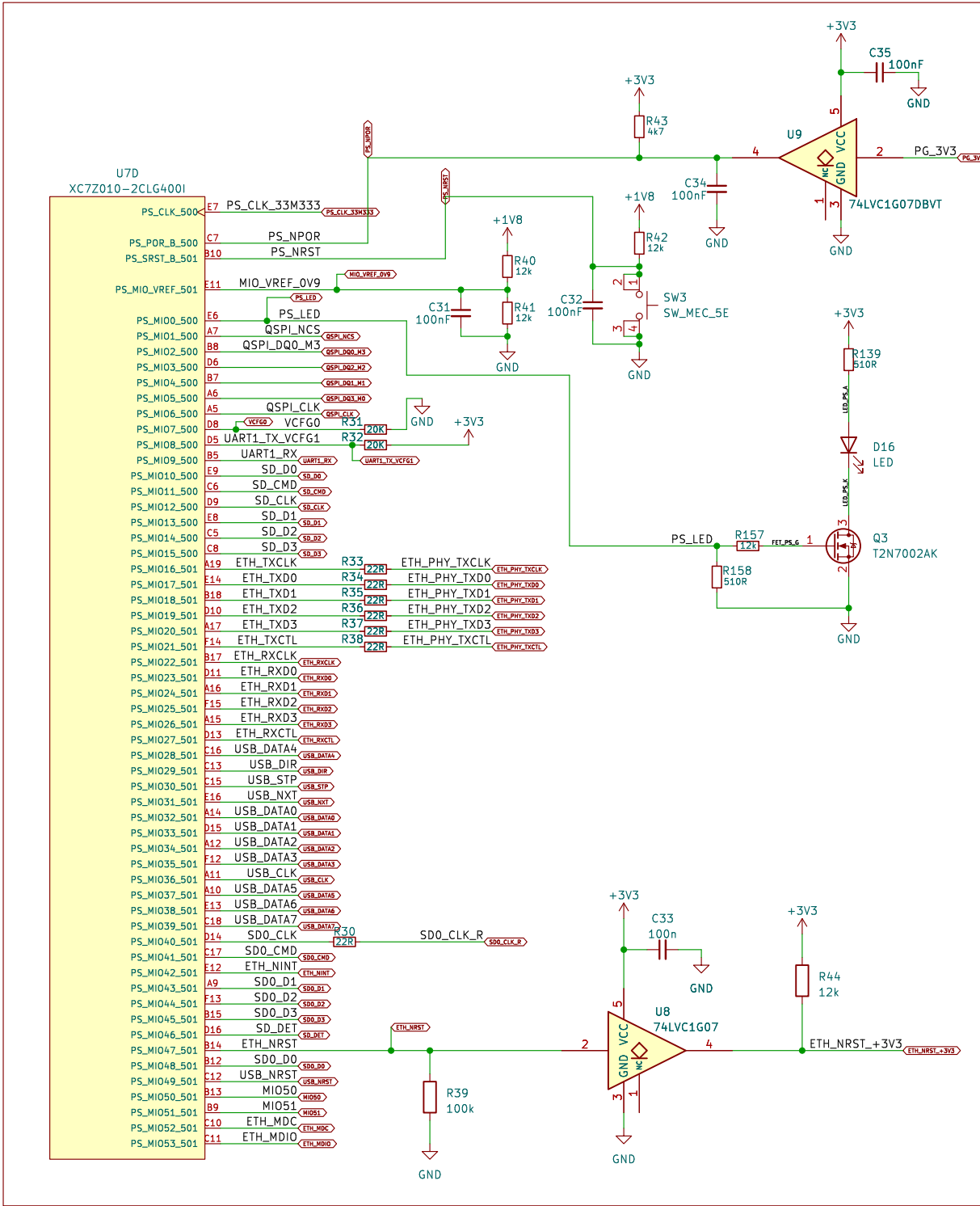
BANK 35



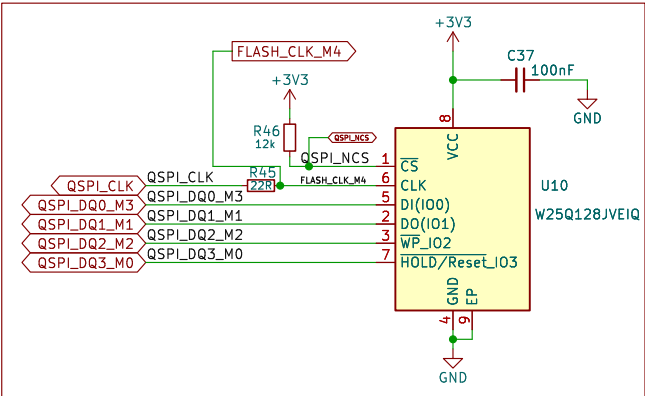
PROCESSING SYSTEM (PS)

change to 256?

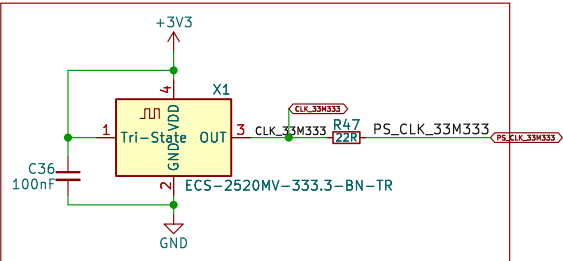
PROCESSING SYSTEM BANKS(500 AND 501)



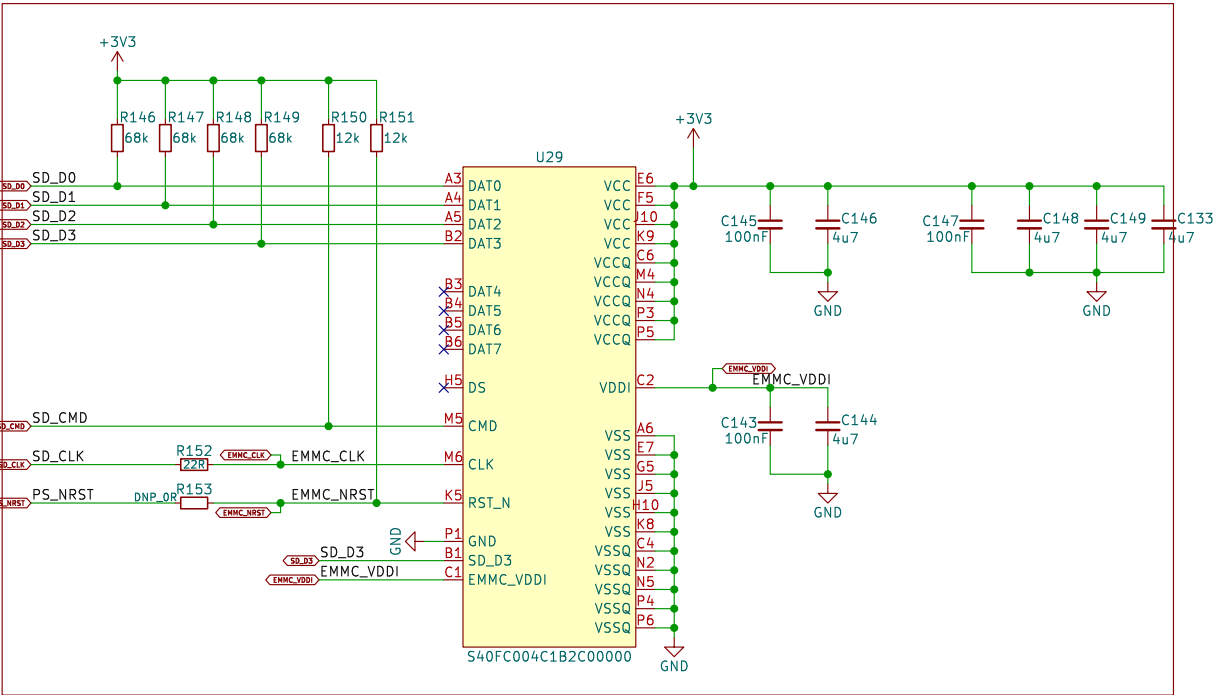
QSPI FLASH MEMORY (128MBit)



PS CLOCK (33.33 MHz)

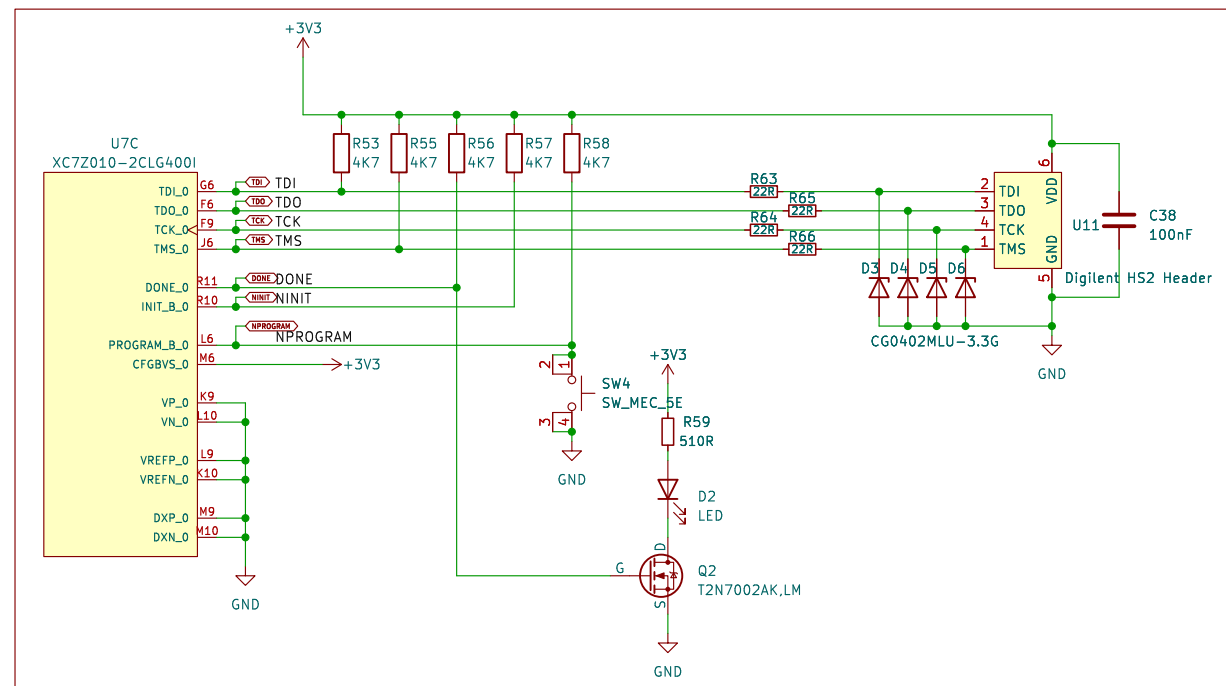


eMMC MEMORY

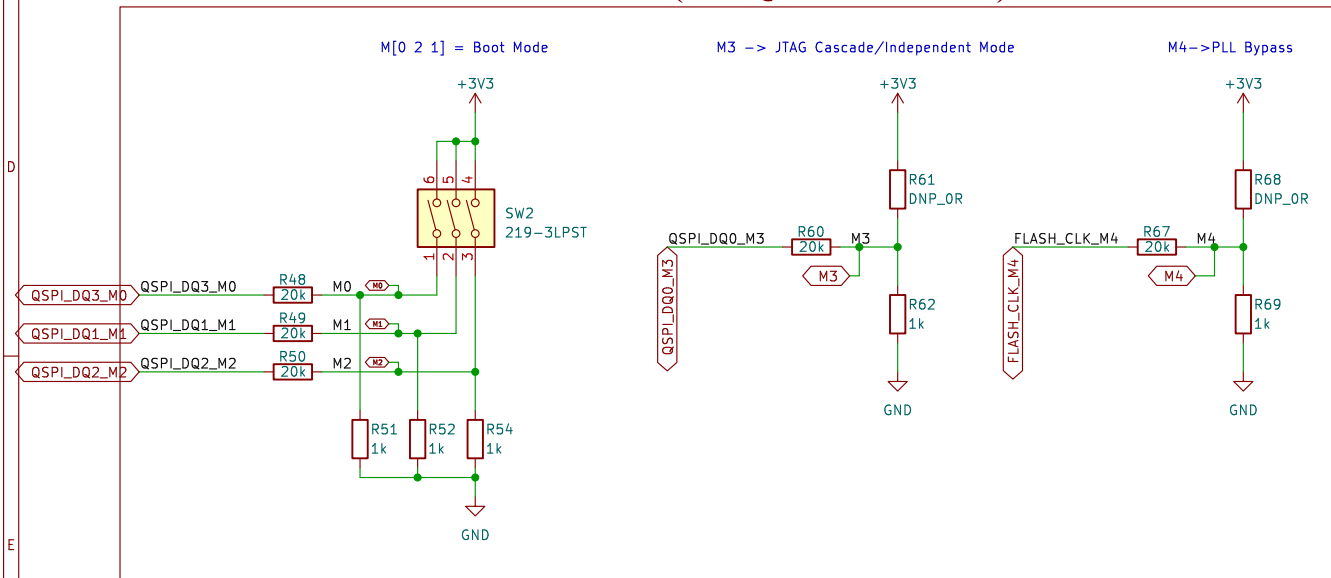


# JTAG

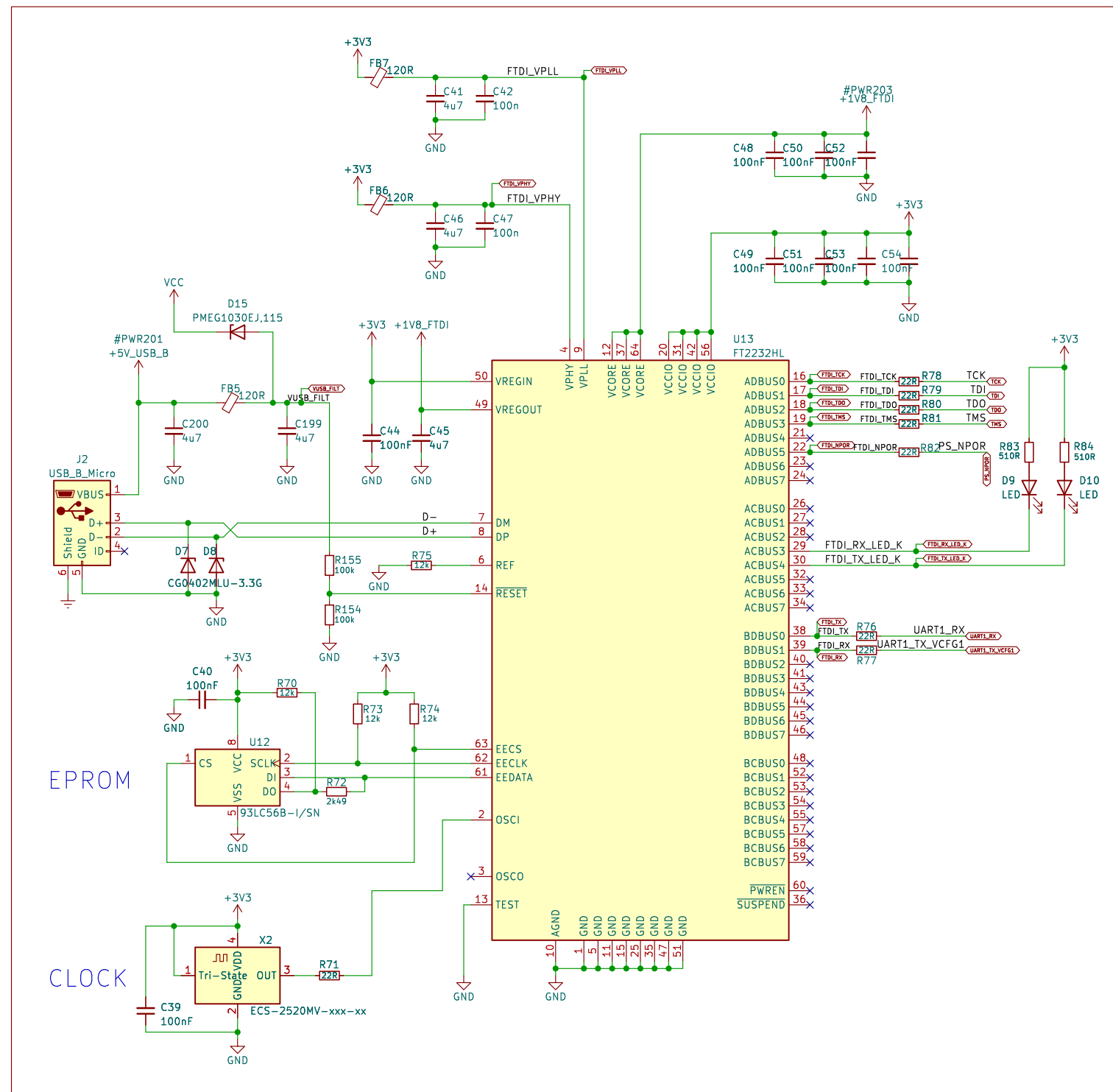
## JTAG



## BOOT MODE MIO STRAPPING PINS (ZYNQ TRM PAGE167)

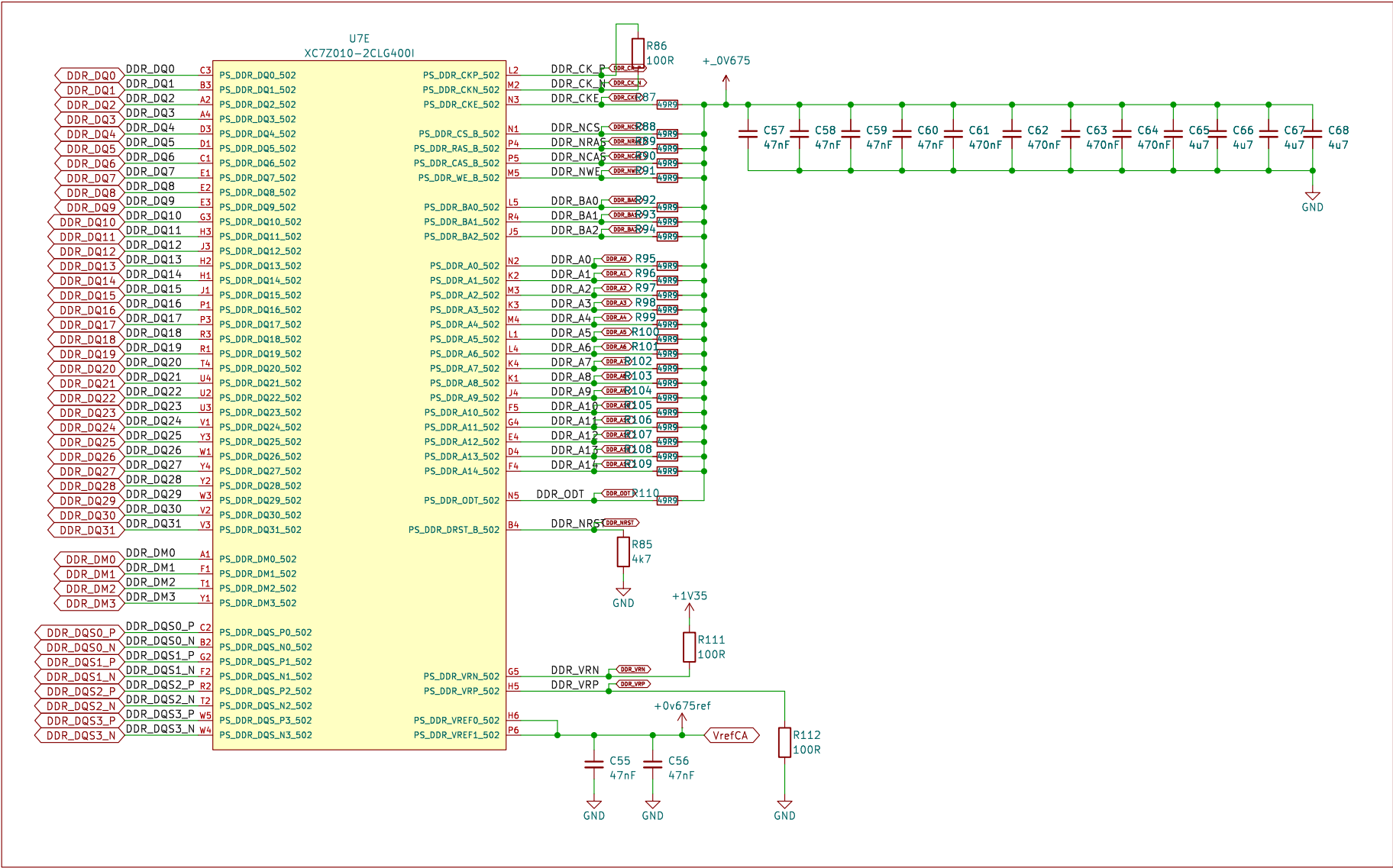


# FTDI JTAG PROGRAMMER



ZYNQ DDR

ZYNQ DDR INTERFACE



Sheet: /[06] - Zync DDR/  
File: Memory.kicad\_sch

Title:

Size: A3

Date:

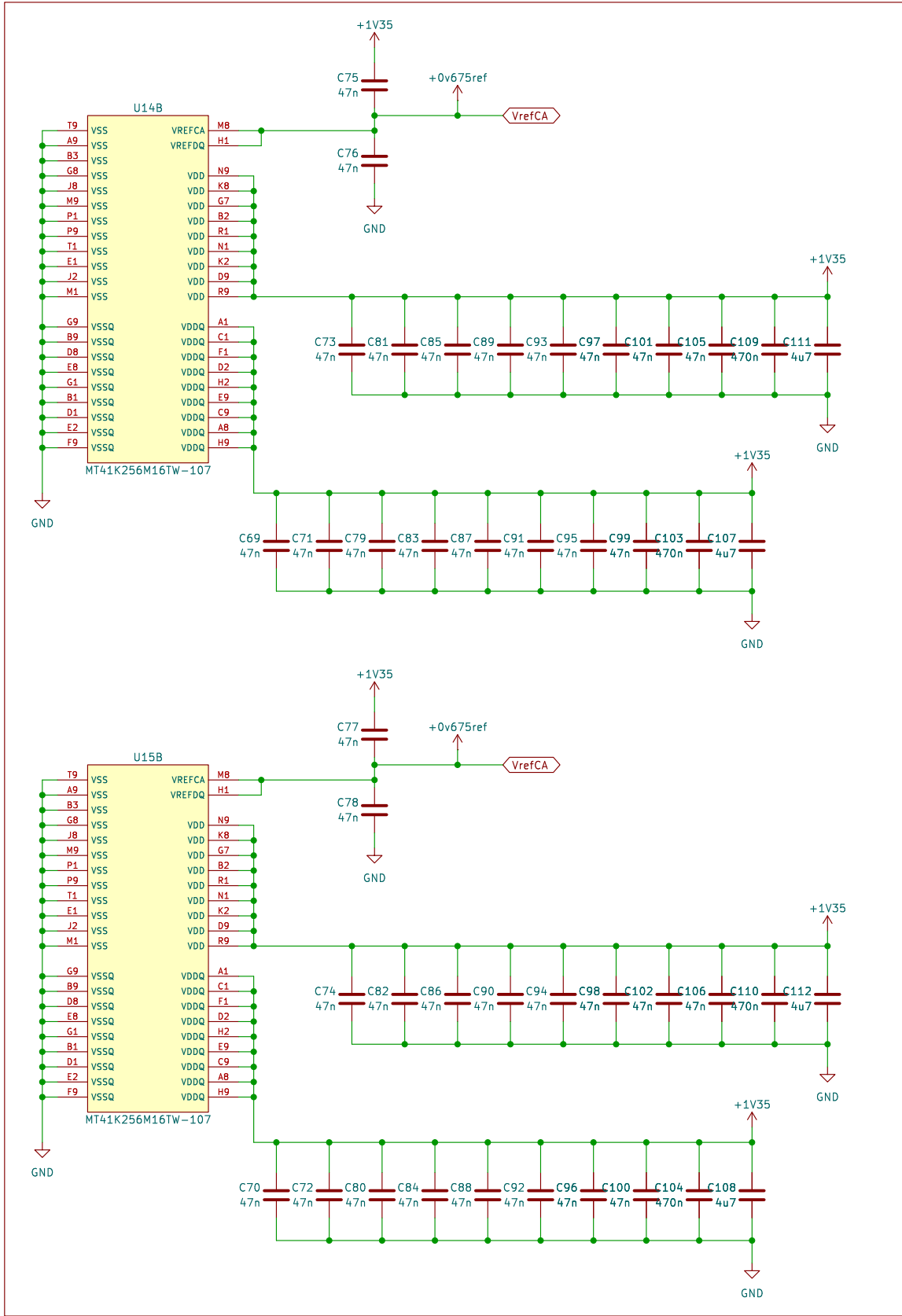
Rev:

KiCad E.D.A. 8.0.1

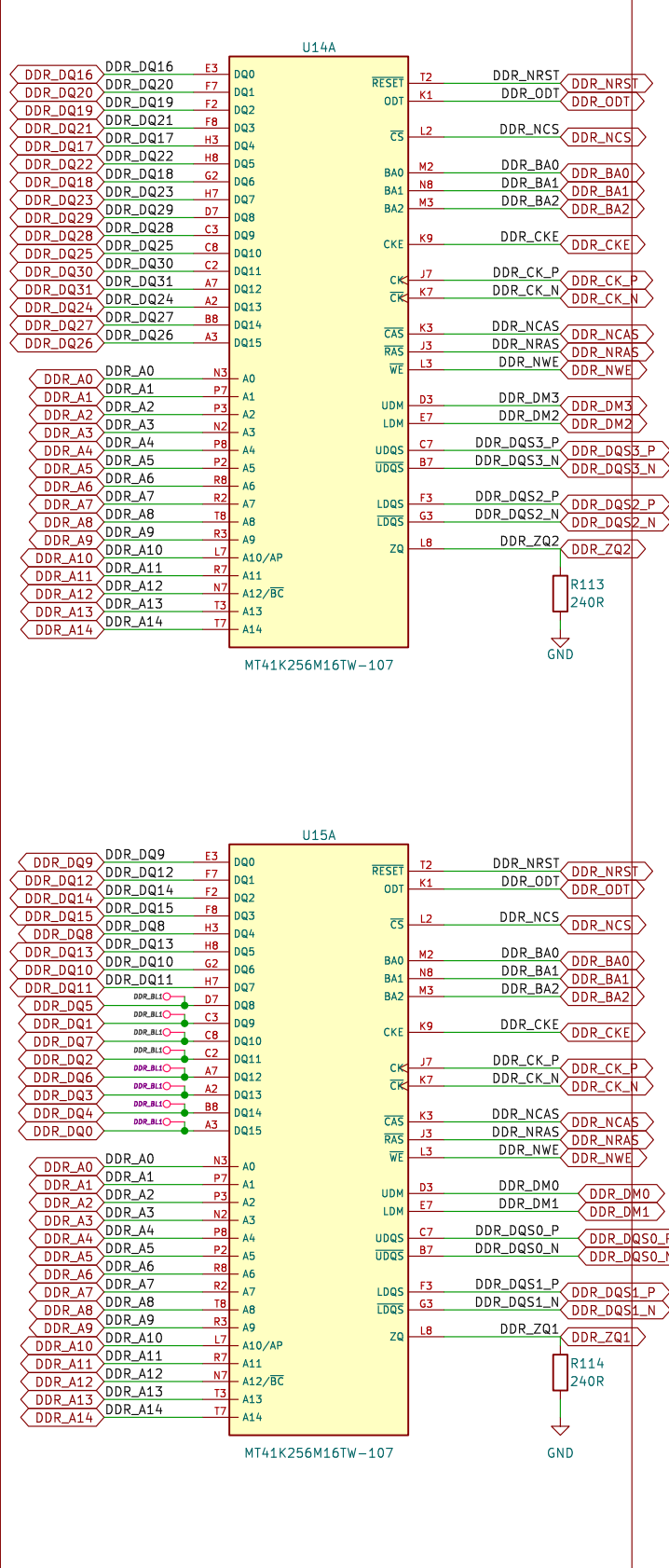
Id: 7/11

# 1GB DDR3

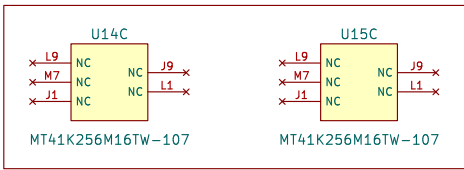
## POWER & DECAP



## ACC & DAT CONNECTIONS



## NOT CONNECTED



Sheet: /[07] - DDR3/  
File: DDR3.kicad\_sch

Title:

Size: A3

Date:

Rev:

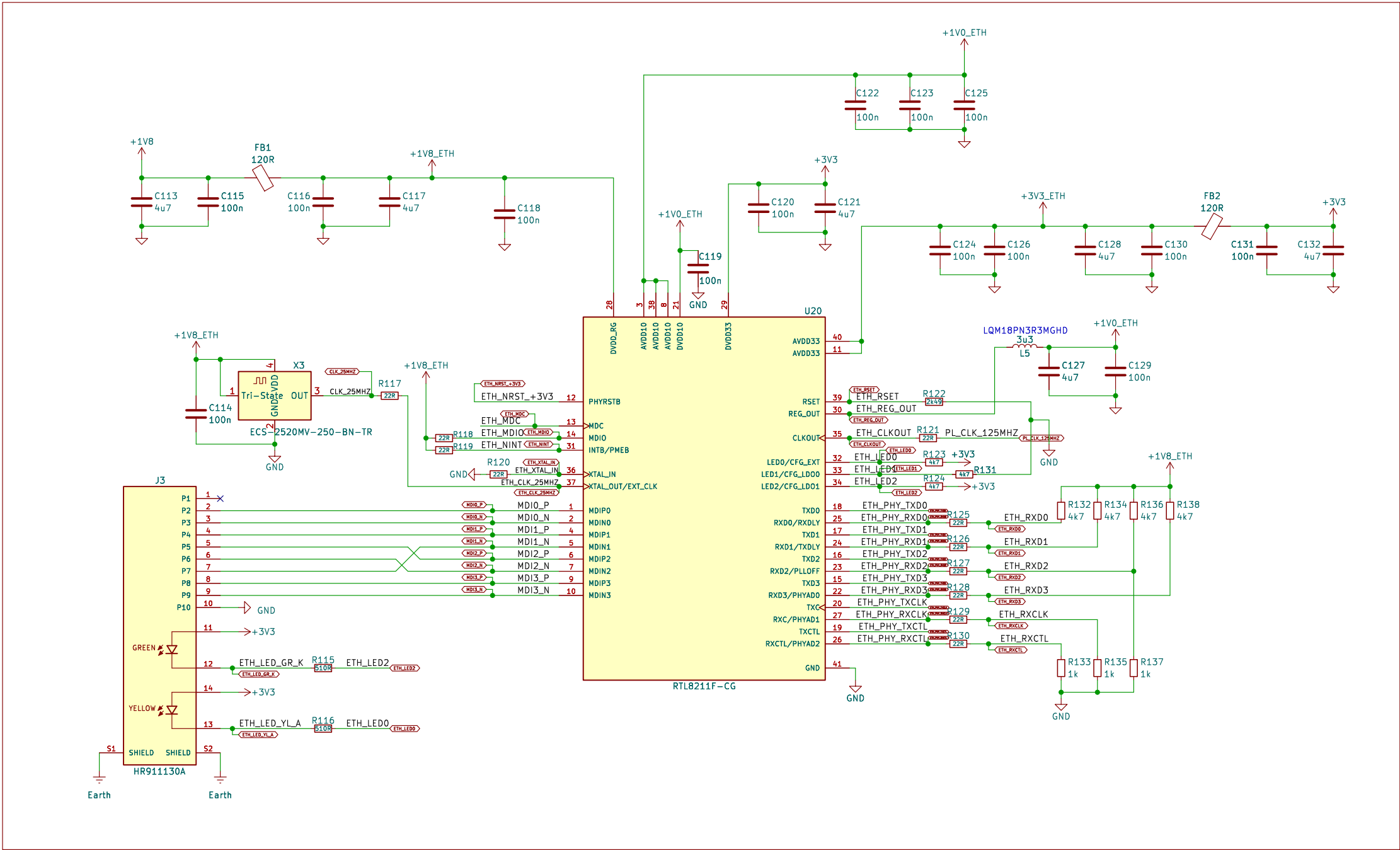
KiCad E.D.A. 8.0.1

Id: 8/11



# ETHERNET

## POWER & DECAP



Sheet: /[08] - Ethernet/  
File: Ethernet.kicad\_sch

### Title:

Size: A3

Date:

Rev:

KiCad E.D.A. 8.0.1

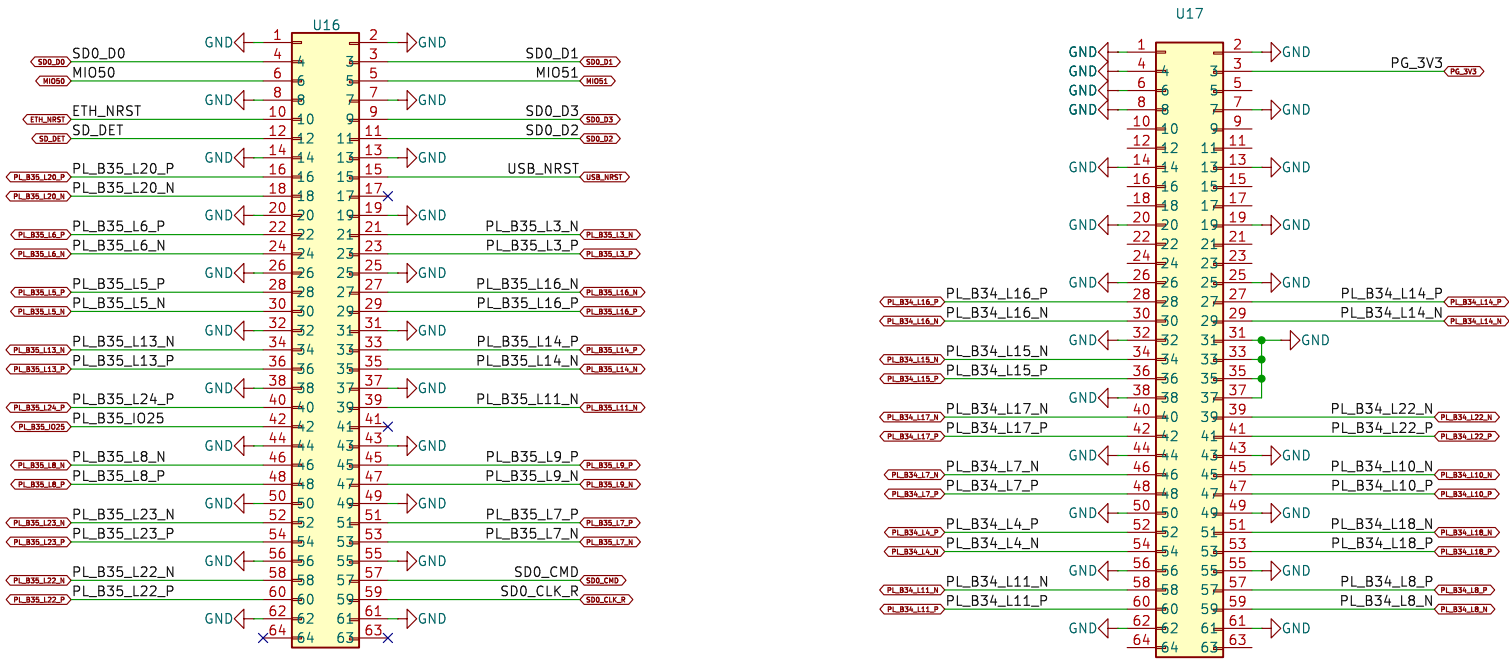
Id: 9/11

[illegible]

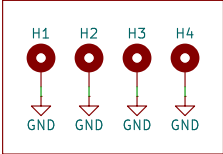
<b>Title:</b>		
Size: A3	Date:	<b>Rev:</b>
KiCad E.D.A. 8.0.1		Id: 10/11

# MECHANICAL & PERIPHERALS

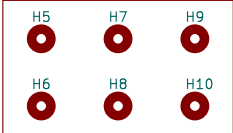
## MEZZANINE CONNECTORS



### MOUNTING HOLES



### FEDUCIALS



### EARTH TO GROUND

