THE FOLLOWING TESTBENCH SIMULATE THE SIMPLE ADDING OPERATION WHICH IS WRITTEN IN THE ASSEMBLY LEVEL LANGUAGE THEN CONVERTED INTO MACHINE CODE THOSE MACHINE CODE IS CONVERTED INTO HEXADECIMAL VALUES AND LOADED TO THE MEMORY

ASSEMBLY CODE

```
ADDI R1,R0,10 // I-type
ADDI R2,R0,20 // I-type
ADD R4,R1,R2 // R-type
ADD R5,R4,R3 // R-type
HLT
```

MACHINE CODE

001010 00000 00001 0000000000001010

001010 00000 00010 0000000000010100

001010 00000 00011 0000000000011001

000000 00001 00010 00100 00000 000000

000000 00100 00011 00101 00000 000000

111111 00000 00000 00000 00000 000000

THE FOLLOWING PROCCESOR BULIT ON THE RISC V MIPS32 ACRCHITETURE WHICH HAS 32 BIT INSTRUCTION

Which has 3 type of instruction R-type(register), I-type(immediate) and J-type(jump)

R-type : in R type 31-26 (6-bit) are opcode, 25-21(6-bit) are source register 1, 20-16(6-bit) source register 2, 15-11(6-bit) destination register, 10-6(5-bit) shift amount, 5-0(5-bit) opcode extension

I-type : in I type 31-26 (6-bit) opcode, 25-21(6-bit) source register 1, 20-16(6-bit) destination register, 15-0(16-bit) immediate data

J-type : in J-type 31-26 (6-bit) are opcode, 25-0(26-bit) are immediate data

Output

```
Transcript
#       pipe_MIPS32
# End time: 19:19:16 on Dec 21,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
#
# vlog -vlog01compat -work work +incdir+C:/Users/Yashwanth/verilog/32_bit_processor {C:/Users/Yashwanth/verilog/32_bit_processor/tb_MIPS32.v}
# Model Technology ModelSim - Intel FPGA Edition vlog 10.5b Compiler 2016.10 Oct  5 2016
# Start time: 19:19:16 on Dec 21,2024
# vlog -reportprogress 300 -vlog01compat -work work "+incdir+C:/Users/Yashwanth/verilog/32_bit_processor" C:/Users/Yashwanth/verilog/32_bit_processor/tb_MIPS32.v
# -- Compiling module tb_MIPS32
#
# Top level modules:
#       tb_MIPS32
# End time: 19:19:16 on Dec 21,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
#
# vsim -t lps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L fiftyfivenm_ver -L rtl_work -L work -voptargs="+acc"  tb_MIPS32
# vsim -t lps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L fiftyfivenm_ver -L rtl_work -L work -voptargs=""+acc"" tb_MIPS32
# Start time: 19:19:16 on Dec 21,2024
# Loading work.tb_MIPS32
# Loading work.pipe_MIPS32
#
# add wave *
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#           File in use by: Yashwanth  Hostname: YASH  ProcessID: 16344
#           Attempting to use alternate WLF file "./wlft0bcxaq".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#           Using alternate file: ./wlft0bcxaq
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# R0 =  0
# R1 = 10
# R2 = 20
# R3 = 25
# R4 = 30
# R5 = 55

/SIM 2>
```