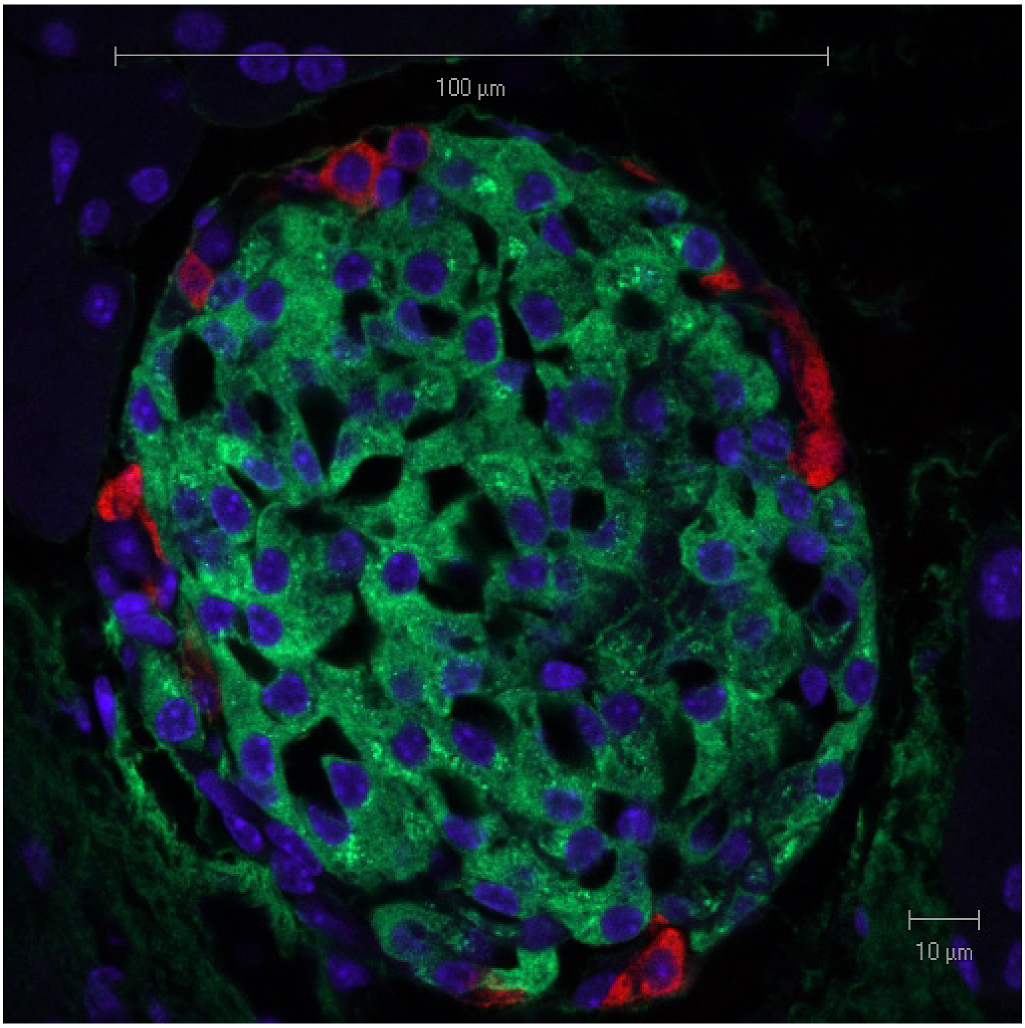
Langerhanske Øer
Projektrapport



Bachelorprojekt
Projektnr: 15137
Ingeniørhøjskolen, Aarhus Universitet
Den 16. december 2015

11424 Anders Toft Andersen
201270874 Anders Esager
Projektvejleder: Samuel Alberg Thrysøe

Forord

Dette dokument indeholder projektdokumentationen for projektet *Cell sorter for isolation of insulin producing cells*. Dokumentet indeholder kravspecifikation og accepttest for systemet, samt beskrivelse af projektets design og implementeringsfase.

Kravspecifikationen er udarbejdet i samarbejde med Søren Gregersen, overlæge på Medicinsk Endokrinologisk Afdeling, Aarhus Universitetshospital, der agerer som projektets kunde.

Læsevejledning

Alle under dokumenter i denne rapport indeholder en indledning, hvor det enkelte dokuments formål er beskrevet. Hvert dokument indeholder en seperat læsevejledning.

Alle dokumenterne og referencer er vedlagt på den afleverede USB.

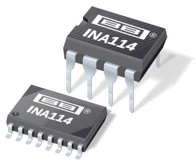
Anders Toft Andersen	Anders Esager
Samuel Alberg Thrysøe	Søren Gregersen

Indholdsfortegnelse

1 Datablade

1.1 Operationsforstærker - INA114

BURR - BROWN®



INA114

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

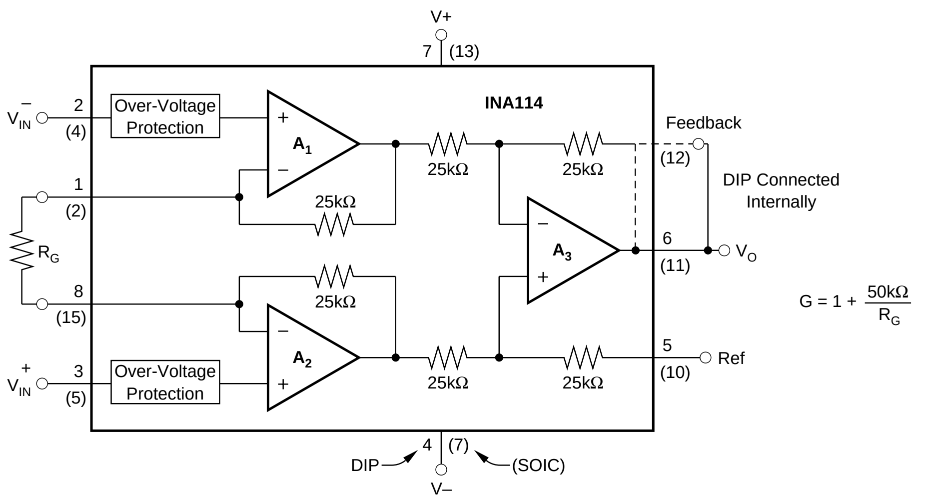
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the –40°C to +85°C temperature range.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1142D

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SBOS014

SPECIFICATIONS

ELECTRICAL

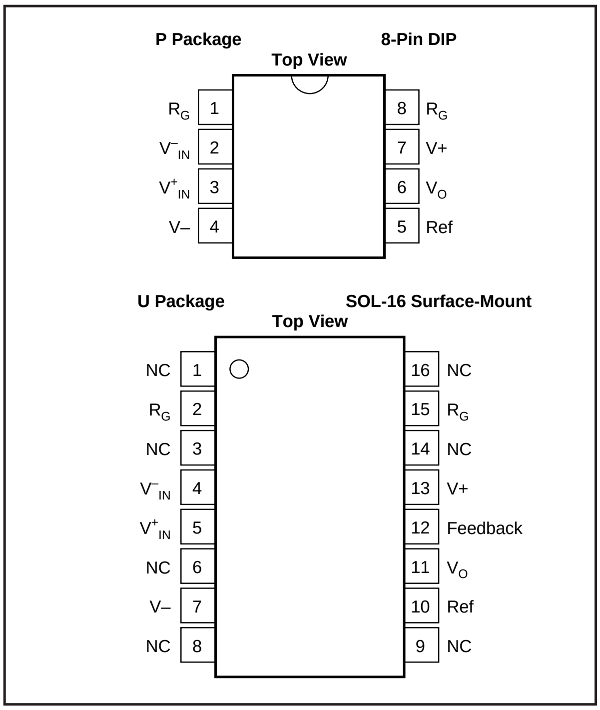
At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, unless otherwise noted.

PARAMETER	CONDITIONS	INA114BP, BU MIN	INA114BP, BU TYP	INA114BP, BU MAX	INA114AP, AU MIN	INA114AP, AU TYP	INA114AP, AU MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25°C$		±10 + 20/G	±50 + 100/G		±25 + 30/G	±125 + 500/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.1 + 0.5/G	±0.25 + 5/G		±0.25 + 5/G	±1 + 10/G	µV/°C
vs Power Supply	$V_S = ±2.25V$ to $±18V$		0.5 + 2/G	3 + 10/G		*	*	µV/V
Long-Term Stability			±0.2 + 0.5/G			*		µV/mo
Impedance, Differential			10^{10} || 6			*		Ω || pF
Common-Mode			10^{10} || 6			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	$V_{CM} = ±10V$, $ΔR_S = 1kΩ$							
	G = 1	80	96		75	90		dB
	G = 10	96	115		90	106		dB
	G = 100	110	120		106	110		dB
	G = 1000	115	120		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0Ω$							
f = 10Hz			15			*		nV/√Hz
f = 100Hz			11			*		nV/√Hz
f = 1kHz			11			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.4			*		µVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B = 0.1Hz to 10Hz			18			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	*	%
	G = 10		±0.02	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5	±1		*	±2	%
Gain vs Temperature	G = 1		±2	±10		*	±10	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0001	±0.001		*	±0.002	% of FSR
	G = 10		±0.0005	±0.002		*	±0.004	% of FSR
	G = 100		±0.0005	±0.002		*	±0.004	% of FSR
	G = 1000		±0.002	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage	$I_O = 5mA$, T_{MIN} to T_{MAX}	±13.5	±13.7		*	*		V
	$V_S = ±11.4V$, $R_L = 2kΩ$	±10	±10.5		*	*		V
	$V_S = ±2.25V$, $R_L = 2kΩ$	±1	±1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+20/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		1			*		MHz
	G = 10		100			*		kHz
	G = 100		10			*		kHz
	G = 1000		1			*		kHz
Slew Rate	$V_O = ±10V$, G = 10	0.3	0.6		*	*		V/µs
Settling Time, 0.01%	G = 1		18			*		µs
	G = 10		20			*		µs
	G = 100		120			*		µs
	G = 1000		1100			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	$V_{IN} = 0V$		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
$θ_{JA}$			80			*		°C/W

* Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA114AP	8-Pin Plastic DIP	006	–40°C to +85°C
INA114BP	8-Pin Plastic DIP	006	–40°C to +85°C
INA114AU	SOL-16 Surface-Mount	211	–40°C to +85°C
INA114BU	SOL-16 Surface-Mount	211	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

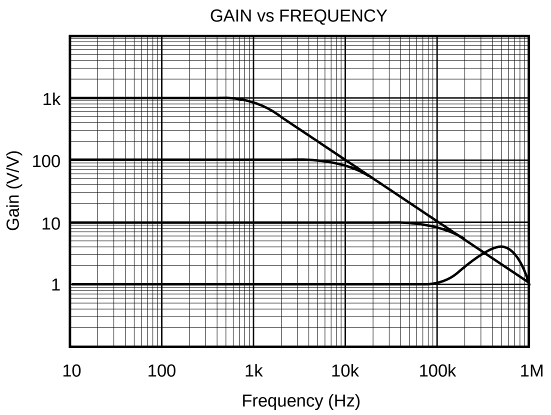
ABSOLUTE MAXIMUM RATINGS(1)

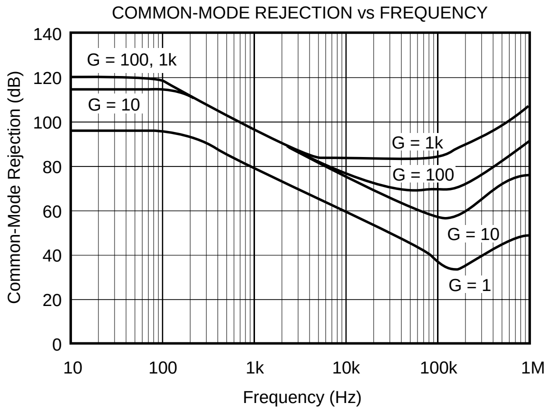
Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

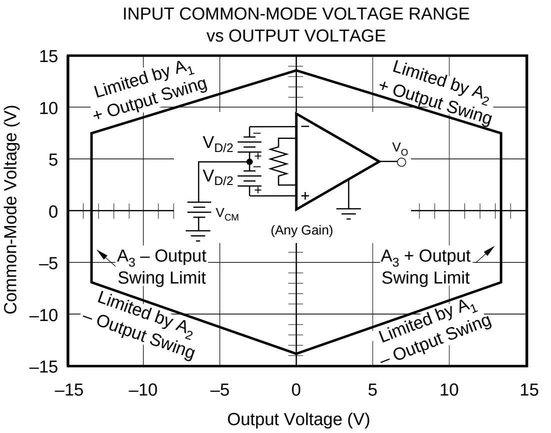
NOTE: (1) Stresses above these ratings may cause permanent damage.

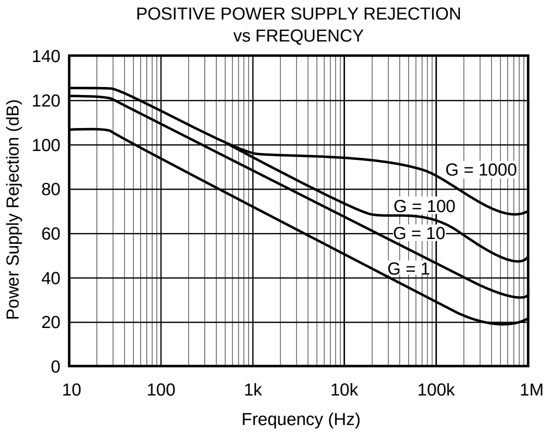
TYPICAL PERFORMANCE CURVES

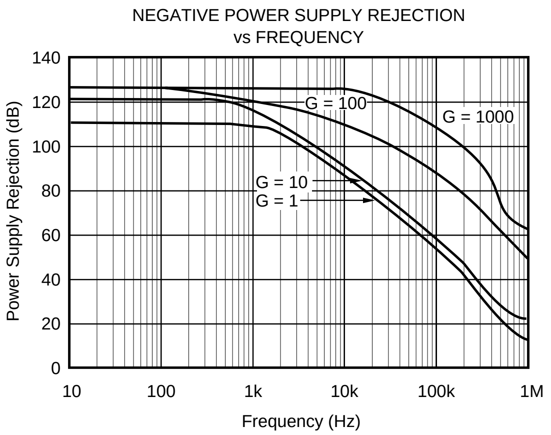
At $T_A = +25°C$, $V_S = \pm15V$, unless otherwise noted.

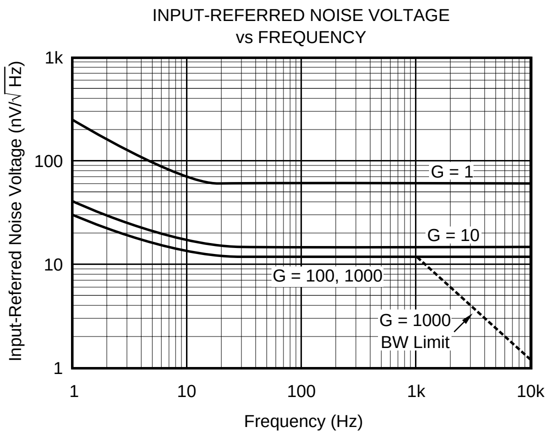






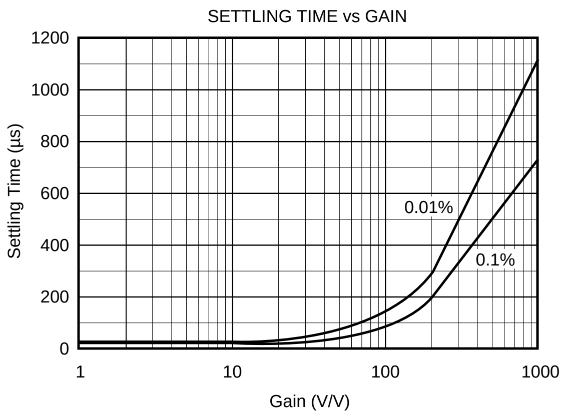


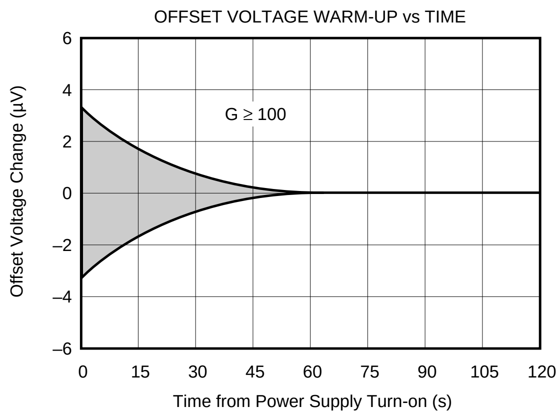


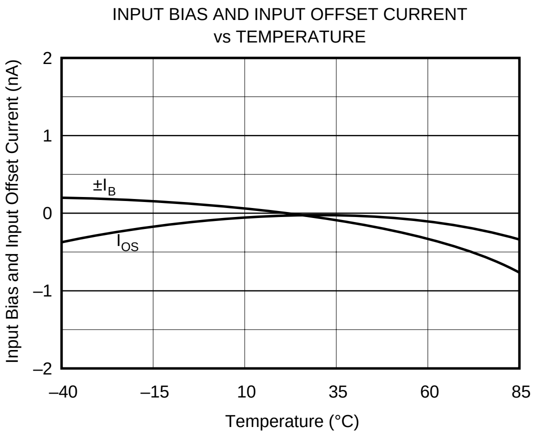


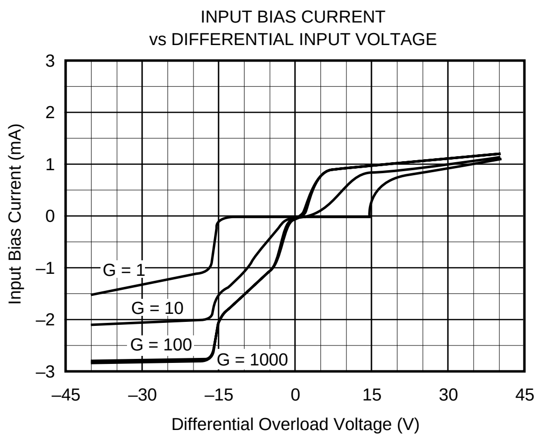
TYPICAL PERFORMANCE CURVES (CONT)

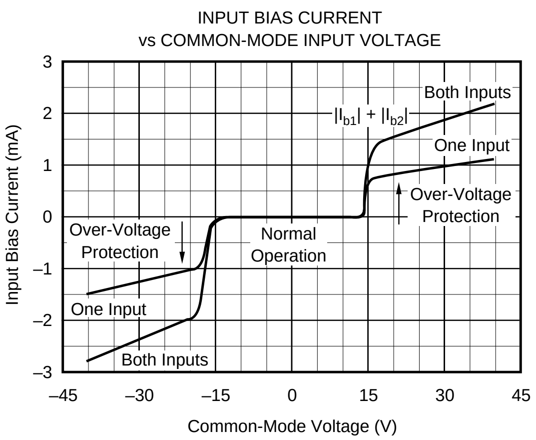
At T_A = +25°C, V_S = ±15V, unless otherwise noted.

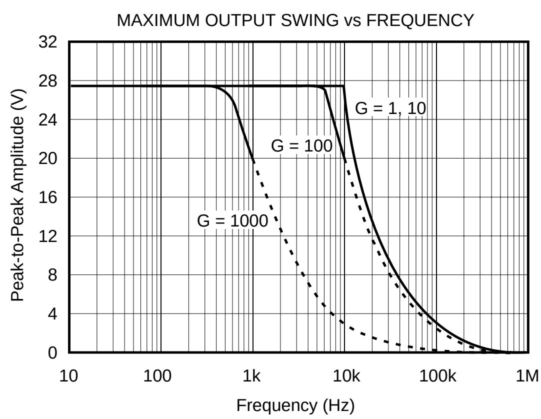






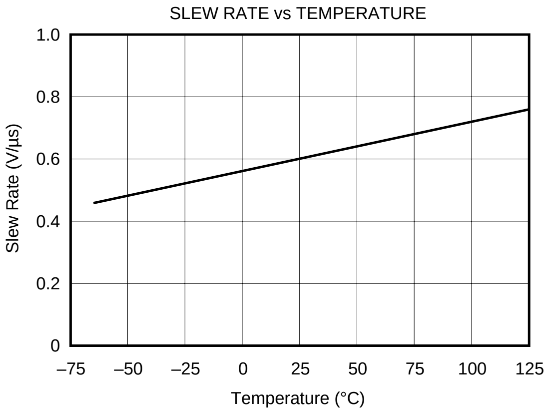


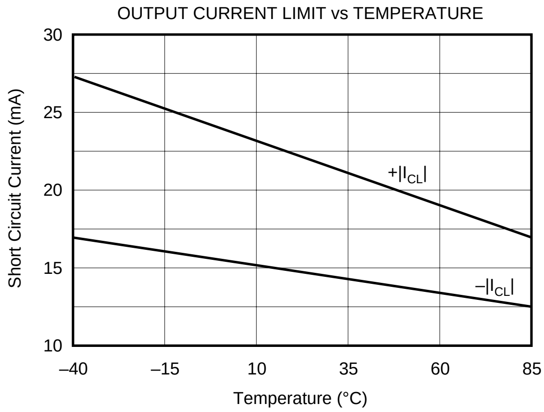


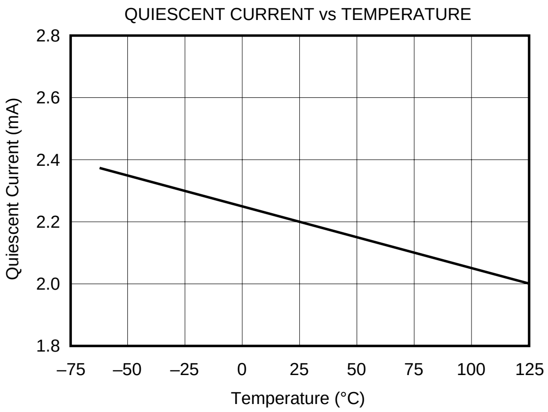


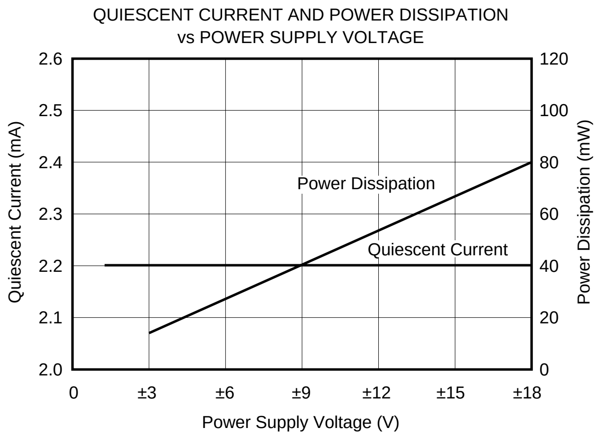
TYPICAL PERFORMANCE CURVES (CONT)

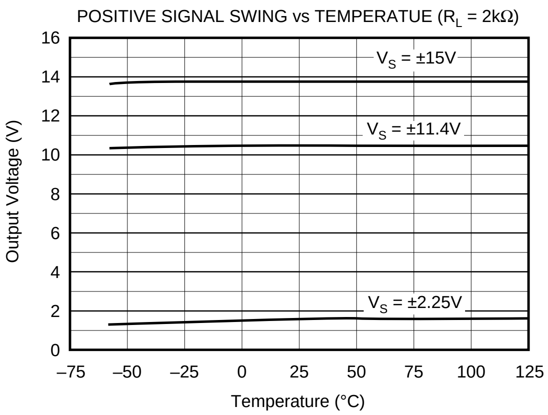
At T_A = +25°C, V_S = ±15V, unless otherwise noted.

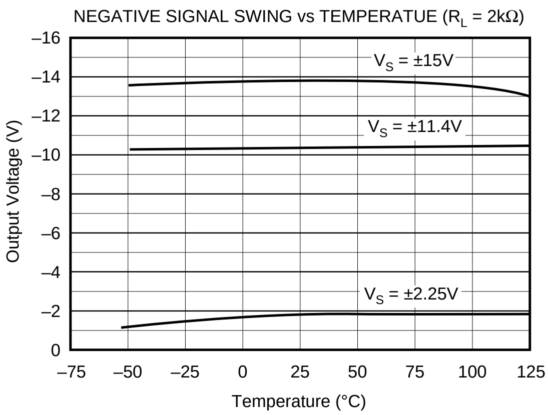








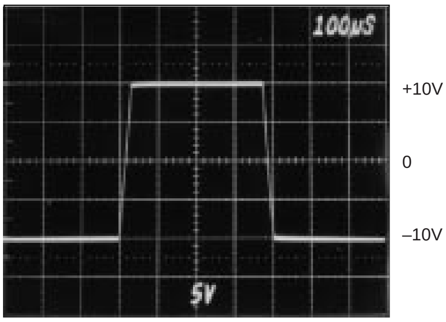




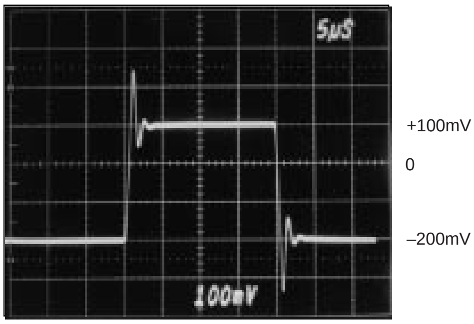
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

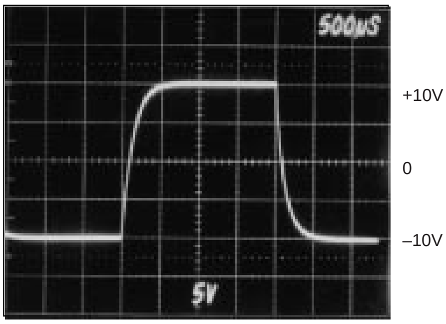
LARGE SIGNAL RESPONSE, G = 1



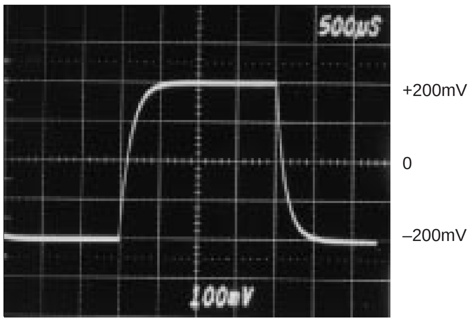
SMALL SIGNAL RESPONSE, G = 1



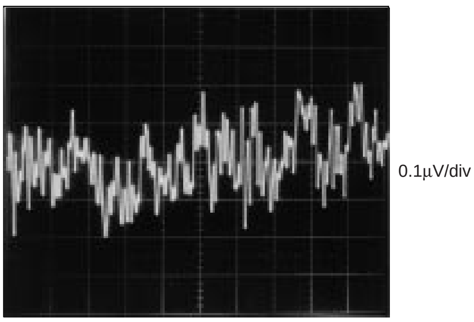
LARGE SIGNAL RESPONSE, G = 1000



SMALL SIGNAL RESPONSE, G = 1000



INPUT-REFERRED NOISE, 0.1 to 10Hz



1 s/div

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50\ k\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

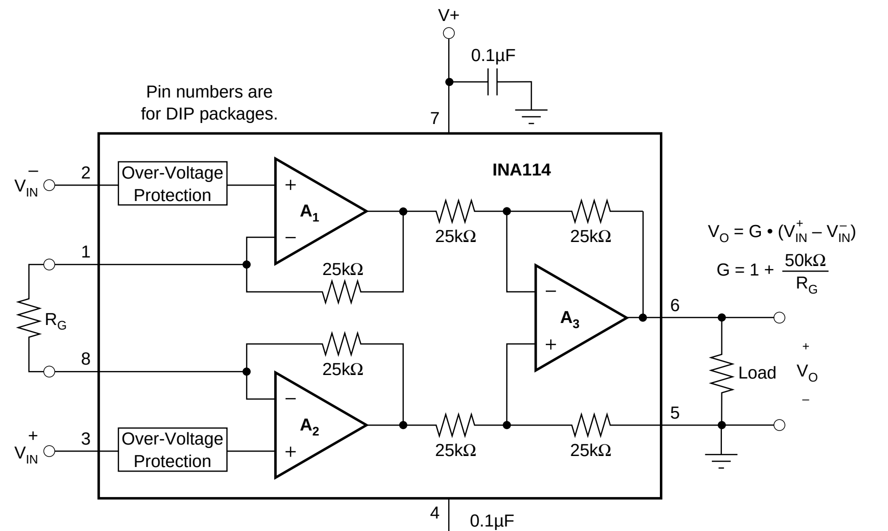
The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

Also drawn in simplified form:

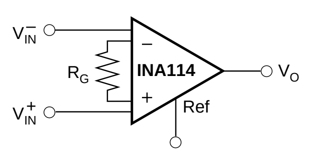


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

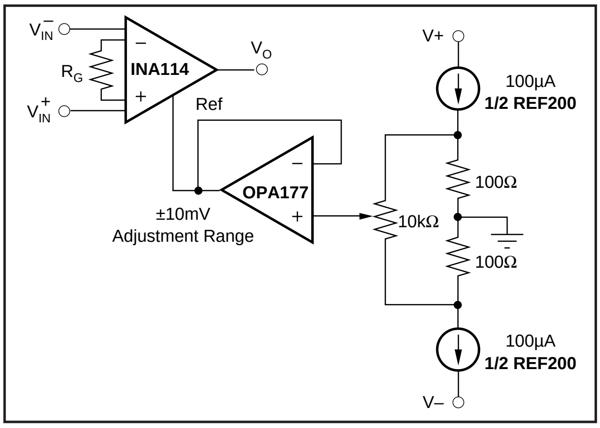


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

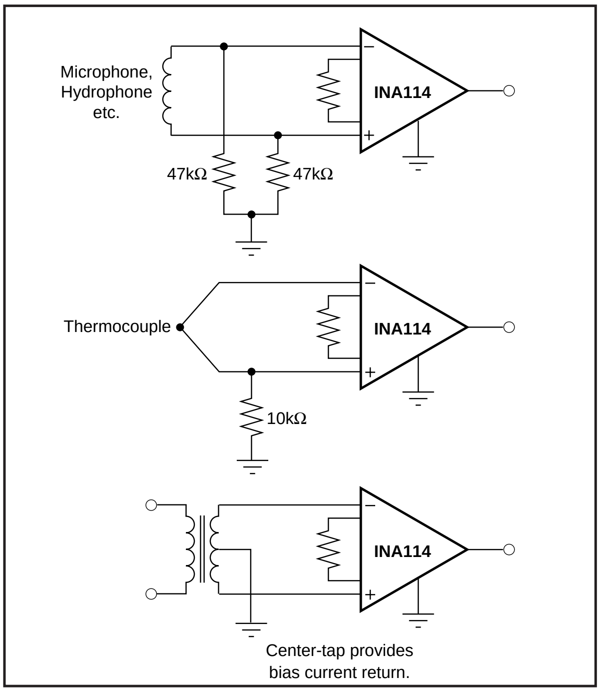


FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).

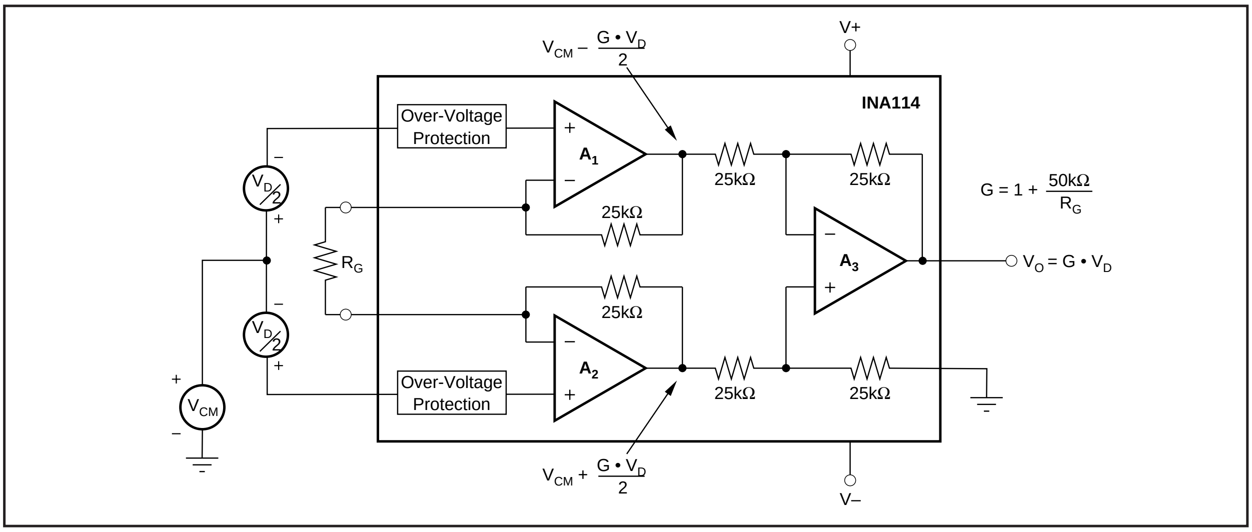


FIGURE 4. Voltage Swing of A_1 and A_2.

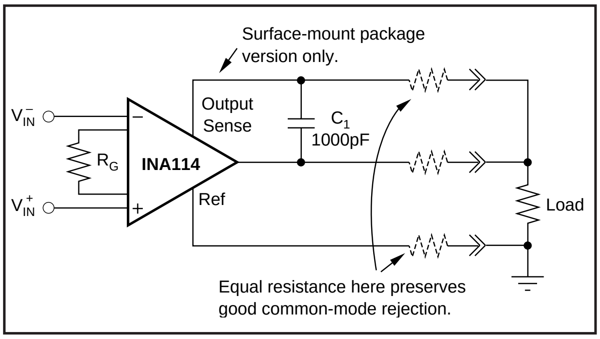


FIGURE 5. Remote Load and Ground Sensing.

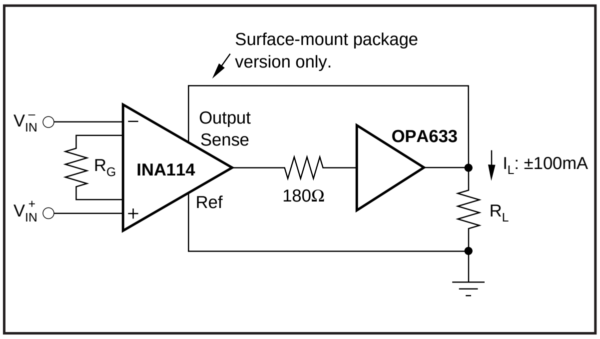


FIGURE 6. Buffered Output for Heavy Loads.

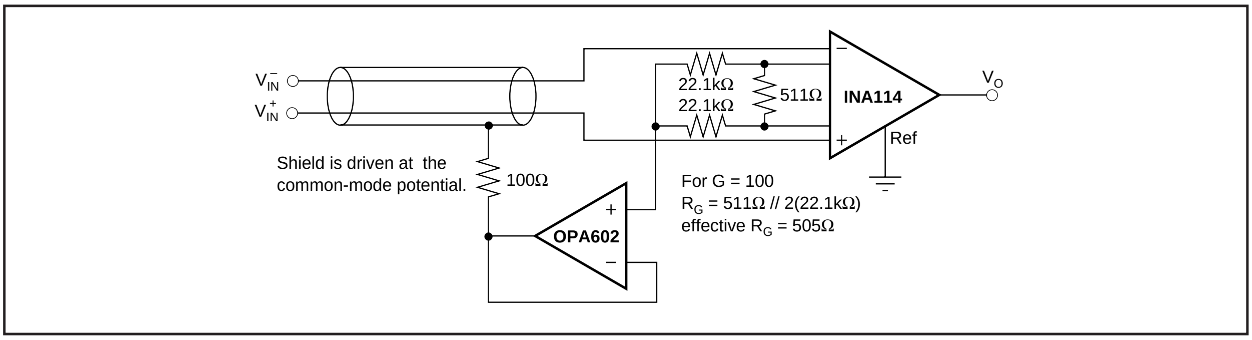


FIGURE 7. Shield Driver Circuit.

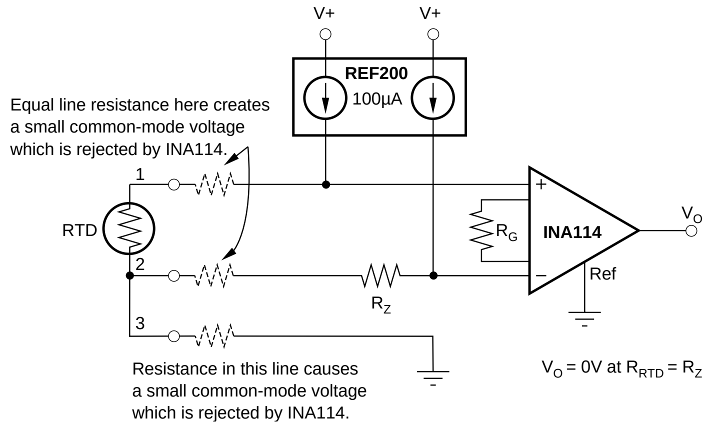
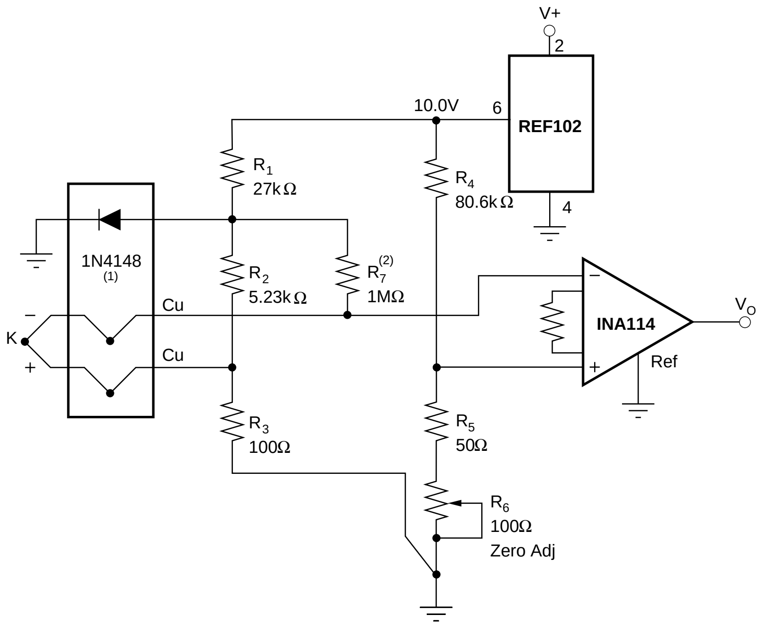


FIGURE 8. RTD Temperature Measurement Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200μA. (2) R_7 provides down-scale burn-out indication.

FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

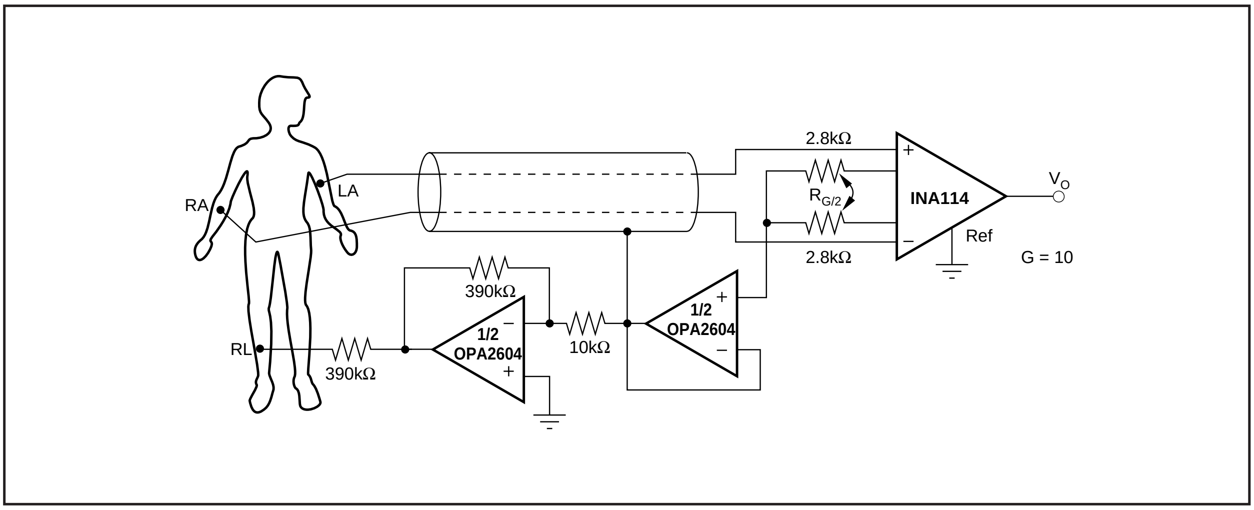


FIGURE 10. ECG Amplifier With Right-Leg Drive.

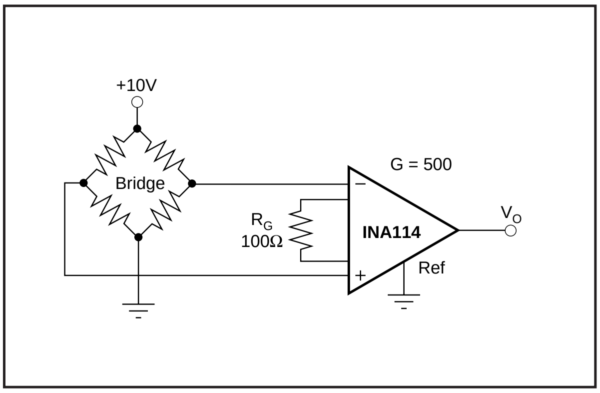


FIGURE 11. Bridge Transducer Amplifier.

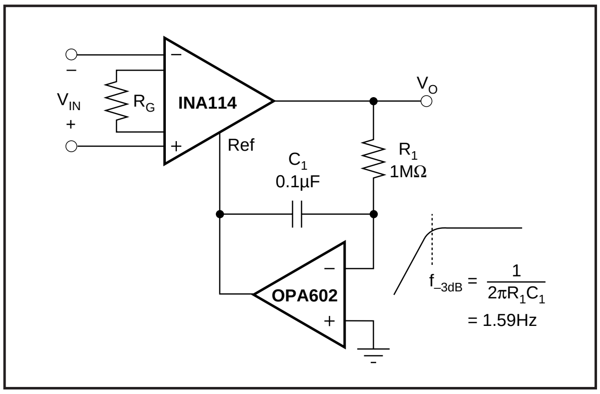
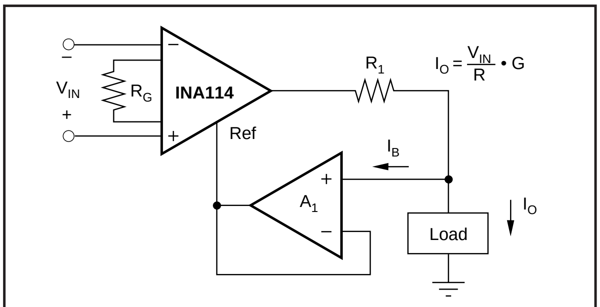


FIGURE 12. AC-Coupled Instrumentation Amplifier.



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

FIGURE 13. Differential Voltage-to-Current Converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA114AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA114AP	Samples
INA114APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA114AP	Samples
INA114AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114AU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114AUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114AUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114BP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA114BP	Samples
INA114BPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA114BP	Samples
INA114BU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		INA114BU	Samples
INA114BU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		INA114BU	Samples
INA114BU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		INA114BU	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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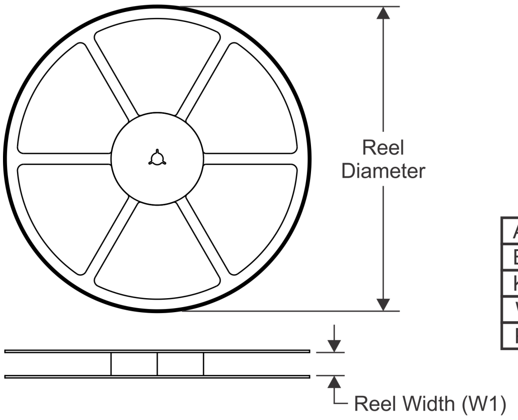
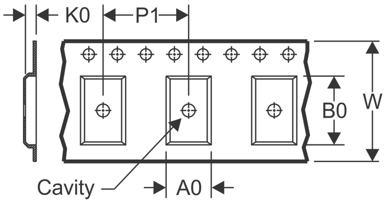
TAPE AND REEL INFORMATION

REEL DIMENSIONS

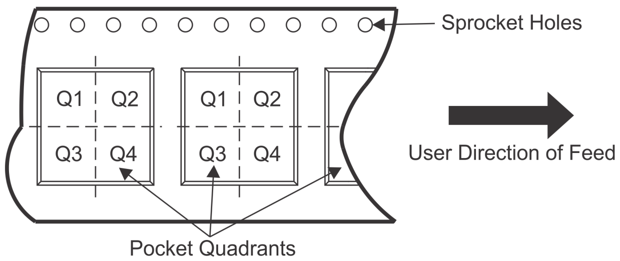


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

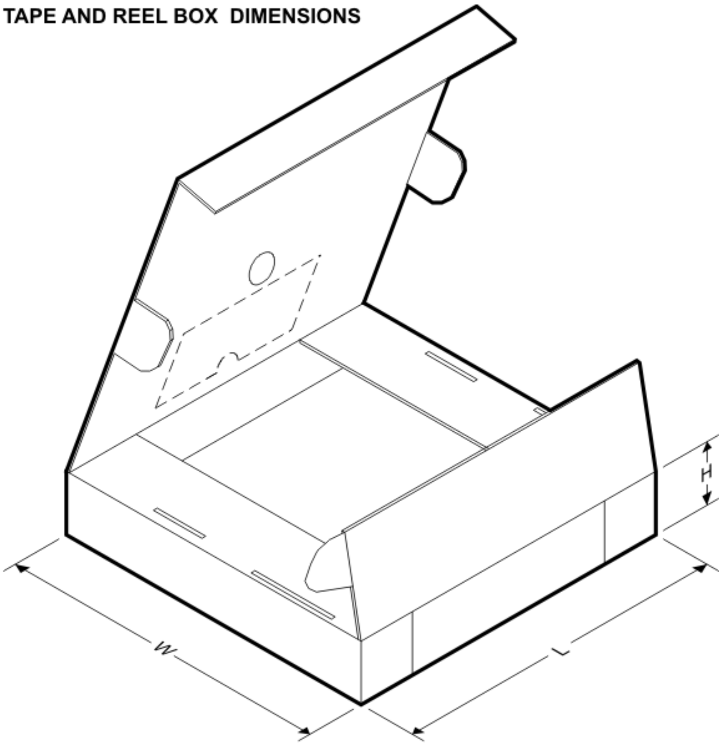
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA114AU/1K	SOIC	DW	16	1000	367.0	367.0	38.0

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
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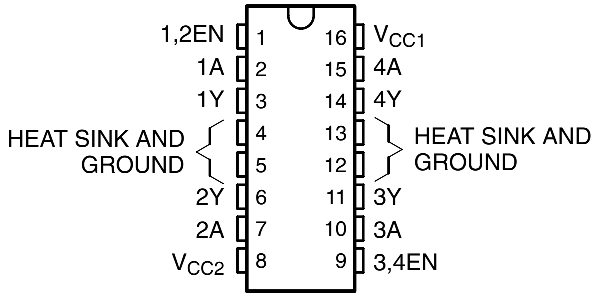
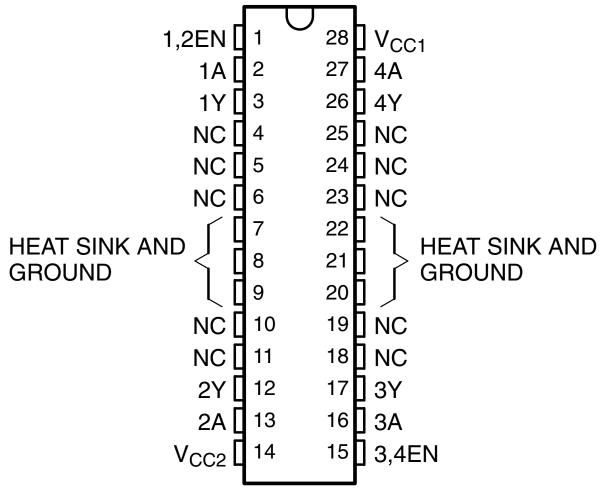
1.2 Motordriver - L293D

- **Featuring Unitrode L293 and L293D Products Now From Texas Instruments**
- **Wide Supply-Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Internal ESD Protection**
- **Thermal Shutdown**
- **High-Noise-Immunity Inputs**
- **Functionally Similar to SGS L293 and SGS L293D**
- **Output Current 1 A Per Channel (600 mA for L293D)**
- **Peak Output Current 2 A Per Channel (1.2 A for L293D)**
- **Output Clamp Diodes for Inductive Transient Suppression (L293D)**

L293 . . . N OR NE PACKAGE
L293D . . . NE PACKAGE
(TOP VIEW)



L293 . . . DWP PACKAGE
(TOP VIEW)



description/ordering information

The L293 and L293D are quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL compatible. Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	HSOP (DWP)	Tube of 20	L293DWP	L293DWP
	PDIP (N)	Tube of 25	L293N	L293N
	PDIP (NE)	Tube of 25	L293NE	L293NE
		Tube of 25	L293DNE	L293DNE

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

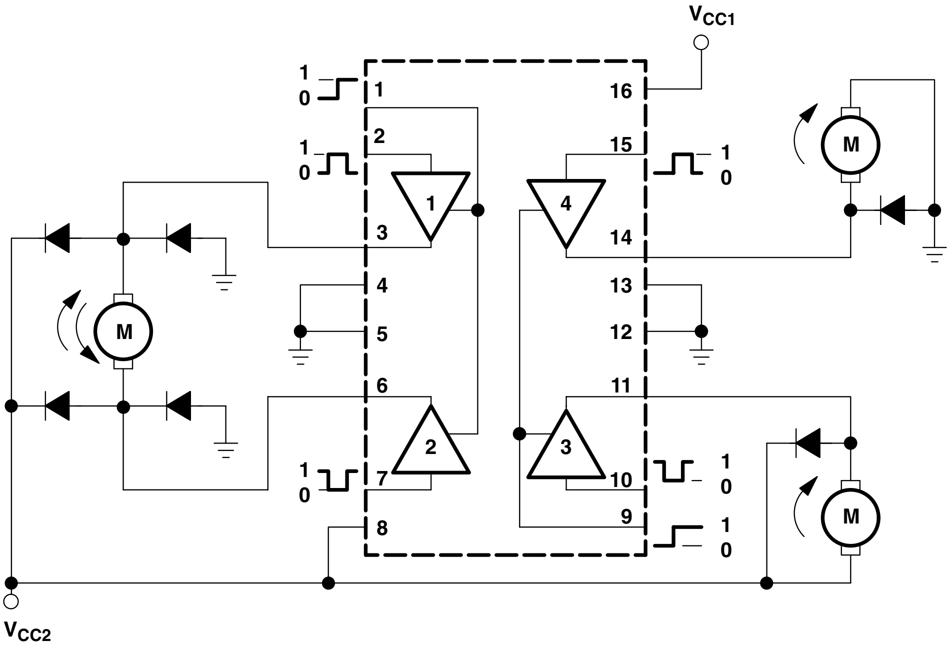
description/ordering information (continued)

On the L293, external high-speed output clamp diodes should be used for inductive transient suppression.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

The L293and L293D are characterized for operation from 0°C to 70°C.

block diagram



NOTE: Output diodes are internal in L293D.

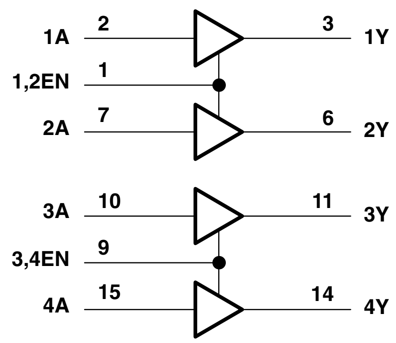
FUNCTION TABLE
(each driver)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

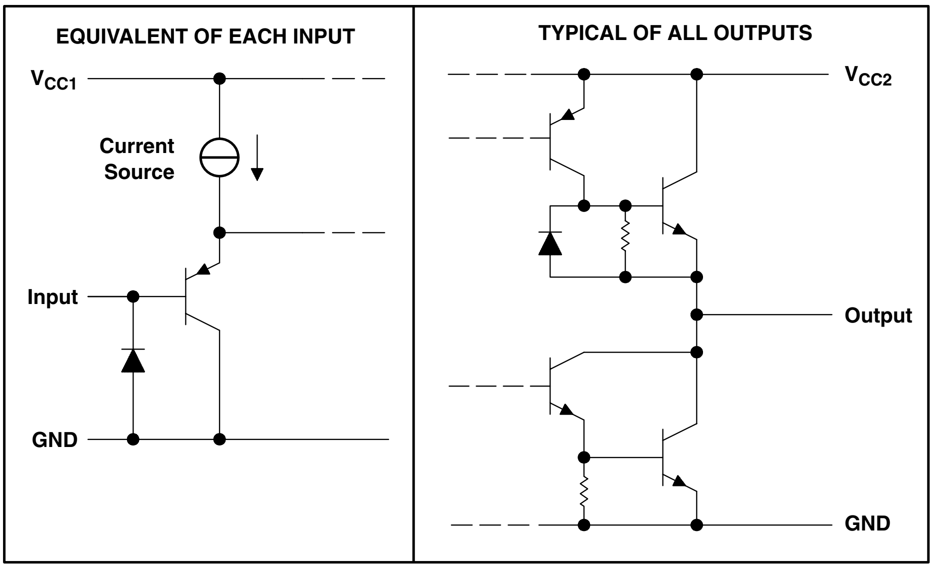
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† In the thermal shutdown mode, the output is in the high-impedance state, regardless of the input levels.

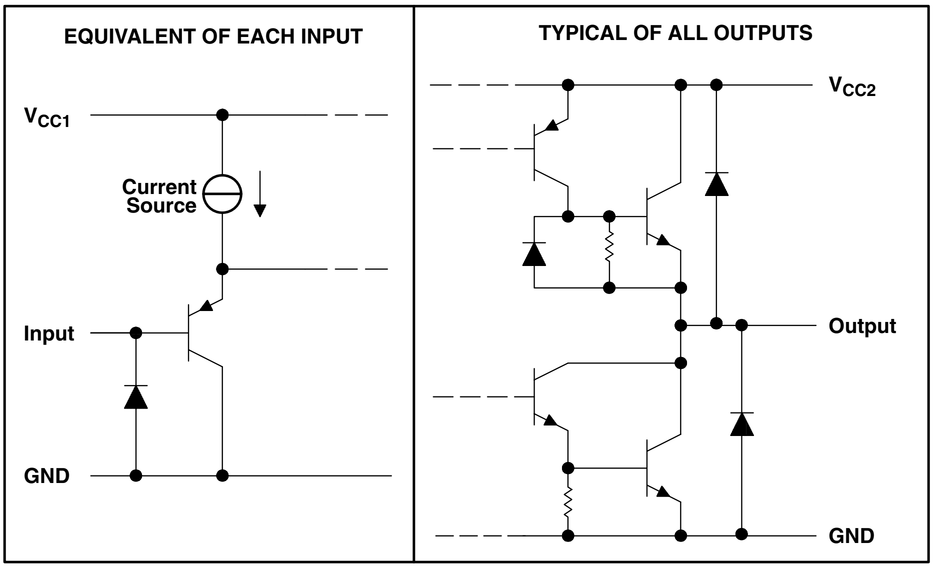
logic diagram



schematics of inputs and outputs (L293)



schematics of inputs and outputs (L293D)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1} (see Note 1)	36 V
Output supply voltage, V_{CC2}	36 V
Input voltage, V_I	7 V
Output voltage range, V_O	–3 V to V_{CC2} + 3 V
Peak output current, I_O (nonrepetitive, $t \le 5$ ms): L293	±2 A
Peak output current, I_O (nonrepetitive, $t \le 100$ µs): L293D	±1.2 A
Continuous output current, I_O: L293	±1 A
Continuous output current, I_O: L293D	±600 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DWP package	TBD°C/W
N package	67°C/W
NE package	TBD°C/W
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
	Supply voltage	V_{CC1}	4.5	7	V
		V_{CC2}	V_{CC1}	36	
V_{IH}	High-level input voltage	$V_{CC1} \le 7$ V	2.3	V_{CC1}	V
		$V_{CC1} \ge 7$ V	2.3	7	V
V_{IL}	Low-level output voltage		–0.3†	1.5	V
T_A	Operating free-air temperature		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		L293: I_{OH} = –1 A L293D: I_{OH} = – 0.6 A		V_{CC2} – 1.8	V_{CC2} – 1.4		V
V_{OL}	Low-level output voltage		L293: I_{OL} = 1 A L293D: I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		L293D: I_{OK} = – 0.6 A			V_{CC2} + 1.3		V
V_{OKL}	Low-level output clamp voltage		L293D: I_{OK} = 0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	10	
I_{IL}	Low-level input current	A	V_I = 0			–3	–10	μA
		EN				–2	–100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

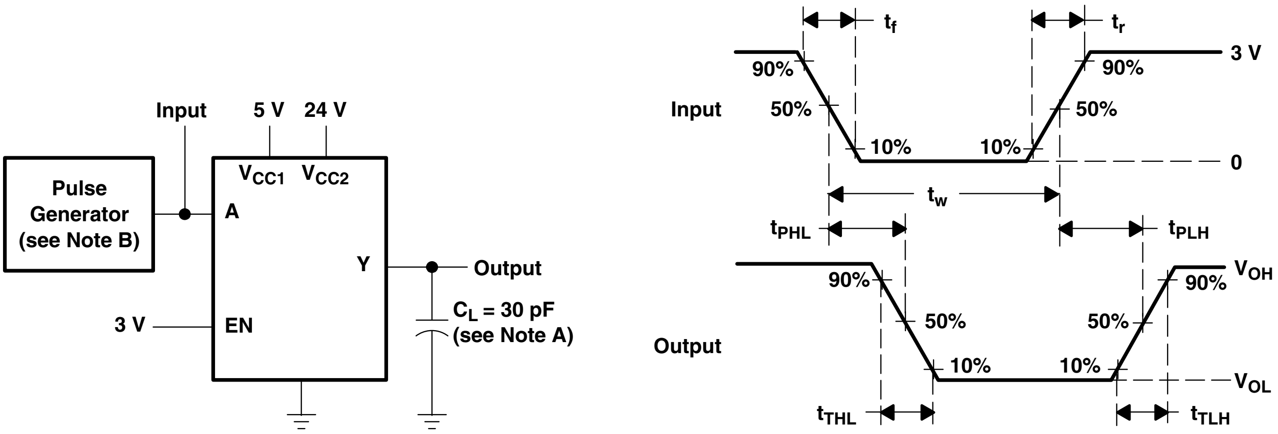
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293NE, L293DNE			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293DWP, L293N L293DN			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			200		ns
t_{TLH}	Transition time, low-to-high-level output			100		ns
t_{THL}	Transition time, high-to-low-level output			350		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ µs, PRR = 5 kHz, $Z_O = 50\ \Omega$.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

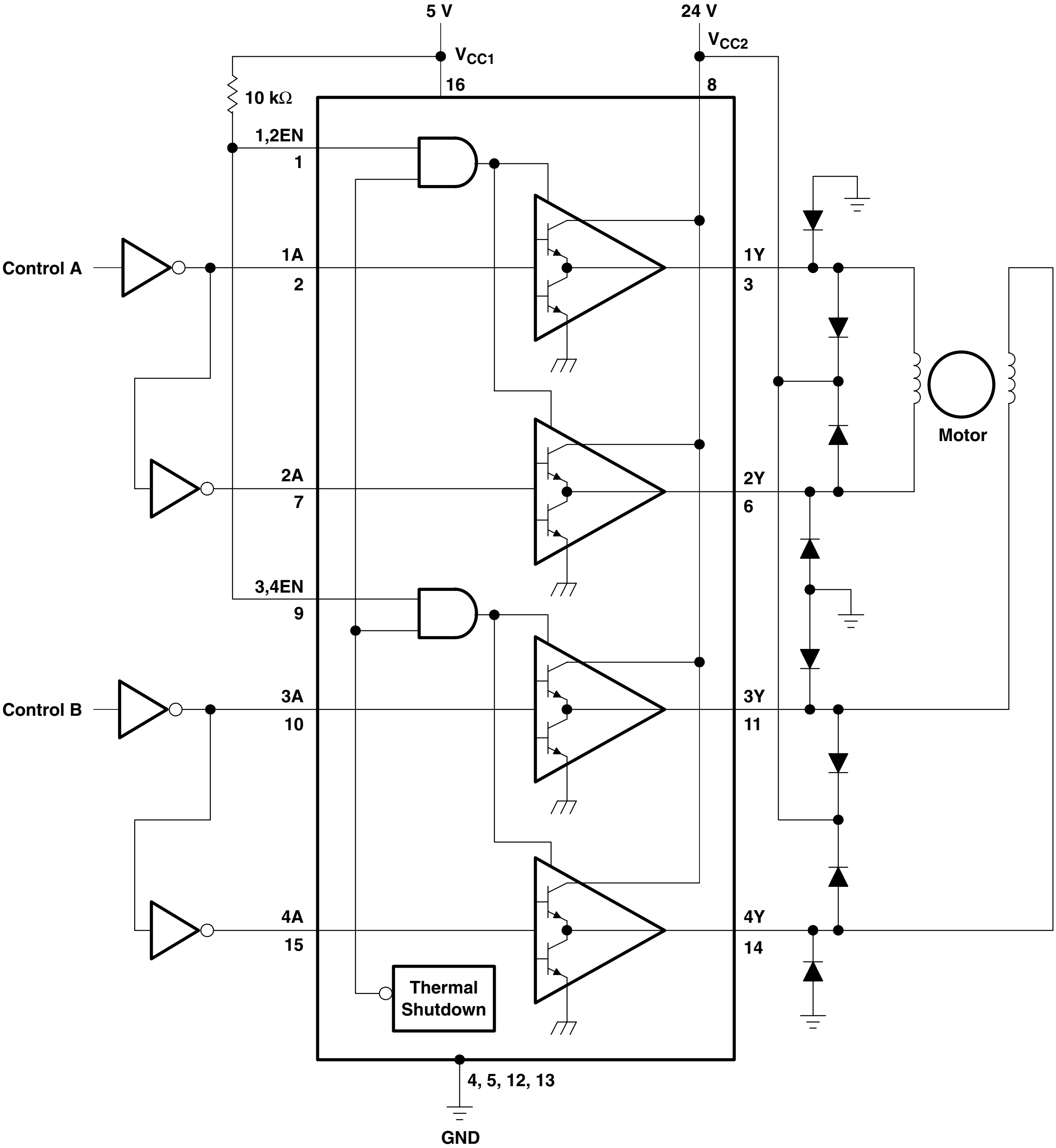


Figure 2. Two-Phase Motor Driver (L293)

APPLICATION INFORMATION

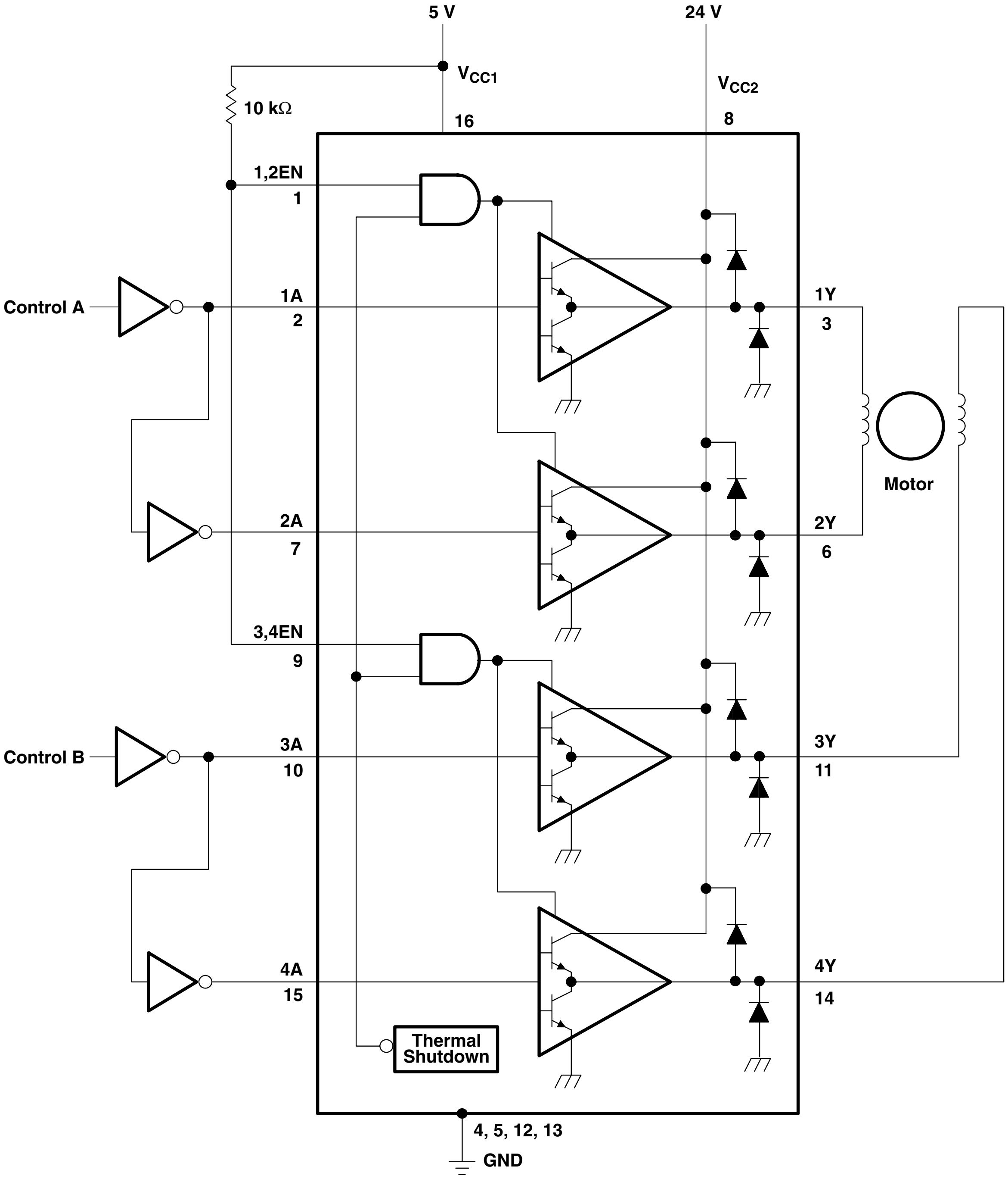
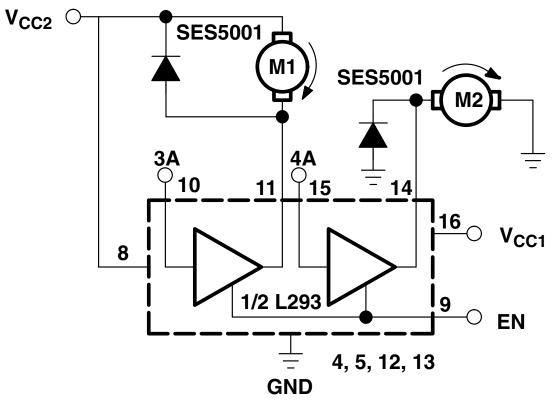


Figure 3. Two-Phase Motor Driver (L293D)

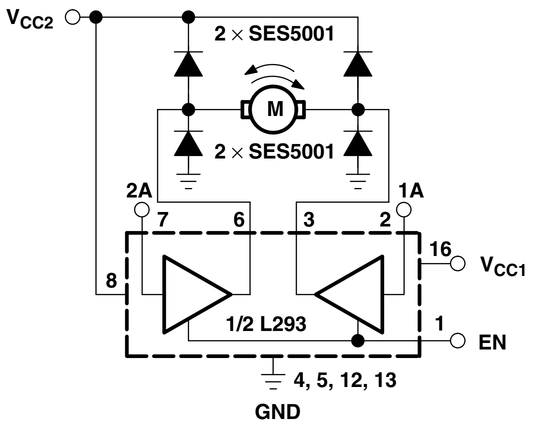
APPLICATION INFORMATION



EN	3A	M1	4A	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free-running motor stop	X	Free-running motor stop

L = low, H = high, X = don't care

Figure 4. DC Motor Controls (connections to ground and to supply voltage)



EN	1A	2A	FUNCTION
H	L	H	Turn right
H	H	L	Turn left
H	L	L	Fast motor stop
H	H	H	Fast motor stop
L	X	X	Fast motor stop

L = low, H = high, X = don't care

Figure 5. Bidirectional DC Motor Control

APPLICATION INFORMATION

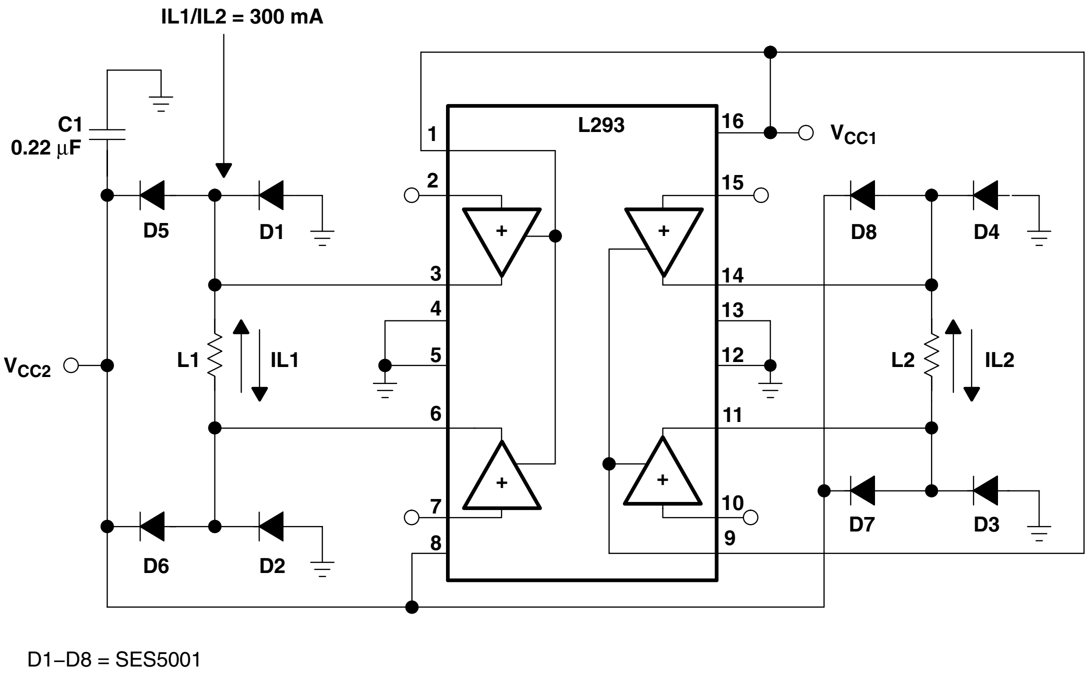


Figure 6. Bipolar Stepping-Motor Control

mounting instructions

The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

Figure 9 shows the maximum package power P_{TOT} and the θ_{JA} as a function of the side ℓ of two equal square copper areas having a thickness of 35 µm (see Figure 7). In addition, an external heat sink can be used (see Figure 8).

During soldering, the pin temperature must not exceed 260°C, and the soldering time must not exceed 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

APPLICATION INFORMATION

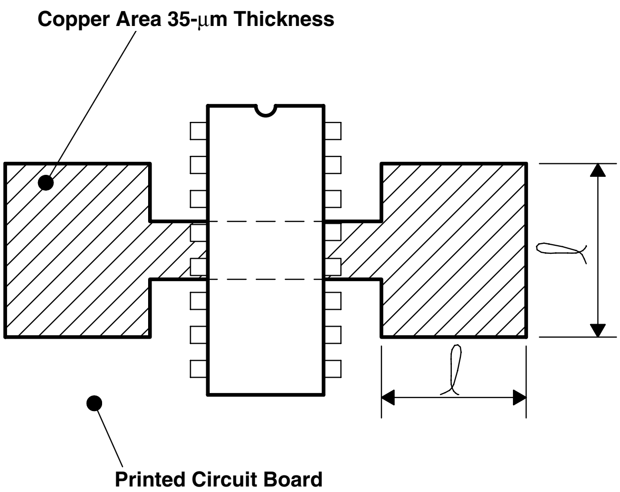


Figure 7. Example of Printed Circuit Board Copper Area (used as heat sink)

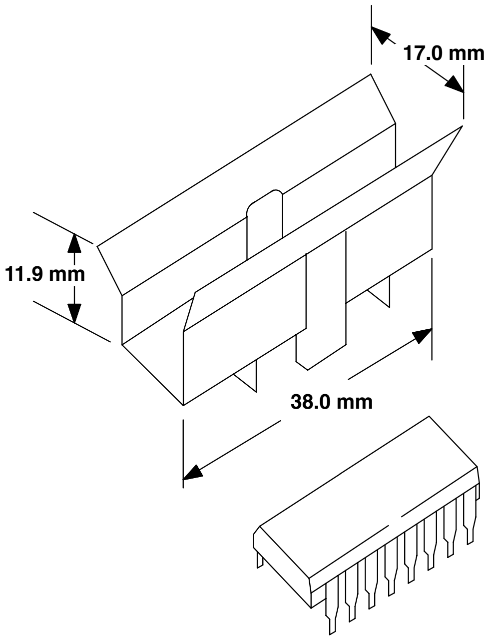


Figure 8. External Heat Sink Mounting Example (θ_{JA} = 25°C/W)

APPLICATION INFORMATION

MAXIMUM POWER AND JUNCTION vs THERMAL RESISTANCE

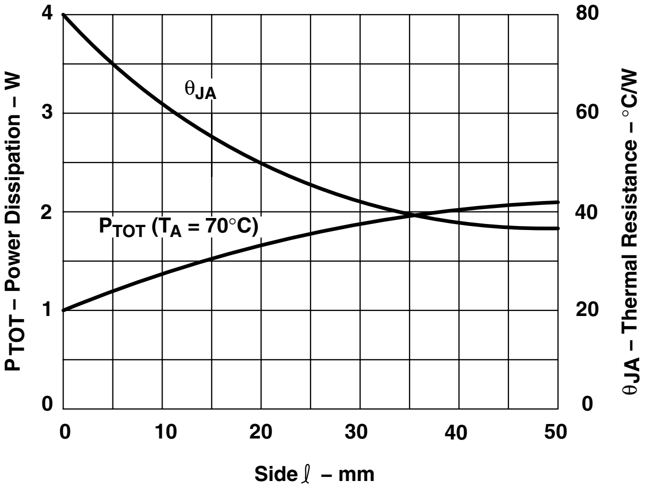


Figure 9

MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE

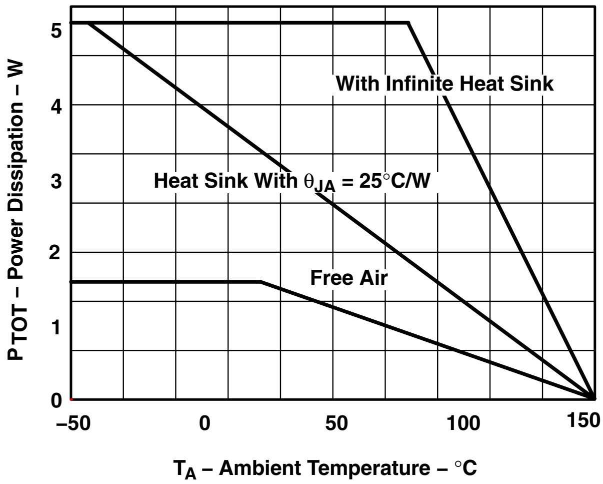


Figure 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
L293DNE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293DNE	Samples
L293DNEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293DNE	Samples
L293DWP	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70	L293DWP	
L293DWPG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70		
L293DWPTR	OBSOLETE	SO PowerPAD	DWP	28		TBD	Call TI	Call TI	0 to 70		
L293N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70	L293N	
L293NE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293NE	Samples
L293NEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293NE	Samples
L293NG4	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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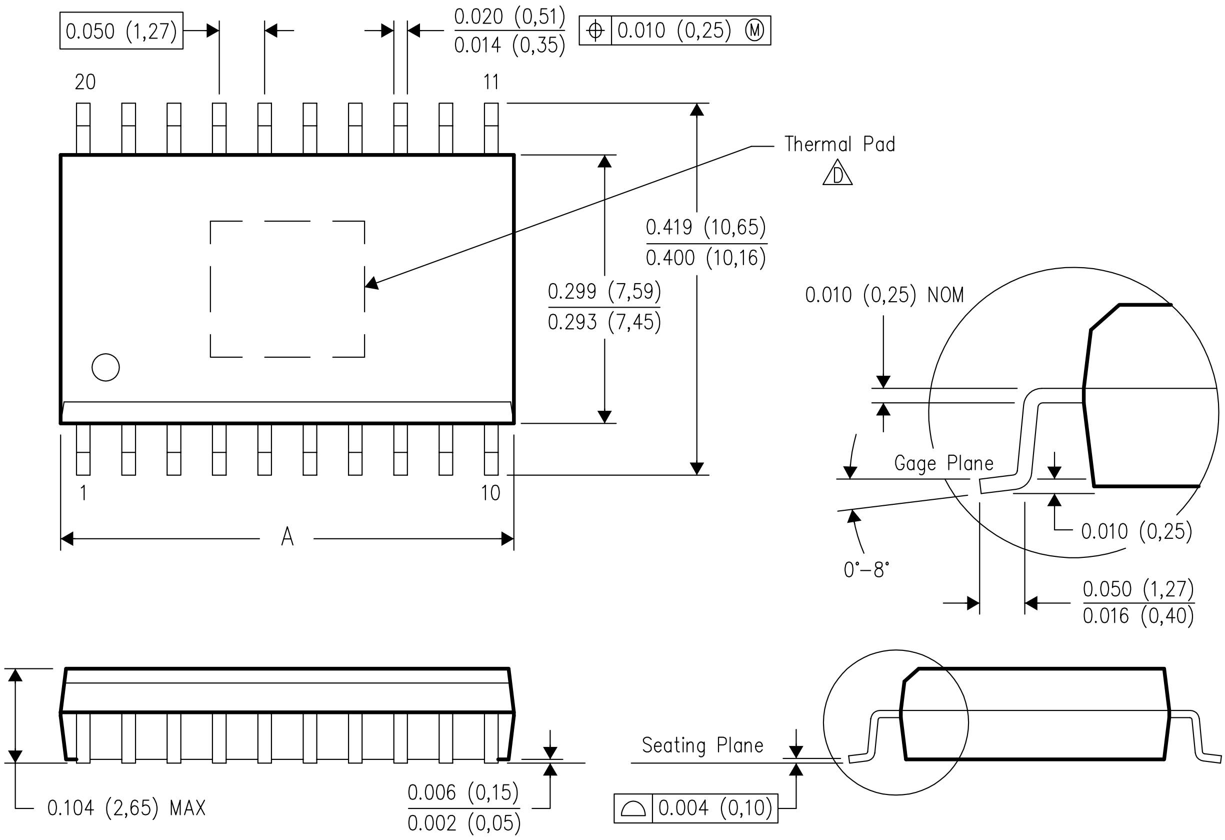
DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN

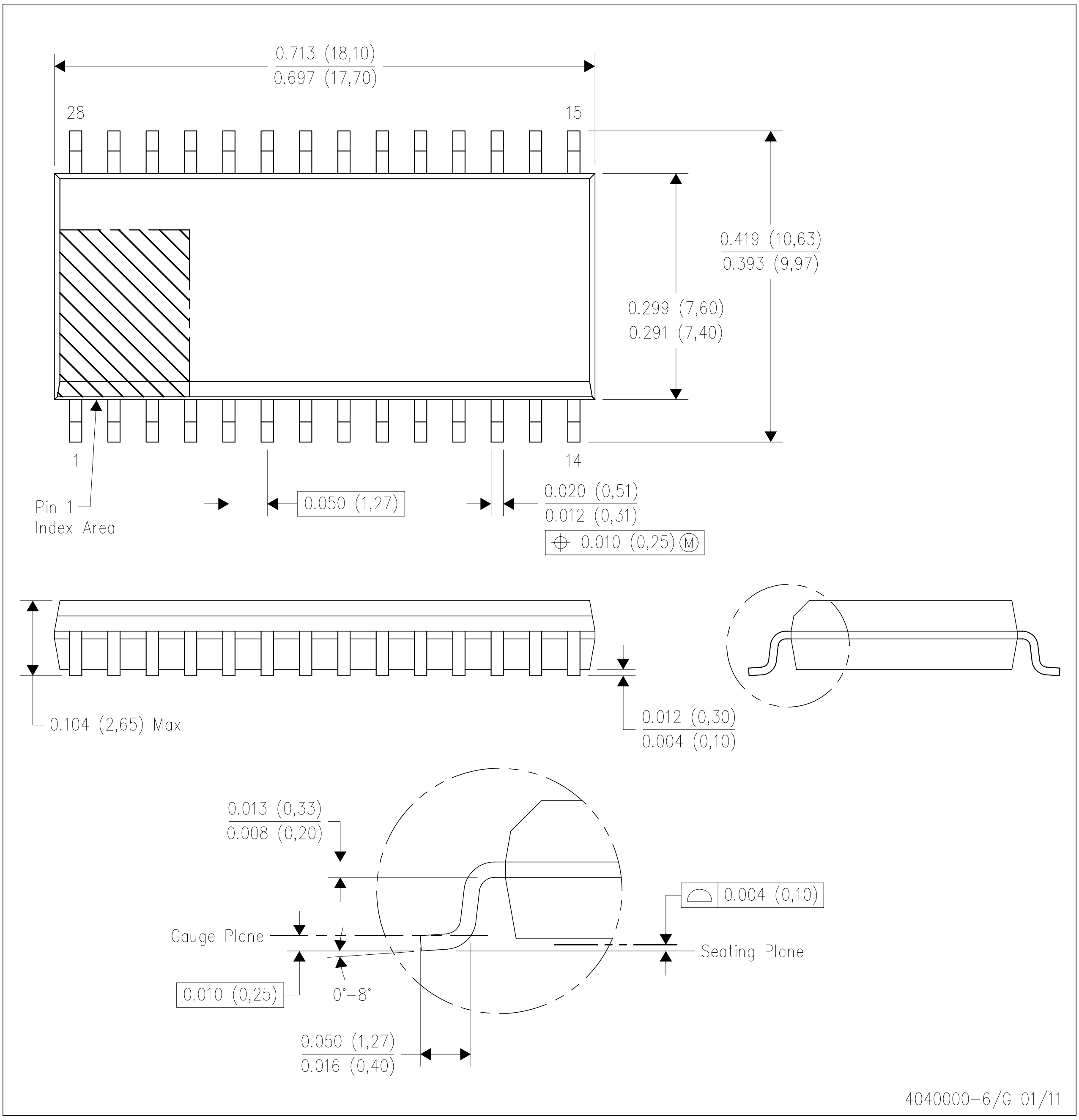


DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

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Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

1.3 Kameralys - L5-W55N-BVW

Series L5 / Ø 5mm

Colour: white

Sloan Part No.: L5-W55N-BVW

Electrical and Optical Characteristics (T_A = 25°C)

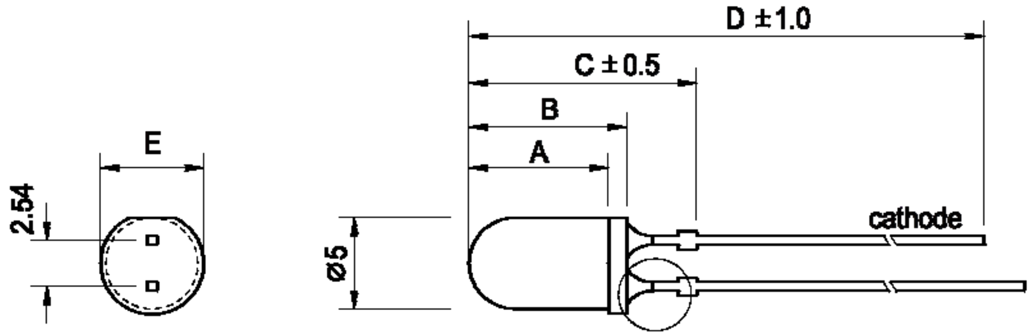
Chip			Lens	Absolute Maximum Ratings				Electro-Optical-Data's **at 20mA**					Viewing Angle
Emitted Colour	Chromaticity Coordinates	Colour Temperature (°K)		Δλ (nm)	Pd (mW)	If (mA)	Peak If (mA)	Forward Voltage Vf (V)		Luminous Intensity Iv (mcd)			2 θ ½ (deg)
								typ.	max.	min.	typ.	max.	
white	x=0.30-0.33 y=0.28-0.32	5500-9000	water clear	-	105	30	100*	3.2	3.5	22'000	33'000	44'000	15°

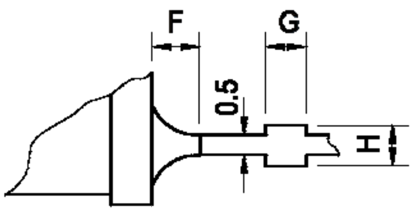
* Peak Forward Current (1/10 Duty Cycle, 10ms Pulse Width)

Absolute Maximum Ratings (T_A = 25°C)

Reverse Voltage	5V
Reverse Current (V_R = 5V)	≤50μA
Operating Temperature Range	- 30°C ~ +85°C
Storage Temperature Range	- 40°C ~ +100°C
Lead Soldering Temperature	265°C for 10 seconds

Package Dimensions





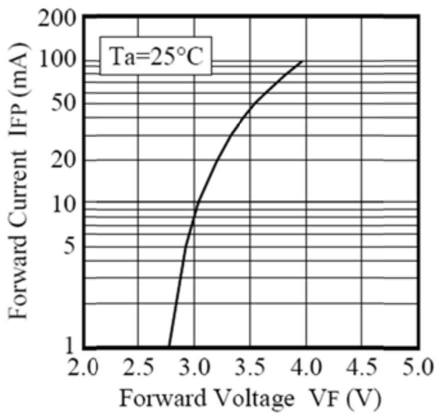
Measurements of Drawing								
	A	B	C	D	E	F	G	H
mm	7.6	8.6	12.4	28.9	5.6	1.5	1.0	1.1

1. All dimensions are in millimetres.
2. Tolerance is ±0.25mm unless otherwise specified.
3. Lead spacing is measured where the leads emerge from the package
4. Specifications are subject to change without notice.

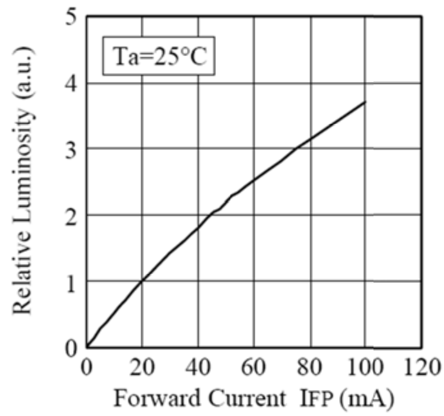
Sloan Part No.: L5-W55N-BVW

Electrical and Optical Characteristics ($T_A = 25°C$)

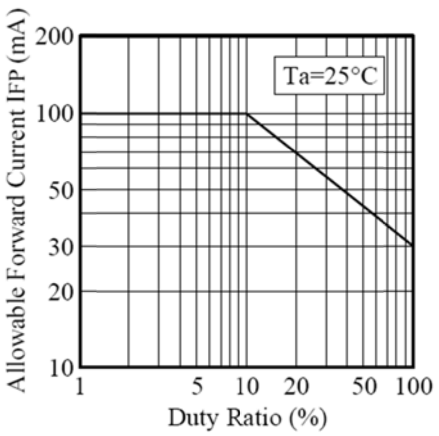
**Forward Voltage vs.
Forward Current**



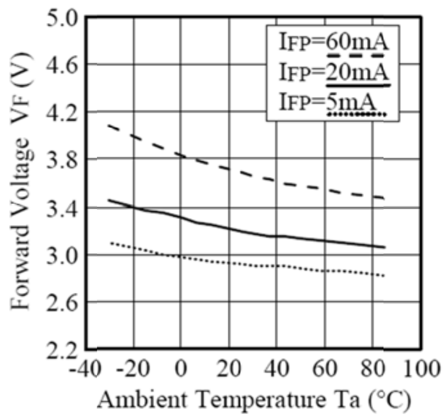
**Forward Current vs.
Relative Luminosity**



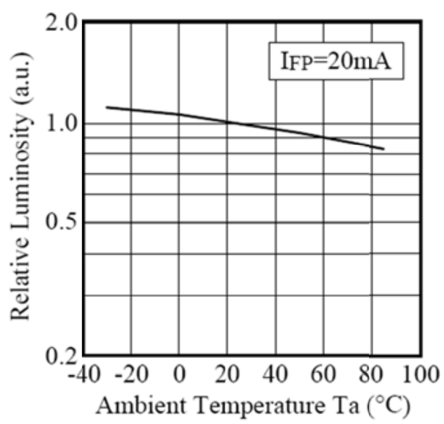
**Duty Ratio vs.
Allowable Forward Current**



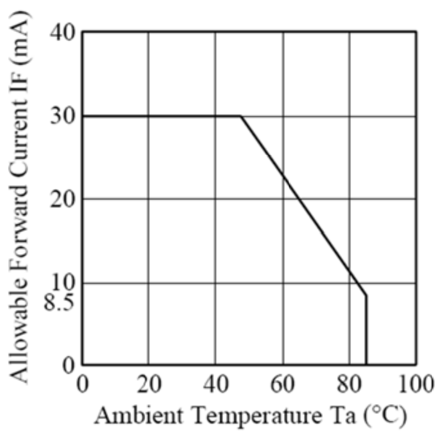
**Ambient Temperature vs.
Forward Voltage**



**Ambient Temperature vs.
Relative Luminosity**



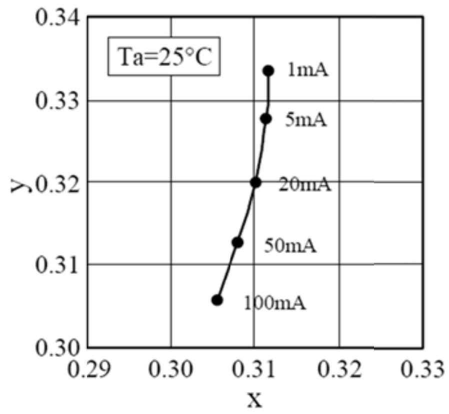
**Ambient Temperature vs.
Allowable Forward Current**



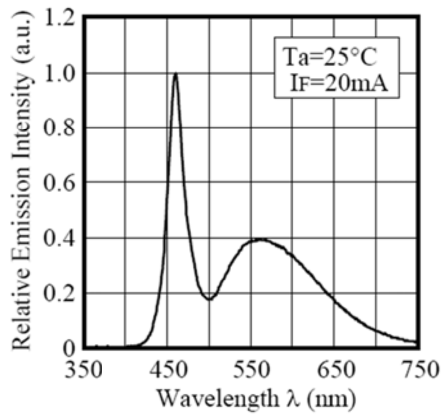
Sloan Part No.: L5-W55N-BVW

Electrical and Optical Characteristics (T_A = 25°C)

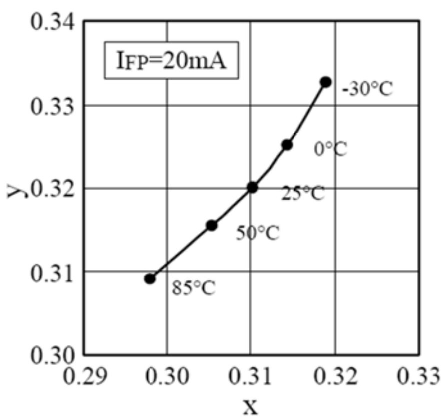
**Forward Current vs.
Chromaticity Coordinate**



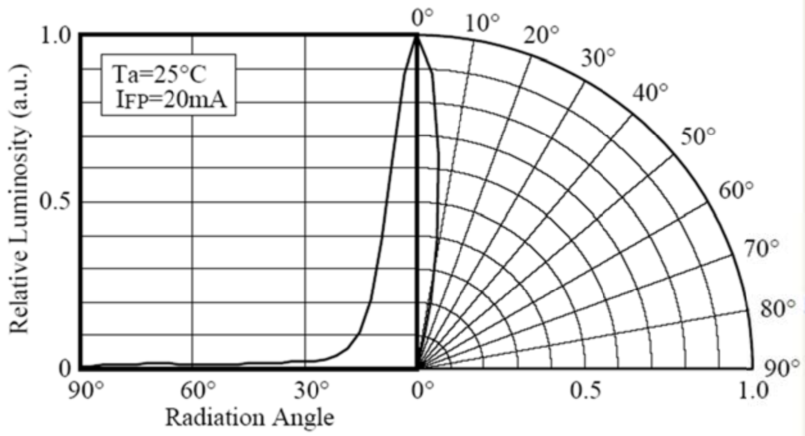
Spectrum



**Ambient Temperature vs.
Chromaticity Coordinate**



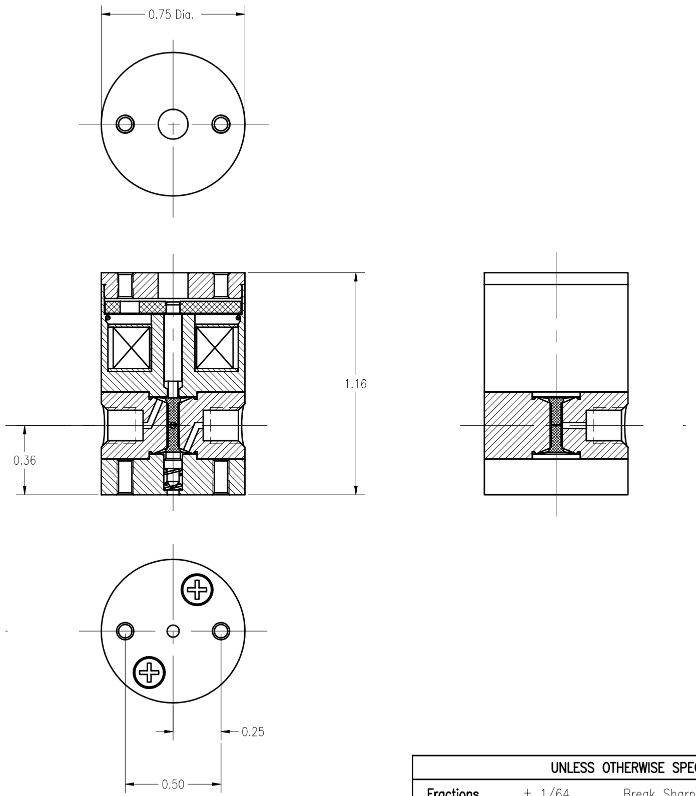
Directivity



Recommended Soldering Conditions:

Dip Soldering		Hand Soldering	
Pre-Heat Pre-Heat Time Solder Bath Temperature Dipping Time Dipping Position	120°C Max. 60 seconds Max. 260°C Max. 10 seconds Max. No lower than 3 mm from the base of the epoxy bulb.	Temperature Soldering Time Position	350°C Max. 3 seconds Max. No closer than 3 mm from the base of the epoxy bulb.

1.4 Ventil - 161T031



SPECIFICATIONS:

Mechanical: (Each Port)

TYPE: 3w diverter
PORT CONNECTION: #10-32 Flat bottom.
NOMINAL ORIFICE: 0.040 In. (1.0 mm)
OPERATING PRESSURE: Vacuum to 30 PSI (2 Bars)
TEST PRESSURE: 30 PSI N_2 (Less than 3μl/Min. Leakage.)
INTERNAL VOLUME: 27 microliters total from bottom of ports.
WETTED MATERIALS: TEFLON®
MOUNTING ORIENTATION: Any Position

Electrical: (At 70° F No Pressure Applied)

OPERATING VOLTAGE: 12 VDC
12 to 24 VDC subject to duty cycle and / or holding voltage applied.
POWER CONSUMPTION: 1.13 Watts at 12 VDC (Approximately)
LEAD WIRES: #26 AWG, TFE Insulated
Yellow 12 Inches (305mm) long.
TEST VOLTAGE (ON): < 9 VDC
TEST VOLTAGE (OFF): 0.5 to 4 VDC
RESPONSE TIME (ON): < 20ms at 12 VDC
5 to 20 ms subject to applied voltage and driving circuits.
RESPONSE TIME (OFF): < 30ms from 12 VDC
30 to 5 ms adjustable by driving circuits.

NOTE 1.)
Continuos rating applies to solenoid construction only. Since other materials incorporated in the product may not tolerate temperature variations as well as the solenoid application of holding voltage is strongly reccommended.

NOTICE:
This product is protected by one or more of the following United States Patents: 4,496,133; 4,993,456; 5,143,118; Re. 34,261 5,433,244. Other Patents Pending.

UNLESS OTHERWISE SPECIFIED			Scale 2 : 1 (B)	Material As noted	NResearch Incorporated
Fractions	± 1/64	Break Sharp Edges 0.003-0.008	**Dr. By** A. Sule	**Date** 07-23-1995	
2 Pl. Dec.	± 0.005	All Small Fin. Radii 0.003-0.008	**Rev. By** F.Tarnok	**Date** 04-21-2010	
3 Pl. Dec.	± 0.002	All surfaces shall be Concentric,	**Part Name**		**Drawing Number**
Angular	± 0.06°	Parallel, Flat, Square and True	.161T031 3w 12vdc		.161V258
All Fin. Surf.		to Each Other within 0.001 T.I.R.			

Rettelser

Bilag A

A.1 Datablade

A.1.1 INA114

A.1.2 L293D

A.1.3 L5-W55N-BVW

A.2 Matlab kode

Alt Matlab kode er vedlagt som .m filer i mappen ...

A.2.1 initArduino.m

A.2.2 cameraFeed.m

A.2.3 detectIslets.m

A.2.4 loadCell.m

A.3 Arduino Testkode

A.3.1 Kode til enhedstest til vægtcelle.pdf

A.3.2 Kode til enhedstest til pumpe.pdf

A.3.3 Kode til enhedstest til ventil.pdf

A.4 Mødereferater

A.4.1 Vejledermøder

A.4.2 Kundemøder

A.4.3 Reviewmøder

A.5 Mail korrespondancer

A.5.1 Kunde

A.5.2 Vejleder

A.5.3 Leverandør

A.5.4 Andre

A.6 Fejlrapport

A.7 Logbøger

A.8 Samarbejdsaftale