ZD <=> BD, ZA<=>BA, ZC<=>BC Buffer States

In the following...

ZD: Z80 Data
ZA: Z80 Address
ZC: Z80 Control (MREQ, IORQ, WR, RD)
BD: Bus (expansion) Data
BA: Bus Address
BC: Bus Control
MB: Main Board Device
EB: Expansion Board Device (on the Bus)
Required: This must occur
Allowed: This can occur (it will not bother anything)
Prohibited: This is not allowed

Master	Operation	ZD<=>BD				ZA<=>BA				ZC<=>BC			
		Required	Allowed	Prohibited	Valid nS (long path)	Required	Allowed	Prohibited	Valid nS (long path)	Required	Allowed	Prohibited	Valid nS (long path)
Z80 Master													
	MB Memory RD (IF, MR below 1M)		ZD => BD	BD <= ZD			ZA0-12+MHA13-23=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	BUS Memory RD (IF, MR above 1M)	BD => ZD		MB device on ZD	**52 (BUSMEM-)**	ZA0-12+MHA13-23=>BA				ZC=>BC			
	MB Memory WR (MW below 1M)		ZD => BD	BD => ZD			ZA0-12+MHA13-23=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	BUS Memory WR (MW above 1M)	ZD => BD		MB device on ZD	**52 (BUSMEM-)**	ZA0-12+MHA13-23=>BA				ZC=>BC			
	MB Refresh						ZA=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	MB I/O RD		ZD => BD	BD <= ZD			ZA0-15=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	BUS I/O RD	BD => ZD		MB device on ZD	52 (BUSIO-)	ZA0-15=>BA				ZC=>BC			
	MB I/O WR		ZD => BD	BD => ZD			ZA0-15=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	BUS i/O WR	ZD => BD			52 (BUSIO-)	ZA0-15=>BA				ZC=>BC			
	MB INT-ACK		ZD => BD				ZA0-15=>BA	BA<=ZA			ZC=>BC	BC<=ZC	
	BUS INT-ACK	BD => ZD			30 (IORQ-)		ZA0-15=>BA	BA<=ZA		ZC=>BC		BC<=ZC	
Master	**Operation**	**ZD<=>BD**				**ZA<=>BA**				**ZC<=>BC**			
BUS Master													
		Required	**Allowed**	**Prohibited**		**Required**	**Allowed**	**Prohibited**		**Required**	**Allowed**	**Prohibited**	
	MB Memory RD (IF, MR below 1M)	ZD => BD			44 (RD-)	BA=>ZA0-12+MHA13-23			**42 (LCLMEM-)**	BC=>ZC			**42 (LCLMEM-)**
	BUS Memory RD (IF, MR above 1M)		BD => ZD	ZD => BD			BA=>ZA0-12+MHA13-23	ZA=>BA			BC=>ZC	ZC=>BC	
	MB Memory WR (MW below 1M)	BD => ZD		MB Device on ZD	44 (WR-)	BA=>ZA0-12+MHA13-23			**42 (LCLMEM-)**	BC=>ZC			**42 (LCLMEM-)**
	BUS Memory WR (MW above 1M)		BD => ZD	ZD => BD			BA=>ZA0-12+MHA13-23	ZA=>BA			BC=>ZC	ZC=>BC	
	MB I/O RD	ZD => BD			44 (RD-)	BA=>ZA0-15			40 (LCLIO-)	BC=>ZC			
	BUS I/O RD		BD => ZD	ZD => BD			BA=>ZA0-15	ZA=>BA			BC=>ZC	ZC=>BC	42 (LCLMEM-)
	MB I/O WR	BD => ZD		MB Device on ZD	44 (WR-)	BA=>ZA0-15			40 (LCLIO-)	BC=>ZC			40 (LCLIO-)
	BUS i/O WR		BD => ZD	ZD => BD			BA=>ZA0-15	ZA=>BA			BC=>ZC	ZC=>BC	
	MB INT-ACK	ZD => BD			30 (IORQ-)		BA=>ZA0-15	ZA=>BA		BC=>ZC			40 (LCLIO-)
	BUS INT-ACK		BD => ZD				BA=>ZA0-15	ZA=>BA			BC=>ZC	ZC=>BC	