**ZD <=> BD, ZA<=>BA, ZC<=>BC Buffer States**

In the following...

ZD: Z80 Data
ZA: Z80 Address
ZC: Z80 Control (MREQ, IORQ, WR, RD)
BD: Bus (expansion) Data
BA: Bus Address
BC: Bus Control
MB: Main Board Device
EB: Expansion Board Device (on the Bus)
**Required**: This must occur
**Allowed**: This can occur (it will not bother anything)
**Prohibited**: This is not allowed

| Master | Operation | ZD<=>BD | | | ZA<=>BA | | | ZC<=>BC | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Required | Allowed | Prohibited | Required | Allowed | Prohibited | Required | Allowed | Prohibited |
| **Z80 Master** | | | | | | | | | | |
| | MB Memory RD (IF, MR below 1M) | | ZD => BD | BD <= ZD | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | BUS Memory RD (IF, MR above 1M) | BD => ZD | | MB device on ZD | ZA=>BA | | | ZC=>BC | | |
| | | | | | | | | | | |
| | MB Memory WR (MW below 1M) | | ZD => BD | BD => ZD | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | BUS Memory WR (MW above 1M) | ZD => BD | | MB device on ZD | ZA=>BA | | | ZC=>BC | | |
| | | | | | | | | | | |
| | MB Refresh | | | | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | MB I/O RD | | ZD => BD | BD <= ZD | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | BUS I/O RD | BD => ZD | | MB device on ZD | ZA=>BA | | | ZC=>BC | | |
| | | | | | | | | | | |
| | MB I/O WR | | ZD => BD | BD => ZD | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | BUS i/O WR | ZD => BD | | | ZA=>BA | | | ZC=>BC | | |
| | | | | | | | | | | |
| | MB INT-ACK | | ZD => BD | | | ZA=>BA | BA<=ZA | | ZC=>BC | BC<=ZC |
| | | | | | | | | | | |
| | BUS INT-ACK | BD => ZD | | | | ZA=>BA | BA<=ZA | ZC=>BC | | BC<=ZC |
| | | | | | | | | | | |
| **Master** | **Operation** | **ZD<=>BD** | | | **ZA<=>BA** | | | **ZC<=>BC** | | |
| **BUS Master** | | | | | | | | | | |
| | | **Required** | **Allowed** | **Prohibited** | **Required** | **Allowed** | **Prohibited** | **Required** | **Allowed** | **Prohibited** |
| | MB Memory RD (IF, MR below 1M) | ZD => BD | | | BA=>ZA | | | BC=>ZC | | |
| | | | | | | | | | | |
| | BUS Memory RD (IF, MR above 1M) | | BD => ZD | ZD => BD | | BA=>ZA | ZA=>BA | | BC=>ZC | ZC=>BC |
| | | | | | | | | | | |
| | MB Memory WR (MW below 1M) | BD => ZD | | MB Device on ZD | BA=>ZA | | | BC=>ZC | | |
| | | | | | | | | | | |
| | BUS Memory WR (MW above 1M) | | BD => ZD | ZD => BD | | BA=>ZA | ZA=>BA | | BC=>ZC | ZC=>BC |
| | | | | | | | | | | |
| | MB I/O RD | ZD => BD | | | BA=>ZA | | | BC=>ZC | | |
| | | | | | | | | | | |
| | BUS I/O RD | | BD => ZD | ZD => BD | | BA=>ZA | ZA=>BA | | BC=>ZC | ZC=>BC |
| | | | | | | | | | | |
| | MB I/O WR | BD => ZD | | MB Device on ZD | BA=>ZA | | | BC=>ZC | | |
| | | | | | | | | | | |
| | BUS i/O WR | | BD => ZD | ZD => BD | | BA=>ZA | ZA=>BA | | BC=>ZC | ZC=>BC |
| | | | | | | | | | | |
| | MB INT-ACK | ZD => BD | | | | BA=>ZA | ZA=>BA | BC=>ZC | | |
| | | | | | | | | | | |
| | BUS INT-ACK | | BD => ZD | | | BA=>ZA | ZA=>BA | | BC=>ZC | ZC=>BC |
| | | | | | | | | | | |