

RGB-to-DPVID 1.0 IP Core User Guide

Revised June 19, 2015; Author Mihaita Nagy

1 Introduction

This user guide describes the Digilent RGB-to-DPVID Video Encoder Intellectual Property. This IP interfaces to an RGB video data bus at its input and outputs a video data interface of the Xilinx LogiCORE™ IP DisplayPort™.

2 Features

- Configurable video bus width input
- Xilinx interfaces used: vid_io

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx®: vid_io
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2014.3.1
Synthesis	Vivado Synthesis 2014.3.1

3 Overview

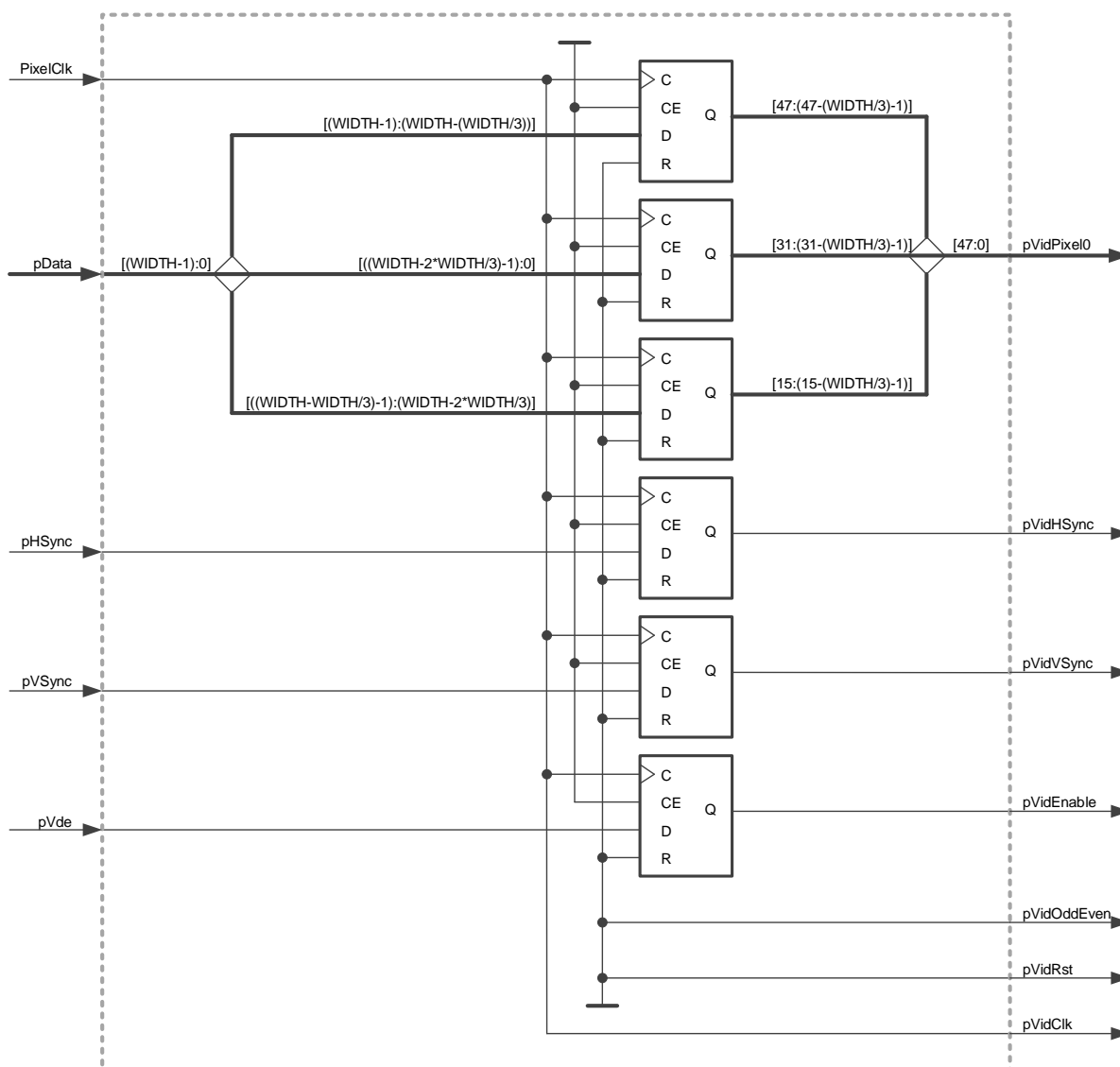


Figure 1. DVI to VGA converter block diagram.

The IP translates the input vid_io interface signals and outputs them to a dpvid interface ready to be connected to a Xilinx DisplayPort™ Source Core (see [1]).

4 Port Descriptions

The signals of the RGB to DPVID Core are listed and described in Table 1.

Signal Name	Interface	Signal Type	Init State	Description
PixelClk	rgb	I	N/A	Video reference clock input (pixel clock).
pData [(WIDTH-1):0]	rgb	I	N/A	RGB video data bus.

pHSync	rgb	I	N/A	Horizontal synchronization video timing signal.
pVSync	rgb	I	N/A	Vertical synchronization video timing signal.
pVde	rgb	I	N/A	Video data valid: • 1 = Active video. • 0 = Blanking period.
pVidClk	dpvid	O	0	Forwarded PixelClk signal.
pVidPixel0 [47:0]	dpvid	O	zeros	Video data output.
pVidHSync	dpvid	O	0	Horizontal synchronization video timing signal.
pVidVSync	dpvid	O	0	Vertical synchronization video timing signal.
pVidEnable	dpvid	O	0	Video data qualifier: • 1 = Video data valid. • 0 = Video data not valid.
pVidOddEven	dpvid	O	0	Unused.
pVidRst	dpvid	O	0	Unused.

Table 1. Port descriptions.

5 Parameter Descriptions

The parameters of the RGB to DPVID Core are listed and described in Table 12 below.

Parameter Name	Range	Type	Default	Description
kDataWidth	0 - 47	integer	24	Sets the input video data bus width containing already the video components. It is limited at a maximum of 48 which is the limit of the dpvid-interface data signal input (see Table 3-3 of [1]).

Table 2. Parameter descriptions.

6 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *PG064: DisplayPort LogiCORE IP Product Guide*, v6.0, April 1, 2015.