AXI DPTI 1.0 IP Core User Guide

Revised October 12, 2016; Author Sergiu Arpadi

1 Introduction

IP quick facts	
Provided with core	
Tested design flows	

2 Features

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3 Performance

4 Overview

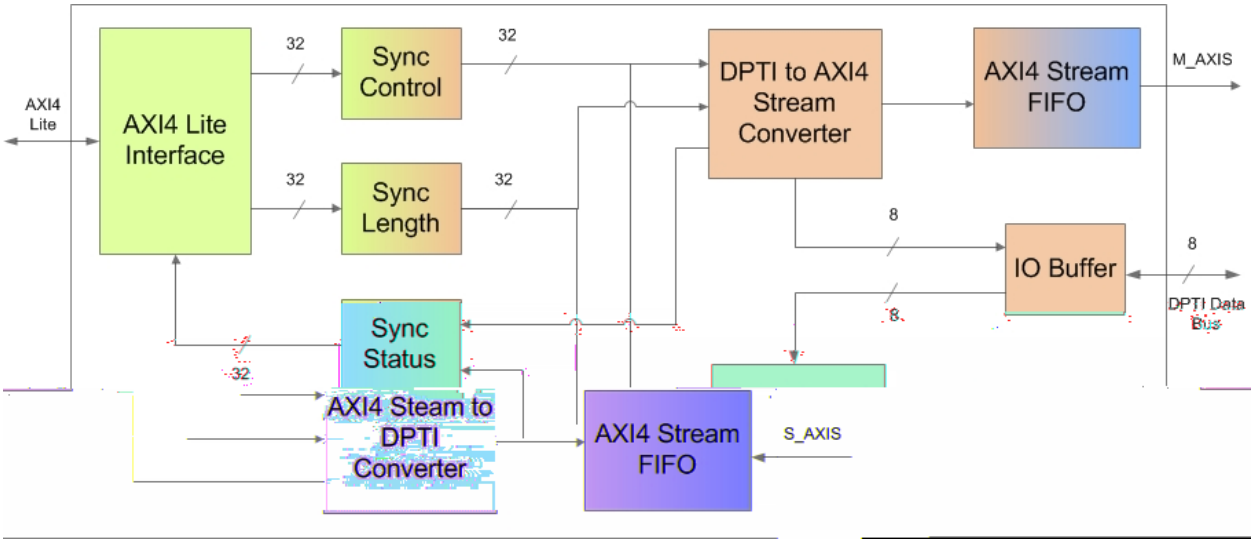
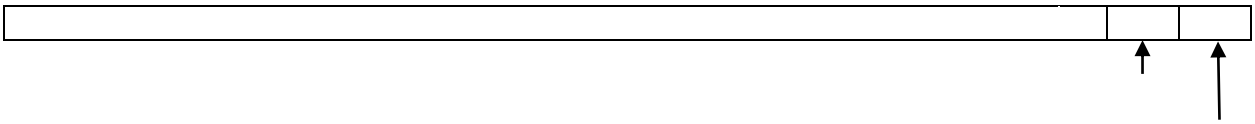


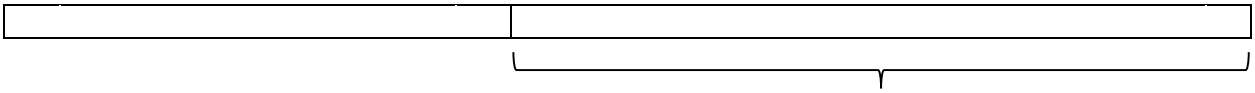
Figure 1. AXI DPTI block diagram.

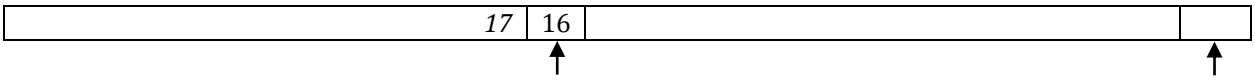
4.1 DPTI protocol

4.2 AXI4 Lite registers

Table 1. AXI4 Lite register space







4.3 Transfer control

5 Port descriptions

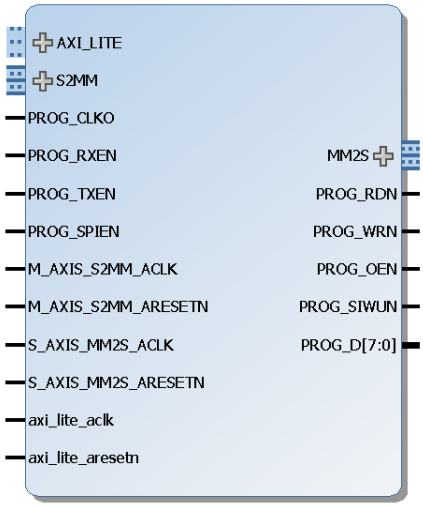


Figure 2. AXI DPTI IP Core.

Table 2. Port descriptions

6 Designing with the core

6.1 Constraints

7 References

UG471: 7 Series FPGAs SelectIO Resources

UG472: 7 Series FPGAs Clocking Resources

3. *UG903: Using Constraints, v2014.3, October 31, 2014*

PG021: AXI DMA logiCORE IP Product Gudie, v7.1, november 18, 2015

FT2232H Dual High Speed USB to Multipurpose UART/FIFO IC

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