RGB-to-DVI (Source) 1.3 IP Core User Guide

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4 Overview

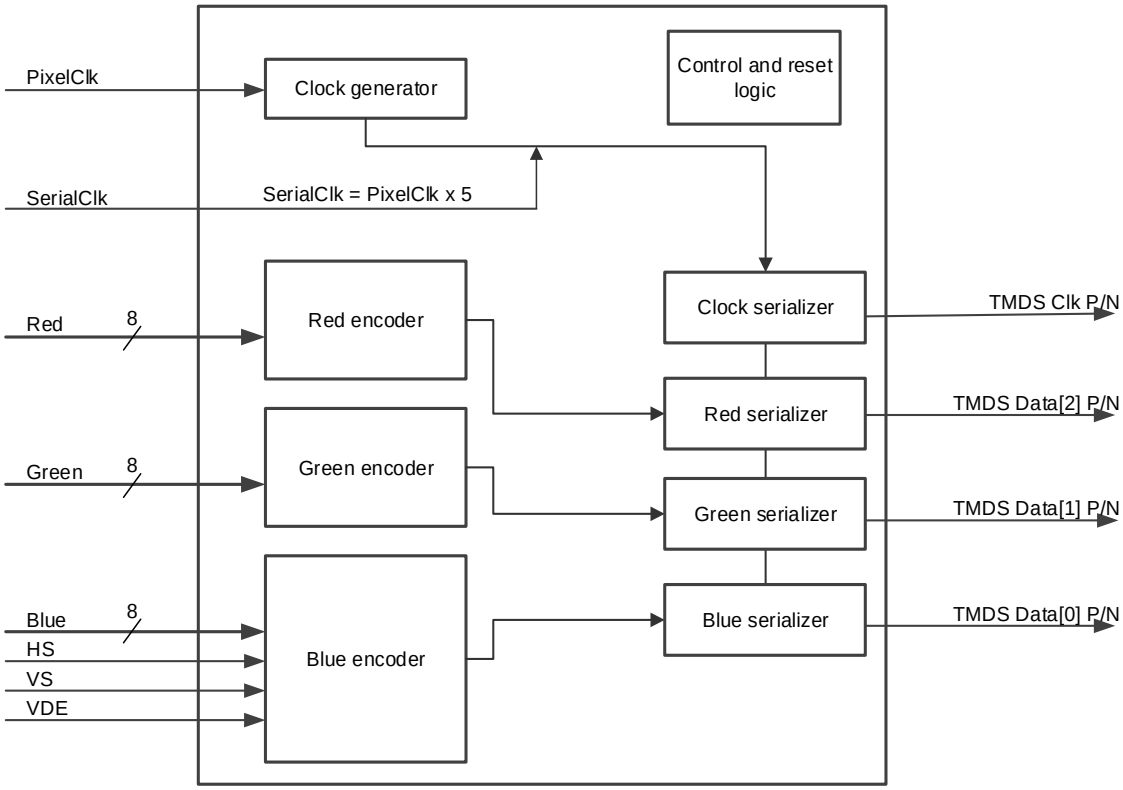

Figure 1. RGB to DVI converter block diagram.

4.1 RGB input

4.2 Clocking

OSERDESE2 Clocking Methods.

4.3 Data encoding

4.4 Serialization

5 Port descriptions

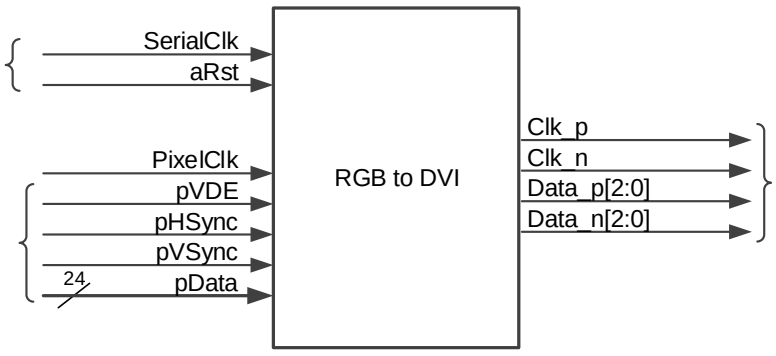

Figure 2. IP top-level diagram.

Table 1. Port descriptions.

6 Designing with the core

6.1 Customization

7 References

UG471: 7 Series FPGAs SelectIO Resources
UG472: 7 Series FPGAs Clocking Resources
XAPP460: Video Connectivity Using TMDS I/O in Spartan-3A FPGAs

XAPP495: Implementing a TMDS Video Interface in the Spartan-6 FPGA

WP249: SPI-4.2 Dynamic Phase Alignment
Digital Visual Interface DVI