DMA Controller

Output

BRAM
(Cache)

Pager

ALU

Regs

LPDDR
(Ram)

Decode

Flags

Pager

Instruction

Sd Card
(Disk)

Interrupts

Audio

Jtag Debug

VGA

Jtag

Leds

RDFIFO

Uart

WRFIFO

Push Buttons

BUS

Dip Switches

Partial Reconfiguration
(ICAP)

Seven Segment

GPIO

Black Box

Timeline	Date
Buttons, Leds, Switches	7/22/2016
Seven Segment	7/26/2016
Uart w/ fifo	8/1/2016
Base Insturction Set (add, store, read, jump, compare)	8/8/2016 (work on flags)
ALU	8/15/2016 (going to take longer)
Bram Cache	8/22/2016
Bus	8/29/2016
Put it together	9/5/2016
Uart-Interupt	9/12/2016
Work on simple input system	9/19/2016
LPDDR	10/17/2016
Simple operating system (read/write)	11/14/2016