Arithmetic Instructions	3											
Mnemonic	Instruction	Туре	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite			
ADD rd, rs1, rs2	Add	R	0	00	0	0000	0	X	1			
SUB rd, rs1, rs2	Subtract	R	0	00	0	1000	0	X	1			
ADDI rd, rs1, imm12	Add Immediate	I	0	00	0	0000	1	000	1			
SLT rd, rs1, rs2	Set Less Than	R	0	00	0	0010	0	Х	1			
SLTI rd, rs1, imm12	Set Less Than Immediate	I	0	00	0	0010	1	000	1			
SLTU rd, rs1, rs2	Set Less Than Unsigned	R	0	00	0	0011	0	X	1			
SLTIU rd, rs1, imm12	Set Less Than Immediate Unsigned	I	0	00	0	0011	1	000	1			
LUI rd, upimm	Load Upper Immediate	U	0	00	0	1001	1	100	1			
AUIP rd, imm20	Add Upper Immediate to PC	U										
Logic Instructions												
Mnemonic	Instruction	Туре	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite			
AND rd, rs1, rs2	AND	R	0	00	0	0111	0	Х	1			
OR rd, rs1, rs2	OR	R	0	00	0	0110	0	Х	1			
XOR rd, rs1, rs2	XOR	R	0	00	0	0100	0	X	1			
ANDI rd, rs1, imm12	AND Immediate	i i	0	00	0	0111	1	000	1			
ORI rd, rs1, imm12	OR Immediate	ı	0	00	0	0110	1	000	1			
XORI rd, rs1, imm12	XOR Immediate	1	0	00	0	0100	1	000	1			
SLL rd, rs1, rs2	Shift Left Logical	R	0	00	0	0001	0	Х	1			
SRL rd, rs1, rs2	Shift Right Logical	R	0	00	0	0101	0	X	1			
SRA rd, rs1, rs2	Shift Right Arithmetic	R	0	00	0	1101	0	X	1			
SLLI rd, rs1, shamt	Shift Left Logical Immediate	1	0	00	0	0001	1	000	1			
SRLI rd, rs1, shamt	Shift Right Logical Immediate	1	0	00	0	0101	1	000	1			
SRAI rd, rs1, shamt	Shift Right Arithmetic Immediate	1	0	00	0	1101	1	000	1			
Load/Store Instruction	s											
Mnemonic	Instruction	Туре	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite	DataWidth		
LW rd, imm12(rs1)	Load Word	I	0	01	0	0000	1	000	1	000		
LH rd, imm12(rs1)	Load Halfword	I	0	01	0	0000	1	000	1	001		
LB rd, imm12(rs1)	Load Byte	I	0	01	0	0000	1	000	1	010		
LHU rd, imm12(rs1)	Load Halfword Unsigned	1	0	01	0	0000	1	000	1	101		
			1				T	000	1	110		
LBU rd, imm12(rs1)	Load Byte Unsigned	1	0	01	0	0000	1	000				
LBU rd, imm12(rs1) SW rs2, imm12(rs1)	Load Byte Unsigned Store Word	s S	0	01 X	1	0000	1	001	0	000		
LBU rd, imm12(rs1) SW rs2, imm12(rs1) SH rs2, imm12(rs1)		S S	+	+	-		<u> </u>		0	000 001		
SW rs2, imm12(rs1)	Store Word		0	X	1	0000	1	001	ļ -			
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1)	Store Word Store Halfword Store Byte	S	0	X X	1	0000	1	001 001	0	001		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi	Store Word Store Halfword Store Byte	S S	0 0 0	X X X	1 1 1	0000 0000 0000	1 1 1	001 001 001	0	001 010		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic	Store Word Store Halfword Store Byte ons Instruction	S S	0	X X X	1 1 1 MemWrite	0000 0000 0000 ALUCtrl	1 1 1 1	001 001 001 ImmSrc	0 0 RegWrite	001 010 PCSrc		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic BEQ rs1, rs2, imm12	Store Word Store Halfword Store Byte ons Instruction Branch Equal	S S Type	0 0 0	X X X ResultSrc X	1 1 1 1 MemWrite	0000 0000 0000 0000 ALUCtrl	1 1 1 1 1 1 ALUSTC 0	001 001 001 001 ImmSrc 010	0 0 RegWrite	001 010 PCSrc Zero		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic BEQ rs1, rs2, imm12 BNE rs1, rs2, imm12	Store Word Store Halfword Store Byte ons Instruction Branch Equal Branch Not Equal	S S Type B B	0 0 0	X X X X ResultSrc X X	1 1 1 MemWrite 0	0000 0000 0000 0000 ALUCtrl 1000	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	001 001 001 001 ImmSrc 010	0 0 RegWrite 0	001 010 PCSrc Zero ~Zero		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic BEQ rs1, rs2, imm12 BNE rs1, rs2, imm12 BGE rs1, rs2, imm12	Store Word Store Halfword Store Byte ons Instruction Branch Equal Branch Not Equal Branch Greater Than Or Equal	S S Type B B B	0 0 0	X X X X X X X X X X X	1 1 1 1 MemWrite 0 0	0000 0000 0000 0000 ALUCtrl 1000 1000	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	001 001 001 001 ImmSrc 010 010	RegWrite 0 0 0	001 010 PCSrc Zero ~Zero Zero		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic BEQ rs1, rs2, imm12 BNE rs1, rs2, imm12 BGE rs1, rs2, imm12 BGEU rs1, rs2, imm12	Store Word Store Halfword Store Byte ons Instruction Branch Equal Branch Not Equal Branch Greater Than Or Equal Unsigned	S S S B B B B B B	0 0 0	X X X X X X X X X X X X X X X X X X X	1 1 1 1 MemWrite 0 0 0	0000 0000 0000 ALUCtrl 1000 1000 0010	ALUSTC 0 0 0 0 0 0	001 001 001 001 ImmSrc 010 010 010	0 0 0 RegWrite 0 0 0	001 010 PCSrc Zero ~Zero Zero Zero		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1) Branch/Jump Instructi Mnemonic BEQ rs1, rs2, imm12 BNE rs1, rs2, imm12 BGE rs1, rs2, imm12 BGEU rs1, rs2, imm12 BLT rs1, rs2, imm12	Store Word Store Halfword Store Byte ons Instruction Branch Equal Branch Not Equal Branch Greater Than Or Equal Unsigned Branch Less Than	S S S Type B B B B	0 0 0	X X X X ResultSrc X X X X X	1 1 1 1 MemWrite 0 0 0 0 0	0000 0000 0000 0000 ALUCtrl 1000 1000 0010 0011	ALUSTC 0 0 0 0 0	001 001 001 001 ImmSrc 010 010 010 010	0 0 0 RegWrite 0 0 0 0	001 010 PCSrc Zero ~Zero Zero Zero Zero Zero Zero ~Zero		
SW rs2, imm12(rs1) SH rs2, imm12(rs1) SB rs2, imm12(rs1)	Store Word Store Halfword Store Byte ons Instruction Branch Equal Branch Not Equal Branch Greater Than Or Equal Unsigned	S S S B B B B B B	0 0 0	X X X X X X X X X X X X X X X X X X X	1 1 1 1 MemWrite 0 0 0	0000 0000 0000 ALUCtrl 1000 1000 0010	ALUSTC 0 0 0 0 0 0	001 001 001 001 ImmSrc 010 010 010	0 0 0 RegWrite 0 0 0	001 010 PCSrc Zero ~Zero Zero Zero	JALR	JAL