Arithmetic Instructions

Mnemonic	Instruction	Type	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite
ADD rd, rs1, rs2	Add	R	0	00	0	0000	0	X	1
SUB rd, rs1, rs2	Subtract	R	0	00	0	1000	0	X	1
ADDI rd, rs1, imm12	Add Immediate	I	0	00	0	0000	1	000	1
SLT rd, rs1, rs2	Set Less Than	R	0	00	0	0010	0	X	1
SLTI rd, rs1, imm12	Set Less Than Immediate	I	0	00	0	0010	1	000	1
SLTU rd, rs1, rs2	Set Less Than Unsigned	R	0	00	0	0011	0	X	1
SLTIU rd, rs1, imm12	Set Less Than Immediate Unsigned	I	0	00	0	0011	1	000	1
LUI rd, upimm	Load Upper Immediate	U	0	00	0	1001	1	100	1
AUIP rd, imm20	Add Upper Immediate to PC	U							

Logic Instructions

Mnemonic	Instruction	Type	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite
AND rd, rs1, rs2	AND	R	0	00	0	0111	0	X	1
OR rd, rs1, rs2	OR	R	0	00	0	0110	0	X	1
XOR rd, rs1, rs2	XOR	R	0	00	0	0100	0	X	1
ANDI rd, rs1, imm12	AND Immediate	I	0	00	0	0111	1	000	1
ORI rd, rs1, imm12	OR Immediate	I	0	00	0	0110	1	000	1
XORI rd, rs1, imm12	XOR Immediate	I	0	00	0	0100	1	000	1
SLL rd, rs1, rs2	Shift Left Logical	R	0	00	0	0001	0	X	1
SRL rd, rs1, rs2	Shift Right Logical	R	0	00	0	0101	0	X	1
SRA rd, rs1, rs2	Shift Right Arithmetic	R	0	00	0	1101	0	X	1
SLLI rd, rs1, shamt	Shift Left Logical Immediate	I	0	00	0	0001	1	000	1
SRLI rd, rs1, shamt	Shift Right Logical Immediate	I	0	00	0	0101	1	000	1
SRAI rd, rs1, shamt	Shift Right Arithmetic Immediate	I	0	00	0	1101	1	000	1

Load/Store Instructions

Mnemonic	Instruction	Type	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite	DataWidth
LW rd, imm12(rs1)	Load Word	I	0	01	0	0000	1	000	1	000
LH rd, imm12(rs1)	Load Halfword	I	0	01	0	0000	1	000	1	001
LB rd, imm12(rs1)	Load Byte	I	0	01	0	0000	1	000	1	010
LHU rd, imm12(rs1)	Load Halfword Unsigned	I	0	01	0	0000	1	000	1	101
LBU rd, imm12(rs1)	Load Byte Unsigned	I	0	01	0	0000	1	000	1	110
SW rs2, imm12(rs1)	Store Word	S	0	X	1	0000	1	001	0	000
SH rs2, imm12(rs1)	Store Halfword	S	0	X	1	0000	1	001	0	001
SB rs2, imm12(rs1)	Store Byte	S	0	X	1	0000	1	001	0	010

Branch/Jump Instructions

Mnemonic	Instruction	Type	Branch	ResultSrc	MemWrite	ALUCtrl	ALUSrc	ImmSrc	RegWrite	PCSrc		
BEQ rs1, rs2, imm12	Branch Equal	B	1	X	0	1000	0	010	0	Zero		
BNE rs1, rs2, imm12	Branch Not Equal	B	1	X	0	1000	0	010	0	~Zero		
BGE rs1, rs2, imm12	Branch Greater Than Or Equal	B	1	X	0	0010	0	010	0	Zero		
BGEU rs1, rs2, imm12	Branch Greater Than Or Equal Unsigned	B	1	X	0	0011	0	010	0	Zero		
BLT rs1, rs2, imm12	Branch Less Than	B	1	X	0	0010	0	010	0	~Zero		
BLTU rs1, rs2, imm12	Branch Less Than Unsigned	B	1	X	0	0011	0	010	0	~Zero		**JAL**
JAL rd, imm20	Jump And Link	UJ	1	10	0	1000	1	011	1	1	**JALR**	1
JALR rd, imm12(rs1)	Jump And Link Register	I	1	10	0	1000	1	000	1	X	1	