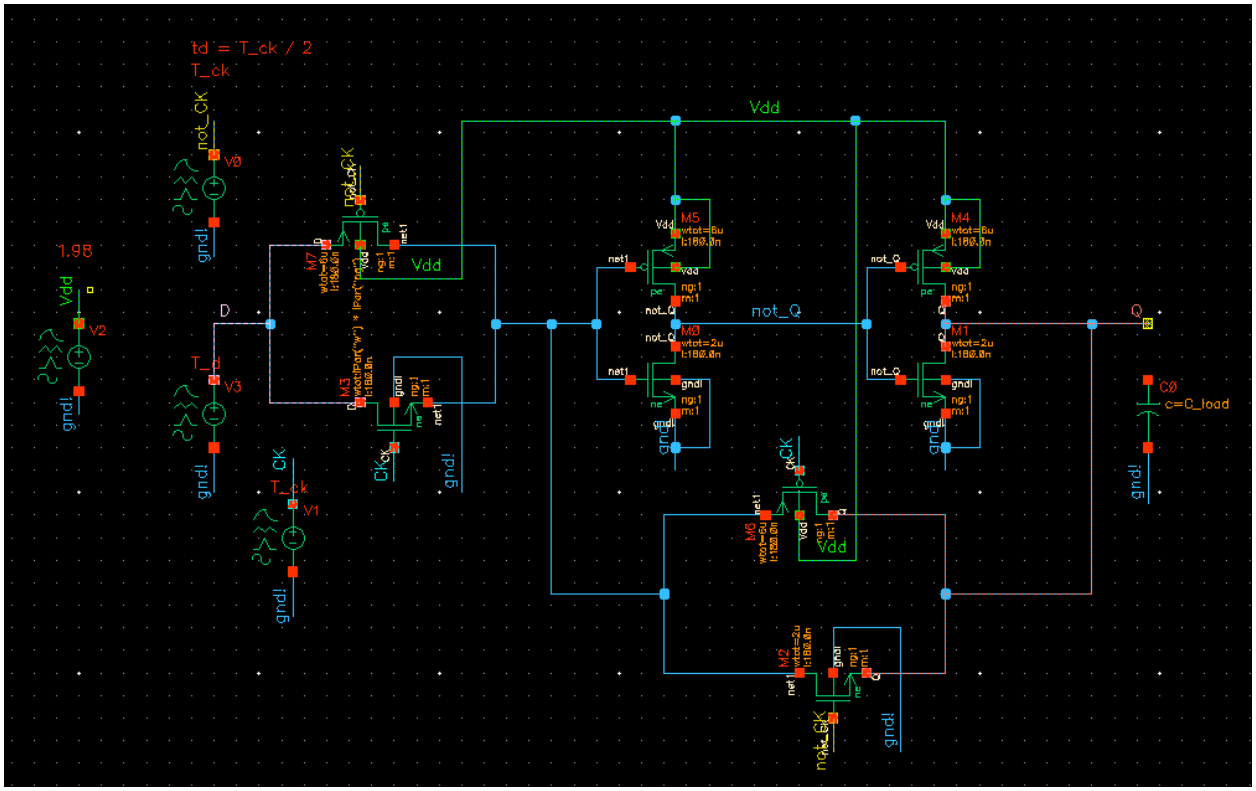
EE302 Spring 2025
Lab 4 Report

3/05/2025

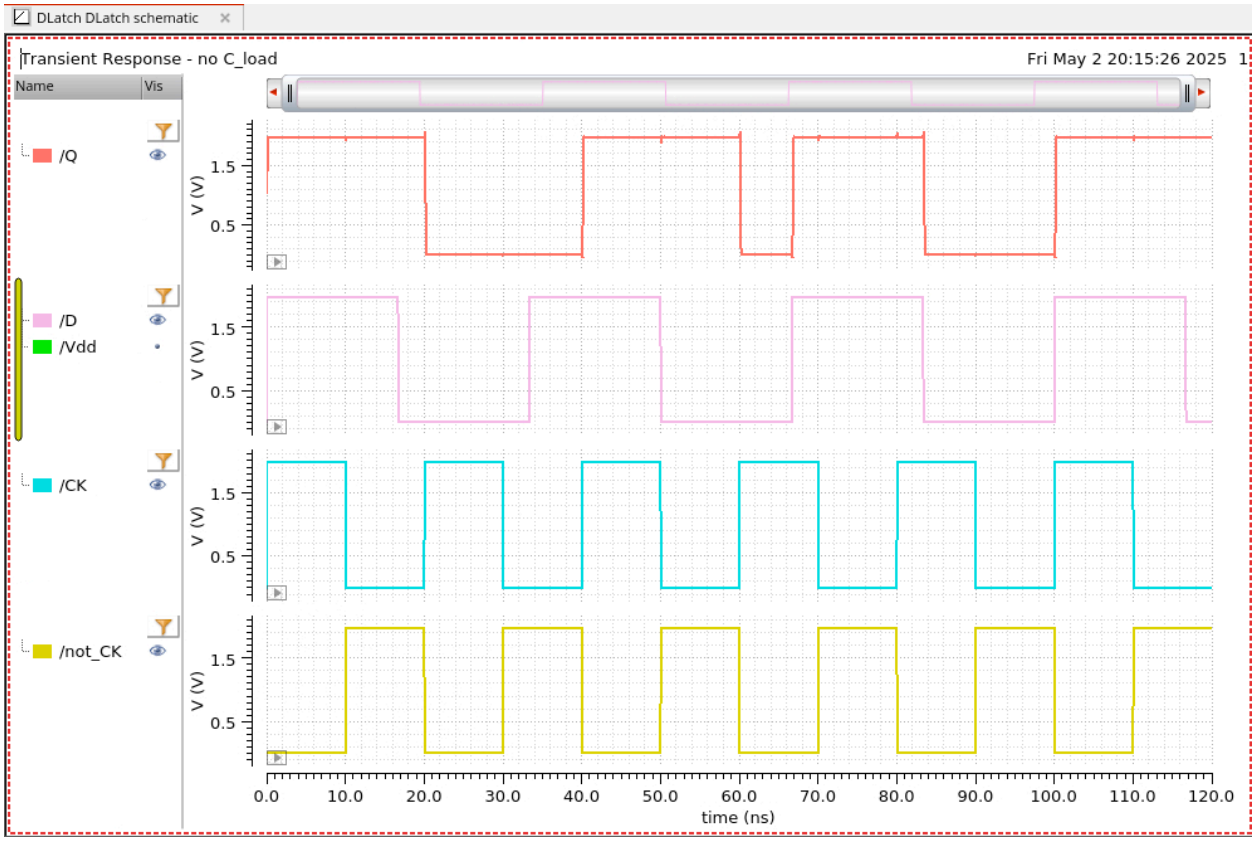
D Latch

Schematic



The D latch is made from two cascaded inverters and two transmission inverters. The first transmission gate provides a connection between input D and the inverters so long as the input CK is high (transmission gate is turned on). The 2nd transmission gate provides a feedback loop from the output, Q, to the cascaded inverters while CK is low. Hence the latch holds its charge while CK is low and samples the input D while CK is high.

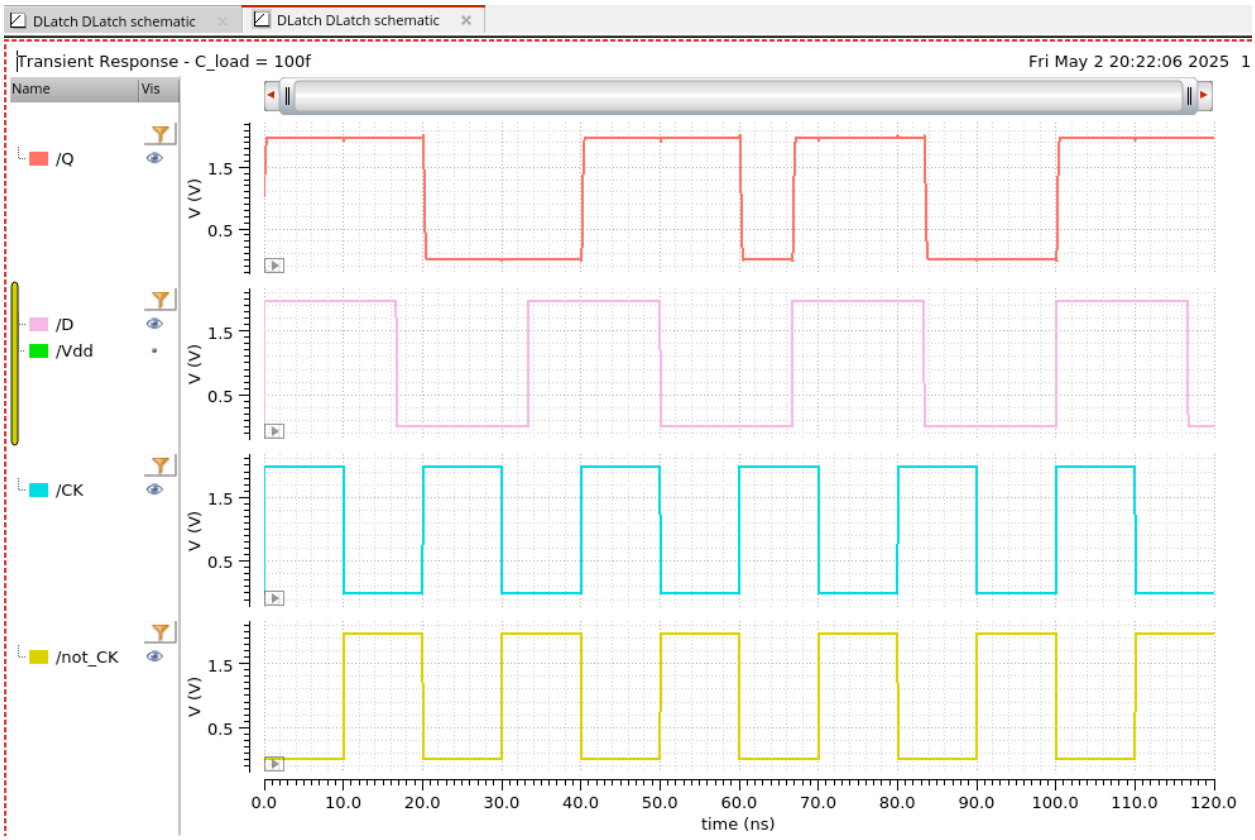
Transient Simulation



Transient simulation with no C_load.

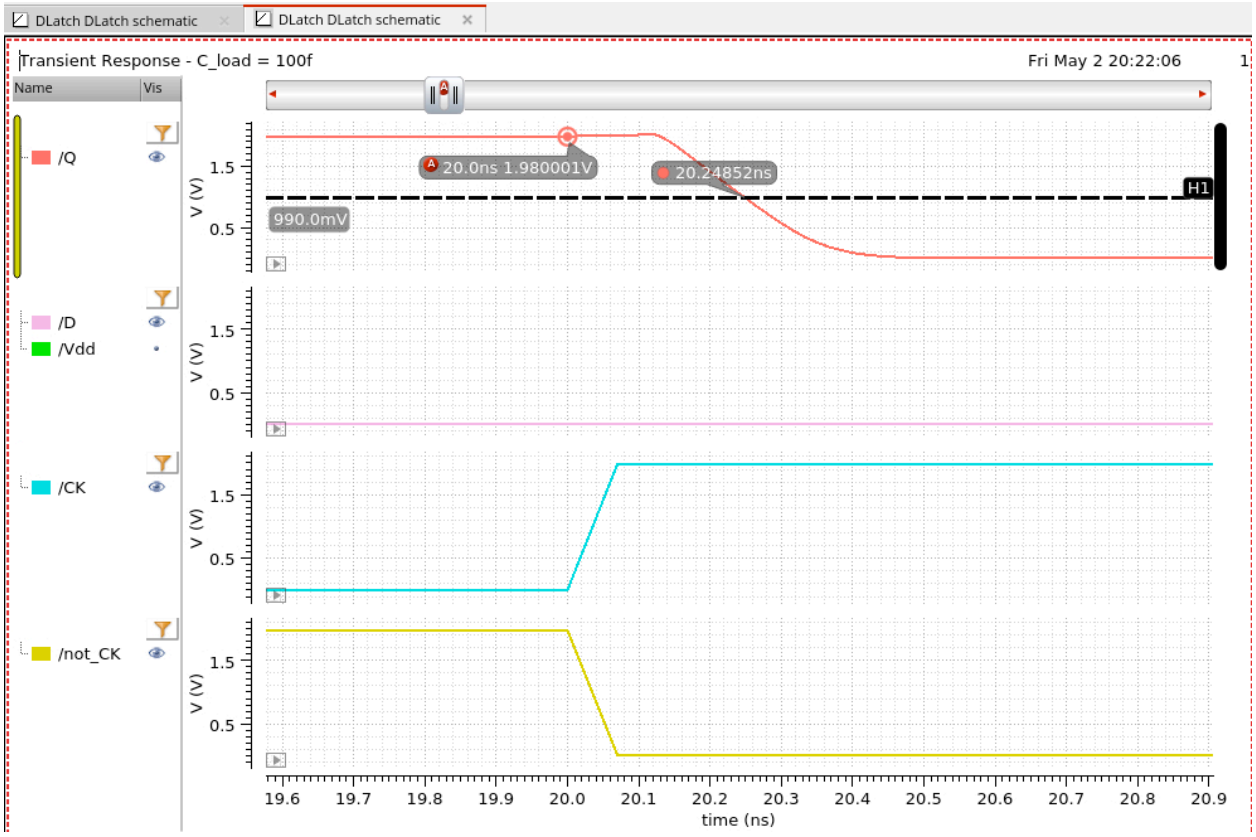
As can be seen on the waveform above, input D only triggers changes in the output Q when the clock signal, CK, is high. Hence the latch circuit is operational.

Propagation Delays

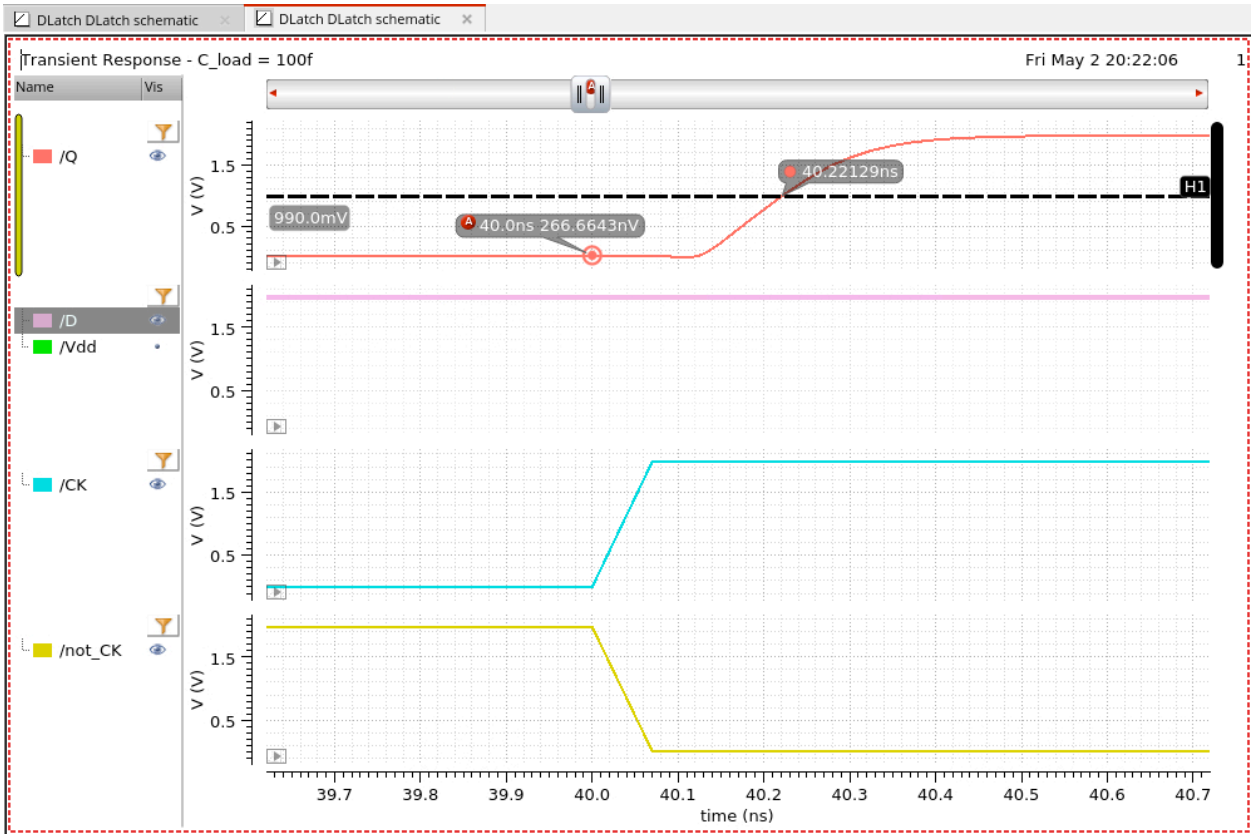


Transient Simulation with C_{load} = 100f F.

The circuit continues to operate as described in the previous parts when a capacitive load is connected to the output.



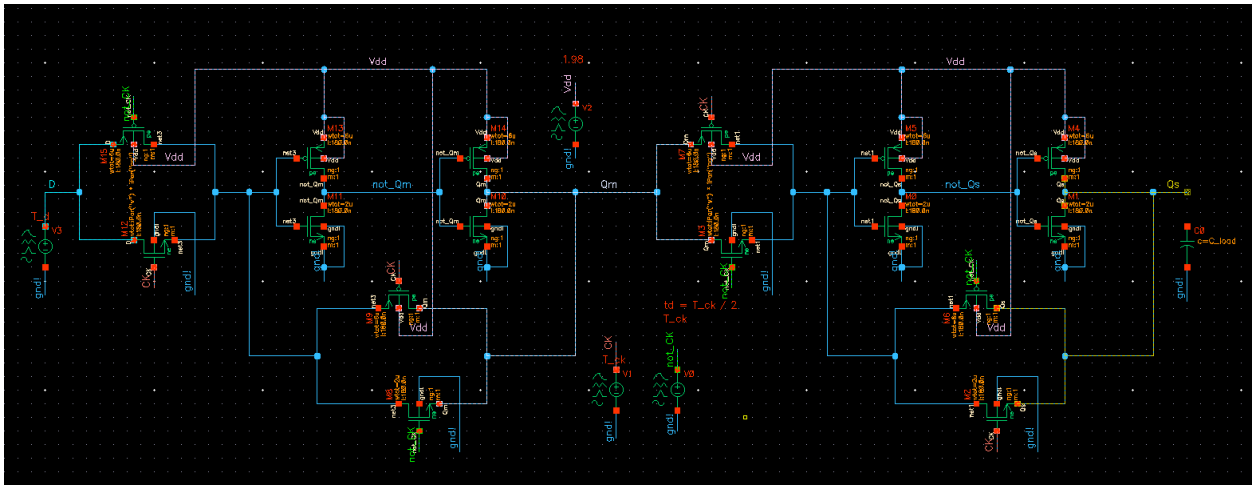
High to low propagation delay of the D latch circuit was measured as 259ps.



Low to high propagation delay of the D latch circuit was measured as 221ps.

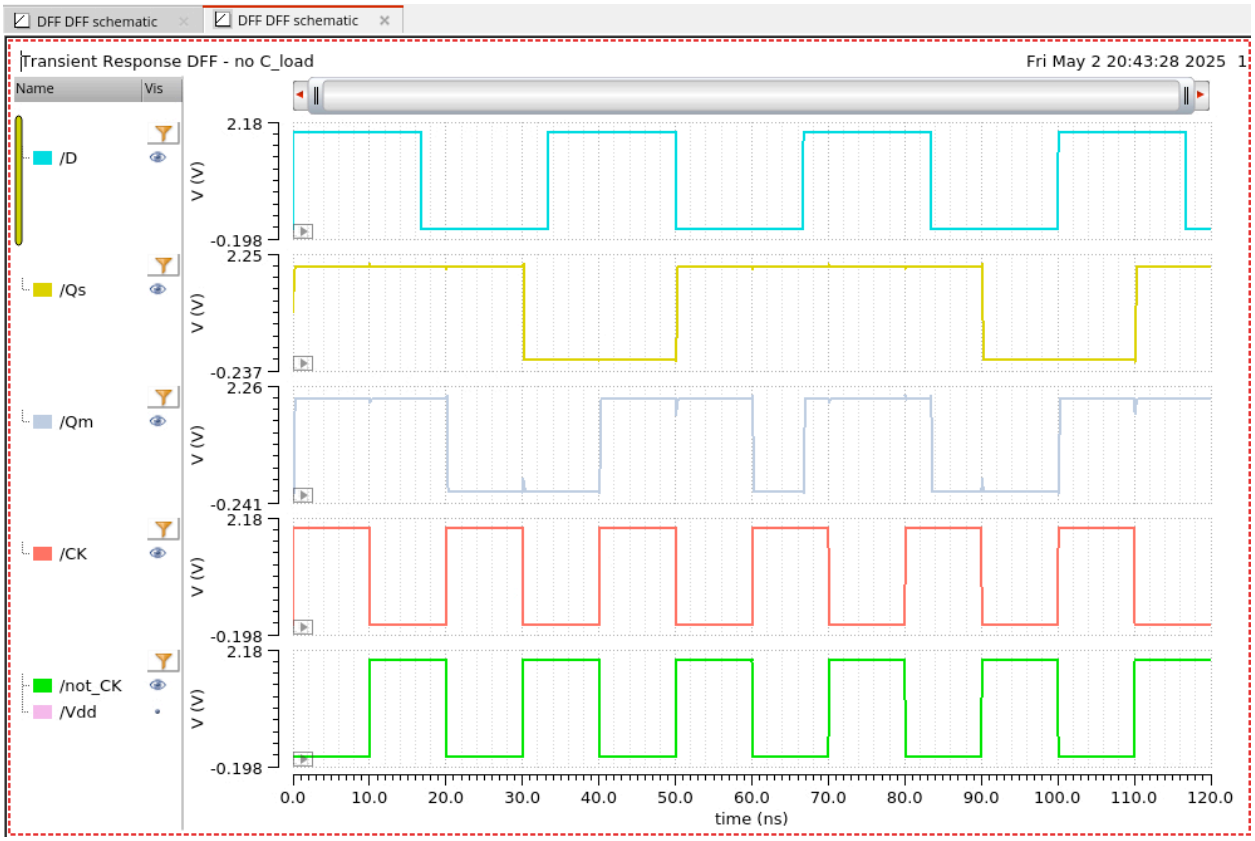
D Flip Flop

Schematic



The schematic for the falling edge triggered D flip flop is provided above. One should note that while the first (left-most) latch is identical to the latch described in the previous section, the CK and not_CK inputs of the 2nd latch are swapped.

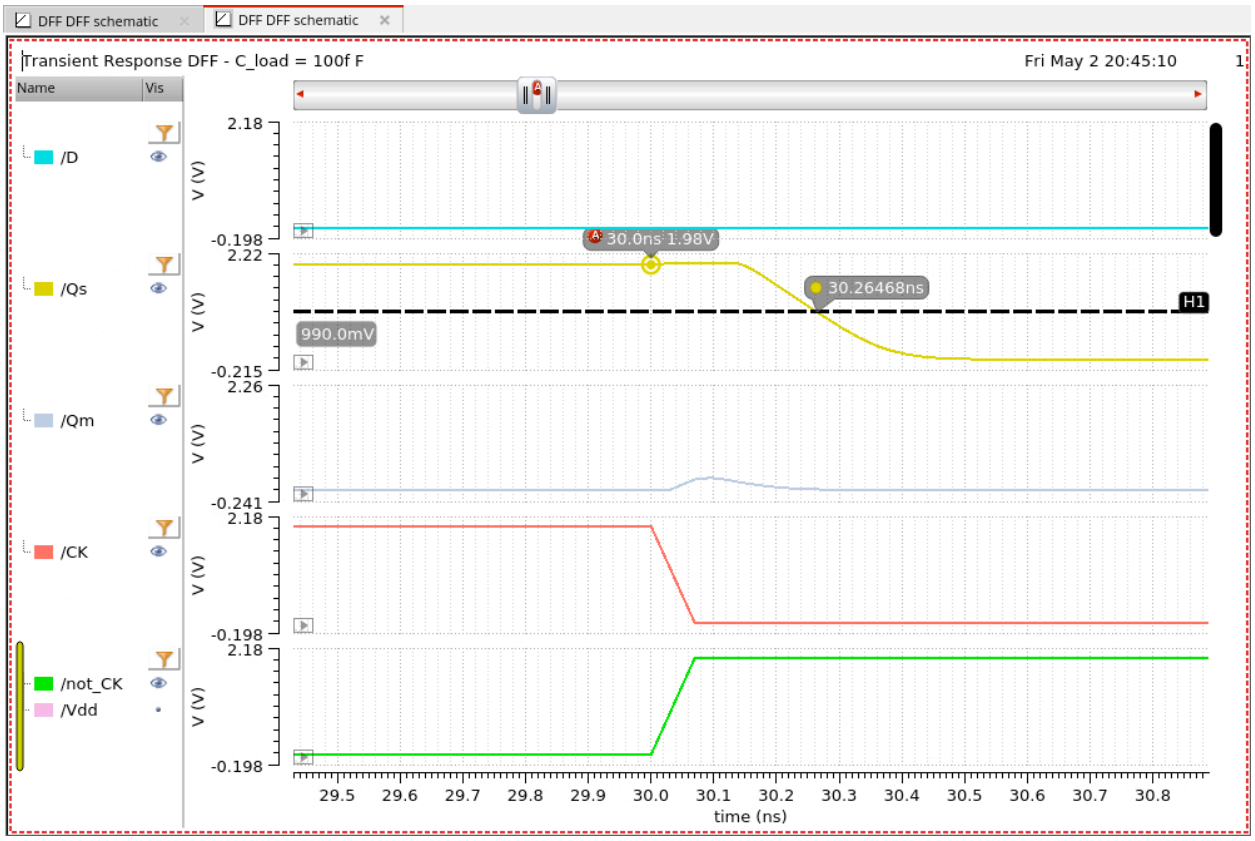
Transient Simulation



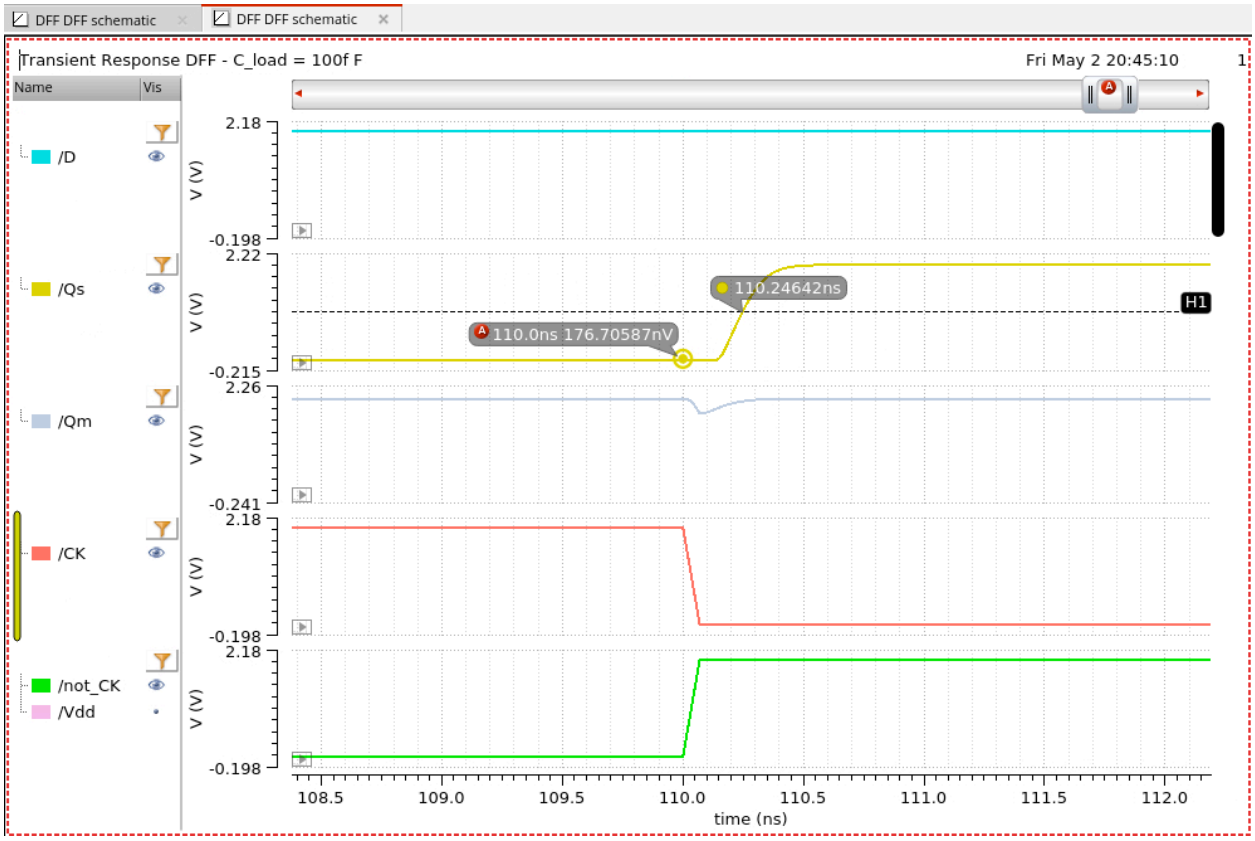
Transient simulation for no C_{load} attached.

As can be observed from the waveform above, the flip flop samples the D input signal as the transition of the signal CK from high to low takes place. Changes in the value at input D do not affect the output signal when at the rising edge or stable signal states of the CK input. Hence the operation of the DFF is fully correct.

Propagation Delays

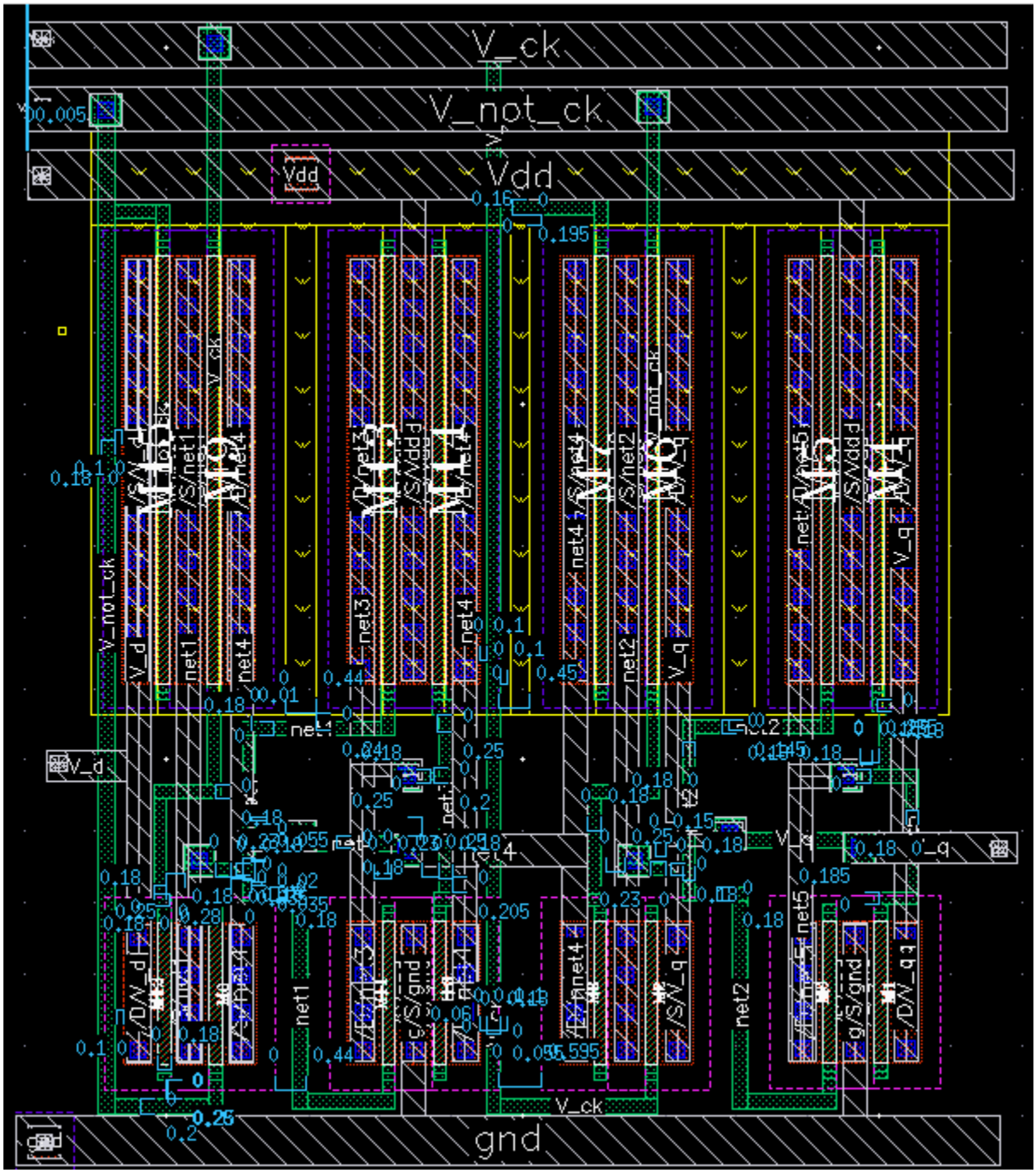


High to low propagation delay of the DFF was measured as 265ps.



Low to high propagation delay of the DFF circuit was measured as 246ps.

Layout & Symbol Extraction

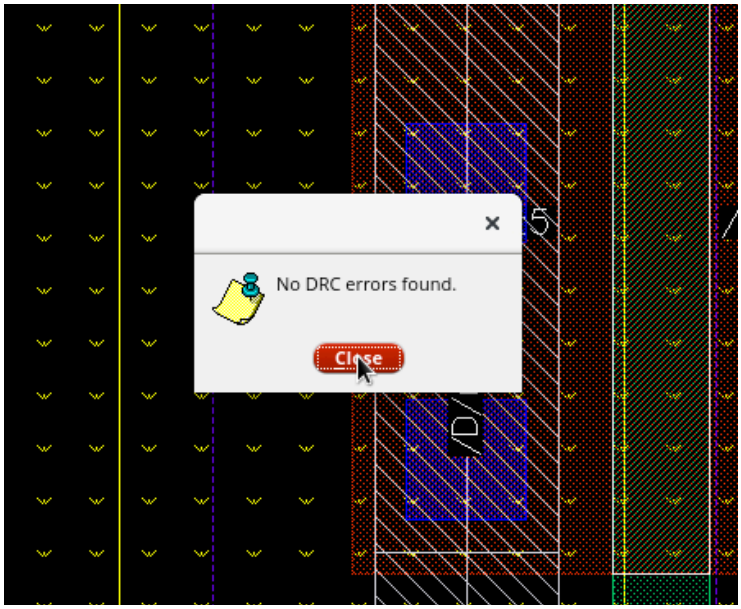


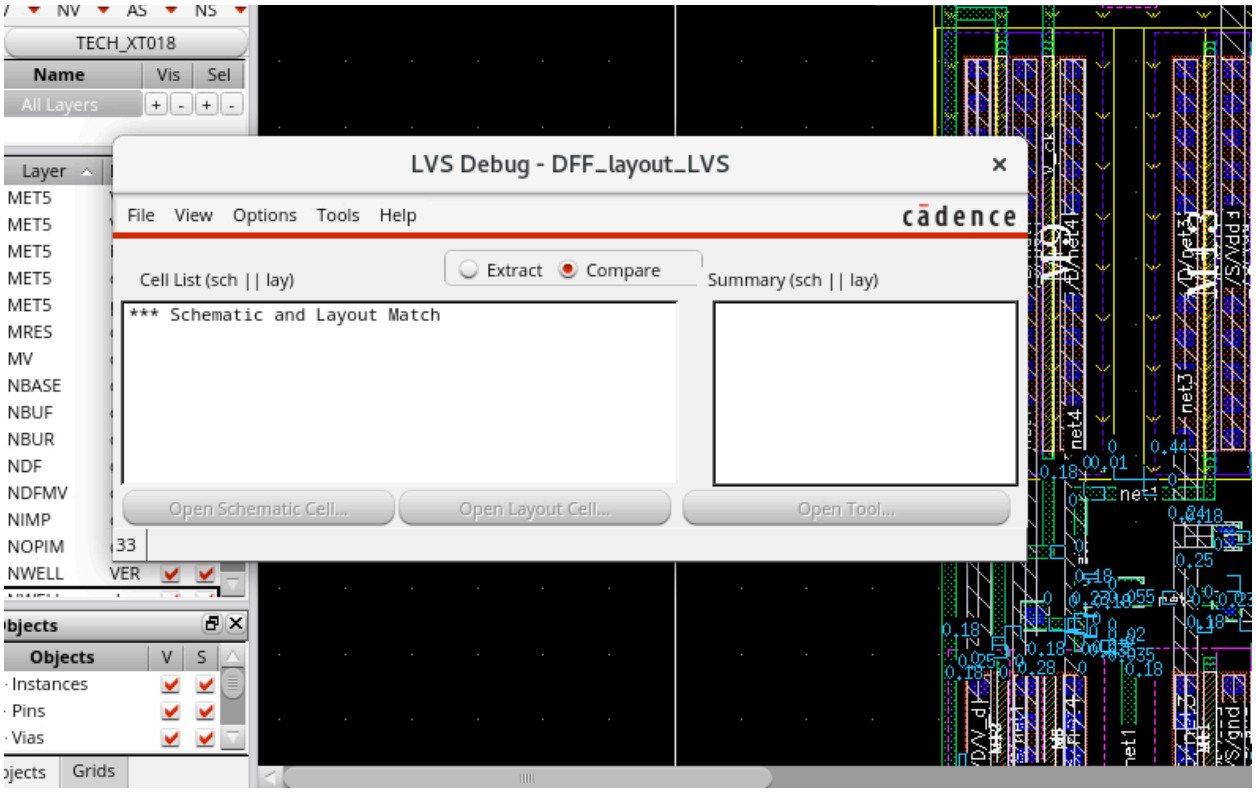
Layout of the DFF circuit.

Given how memory is a very important concern for the full-custom design of high-density memory circuits, I decided to challenge myself to come up with an area optimized design for the DFF circuit. The layout above was modeled after the layout image provided in the main textbook for the course as well as the discussions during the lectures. The layout could roughly be divided vertically into 4 sections. The first section is the transmission gate array for the first

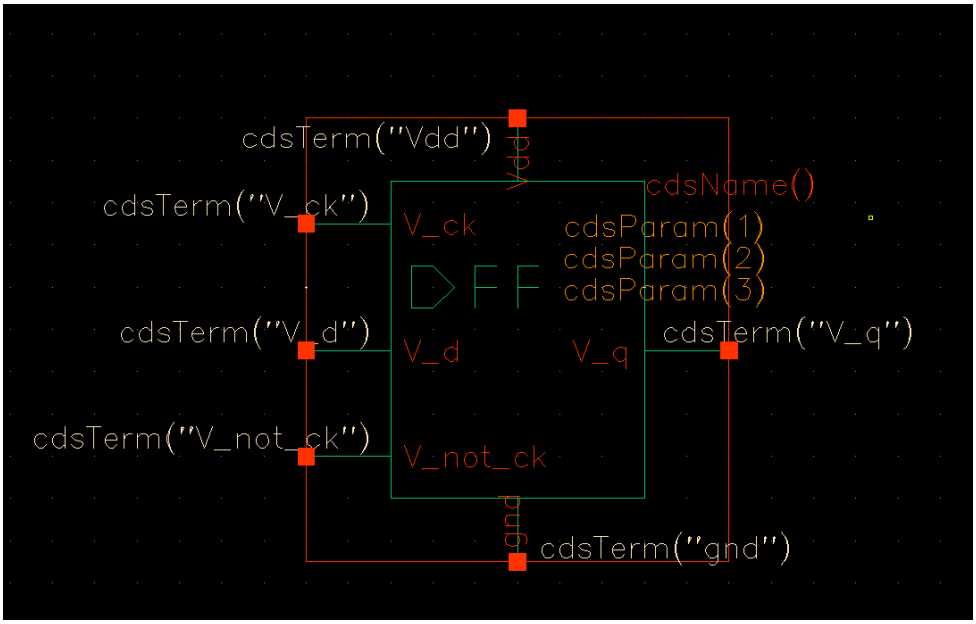
(left-most) D latch in the circuit. The 2nd section is the cascaded inverter stage corresponding to the first D latch. The 3rd and 4th sections correspond to the transmission gate and the inverter arrays for the right-most D latch respectively.

As can be seen below, the design passes DRC and LVS checks:



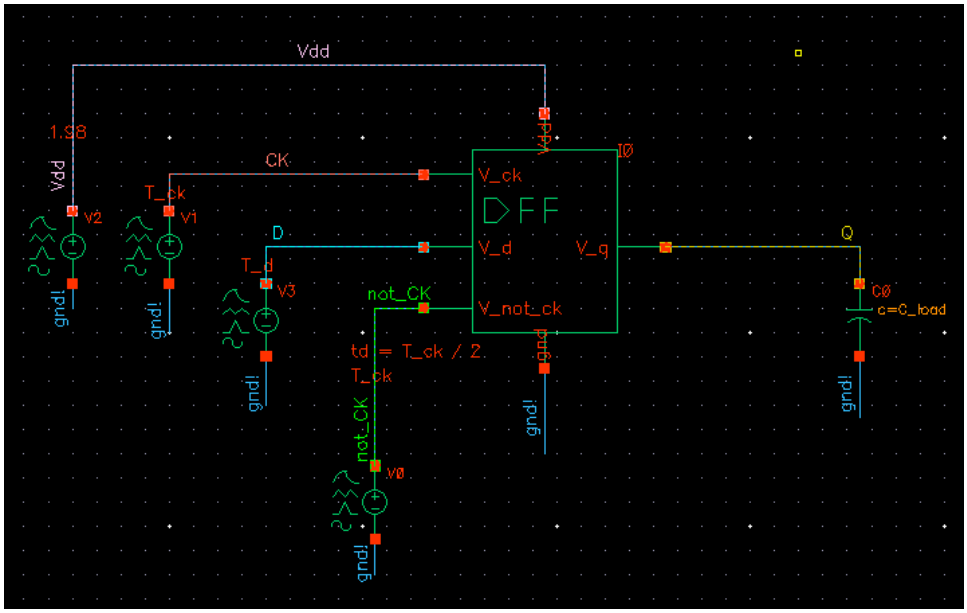


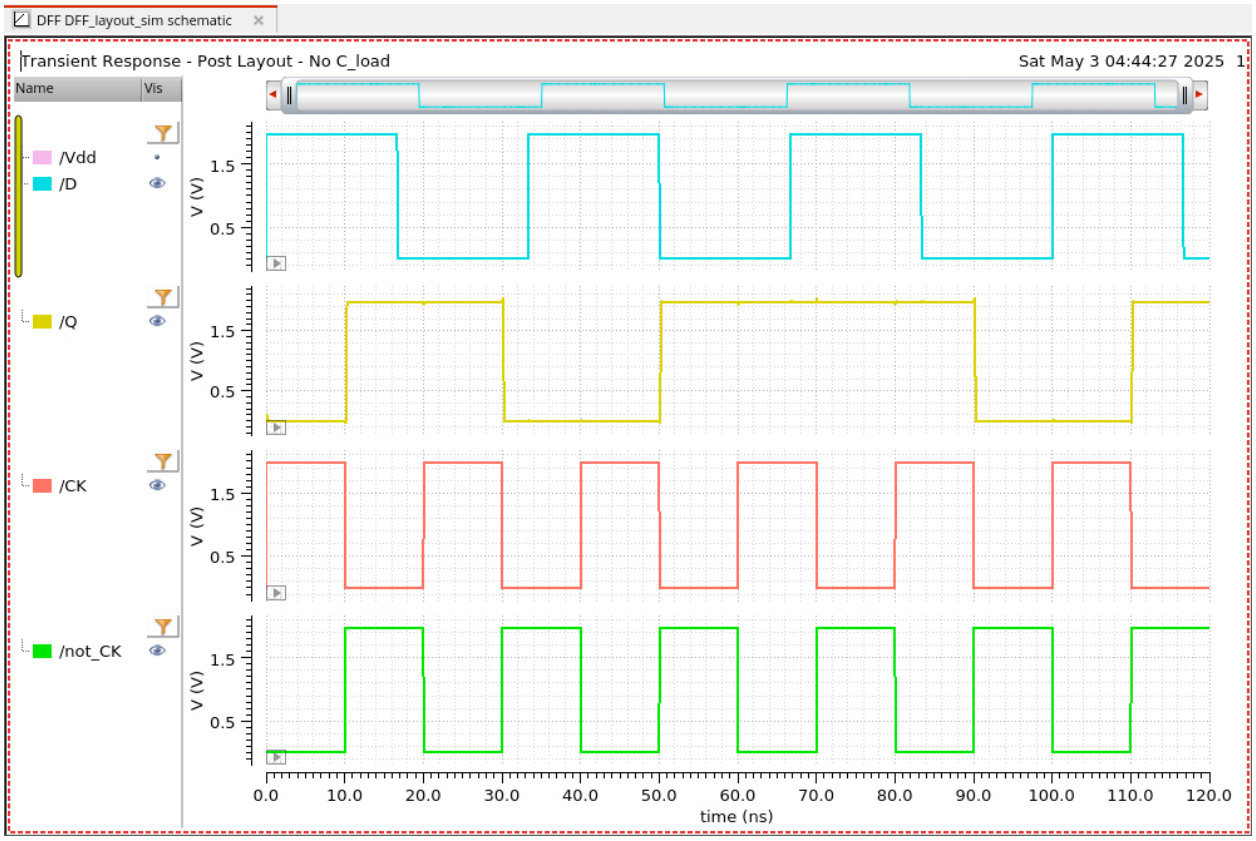
As for the symbol extraction, I chose to move forward with the classical DFF symbol:



Post-layout Transient Simulation

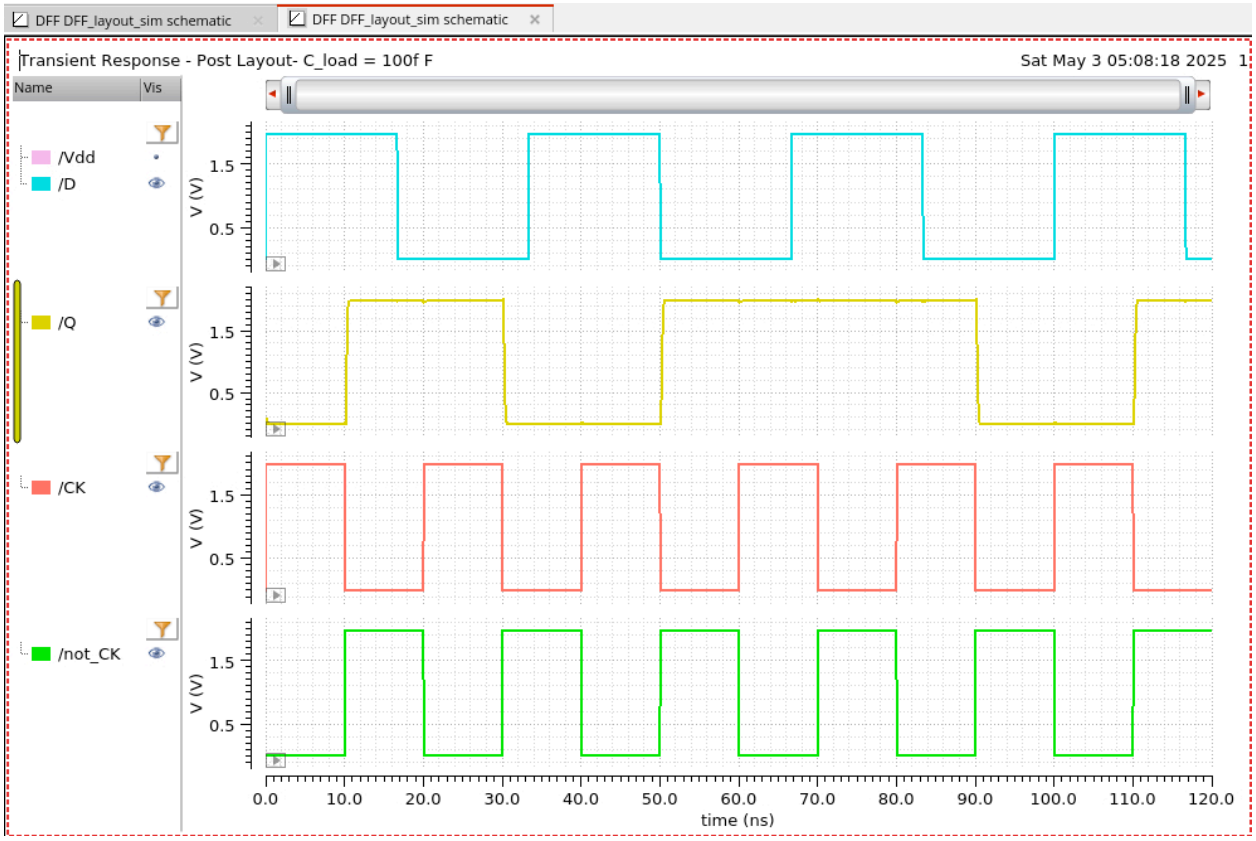
The post-layout testbench is provided below:



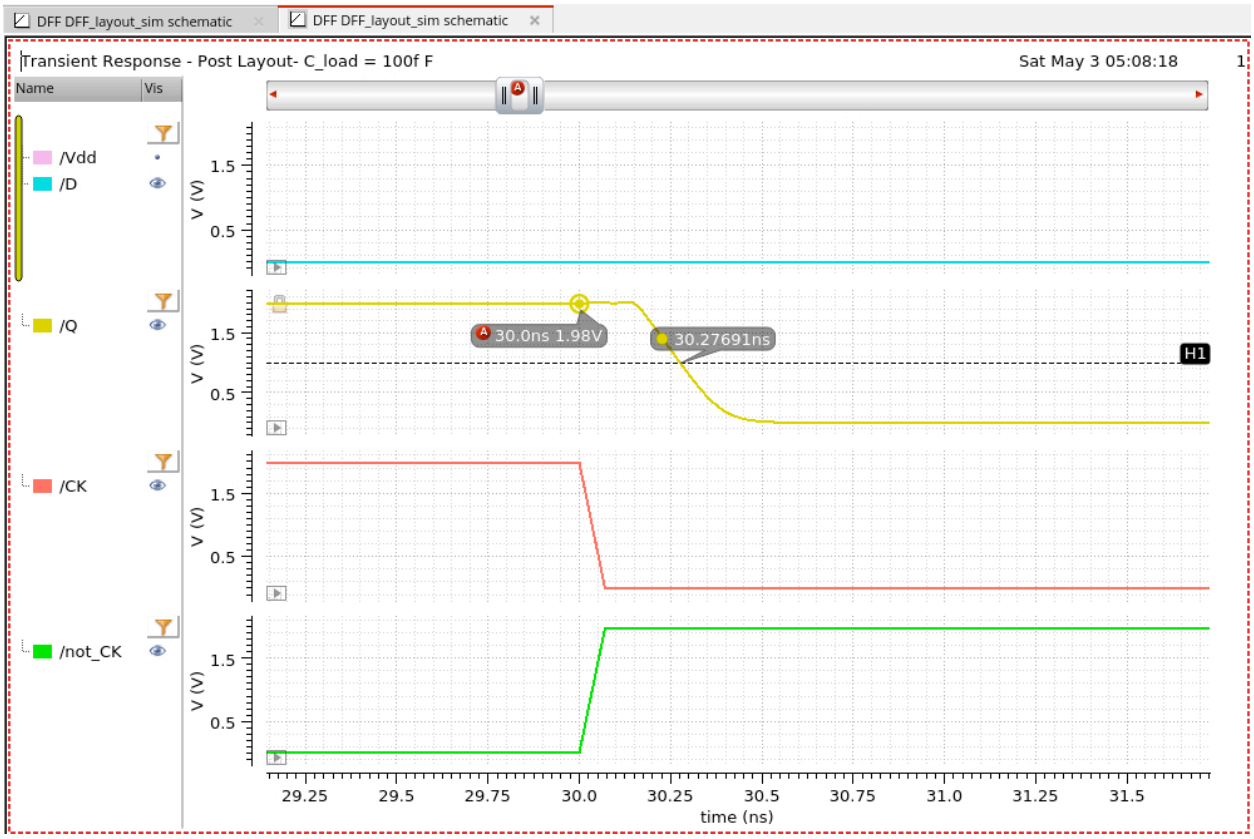


Transient simulation waveform output for no C_{load} connected to the circuit output. The outputs of the circuit are identical to the outputs of the pre-layout simulation, hence correctly characterize a falling edge DFF.

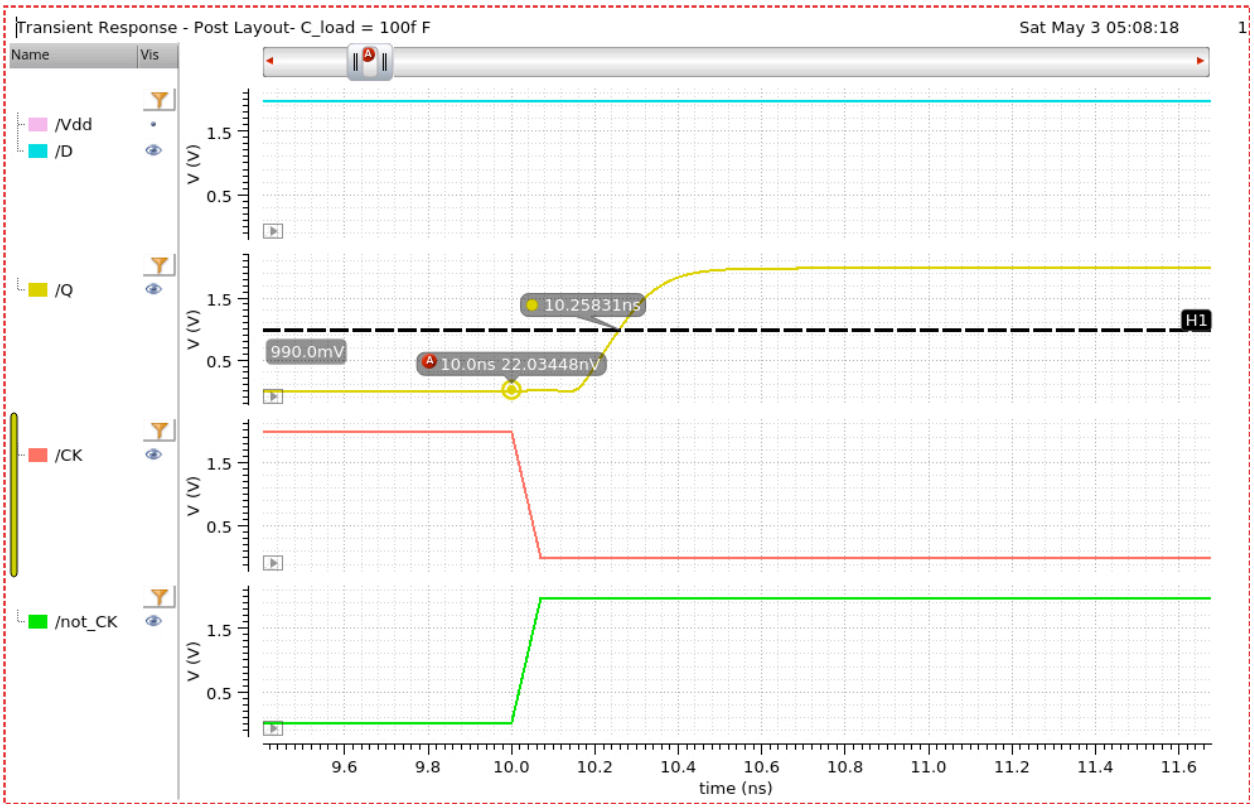
Propagation Delays



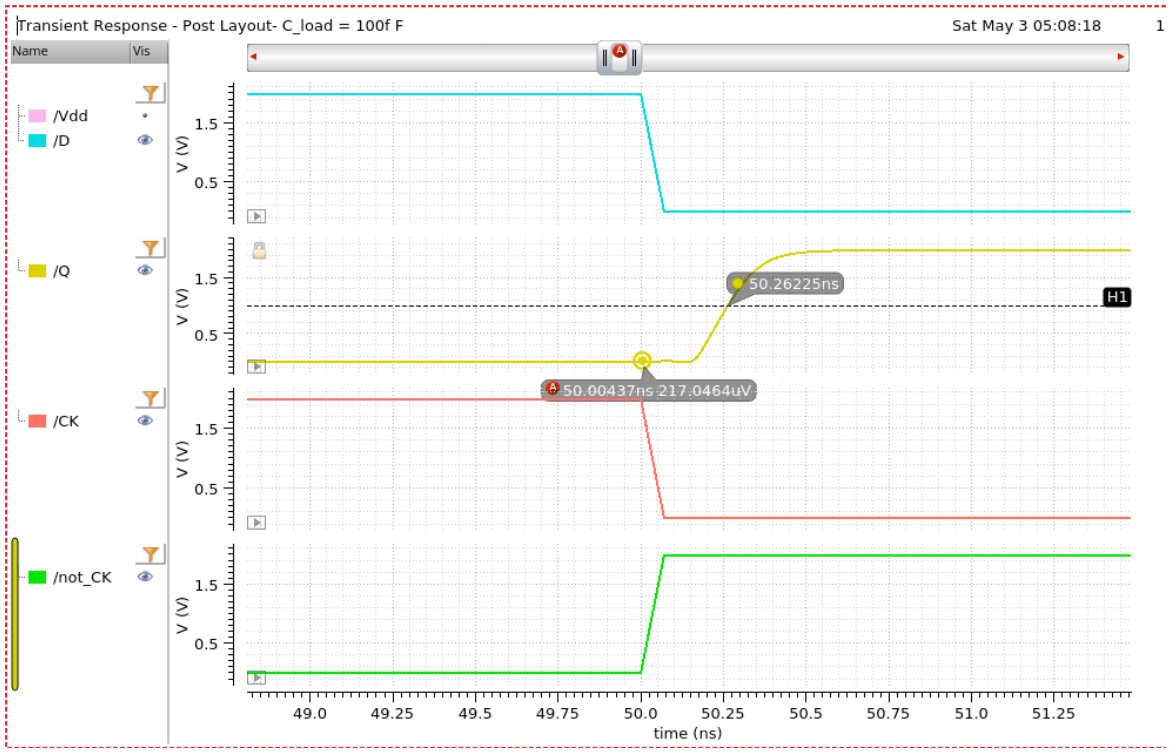
Transient simulation waveform output for no C_{load} = 100f F.



High to low propagation delay was found as 277ps for the laid-out circuit.



Low-to-high propagation delay for the circuit with input D stable was found as 258ps.



This waveform is important in the way it illustrates the working principle of the DFF. Despite the change from high to low of the input D at the same instance where a negative edge was

encountered in the clock signal, the output correctly sampled the (previous) high value of input D. The change of input D, despite resulting in correct behaviour, increased the low to high propagation delay of the circuit to 262ps. This corresponds to an increase by 4ps which is highly negligible.