

EE302 Spring 2025

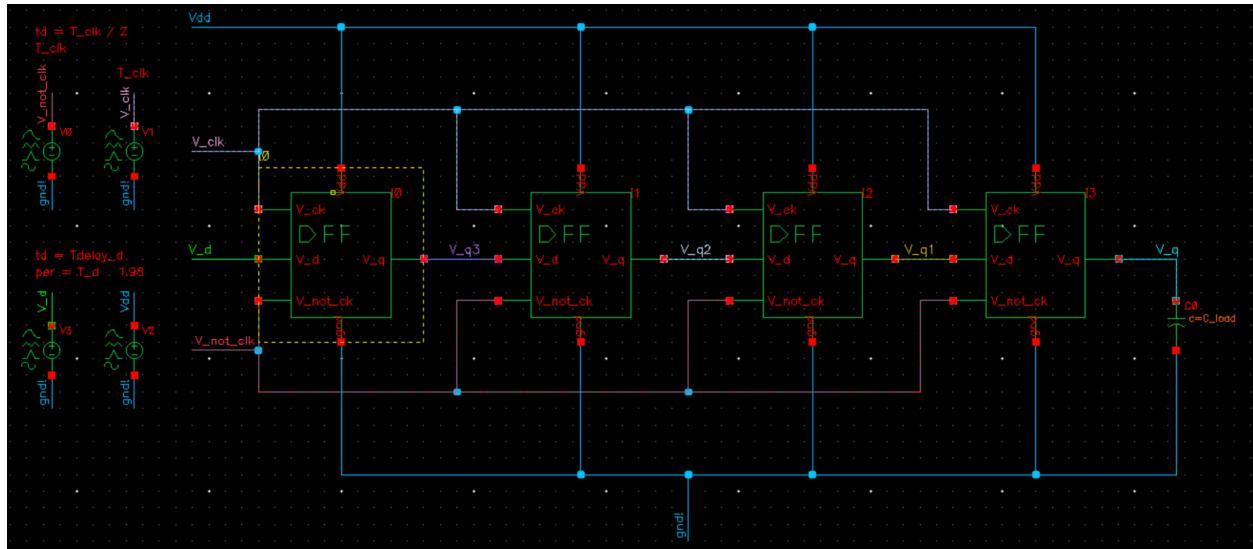
Lab 5 Report

12/05/2025

4 Bit Serial-In-Serial-Out Register

Schematic

The schematic of the siso circuit is shown below. One should note that the intermediary outputs are in decreasing order: **Hence the input will propagate to V_q3, V_q2 and V_q1 in that order.** The naming of the intermediary wires differs from the lab document which is it requires highlighting.



Transient Simulation

Transient simulation with **no C_{load} attached** is provided below:

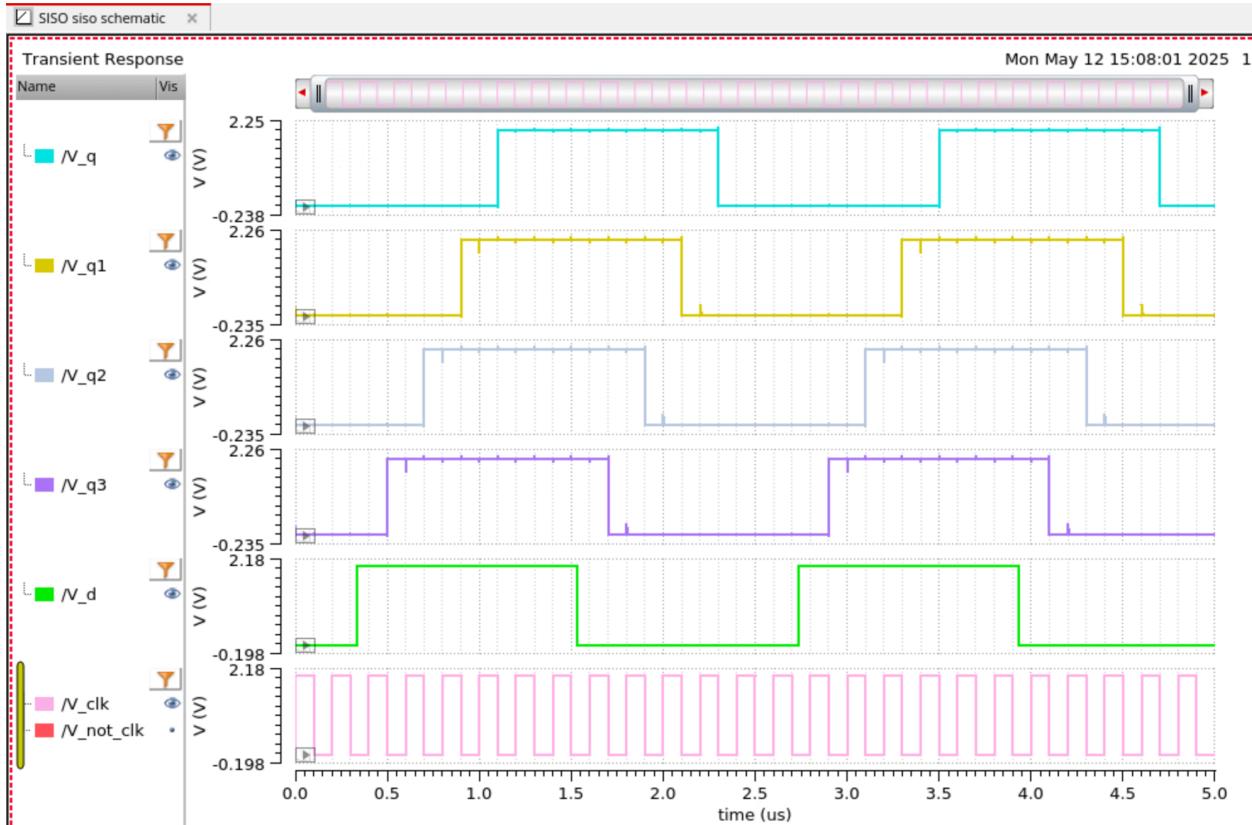


Fig. 2: Transient simulation with no C_{load} attached.

One can observe that both high and low values of the input D propagate through the flip flops at every negedge of the clk signal. This plot matches the plot provided on the lab document.

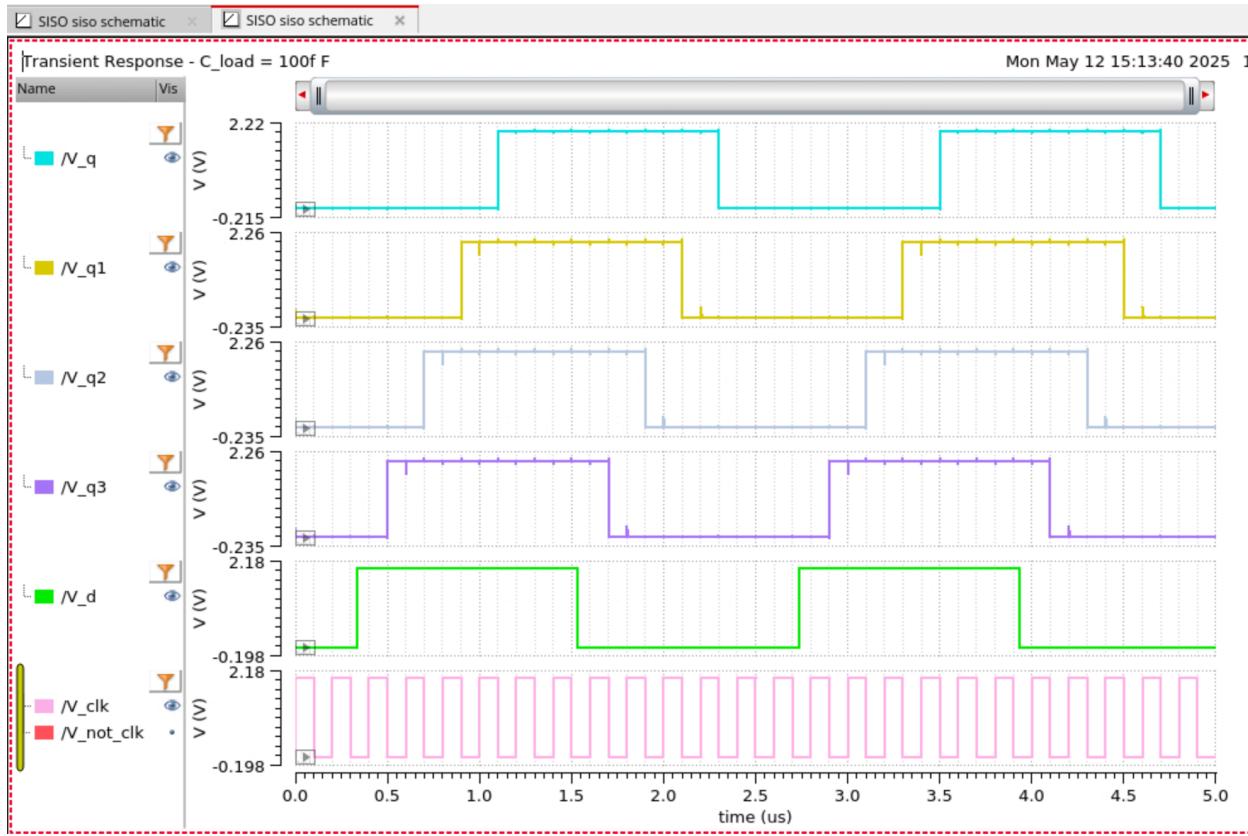


Fig. 3: Transient simulation with $C_{load} = 100f F$

Provided above is the transient response of the circuit for $100f F C_{load}$. The output waveform matches the waveform provided in the lab document as well as Fig. 2.

The table below shows the operation of the SISO register in the waveform above in more detail:

Input (V_d)	Current Output (V_q)	Output at next negedge (V_q)
0	0	0
1	0	0
1	0	0
1	0	0
1	0	1
1	1	1
1	1	1
0	1	1

0	1	1
0	1	1
0	1	0
0	0	0

The high input value of d appears at the output 4 negative clock edges later. The input stays high for 6 clock cycles after which it drops to zero. The low value of the input takes 4 clock cycles to propagate to the output. The output remains high until the low value of the input D propagates to the output.

Propagation Delays

Propagation delay measurements for $C_{load} = 100f\text{ F}$ are provided below:

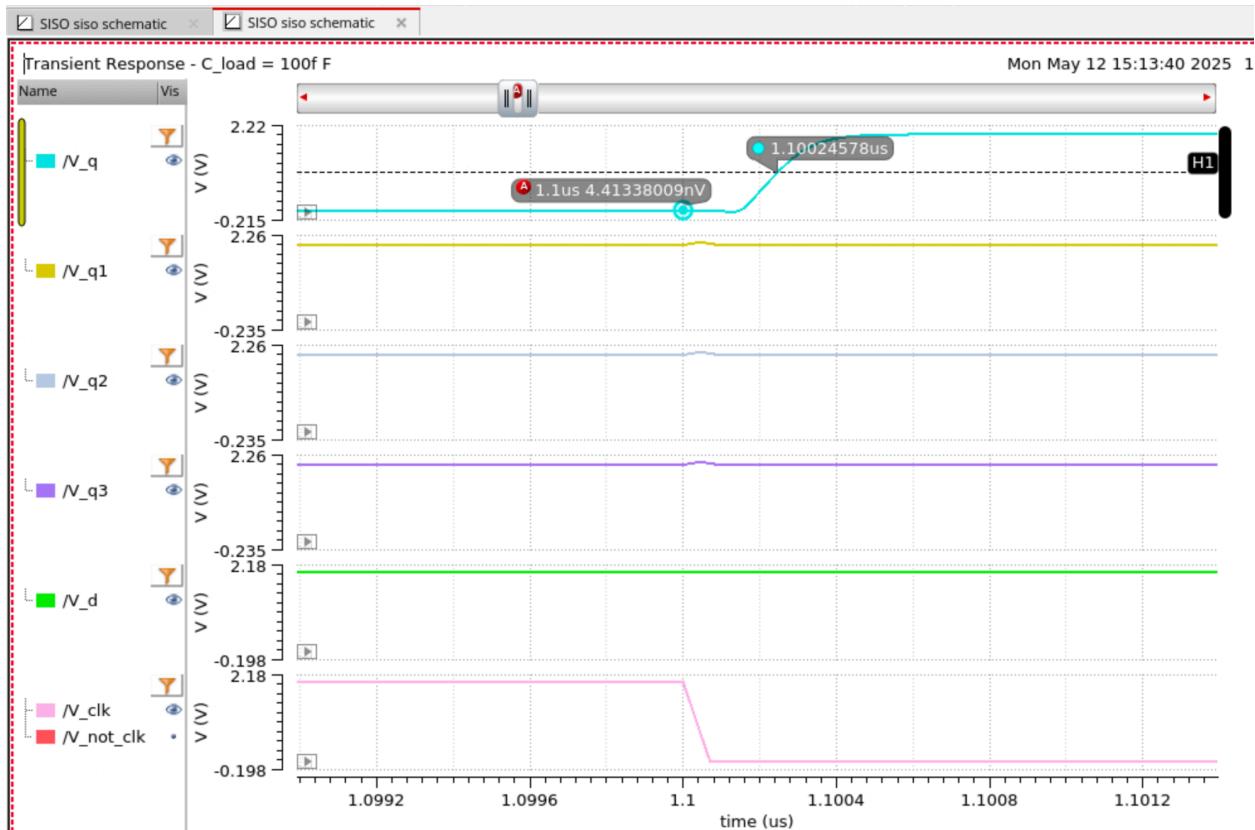


Fig. 4: Low to high propagation delay measurement. τ_{PLH} was measured as 246ps.

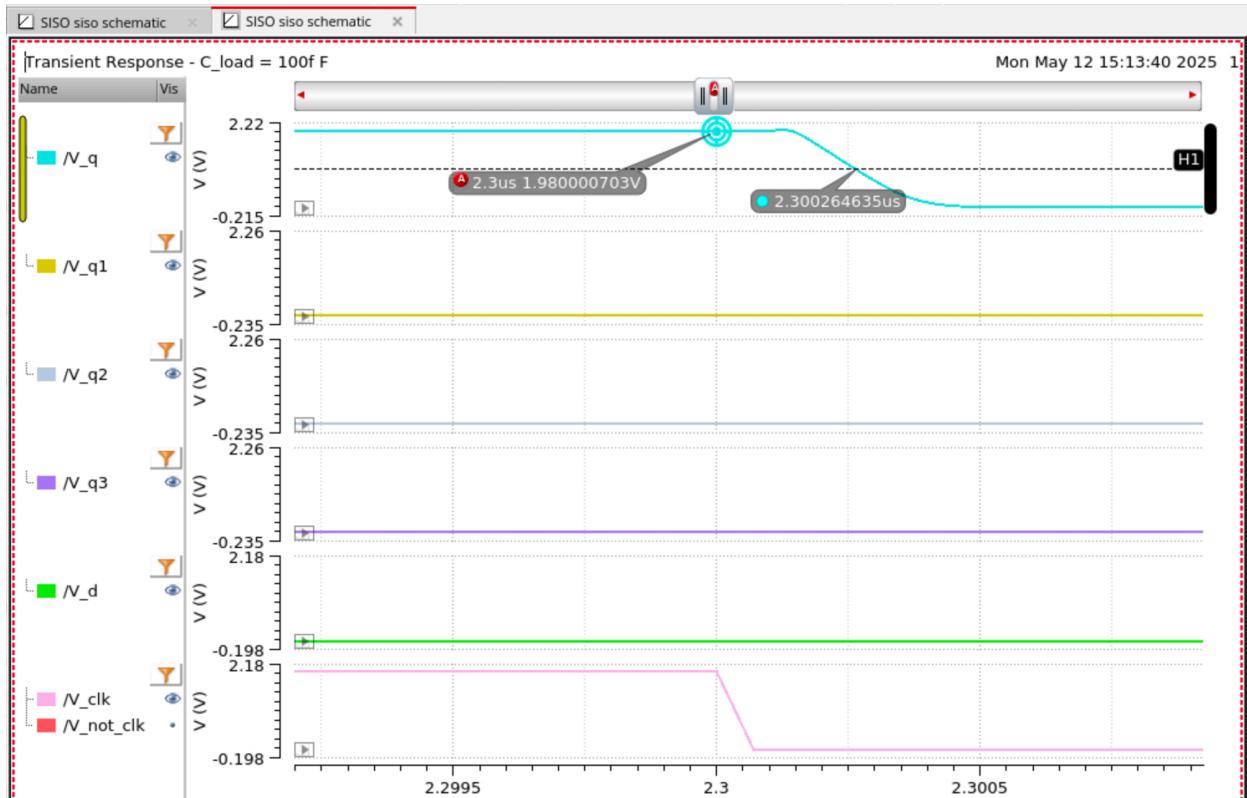


Fig. 5: High to low propagation delay measurement. τ_{PLH} was measured as 265ps.

A summary of the propagation delays for the pre layout schematic is provided in the table below:

Delay Type	Delay Value
τ_{PLH} (low to high)	246 ps
τ_{PHL} (high to low)	265 ps

Layout & Symbol Extraction

The layout consists of the layouts of negative edge flip flops from the previous lab in cascade:

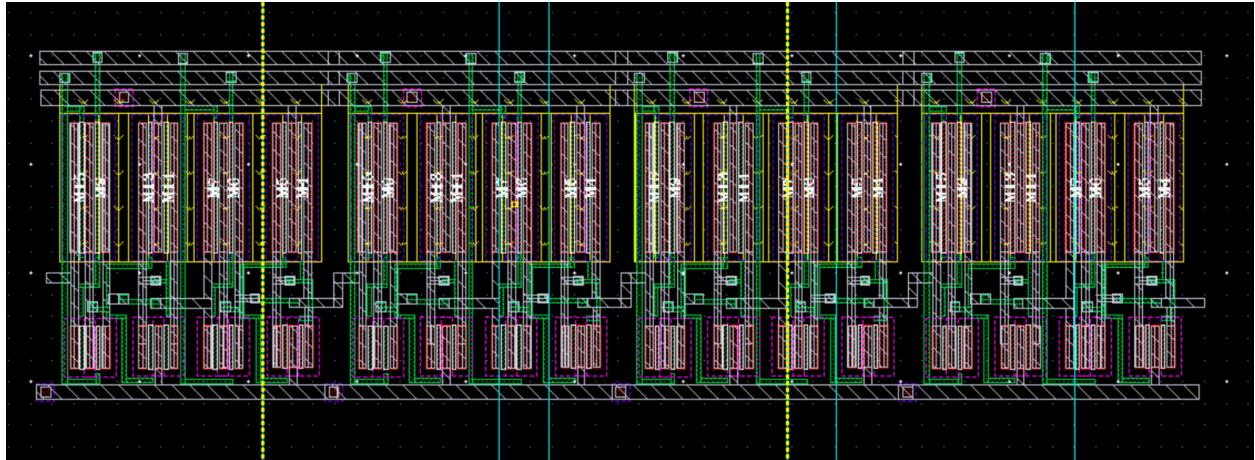


Fig. 6: Layout of the 4 bit SISO register.

DRC and LVS results are provided below:

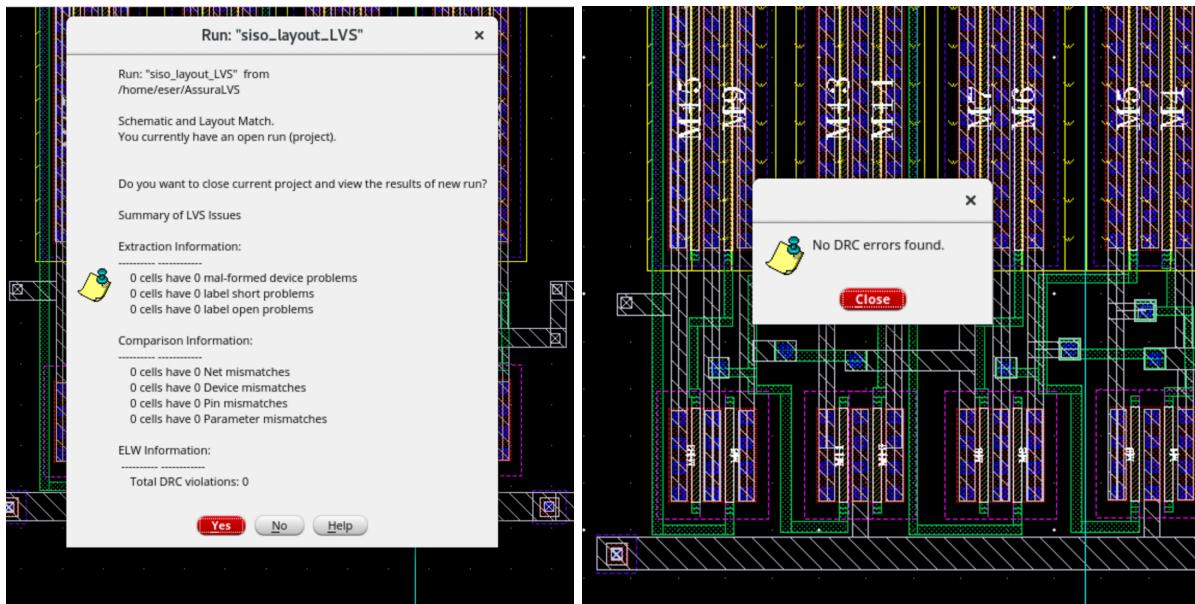


Fig. 7: LVS (left) and DRC (right) check results. The layout passes both tests successfully.

The extracted symbol for the SISO register is provided below:

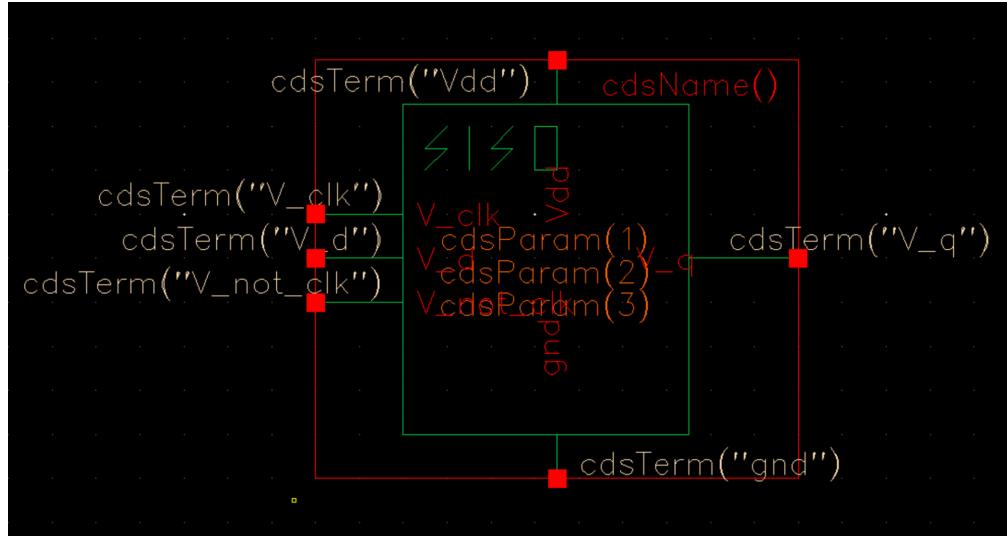


Fig. 8: Symbol for the 4 bit SISO register.

Post-layout Transient Simulation

The post layout testbench is identical to the pre-layout testbench except for the replacement of the 4 D flip flops with the extracted SISO symbol.

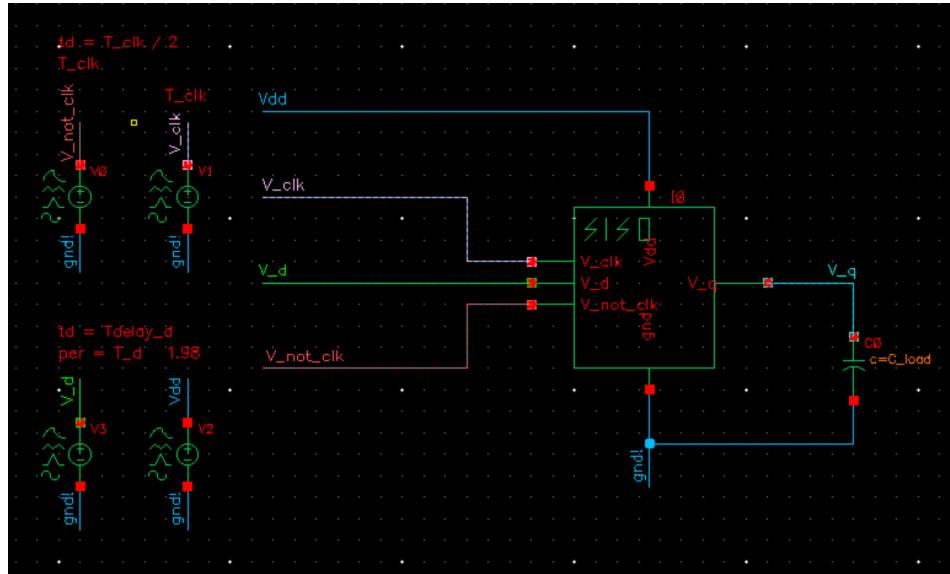


Fig. 9: Post-layout simulation testbench with extracted SISO symbol.

Transient post-layout simulation of the circuit is provided below:

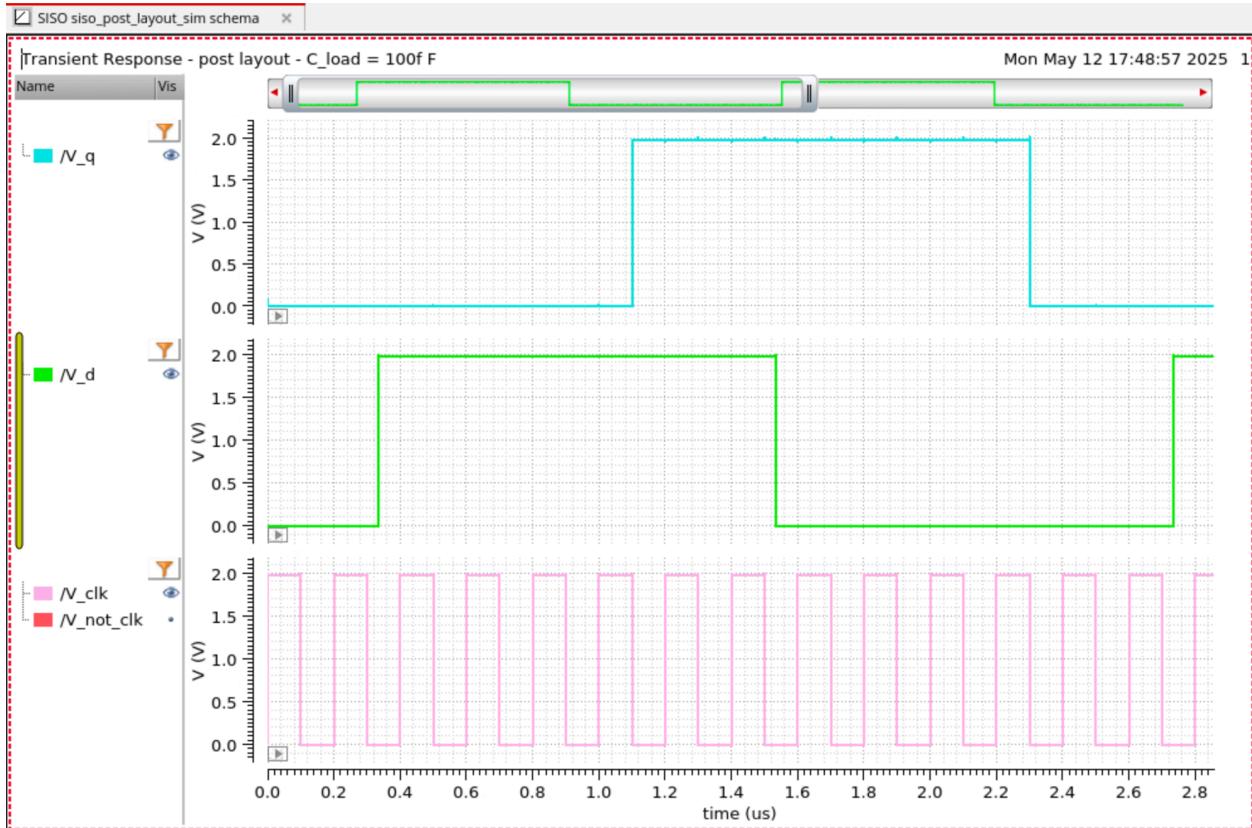


Fig. 10: Post layout transient simulation of the circuit with $C_{load} = 100f\text{ F}$.

As can be seen in the waveform above, the value of the input D propagates to the output 4 negative clock edges later. Which matches our expectations. The figure above shows two transitions of the output, with the first one being from low to high and the other from high to low. Each transition occurs exactly 4 clock cycles after input D changes.

Propagation Delays

Post layout propagation delay measurements are provided below:

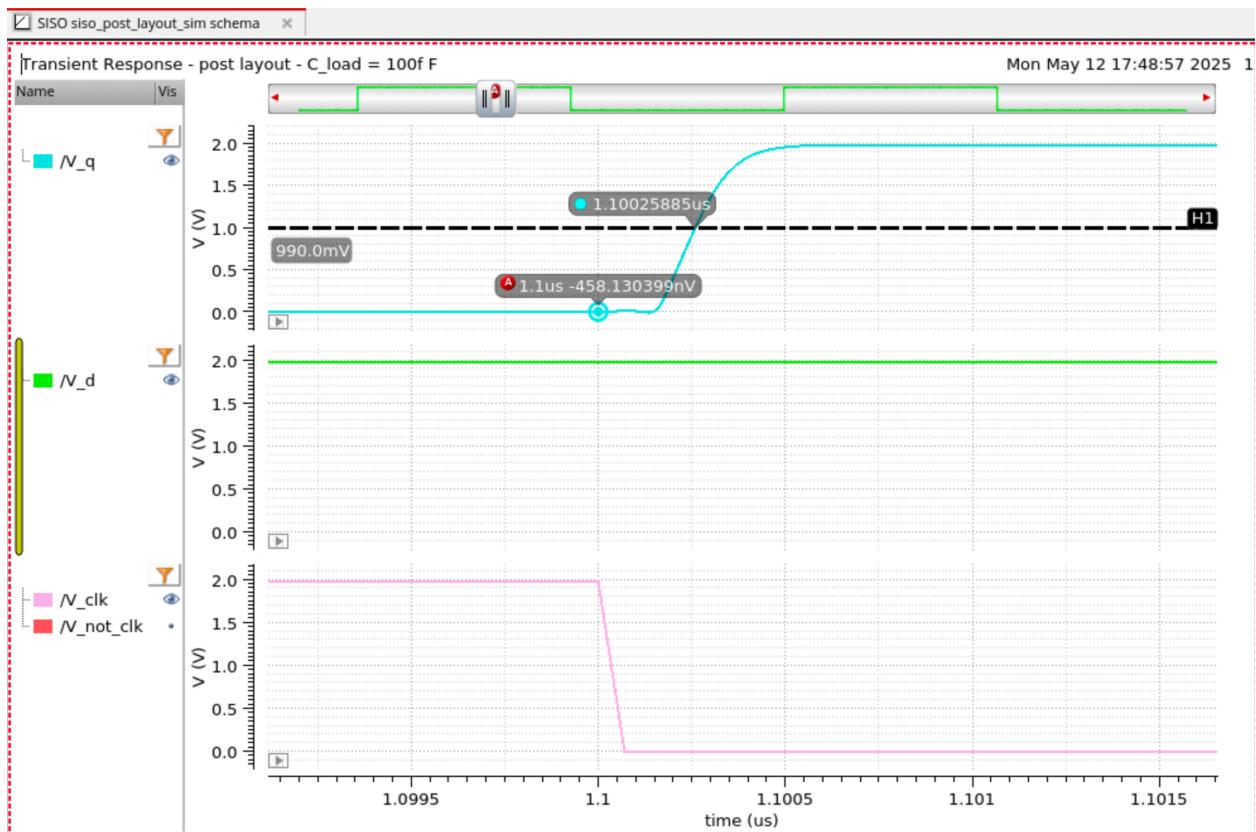


Fig. 11: Low to high propagation delay measurement. τ_{PLH} was measured as 259ps.

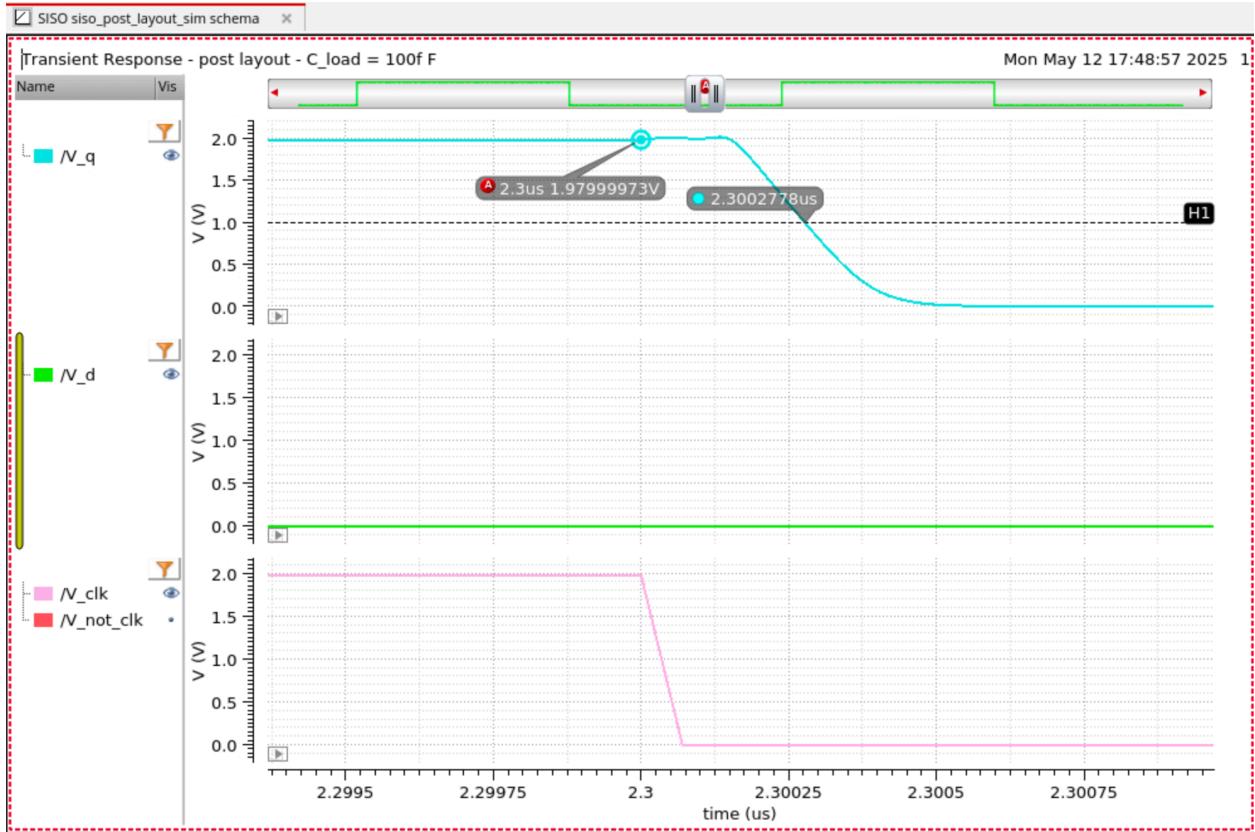


Fig. 12: High to low propagation delay measurement. τ_{PLH} was measured as 278ps.

There has been a ~ 10 ps increase in both propagation delays which is most likely due to layout parasitics. You may find a summary of the post layout propagation delays in the table below:

Delay Type	Delay Value
τ_{PLH} (low to high)	259 ps
τ_{PHL} (high to low)	278 ps