

06/03/2025

# EE302 Lab #1 Report

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## Part 1: Resistive Load Inverter

You may access the cellview of the resistive load inverter presented here by booting cadence and selecting the schematic under “lab\_1\_resistive\_load\_inverter\_schematic\_only” > “res\_load\_inverter” in the library manager window.

## Schematic

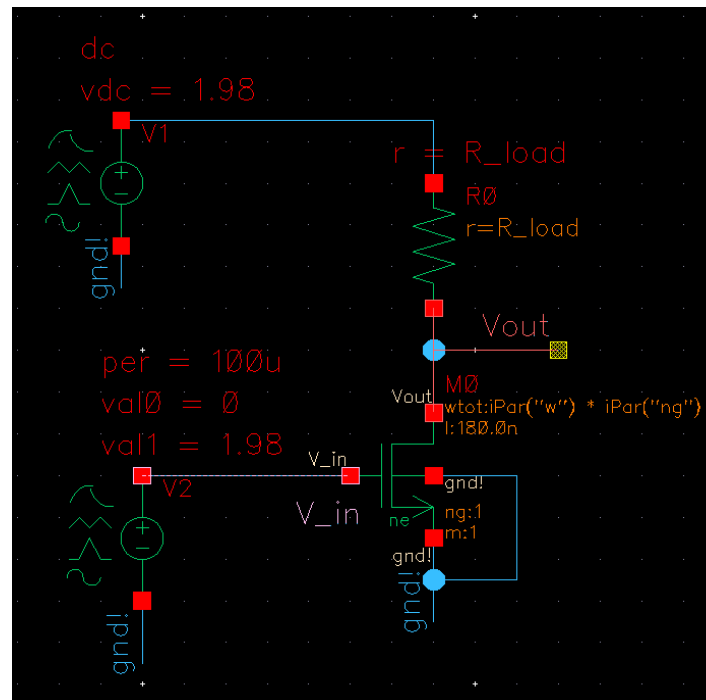


Fig 1. Resistive Load Inverter Schematic in Cadence Virtuoso. The resistance value of  $R_{load}$  has been tied to the parameter 'R\_load' which could be specified in the simulation screen.

### Edit Object Properties

Apply To: only current instance

Show: ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	PRIMLIB	off
Cell Name	PRIMLIB	value
View Name	symbol	off
Instance Name	M0	off

Add Delete Modify

CDF Parameter	Value	Display
Model name	ne	off
Voltage	1.98	off
Advanced Simulation Parameters	<input type="checkbox"/>	off
Calculate Width Method	<input checked="" type="radio"/> FingerWidth <input type="radio"/> DeviceWidth	off
Model Limits	<input checked="" type="checkbox"/>	off
Device Width	Par("w") * iPar("ng") M	off
Width per Finger	2u M	off
Length	180.0n M	off
Number of Fingers	1	off
Multiplier	1	off
m for Simulators	iPar("m")*iPar("ng")	off
Calculation Method	callbacks enabled	off
Drain diffusion area	9.6e-13	off
Source diffusion area	9.6e-13	off

OK Cancel Apply Defaults Previous Next Help

Fig 2. Configuration of MOSFET parameters for the NMOS driver transistor. The  $W_n$  value has been specified as  $2\mu\text{m}$  and  $L_n$  as  $180\text{nm}$ .

## Transient Simulation Testbench

Transient testbench features a pulse voltage source for  $V_{in}$  that have been configured with the following parameters:

- Zero Value: 0V
- One value: 1.98 V
- Period of waveform = 100 $\mu$ s
- Rise and fall times = 70ps

One should note that the parameters above were copied from the design guides shared over SuCourse and do not represent an ideal square wave/step input signal.

Property	Value	Display
Library Name	analogLib	off
Cell Name	vsource	off
View Name	symbol	off
Instance Name	V2	off

User Property	Master Value	Local Value	Display
lvignore	TRUE		off

CDF Parameter	Value	Display
DC voltage	0 V	off
Source type	pulse	off
Frequency name 1		off
Delay time		off
Zero value	0 V	both
One value	1.98 V	both
Period of waveform	100u s	both
Rise time	70p s	off
Fall time	70p s	off
Type of rising & falling edge		off
Pulse width		off
Display small signal params	<input type="checkbox"/>	off
Display temperature params	<input type="checkbox"/>	off
Display noise parameters	<input type="checkbox"/>	off
Multiplier		off

Fig 3. Configuration of the pulse voltage source connected to  $V_{in}$

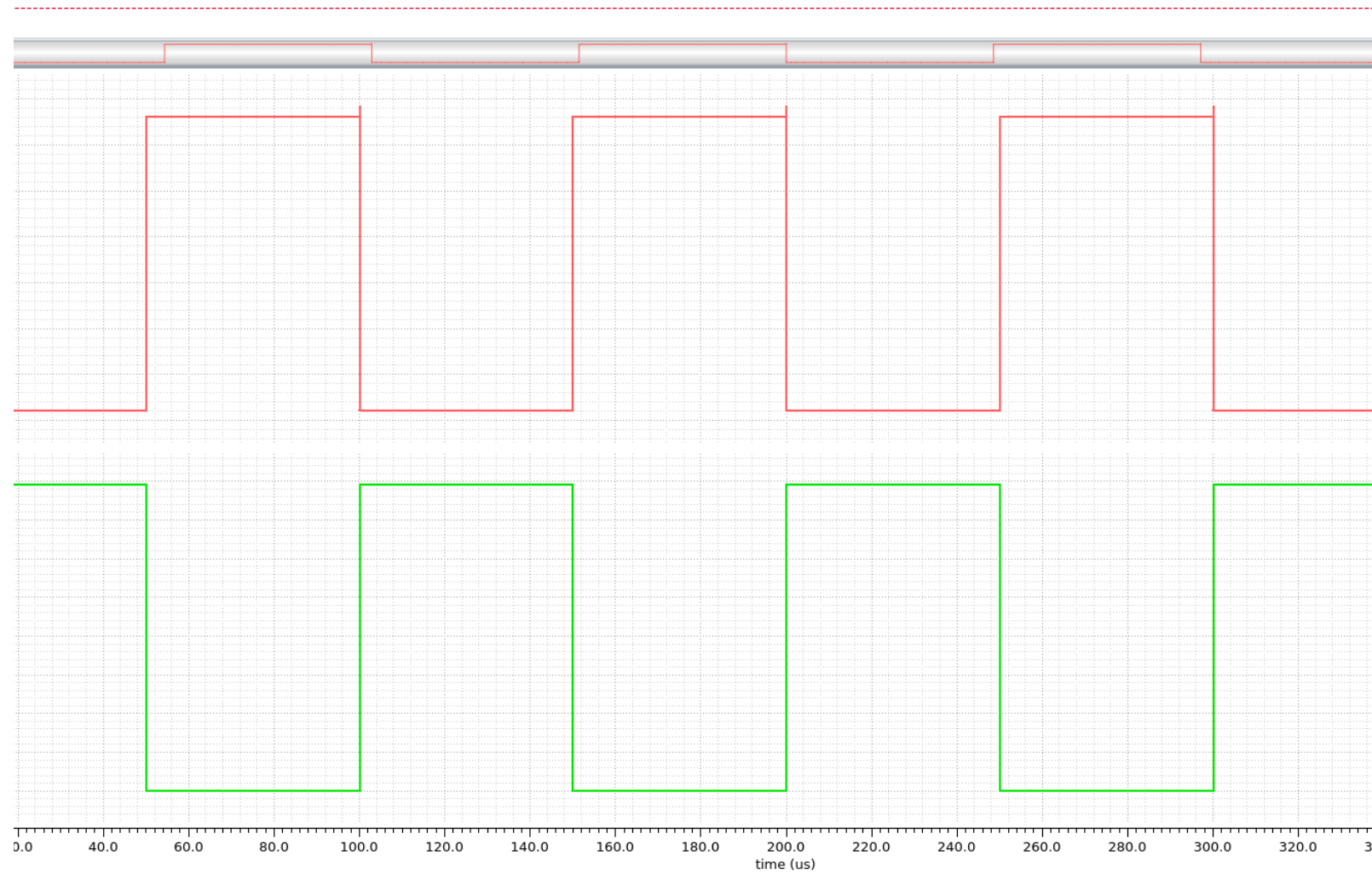
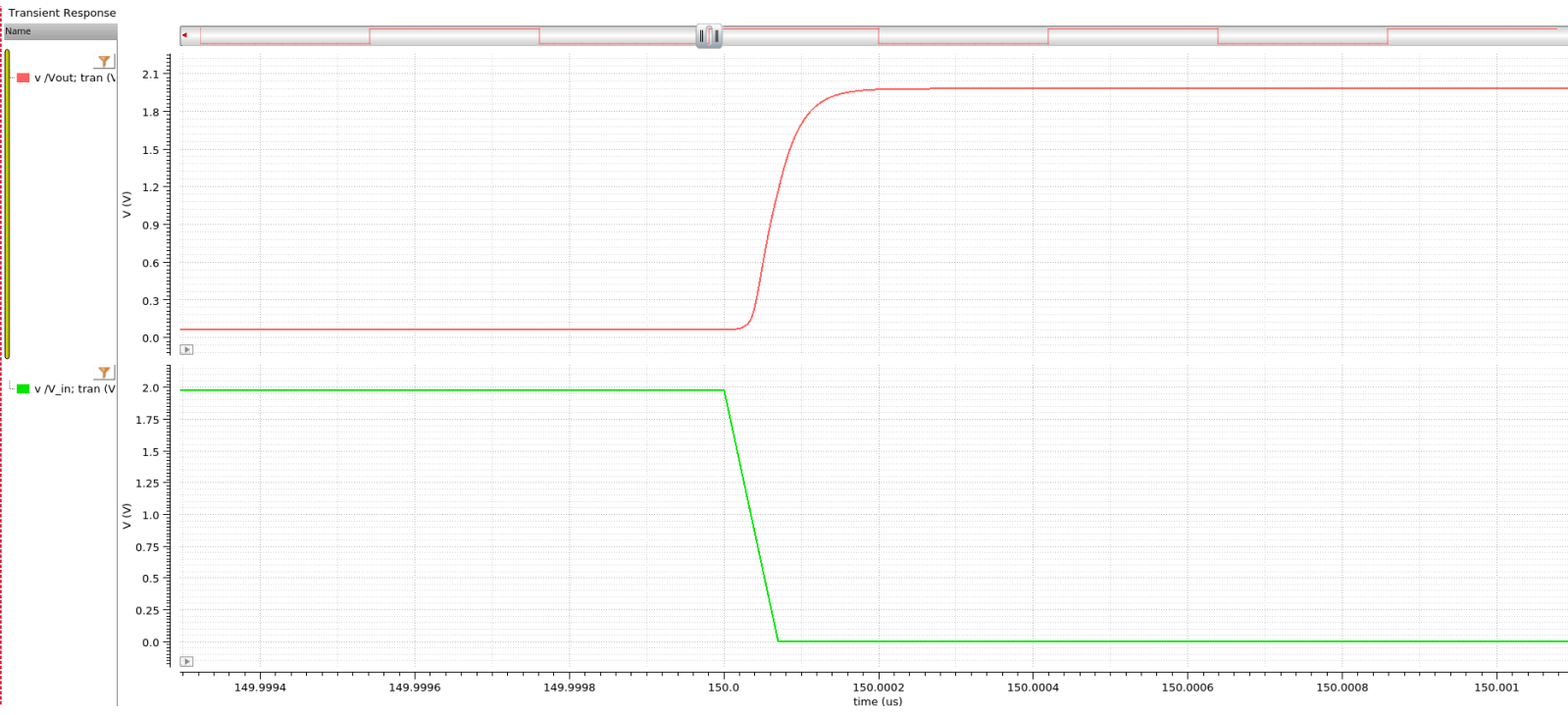


Fig 4. Transient testbench simulation results

Zooming in to see rise and fall responses of the inverter better:



Figs 5-6. Fall and rise responses of the resistive load inverter.

## VTC Curves

VTC curves for  $R_{load}$  values  $\in \{10k\Omega, 20k\Omega, 30k\Omega\}$  are provided below. The curves have been obtained under a DC simulation with a sweep over values of  $V_{in}$  ranging from 0V to  $V_{DD} = 1.98V$ .

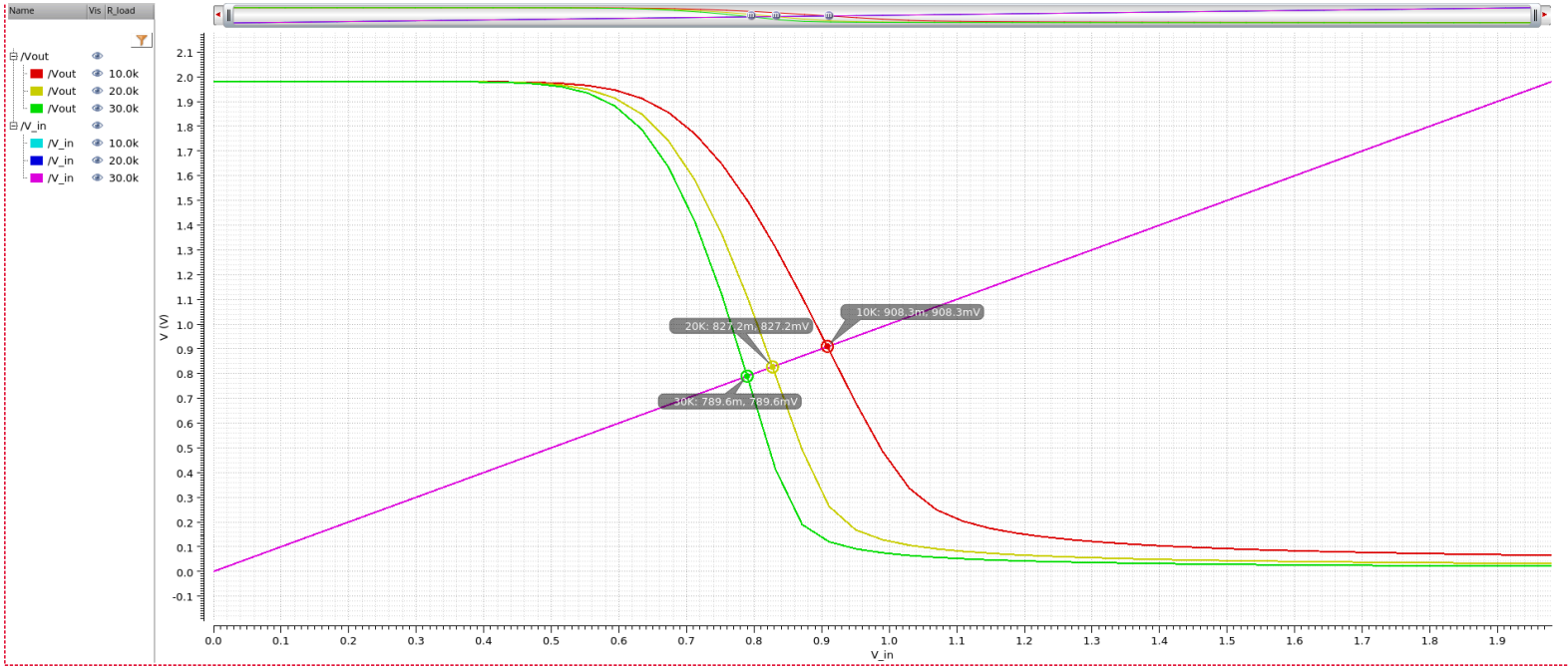


Fig 7. VTC curves for varying  $R_{load}$  values. The threshold voltages were found as:  $V_{th, 30k} = 789.6mV$ ,  $V_{th, 20k} = 827.2mV$ ,  $V_{th, 10k} = 908.3mV$

## Part 2: CMOS Inverter

You may access the cellview of the CMOS inverter presented here by booting cadence and selecting the “cmos\_inverter” (schematic), “cmos\_inverter\_layout” (layout and symbol), “post\_layout\_sim” (sim using extracted symbol) under “lab\_1\_cmos\_inverter” in the library manager window.

### Calculation of $W_p$

We know that when  $V_{in} = V_{th}$ , both the NMOS and PMOS transistors are in saturation.

KCL at the output yields:

$$\frac{k_n}{2} (V_{GS,n} - V_{T0,n})^2 = \frac{k_p}{2} (V_{GS,p} - V_{T0,p})^2$$

Plugging in  $V_{in} = V_{GS,n}$  and  $V_{in} - V_{DD} = V_{GS,p}$ :

$$= \frac{k_n}{2} (V_{in} - V_{T0,n})^2 = \frac{k_p}{2} (V_{in} - V_{DD} - V_{T0,p})^2$$

After algebraic arrangements:

$$V_{in} = V_{Th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} + V_{T0,p})}{1 + \sqrt{\frac{1}{k_R}}}$$

We know that:

$$k_n = k_n' \cdot \left(\frac{W}{L}\right)_n = 160 \frac{\mu A}{V^2} \cdot \left(\frac{2 \mu m}{180 nm}\right) = 1.78 mA/V^2$$

Plugging in parameters and  $V_{Th} = V_{DD} / 2$ :

$$V_{Th} = 0.99 V = \frac{0.55 V + \sqrt{\frac{k_p}{1.78 mA/V^2}} \cdot (1.98 V + -0.57 V)}{1 + \sqrt{\frac{k_p}{1.78 mA/V^2}}}$$

$$\Rightarrow 1.048 = \sqrt{\frac{k_p}{1.78 mA/V^2}} \Rightarrow \left(\frac{W}{L}\right)_p = 34.4 \Rightarrow W_p = 6.19 \mu m$$

Hence we need to set the “width per finger” parameter to 6.19μm in order to obtain a  $V_{Th}$  value of  $V_{DD} / 2 = 0.99 V$



## Schematic

The schematic of the CMOS inverter designed in this part of this lab is given below:

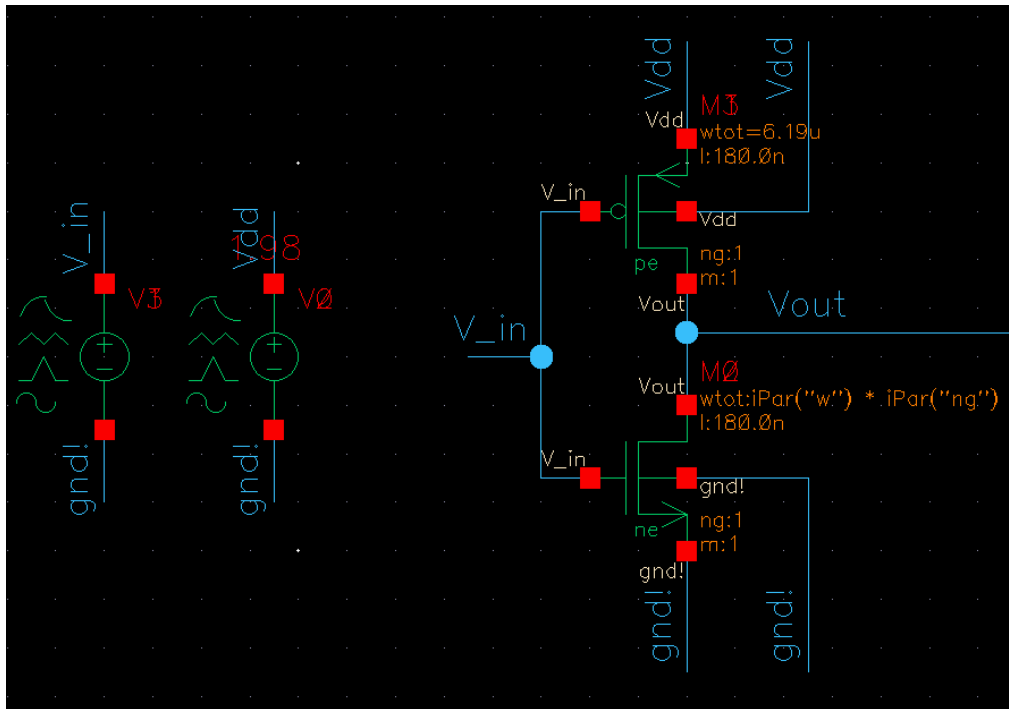


Fig 8. Schematic of a CMOS inverter

## Pre-layout Simulations

The VTC curve of the inverter was obtained as provided below:

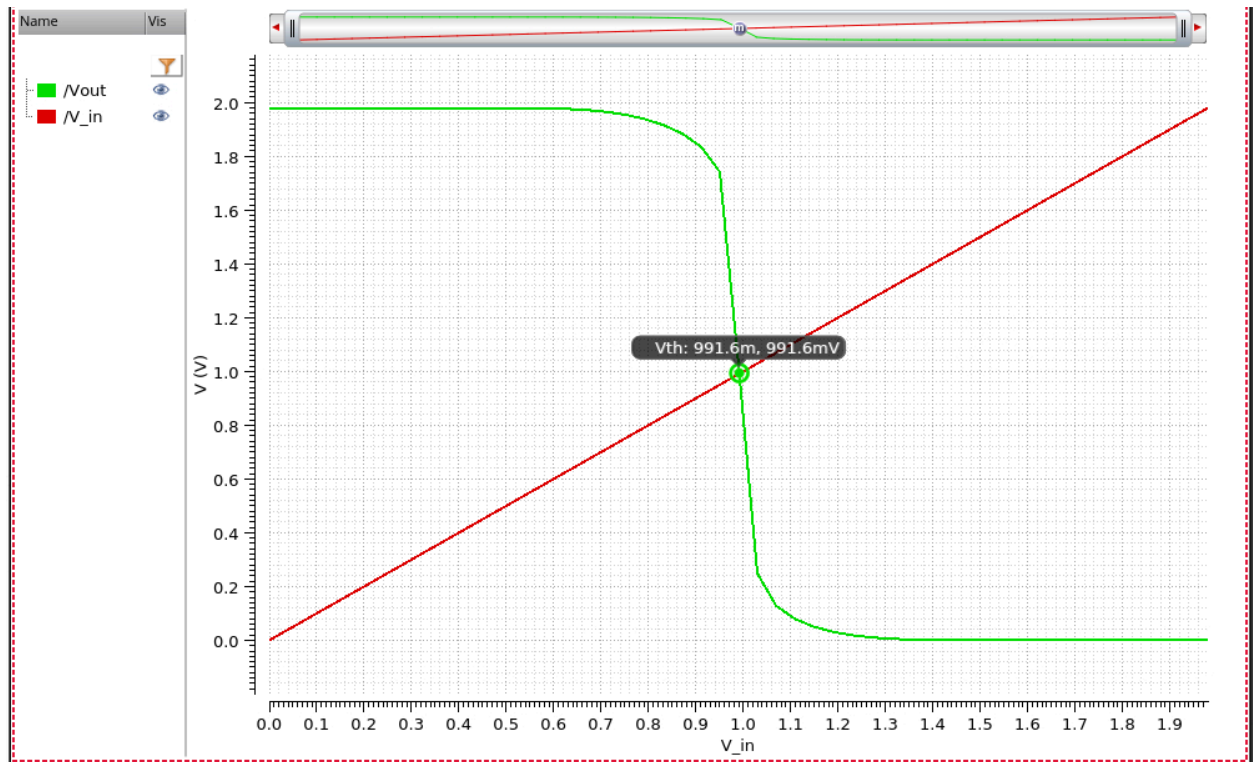


Fig 9. Pre-layout VTC of the CMOS inverter. The threshold voltage was found as 991.6mV which satisfies the  $V_{th} = V_{DD} / 2$  requirement.

## Layout

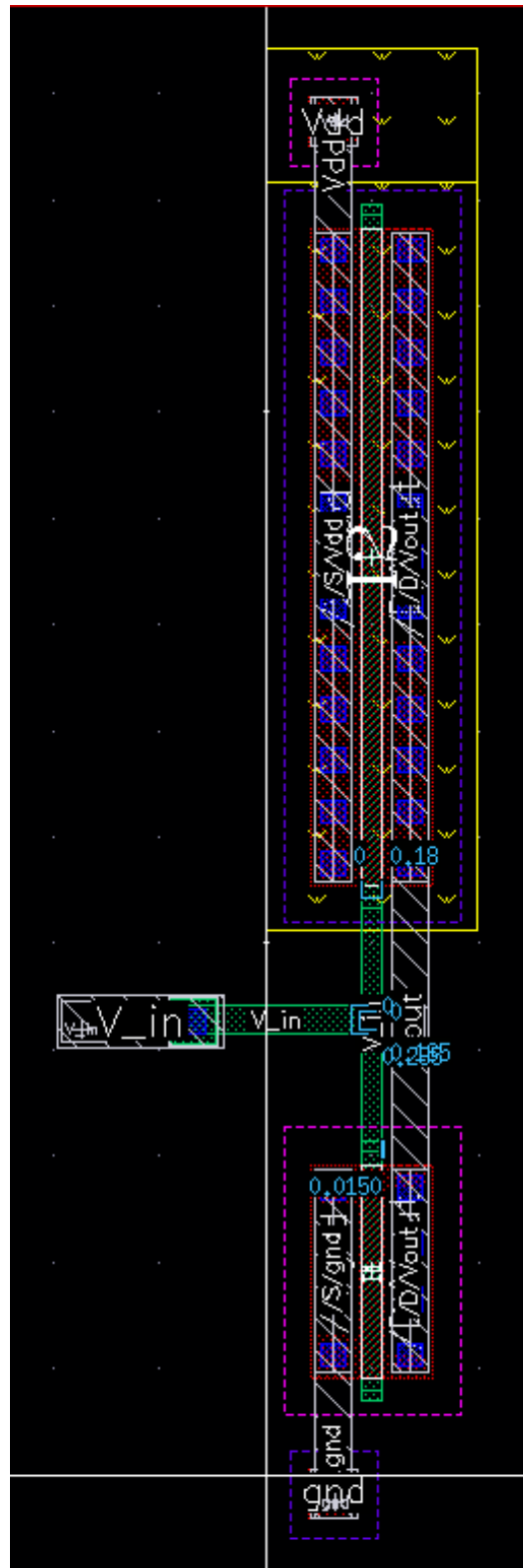


Fig 10. Layout of the CMOS Inverter.

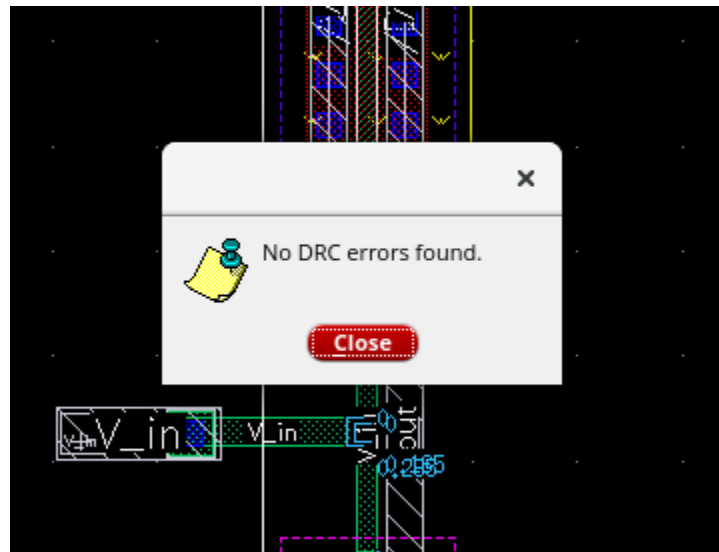


Fig 11. DRC results screen.

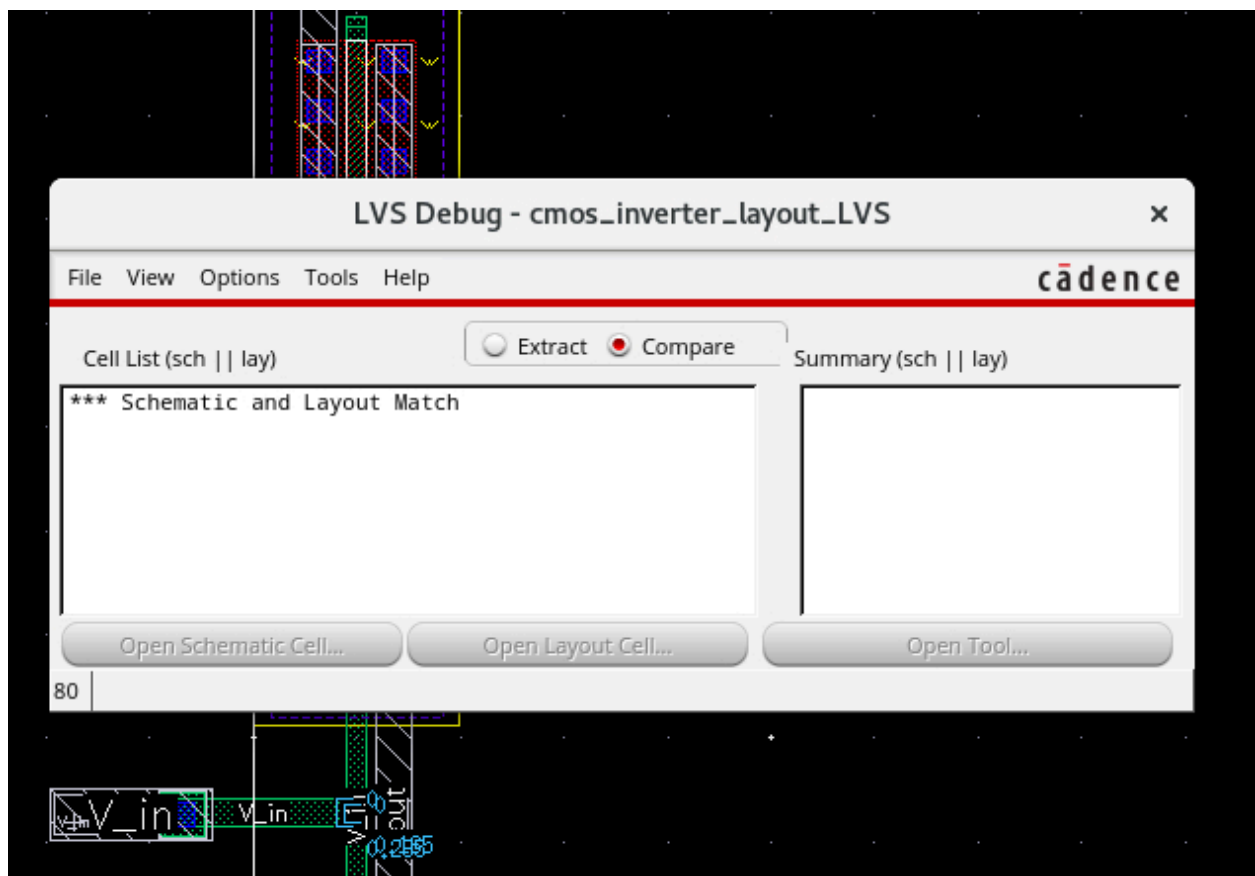


Fig 12. LVS check results screen.

## Symbol Extraction

You may access the symbol by selecting “lab1\_2\_cmos\_inverter” > “cmos\_inverter\_layout” > “symbol” in the library manager window.

I chose to model my inverter layout’s symbol after the inverter logic gate symbol:

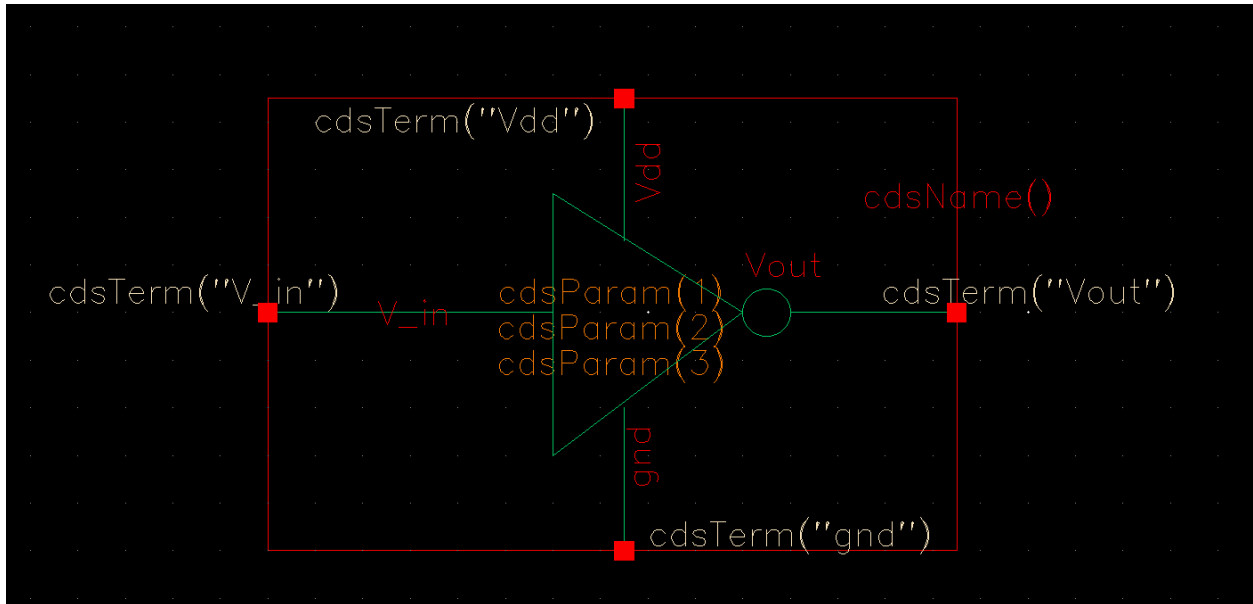


Fig 13. Symbol I chose for the CMOS inverter.

## Post-layout Simulations

For post-layout transient simulations, a capacitor was connected between  $V_{out}$  and GND. The resulting testbench schematic is provided below:

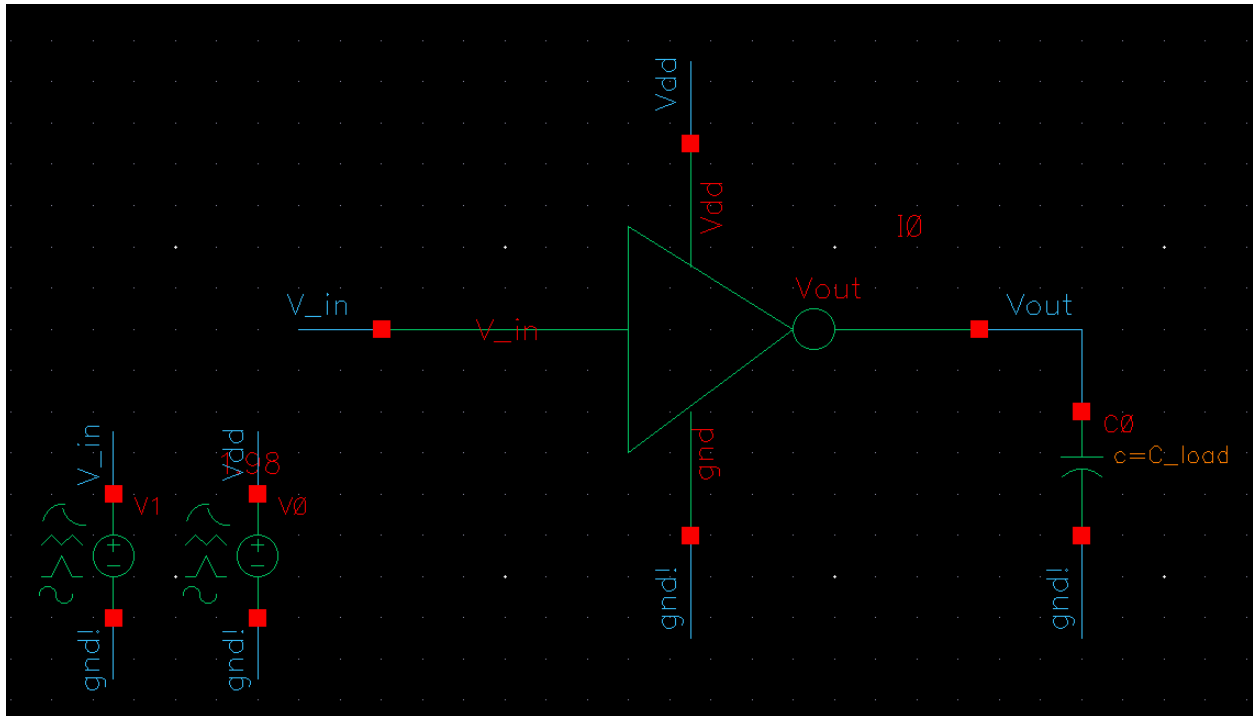


Fig 14. Testbench schematic for post-layout simulation. I chose to set the values for  $C_{load}$  in the simulation window.

## VTC

The VTC of the created layout is provided below:

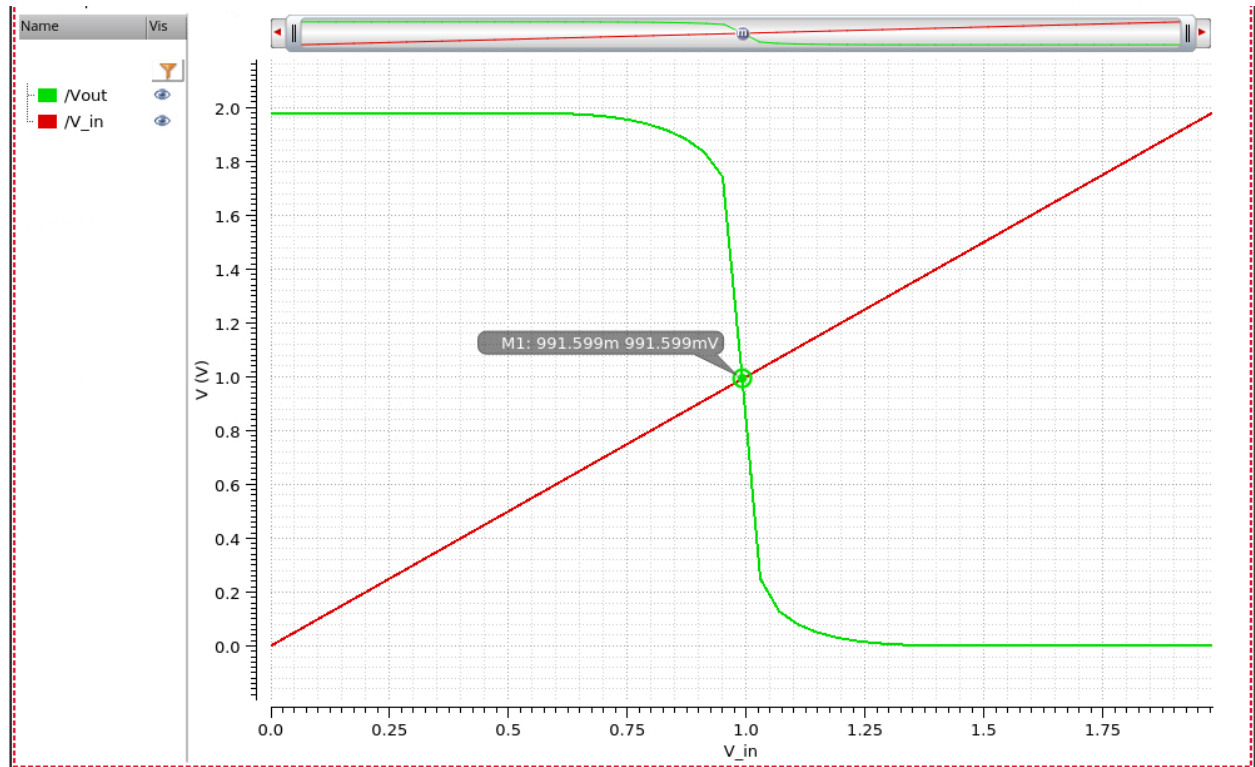


Fig 15. VTC of the created layout.  $V_{th}$  was found as  $\sim 0.9916$  V which matches the design requirements as well as the created schematic.

## Transient Simulation

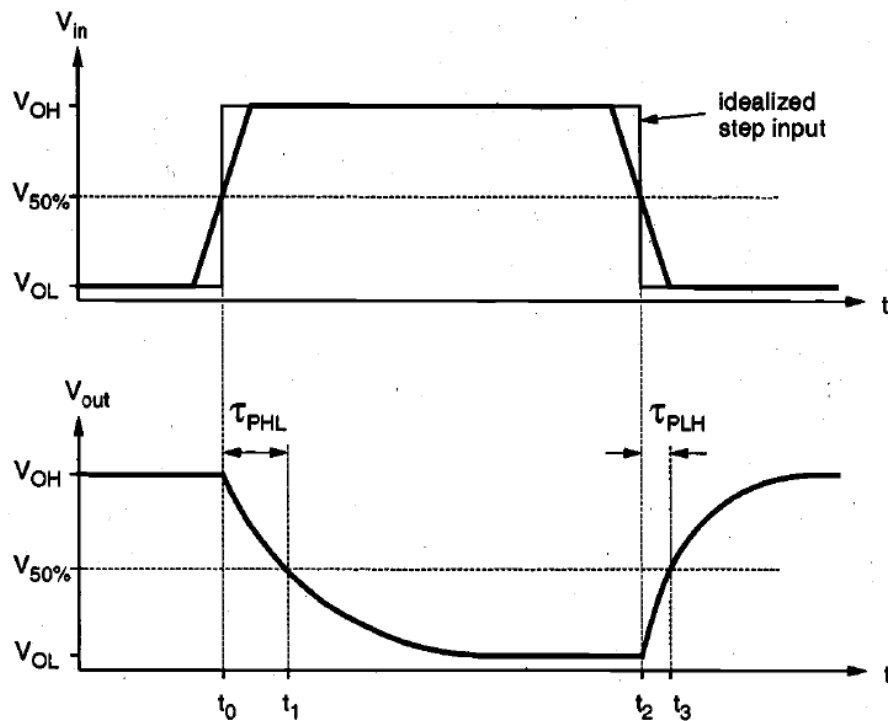
Transient simulation was run for  $C_{load} \in \{200\text{f F}, 500\text{f F}\}$  with  $V_{in}$  configured as follows:

CDF Parameter	Value	Display
DC voltage	0 V	off
Source type	pulse	off
Frequency name 1		off
Delay time	500.0u s	off
Zero value	0 V	off
One value	1.98 V	off
Period of waveform	100m s	off
Rise time	1p s	off
Fall time	1p s	off
Type of rising & falling edge		off
Pulse width	50m s	off
Display small signal params	<input type="checkbox"/>	off
Display temperature params	<input type="checkbox"/>	off
Display noise parameters	<input type="checkbox"/>	off
Multiplier		off

Fig 16.  $V_{in}$  pulse input configuration used for transient simulations.



## Measuring $\tau_{PLH}$ and $\tau_{PHL}$



$\tau_{PLH}$  and  $\tau_{PHL}$  have been defined as  $t_1 - t_0$  and  $t_3 - t_2$  respectively for the plot above. Measuring  $\tau_{PLH}$  and  $\tau_{PHL}$  requires measurement of the time stamps at which  $V_{out}$  begins rising from  $V_{OL}$ /falling from  $V_{OH}$  and reaches  $V_{50\%} = 0.99$  V. You may find the plots obtained for  $C_{load}$  values 200f F and 500f F below.

$C_{load} = 200\text{f F}$  - Measurements

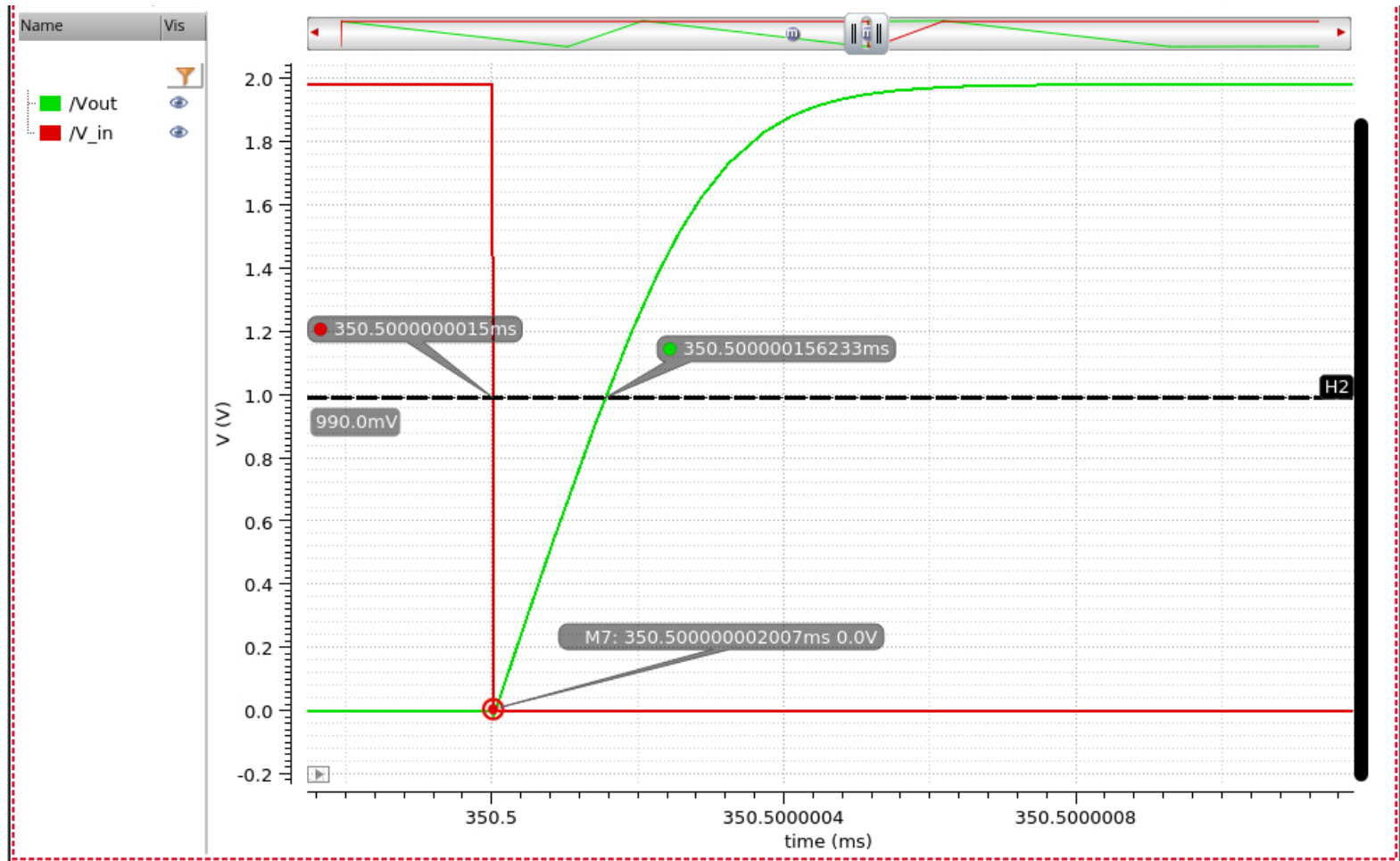


Fig 17.  $t_{50\%}$  and  $t_{OL}$  measurements from transient simulation with  $200\text{f F}$   $C_{load}$  during rising input

Using the markers on the plot outlining timestamps at which  $V_{OL}$  and  $V_{50\%}$  values are attained at  $V_{out}$

$$\tau_{PLH} = 350.500000156233 - 350.50000002007 = 1.54 \cdot 10^{-7} \text{ ms} = 154.2 \text{ ps}$$

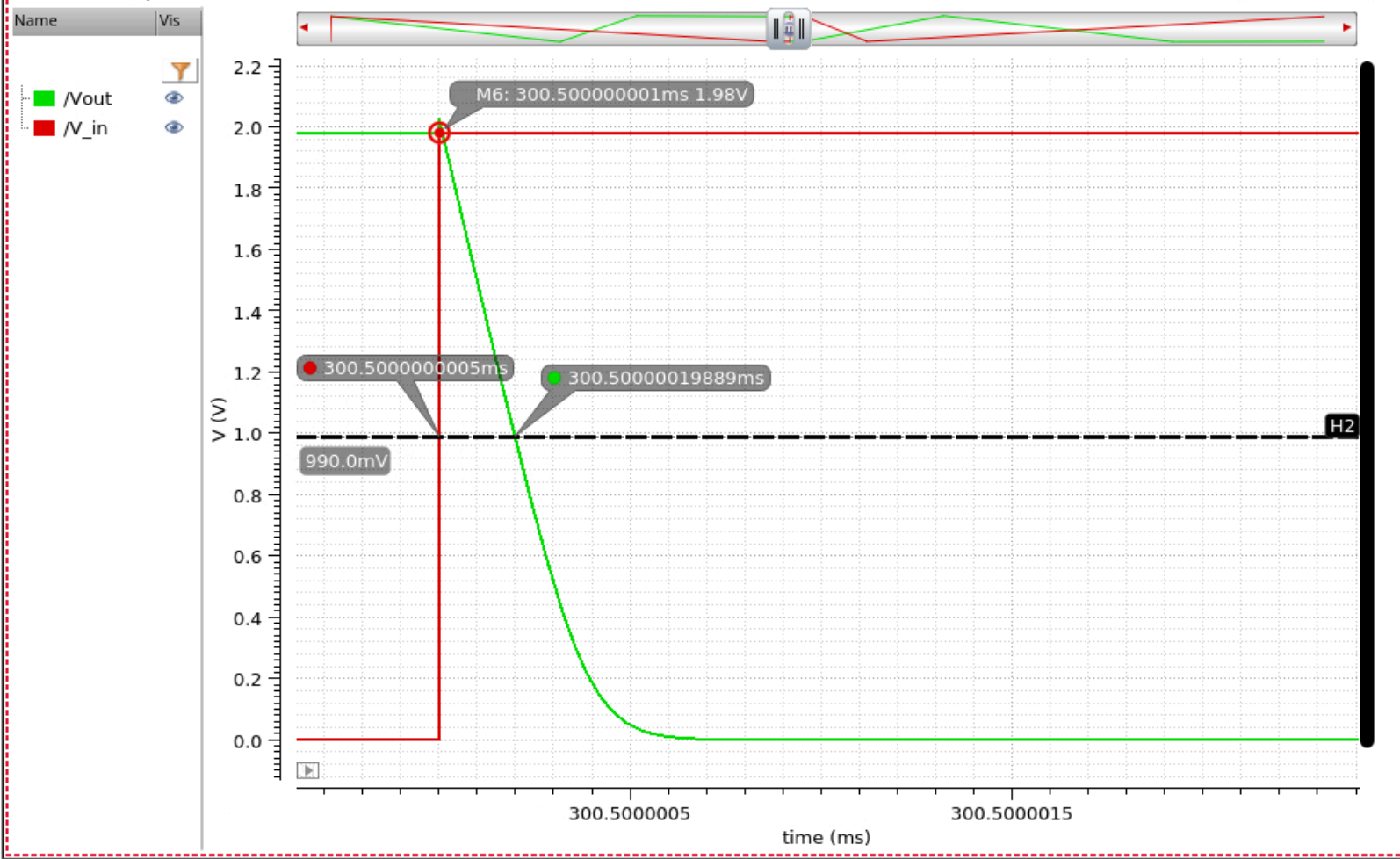


Fig 18.  $t_{50\%}$  and  $t_{OL}$  measurements from transient simulation with 200f  $C_{load}$  during rising input

Using the markers on the plot outlining timestamps at which  $V_{OL}$  and  $V_{50\%}$  values are attained at  $V_{out}$

$$\tau_{PHL} = 300.50000019889 - 300.500000001 = 1.9889 \cdot 10^{-7} ms = 198.9 ps$$

$C_{load} = 200f$  F - Calculations

For a CMOS inverter ( $V_{OH} = V_{DD}$ ,  $V_{OL} = 0V$ ),  $\tau_{PHL}$  is given as:

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0,n})} \cdot \left[ \frac{2V_{T0,n}}{V_{DD} - V_{T0,n}} + \ln\left(\frac{4(V_{DD} - V_{T0,n})}{V_{DD}} - 1\right) \right]$$

Plugging in provided parameters and  $C_{load} = 200f$  F:

$$\tau_{PHL} = \frac{200 \cdot 10^{-15} F}{(1.78 \frac{mA}{V^2})(1.98 V - 0.55 V)} \cdot \left[ \frac{2 \cdot 0.55 V}{1.98 V - 0.55 V} + \ln \left( \frac{4(1.98 V - 0.55 V)}{1.98 V} - 1 \right) \right] = 110.4 ps$$

For a CMOS inverter ( $V_{OH} = V_{DD}$ ,  $V_{OL} = 0V$ ),  $\tau_{PLH}$  is given as:

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0,p}|)} \cdot \left[ \frac{2|V_{T0,p}|}{V_{DD} - |V_{T0,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T0,p}|)}{V_{DD}} - 1 \right) \right]$$

Plugging in provided parameters and  $C_{load} = 200f F$ :

$$\tau_{PLH} = \frac{200 \cdot 10^{-15} F}{(1.95 \frac{mA}{V^2})(1.98 V - 0.57 V)} \cdot \left[ \frac{2 \cdot 0.57 V}{1.98 V - 0.57 V} + \ln \left( \frac{4(1.98 V - 0.57 V)}{1.98 V} - 1 \right) \right] = 103.5 ps$$

$C_{load} = 500f F$  - Measurements

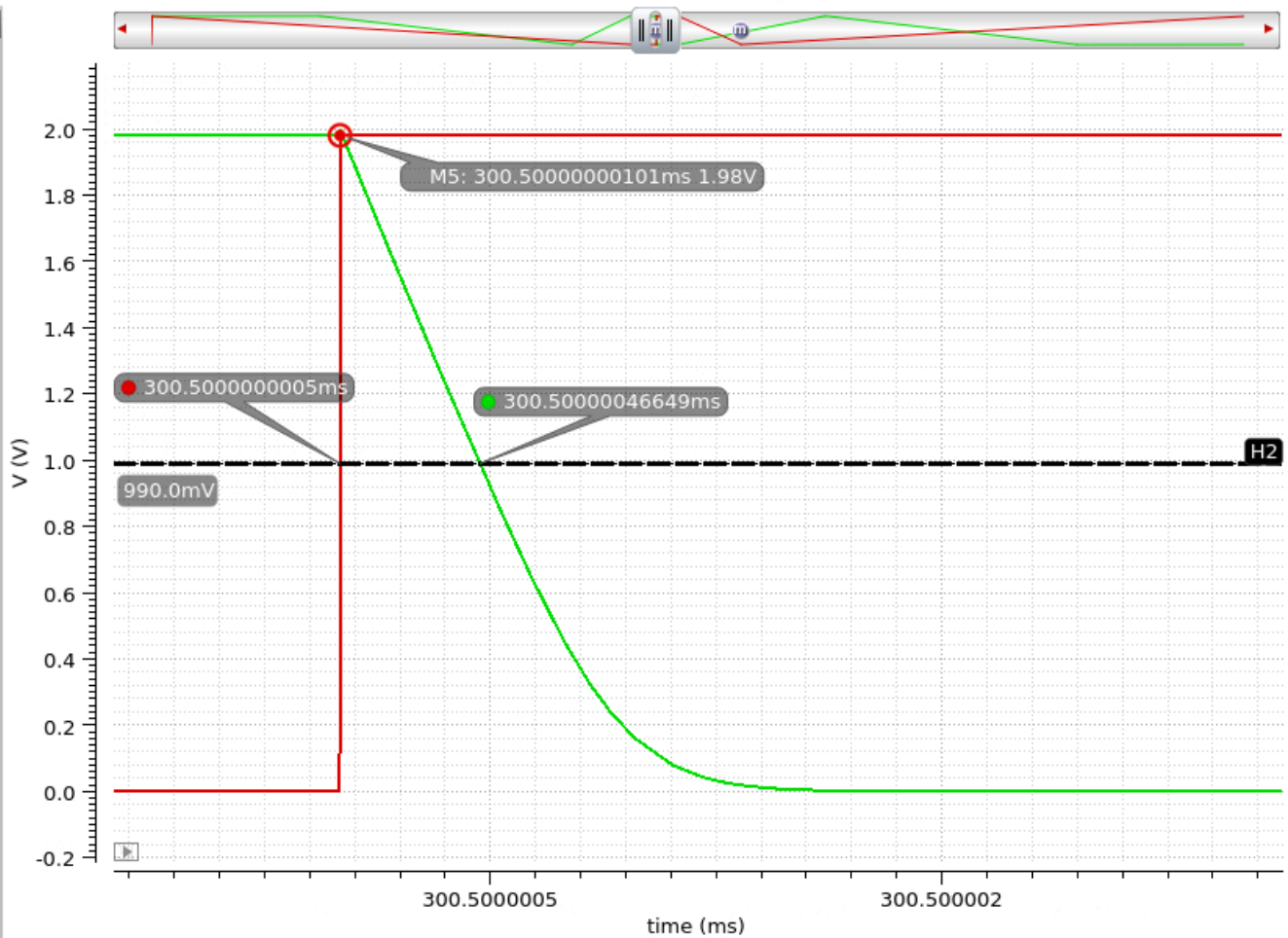


Fig 19.  $t_{50\%}$  and  $t_{OL}$  measurements from transient simulation with 500f  $C_{load}$  during rising input

Using the markers on the plot outlining timestamps at which  $V_{OL}$  and  $V_{50\%}$  values are attained at  $V_{out}$

$$\tau_{PHL} = 300.50000046649 - 300.5000000101 = 3.65 \cdot 10^{-7} ms = 465.5 ps$$

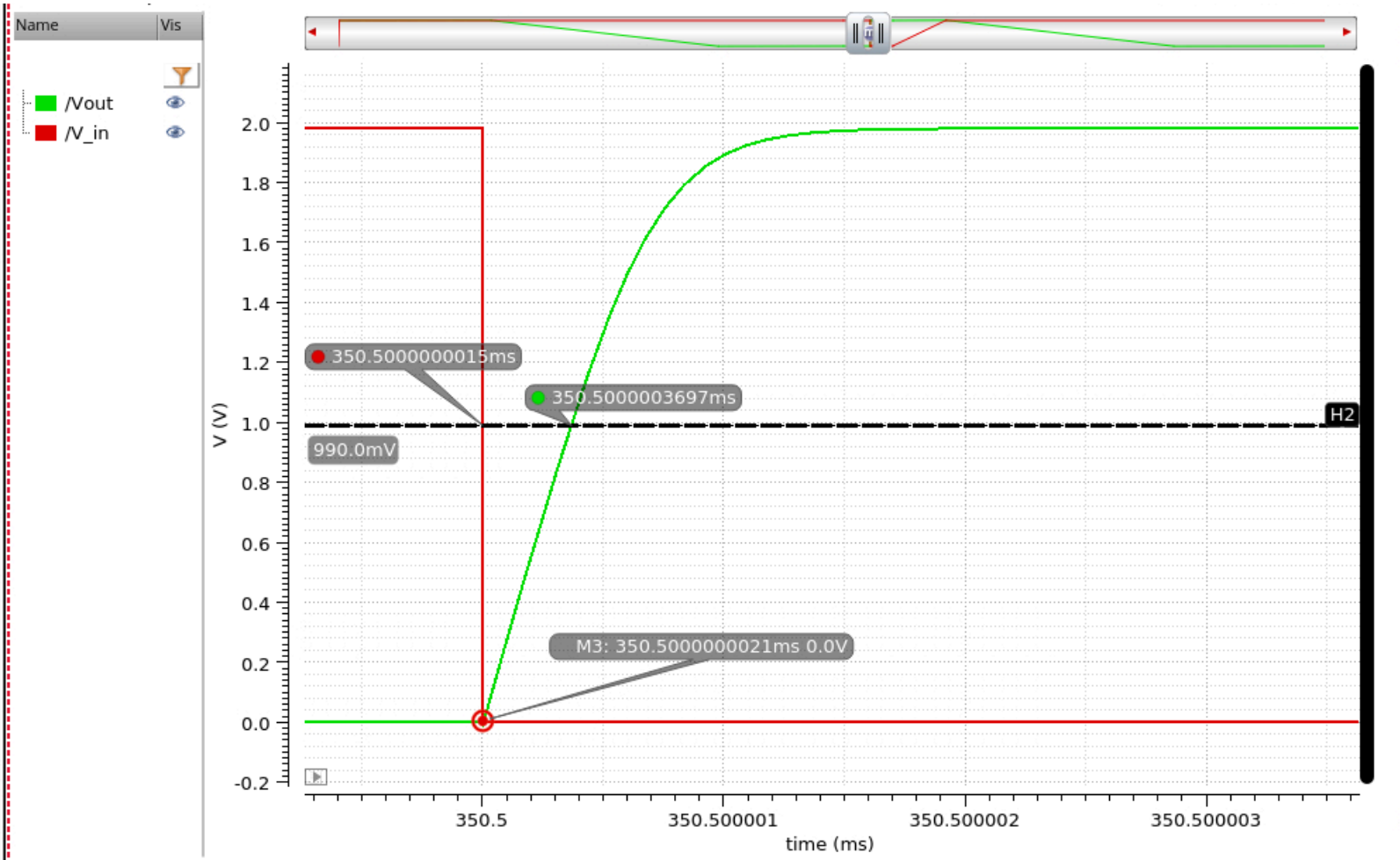


Fig 20.  $t_{50\%}$  and  $t_{OL}$  measurements from transient simulation with 500f  $C_{load}$  during falling input

Using the markers on the plot outlining timestamps at which  $V_{OL}$  and  $V_{50\%}$  values are attained at  $V_{out}$

$$\tau_{PLH} = 350.5000003697 - 350.5000000021 = 3.68 \cdot 10^{-7} ms = 367.6 ps$$

$C_{load} = 500f$  F - Calculation

Using the same formulas as the previous part we get:

$$\tau_{PHL} = \frac{500 \cdot 10^{-15} F}{(1.78 \frac{mA}{V^2})(1.98 V - 0.55 V)} \cdot \left[ \frac{2 \cdot 0.55 V}{1.98 V - 0.55 V} + \ln \left( \frac{4(1.98 V - 0.55 V)}{1.98 V} - 1 \right) \right] = 276.0 ps$$

$$\tau_{PLH} = \frac{500 \cdot 10^{-15} F}{(1.95 \frac{mA}{V^2})(1.98 V - 0.57 V)} \cdot \left[ \frac{2 \cdot 0.57 V}{1.98 V - 0.57 V} + \ln \left( \frac{4(1.98 V - 0.57 V)}{1.98 V} - 1 \right) \right] = 258.8 ps$$

## Evaluation

Calculated and measured values for low-to-high and high-to-low propagation delay are summarized below:

C <sub>load</sub>	Propagation Delay		Value	Percentage Error
200f F	$\tau_{PHL}$	measured	198.9 ps	80.2%
		calculated	110.4 ps	
	$\tau_{PLH}$	measured	154.2 ps	50.0%
		calculated	103.5 ps	
500f F	$\tau_{PHL}$	measured	465.5 ps	68.7%
		calculated	276.0 ps	
	$\tau_{PLH}$	measured	367.6 ps	42.0%
		calculated	258.8 ps	

V<sub>Th</sub> values obtained from pre-layout and post-layout simulations were found to be identical (after truncating digits beyond the required precision). The measured V<sub>Th</sub> value, 991.6mV shows a percentage error of 0.016%.

Overall the design shows desirable VTC characteristics with V<sub>Th</sub> matching the desired value. Unfortunately, the design is slower than expected as the difference between measured and calculated values of propagation delays demonstrate. It is interesting to note that  $\tau_{PLH}$  shows less discrepancy between calculated and measured values compared to  $\tau_{PHL}$ .