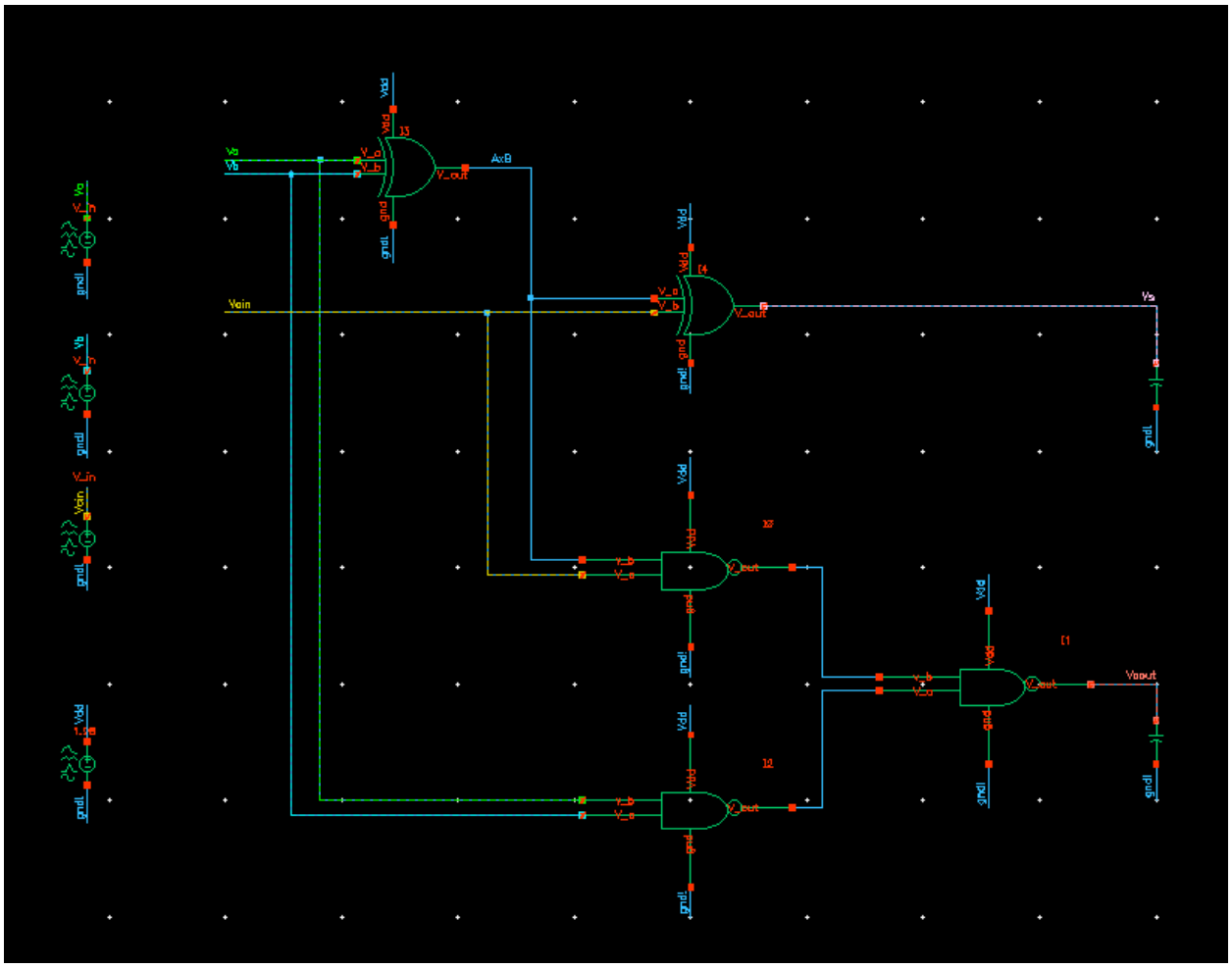
EE302 Spring 2025 Lab 3 Report

20/04/2025

Full Adder Design

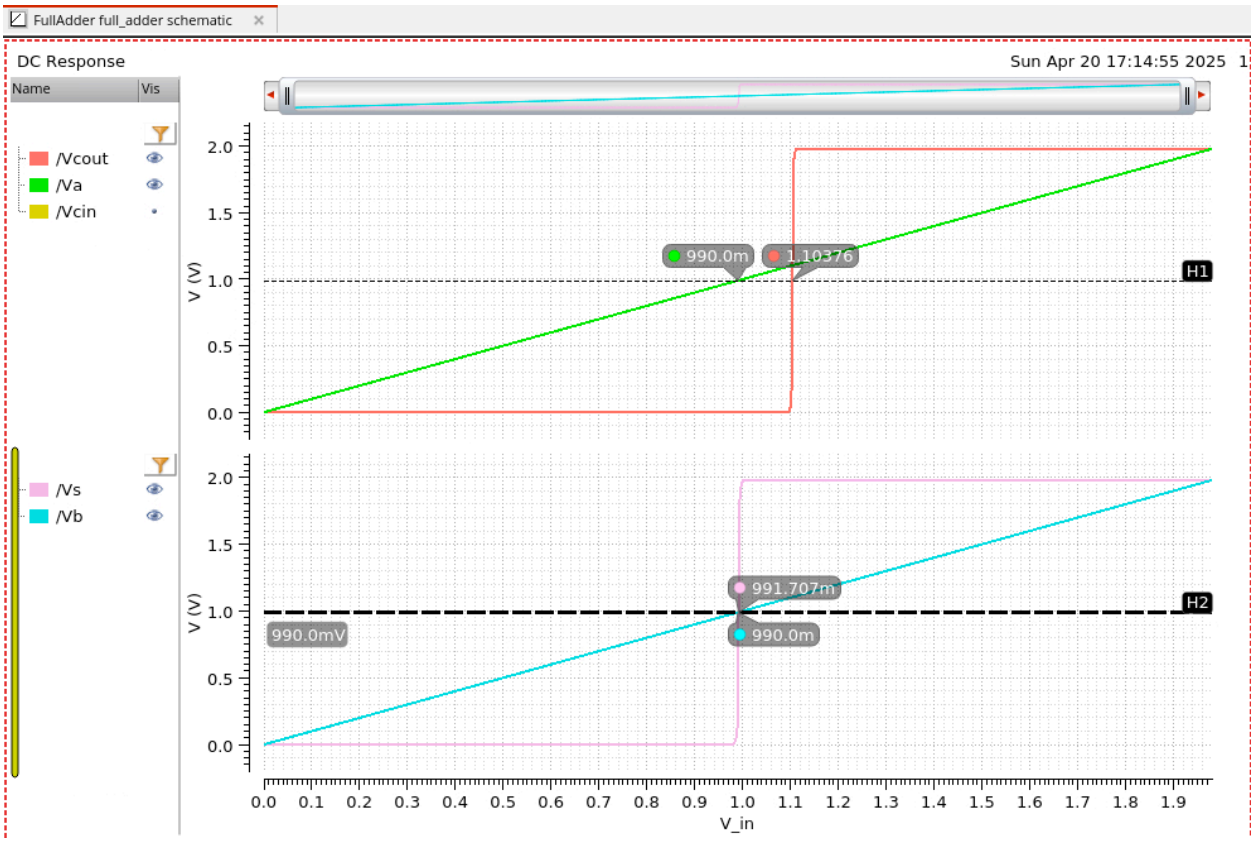
Schematic

My full adder schematic which uses only xor and nand gates is provided below. I used my designs from lab 2 in place of the nand and xor gates.



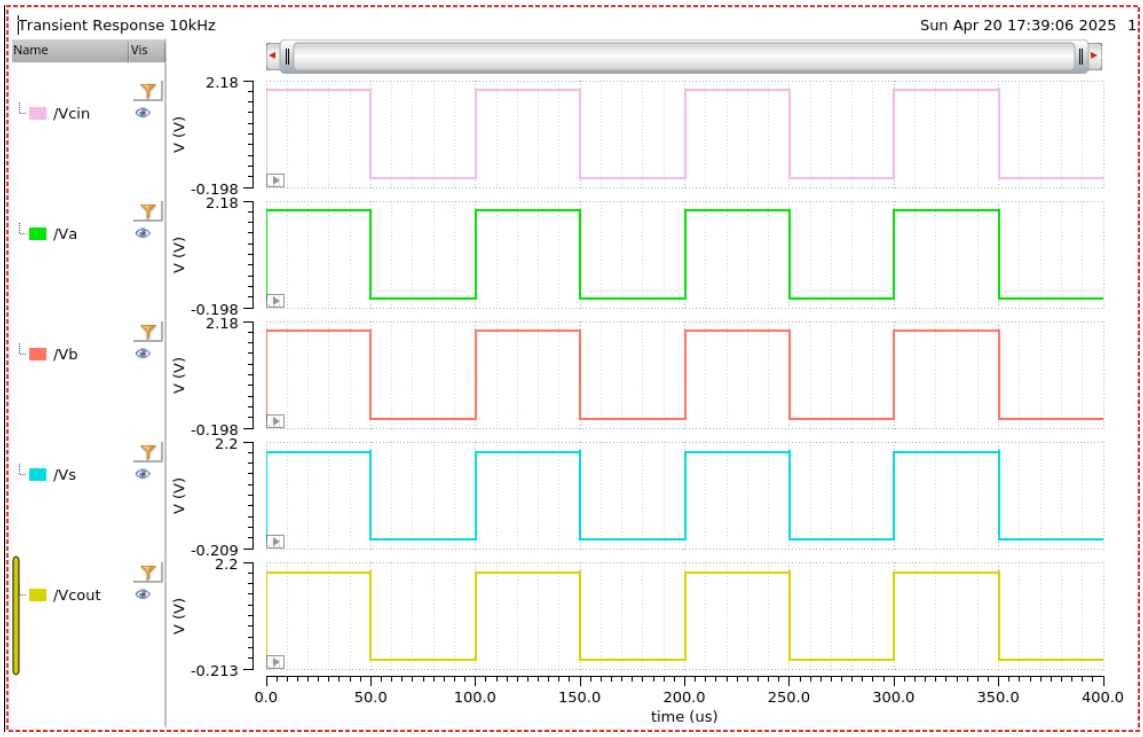
Simulation Results

VTC - DC Simulation

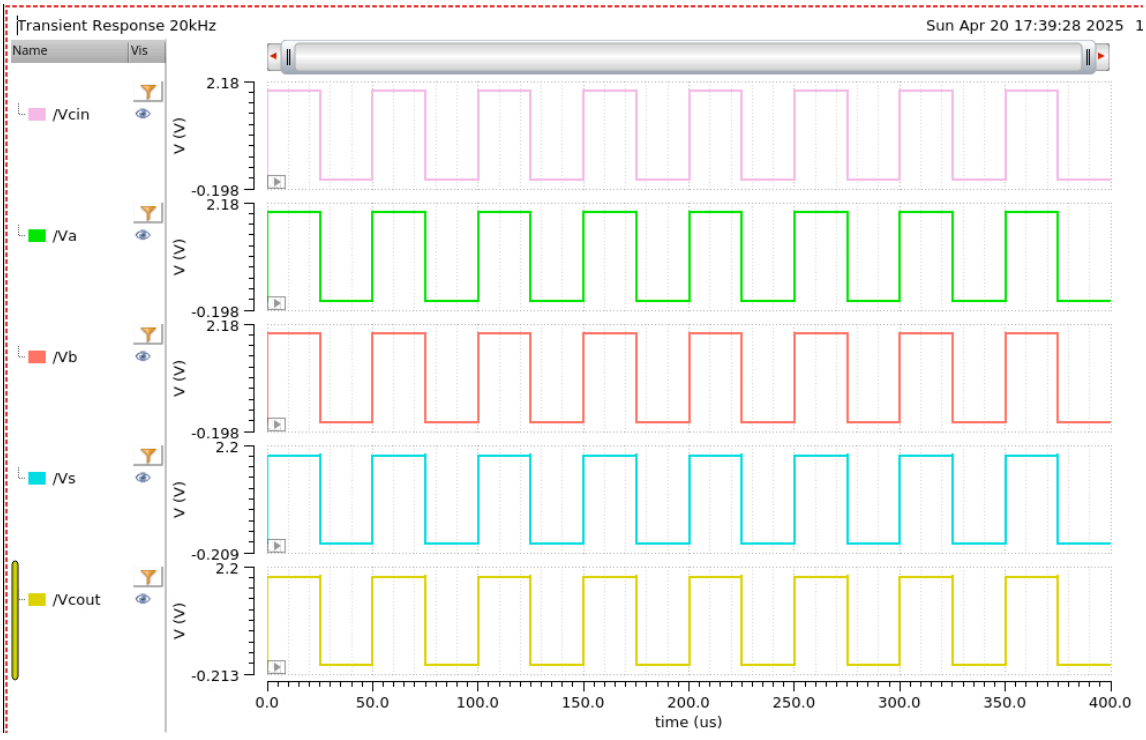


The VTC curves for the full adder are provided above. The threshold point of V_s is almost perfect (error by 1mV which is negligible) while the threshold point of V_{cout} shows much more deviation from the halfway point (990mV) with 1.10V V_{th}.

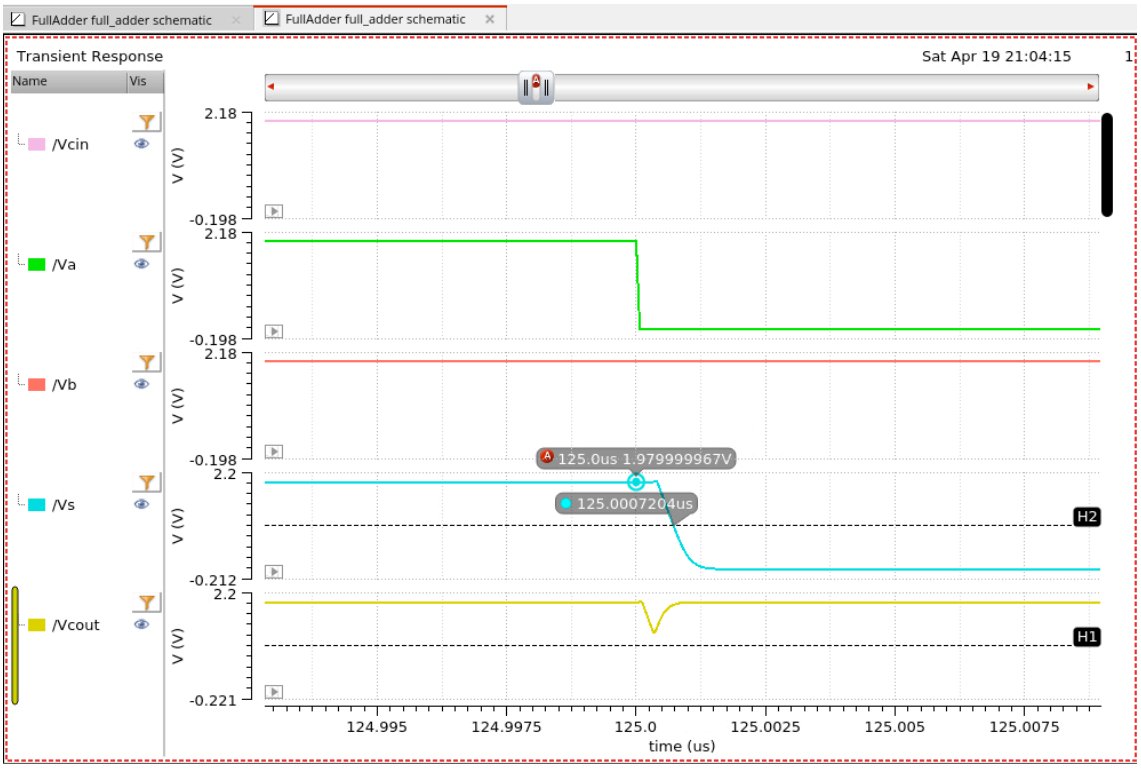
Propagation Delays - Transient Simulation



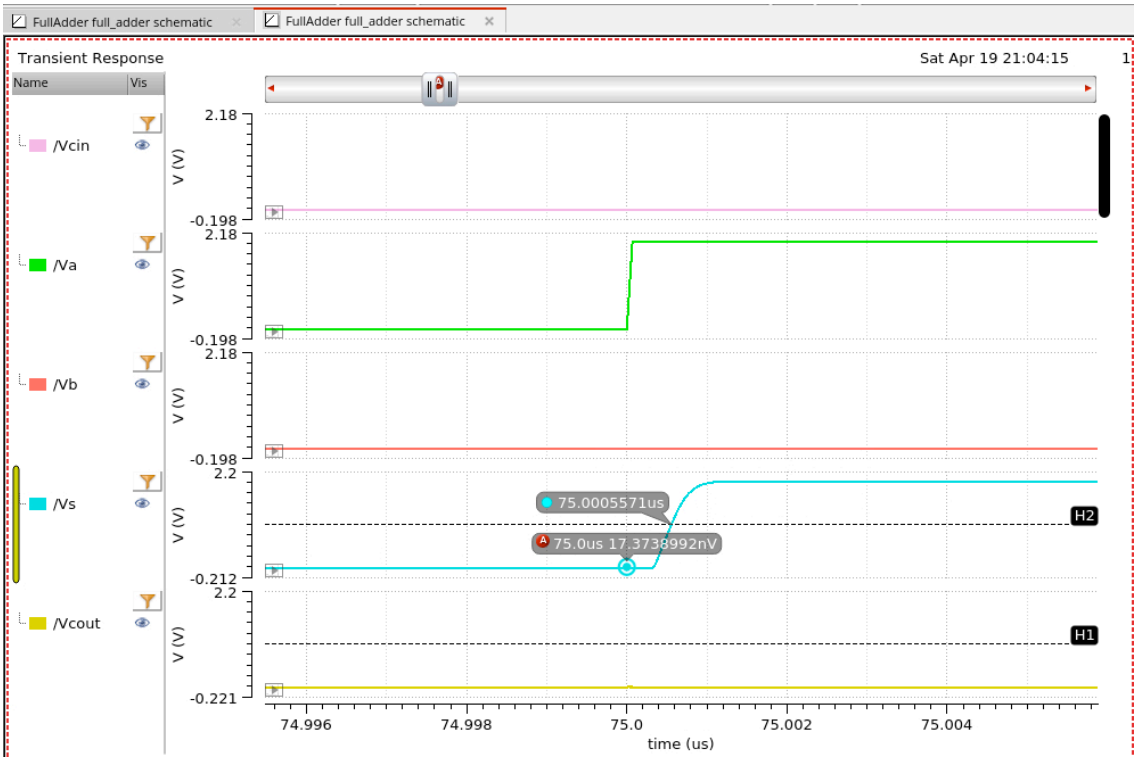
Transient response for input signals at 10kHz



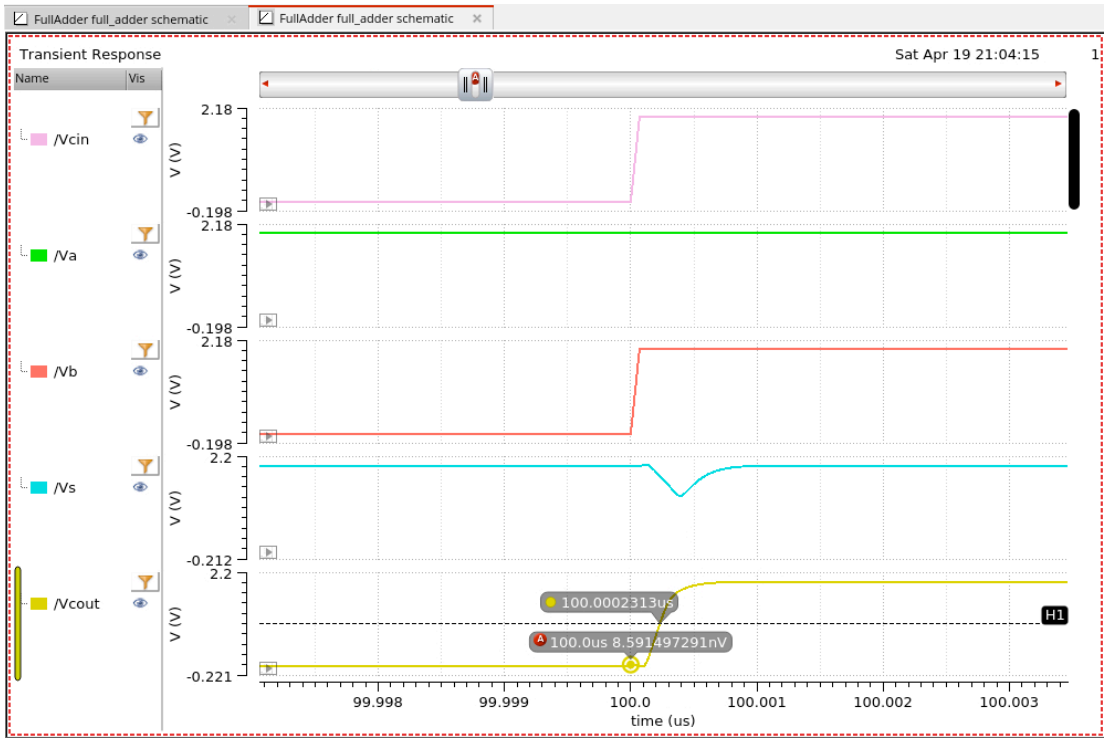
Transient response for input signals at 20kHz



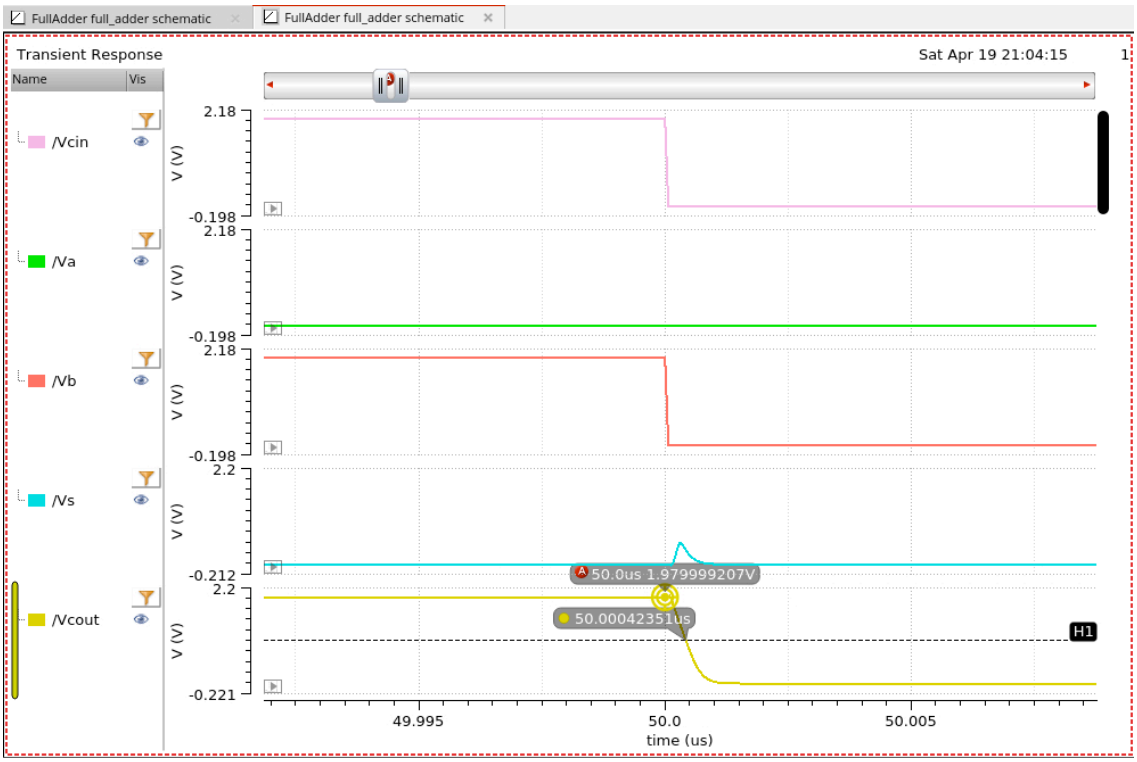
Propagation delay in this set of changing and stable input values: 720ps which exceeds the design constraint



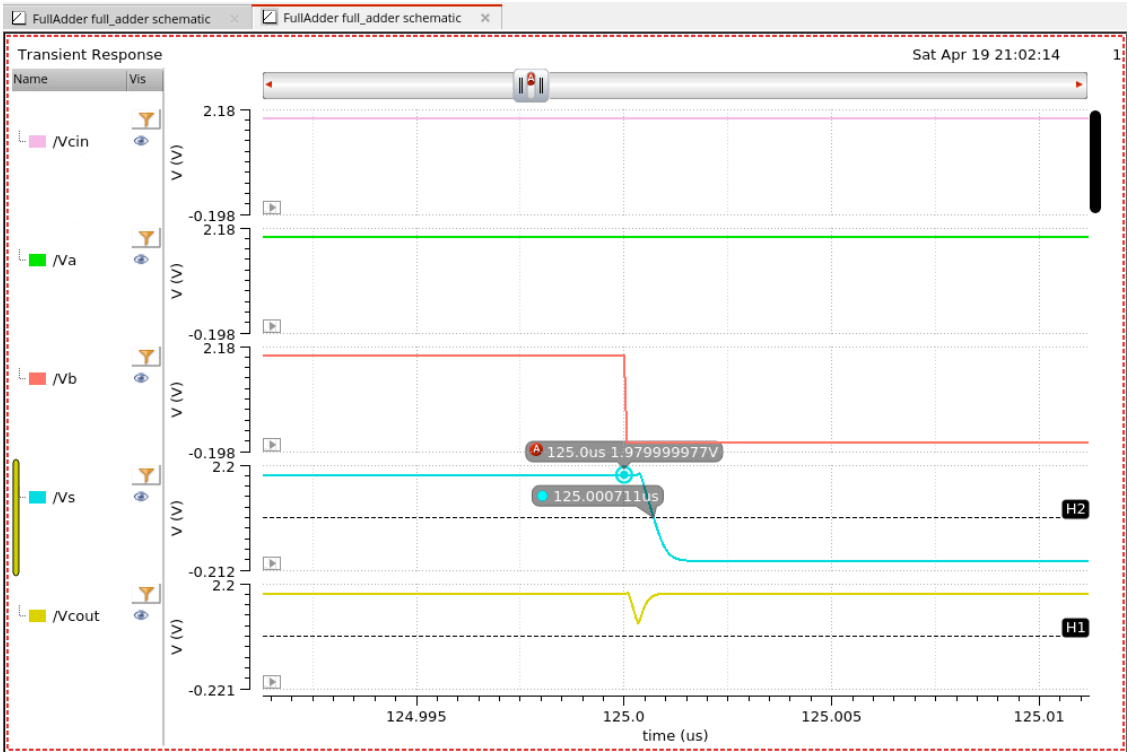
Propagation delay in this set of changing and stable input values: 557ps which exceeds the design constraint by a small margin



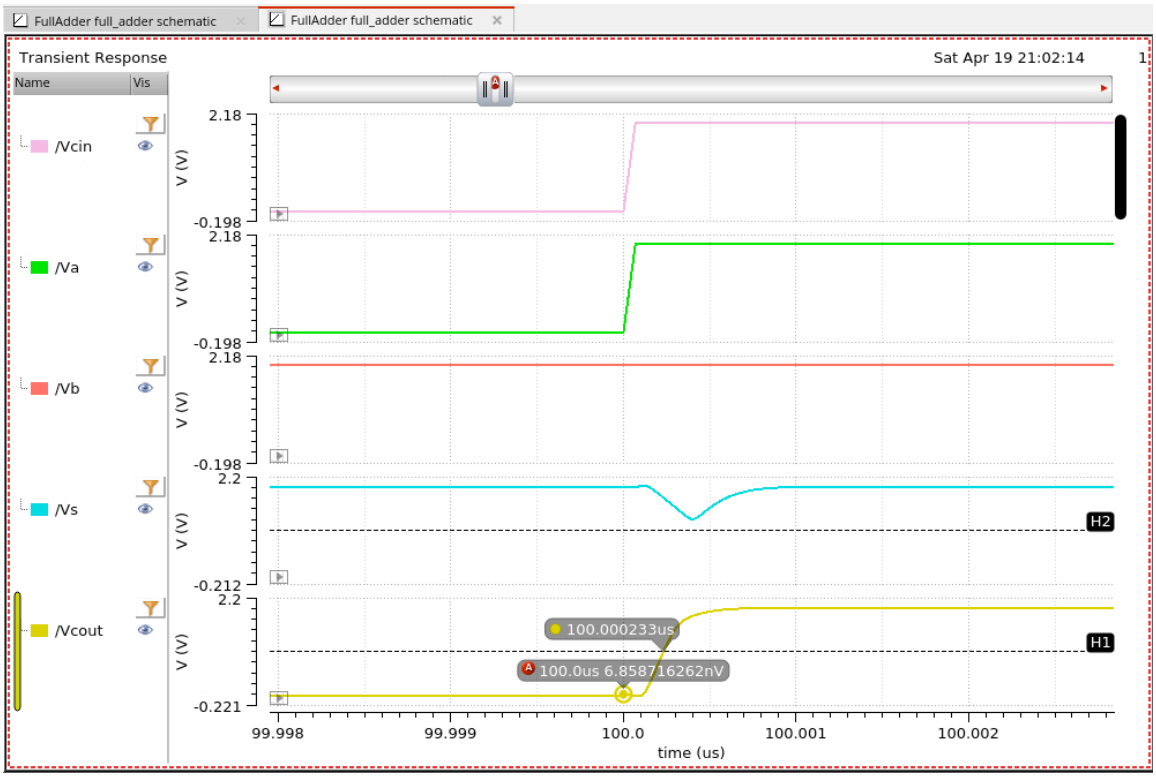
Propagation delay in this set of changing and stable input values: 231ps which meets the design constraints



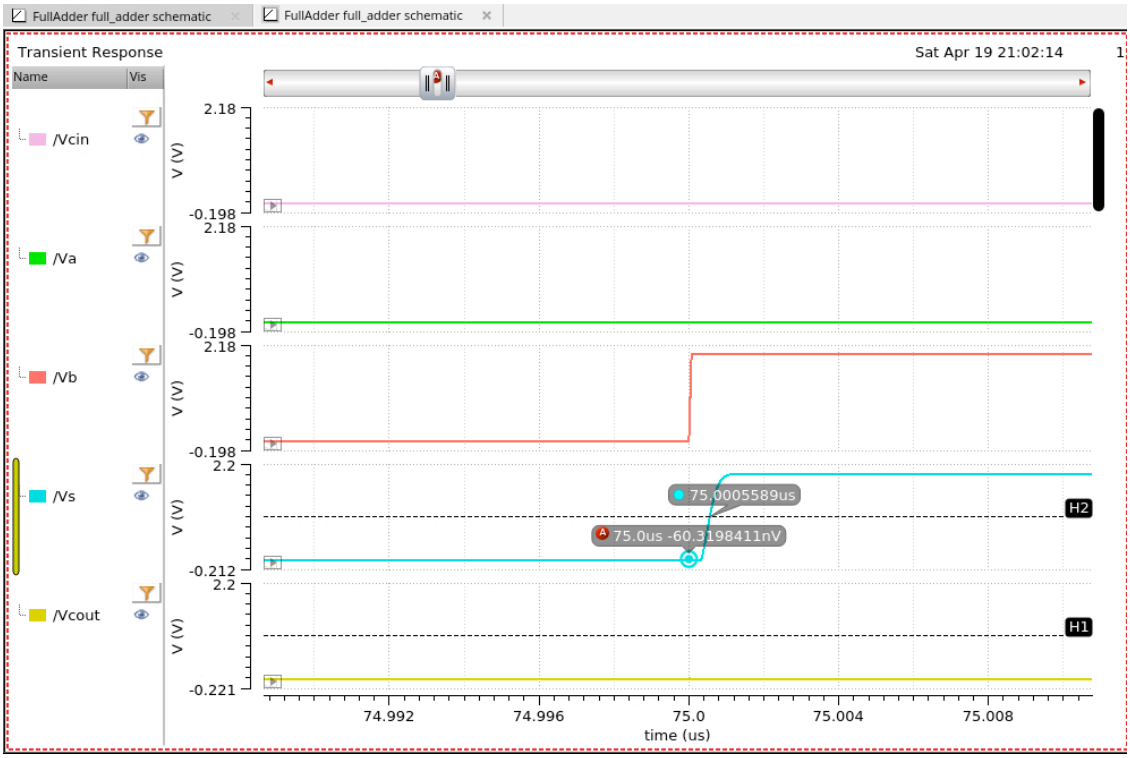
Propagation delay in this set of changing and stable input values: 424ps which meets the design constaints



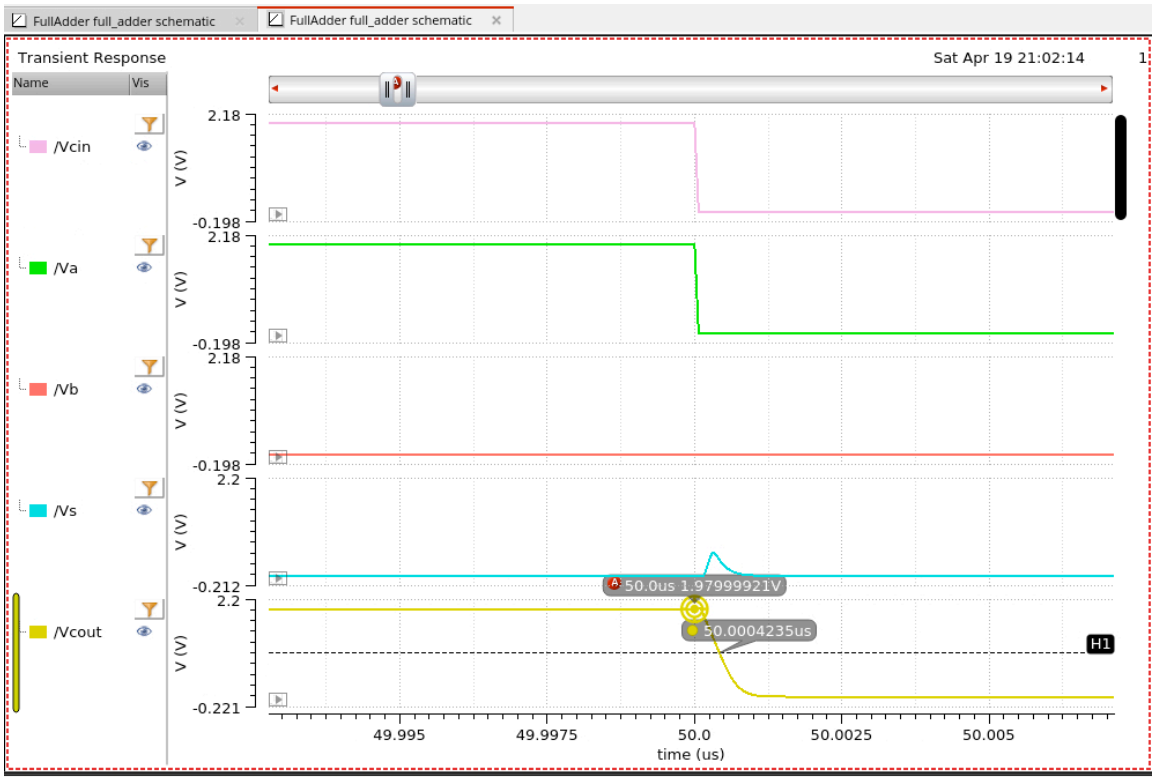
Propagation delay in this set of changing and stable input values: 711ps which exceeds the design constraint



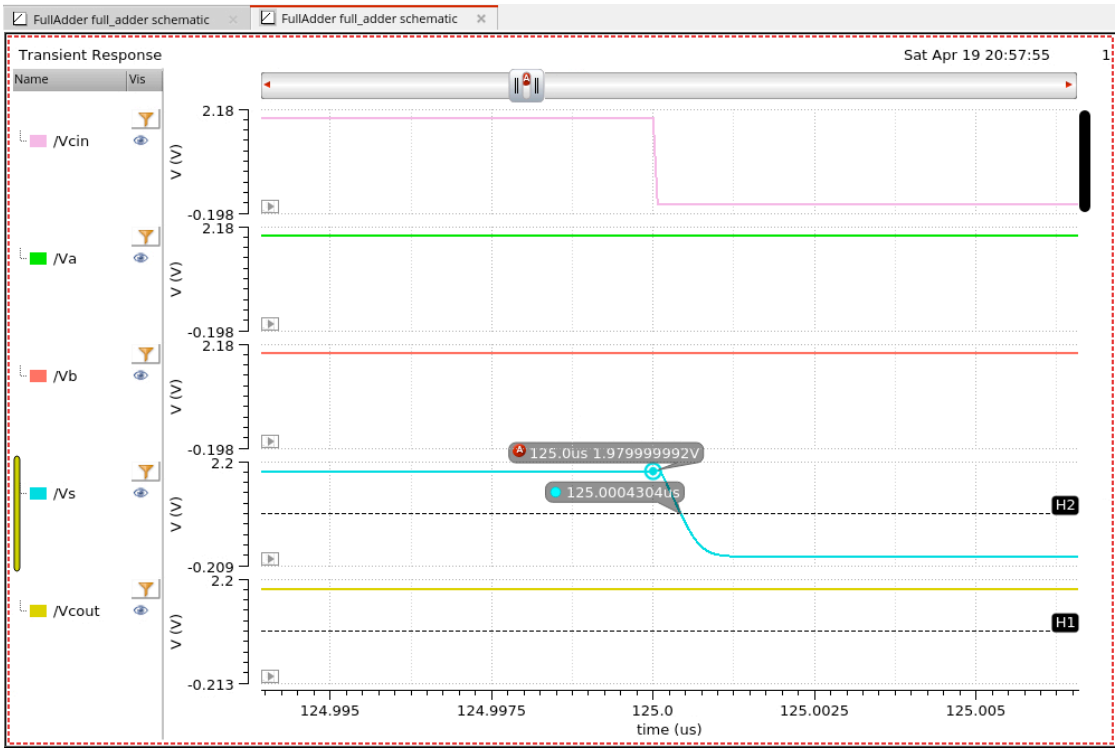
Propagation delay in this set of changing and stable input values: 233ps which meets the design constraints



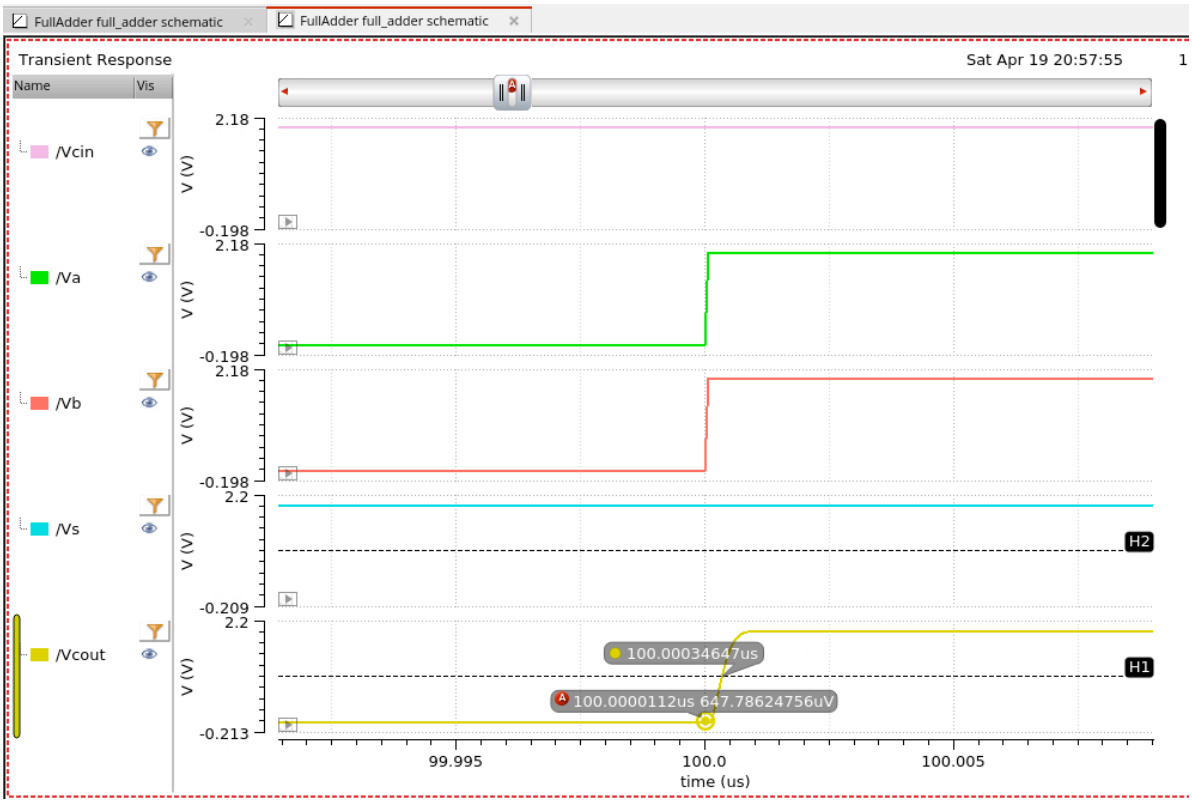
Propagation delay in this set of changing and stable input values: 559ps which exceeds the design constraint by a small margin



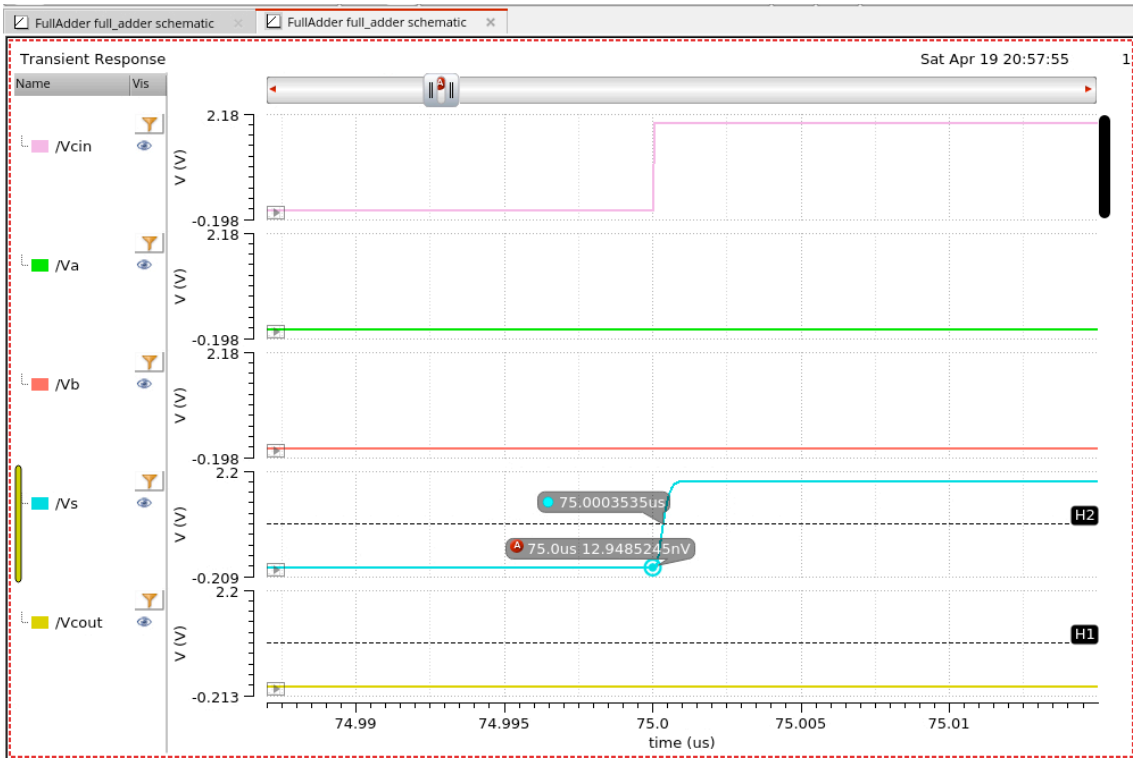
Propagation delay in this set of changing and stable input values: 424ps which meets the design constraint



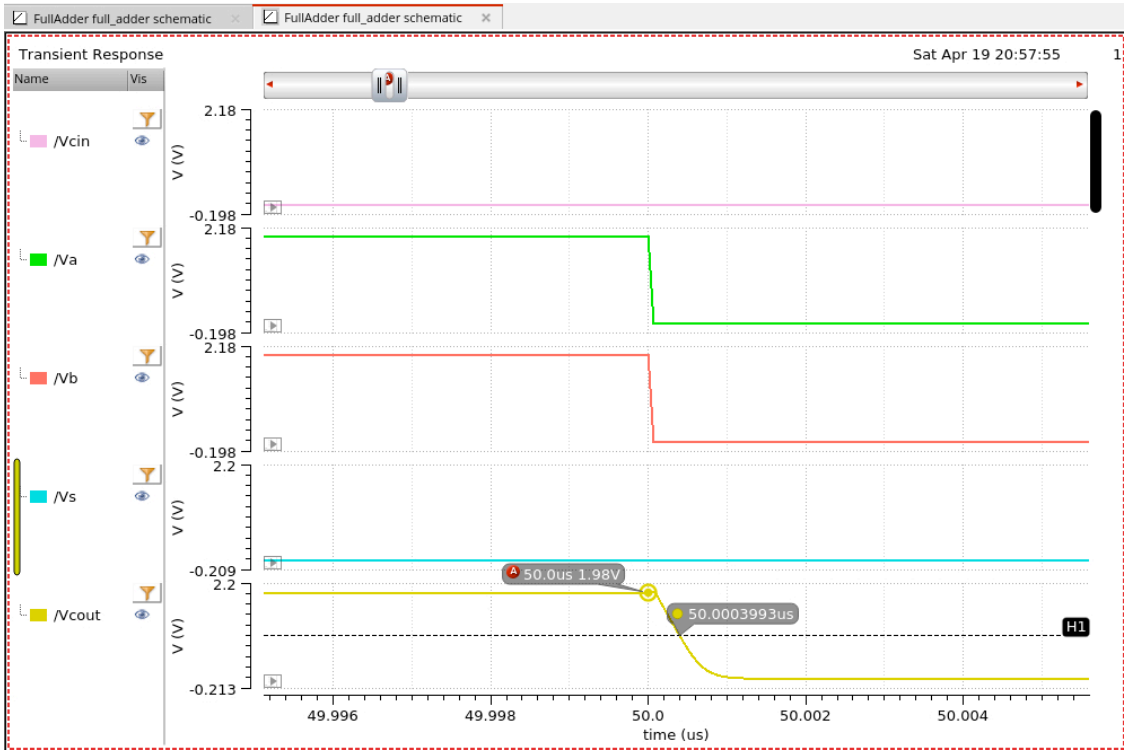
Propagation delay in this set of changing and stable input values: 430ps which meets the design constraint



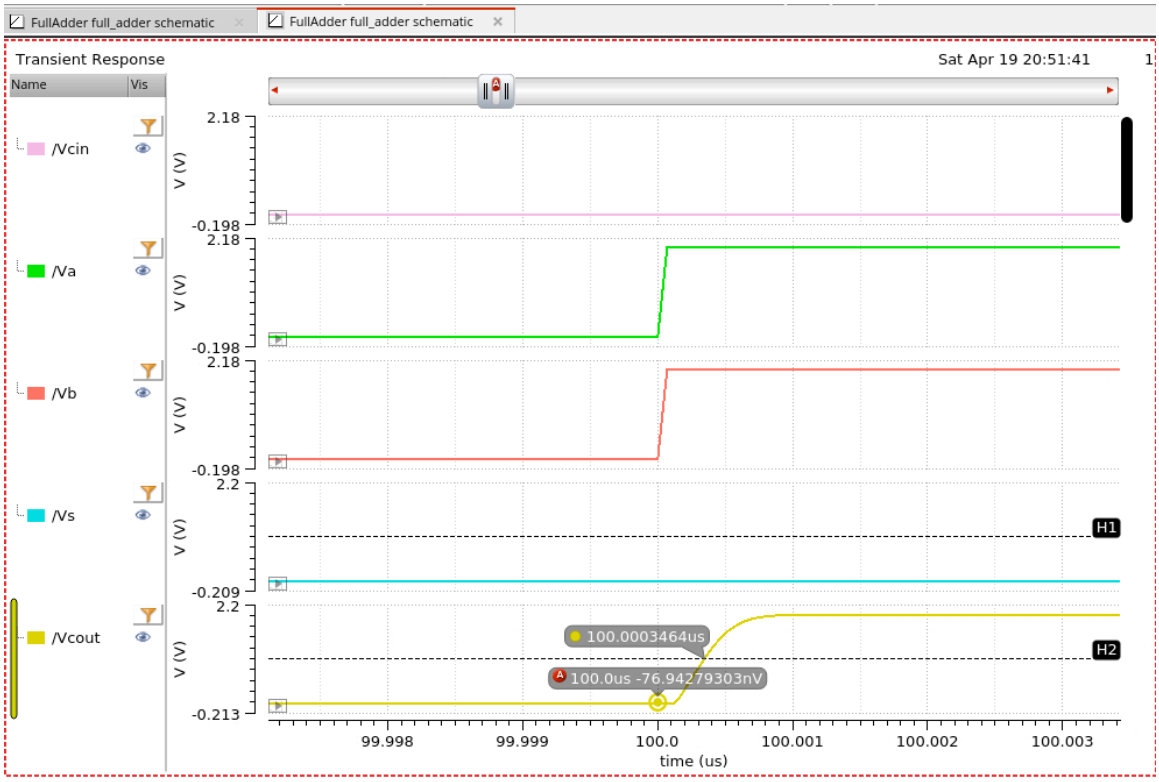
Propagation delay in this set of changing and stable input values: 346ps which meets the design constraint



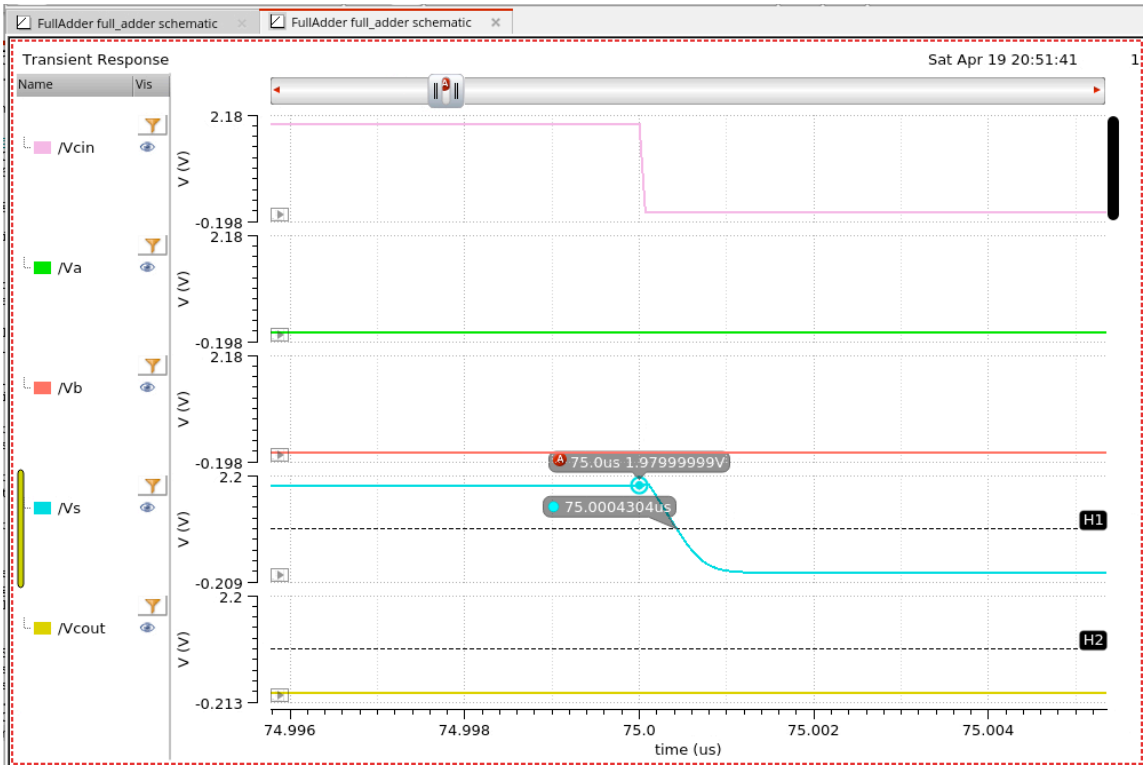
Propagation delay in this set of changing and stable input values: 354ps which meets the design constraint



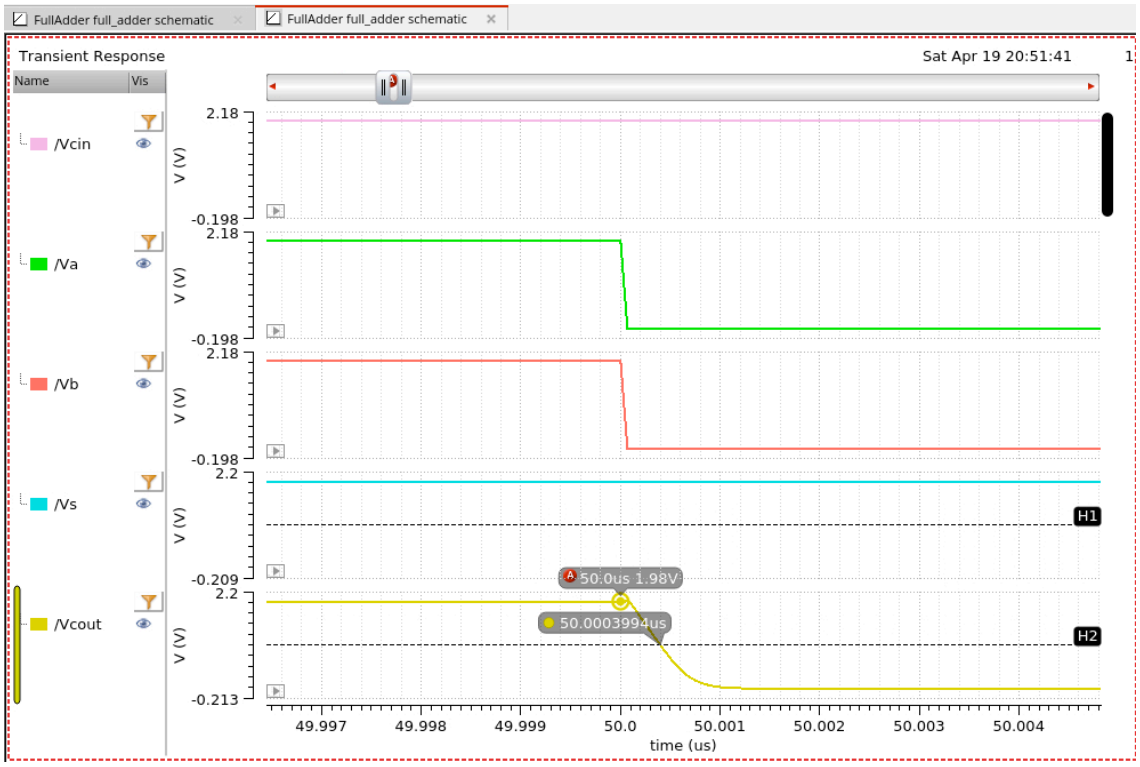
Propagation delay in this set of changing and stable input values: 399ps which meets the design constraint



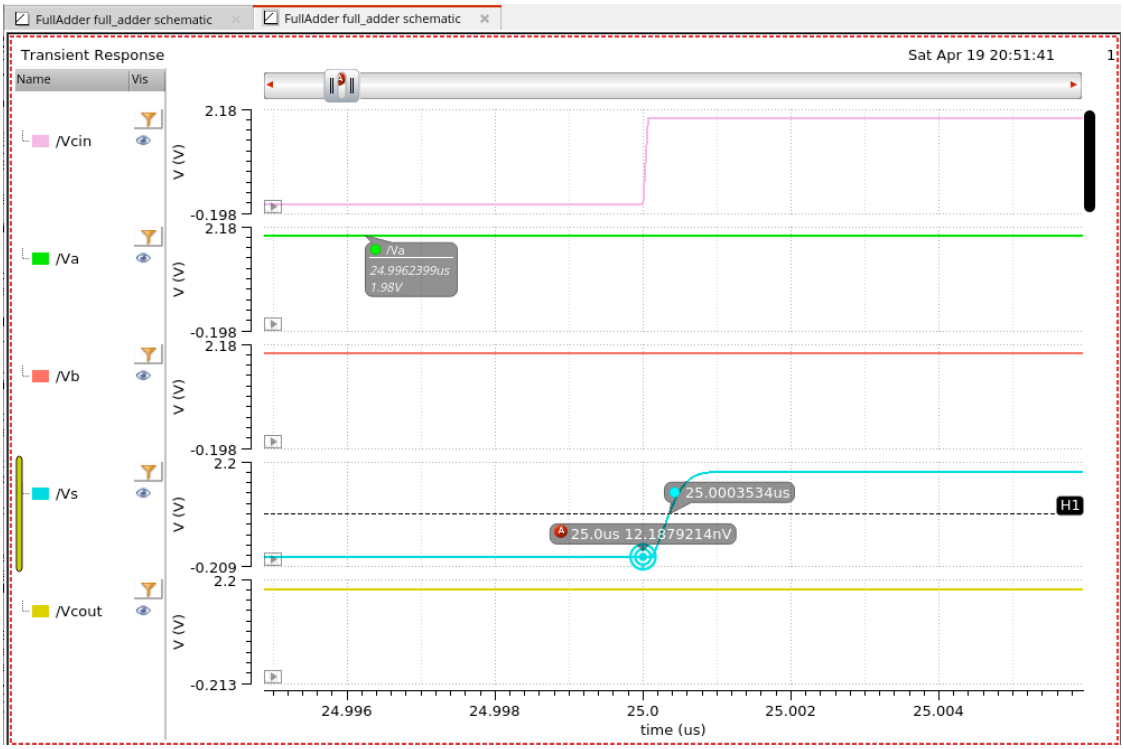
Propagation delay in this set of changing and stable input values: 346ps which meets the design constraint



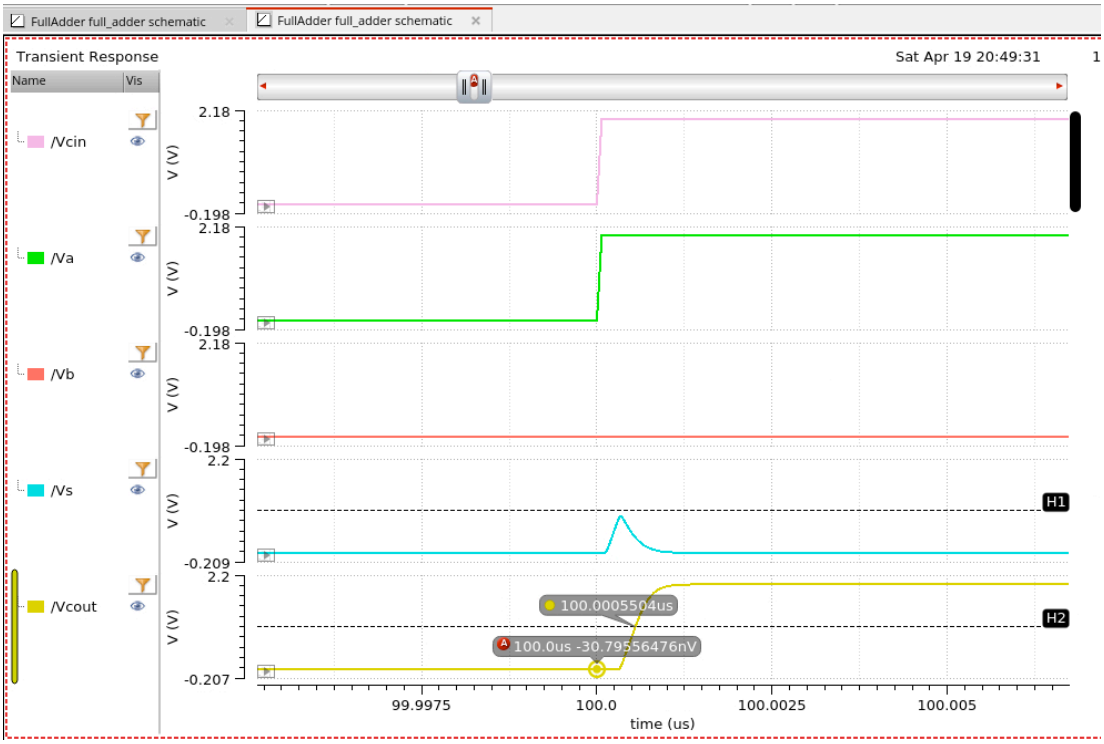
Propagation delay in this set of changing and stable input values: 430ps which meets the design constraint



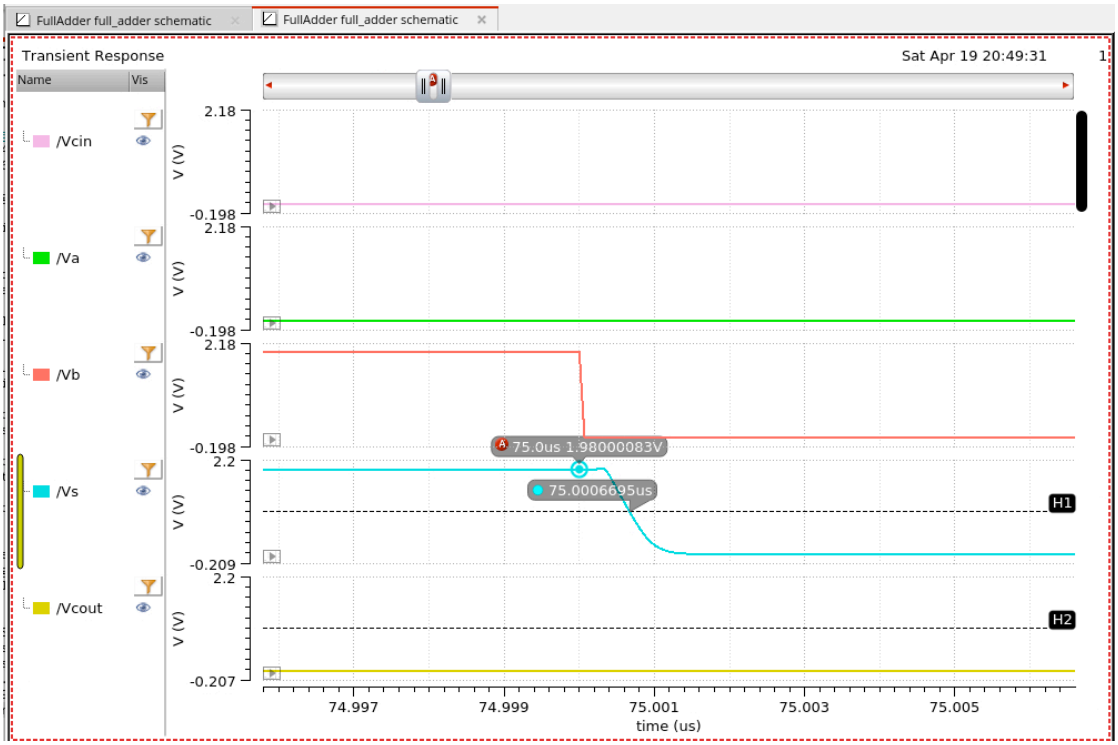
Propagation delay in this set of changing and stable input values: 399ps which meets the design constraint



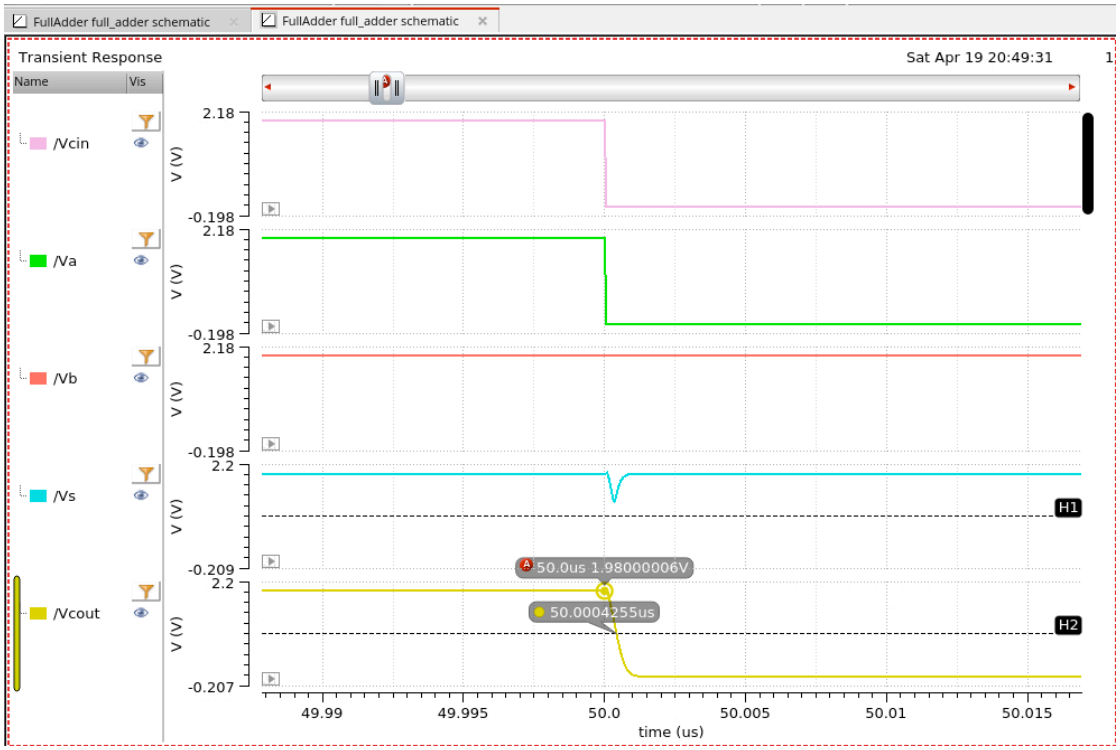
Propagation delay in this set of changing and stable input values: 353ps which meets the design constraint



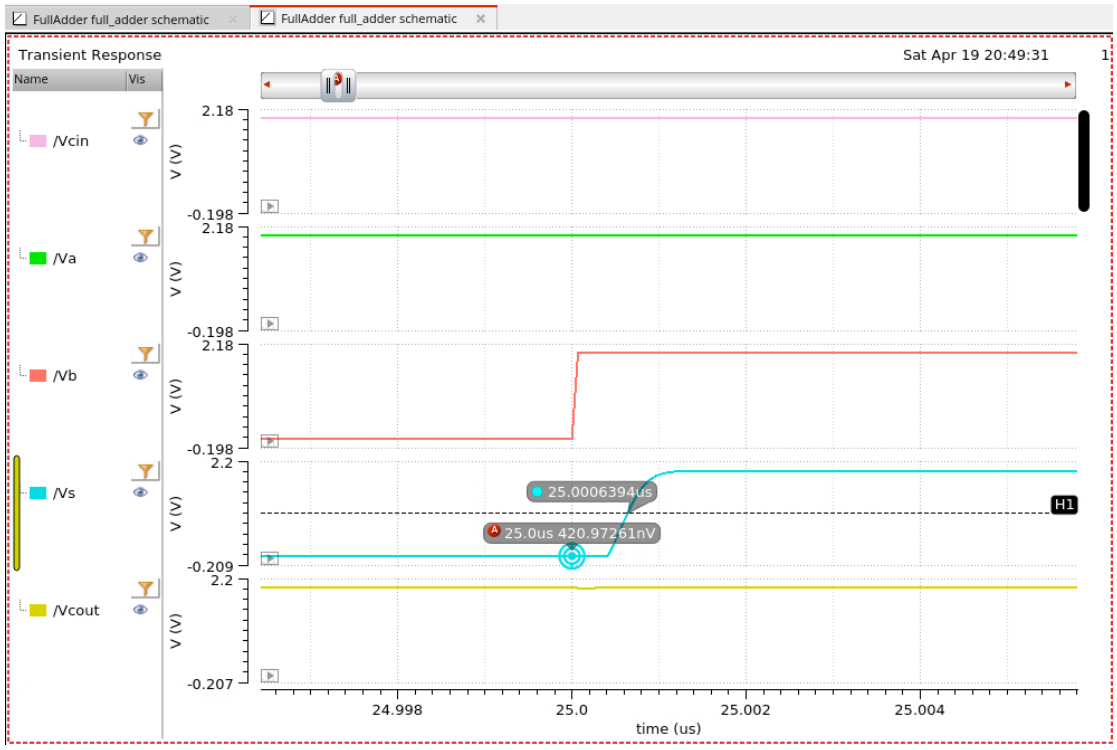
Propagation delay in this set of changing and stable input values: 550ps which exceeds the design constraint by a small margin



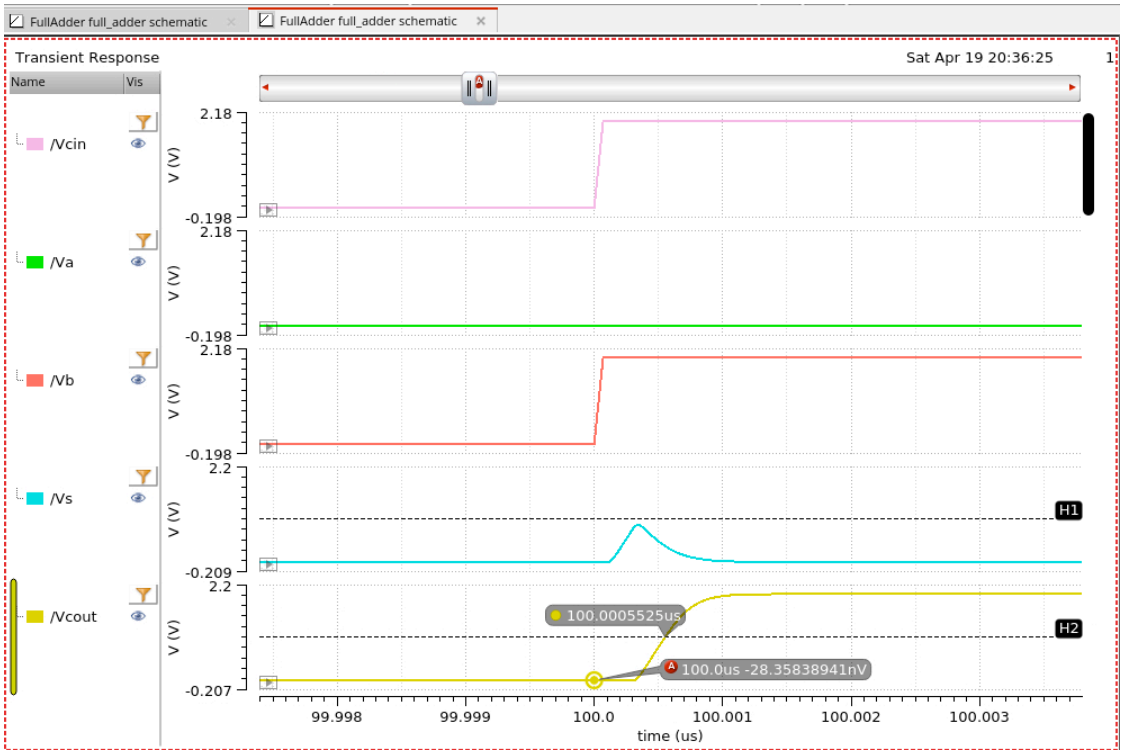
Propagation delay in this set of changing and stable input values: 670ps which exceeds the design constraints



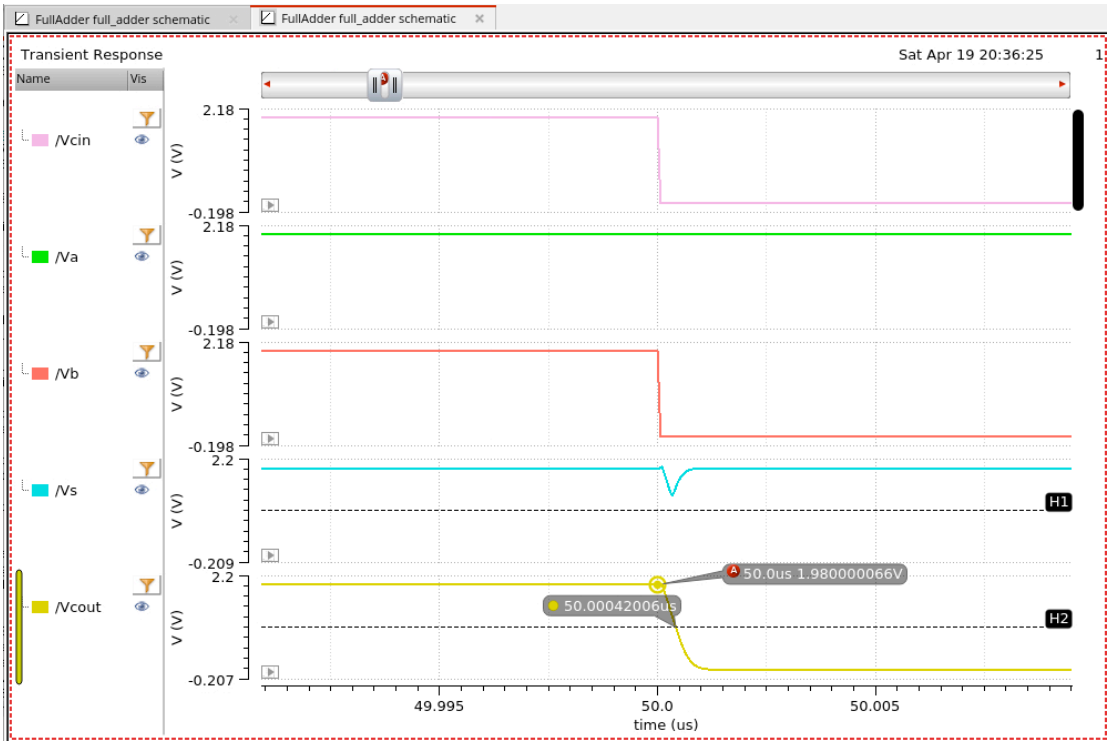
Propagation delay in this set of changing and stable input values: 426ps which meets the design constraint



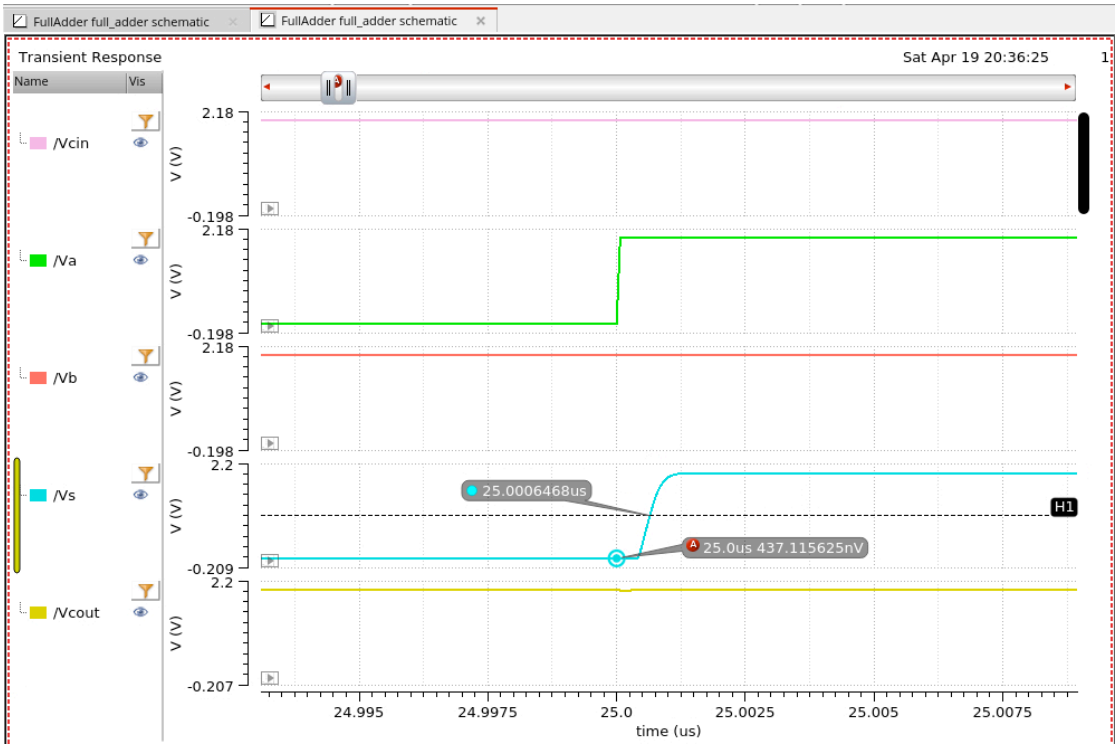
Propagation delay in this set of changing and stable input values: 640ps which exceeds the design constraints



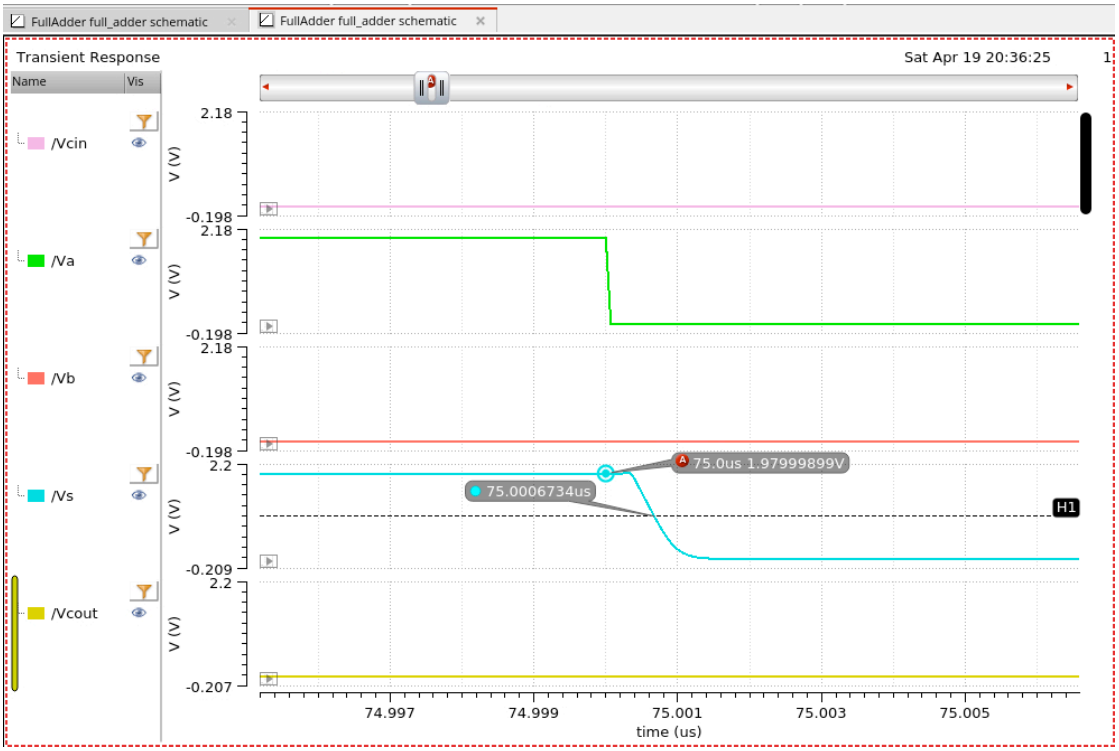
Propagation delay in this set of changing and stable input values: 553ps which exceeds the design constraints by a small margin



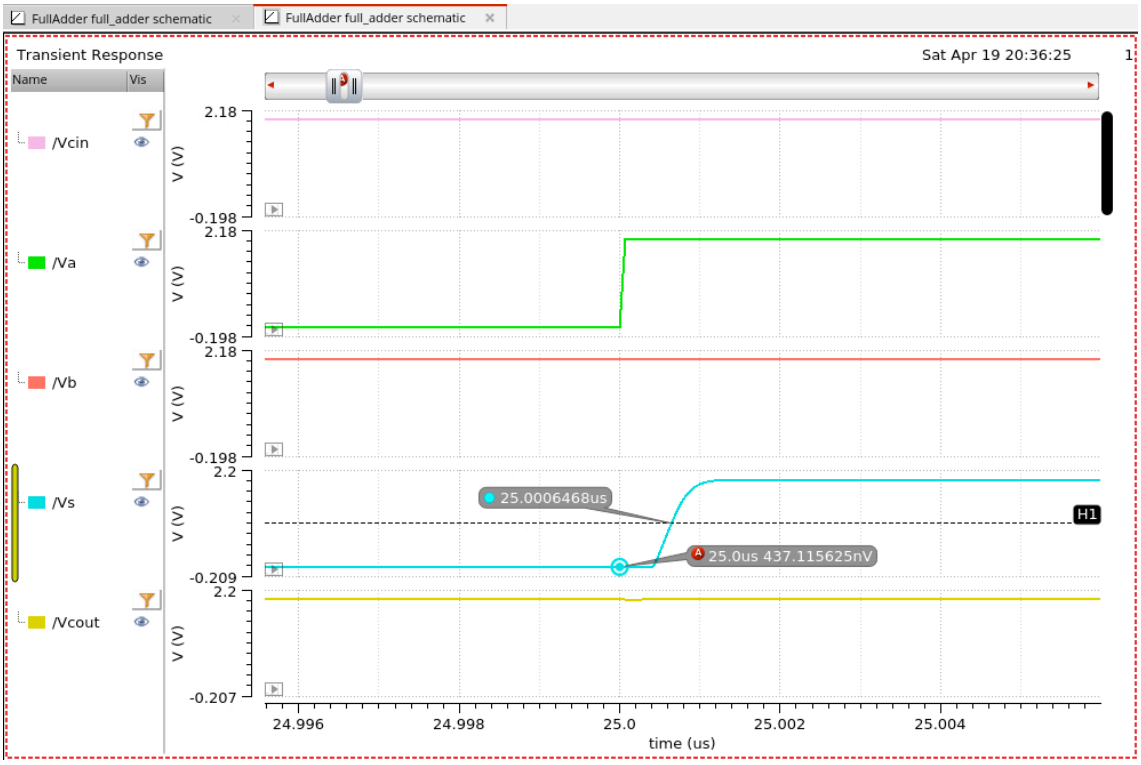
Propagation delay in this set of changing and stable input values: 420ps which meets the design constraint



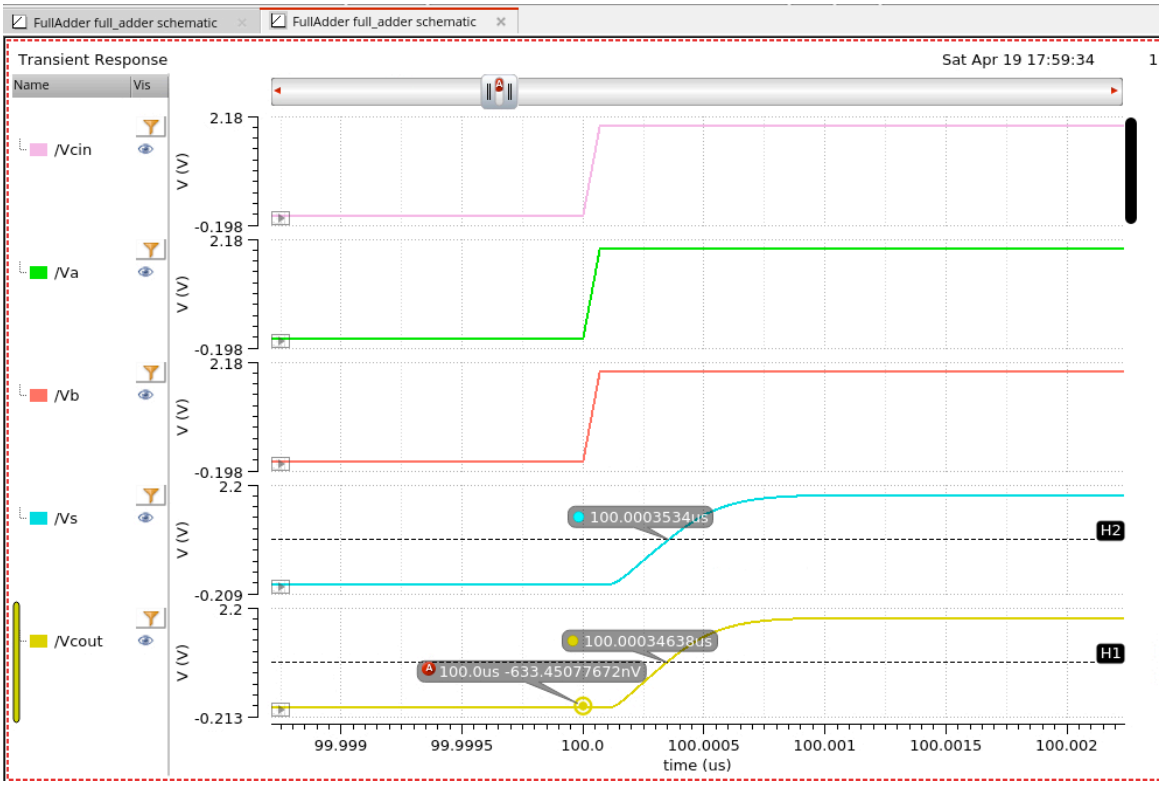
Propagation delay in this set of changing and stable input values: 647ps which exceeds the design constraints



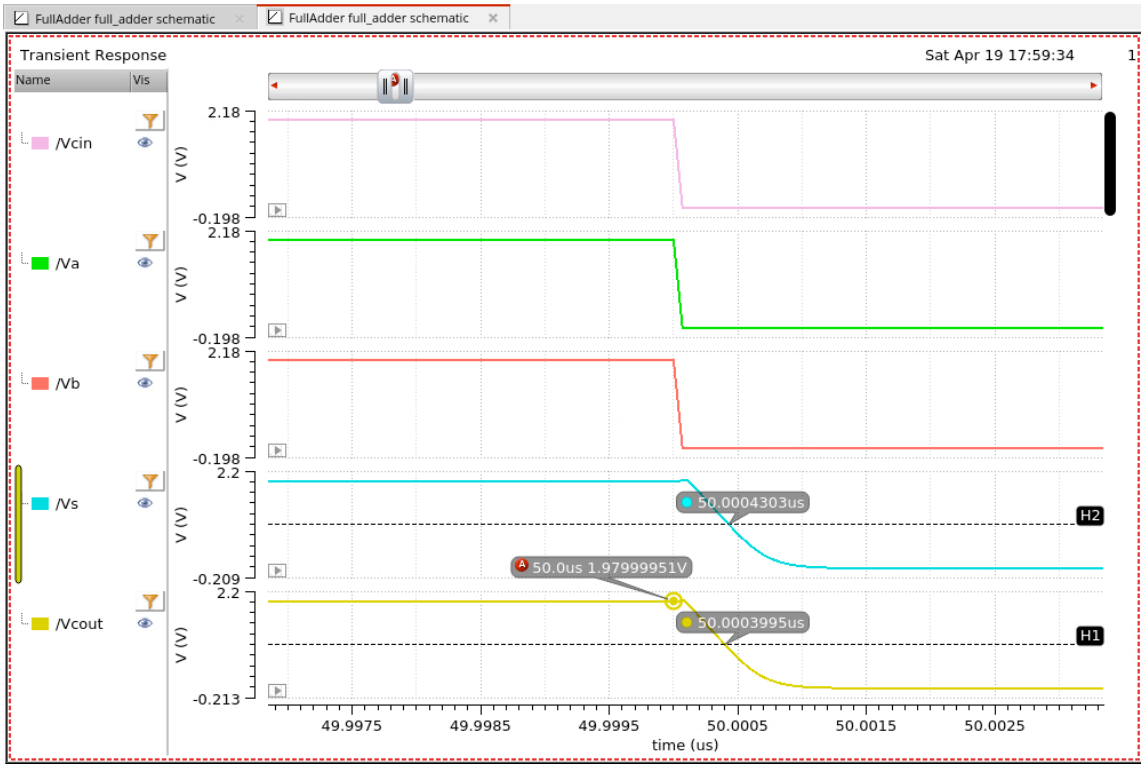
Propagation delay in this set of changing and stable input values: 673ps which exceeds the design constraints



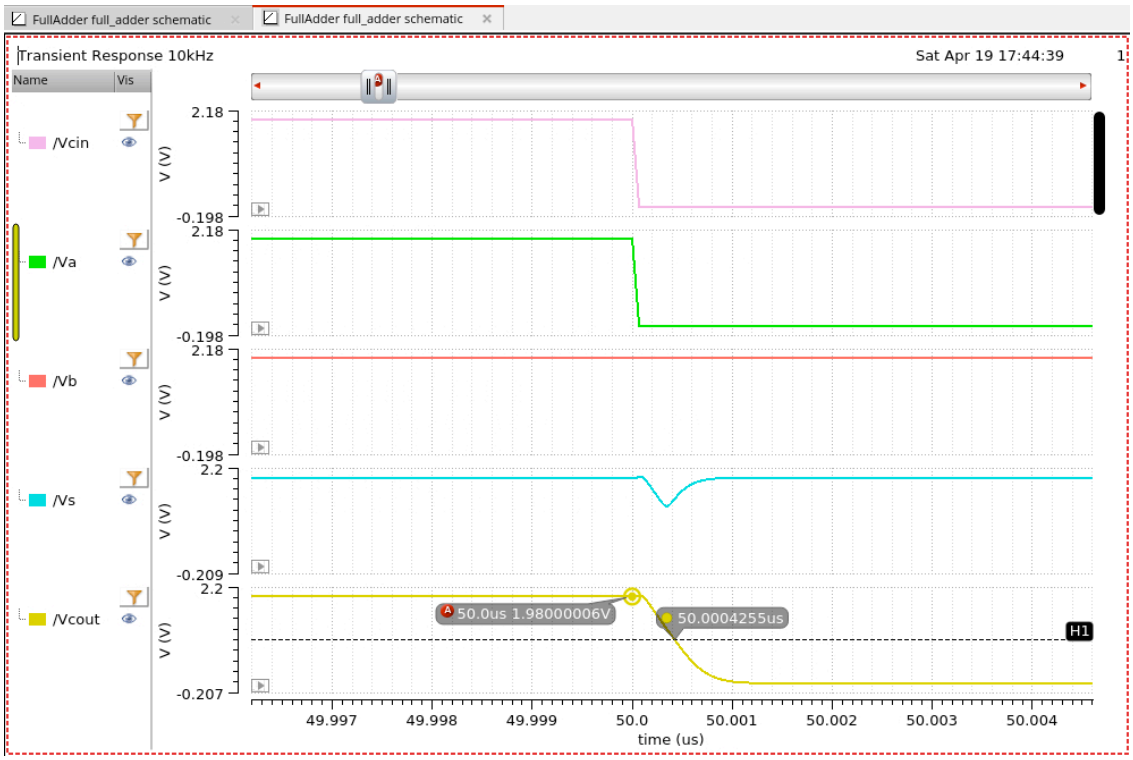
Propagation delay in this set of changing and stable input values: 647ps which exceeds the design constraints



Propagation delay for Vs: 353ps.
Propagation delay for Vcout: 346 ps.



Propagation delay for Vs: 430ps.
Propagation delay for Vcout: 400ps.



Propagation delay in this set of changing and stable input values: 423ps which meets the design constraints

Worst Case Propagation Delays

The worst case high to low propagation delay for Vs was found as 734ps. While the worst case low to high propagation delay was 646ps.

The worst case high to low propagation delay for Vcout was found as 426ps. While the worst case low to high propagation delay was 552ps.

We observed that the propagation delays for Vcout were generally lower than those of Vs. This is likely due to the fact that there is a smaller number of transistors between Vcout and the inputs. The critical path from the inputs to Vcout goes through the first xor gate, then two nand gates. Vs's critical path on the other hand goes through two xor gates.

Fluctuations in Output Signals - Explanation

Another important observation is the presence of small notches and surges in output signals. This is likely due to the difference between the propagation delays of the input signals' paths. As an example, Vcin is directly connected to the 2nd xor gate while Va and Vb go through the first xor gate. This means that the output signal will start changing according to the previous value of Va xor Vb and the new value of Vcin before the result of the first xor triggers a change in the output of the 2nd xor.

Truth Table

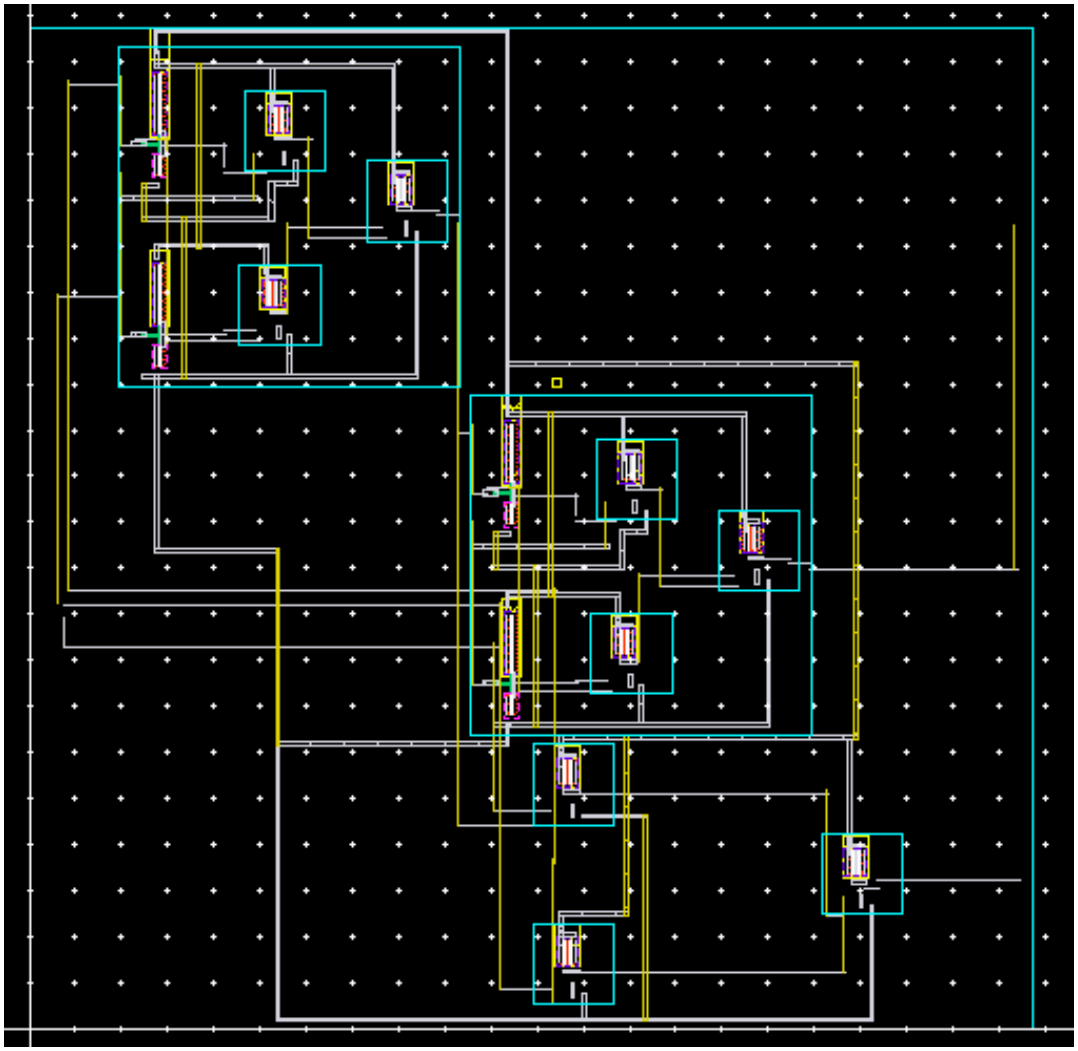
Based on the results of the transient simulation we can come up with the following truth table:

Va	Vb	Vcin	Vs	Vcout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

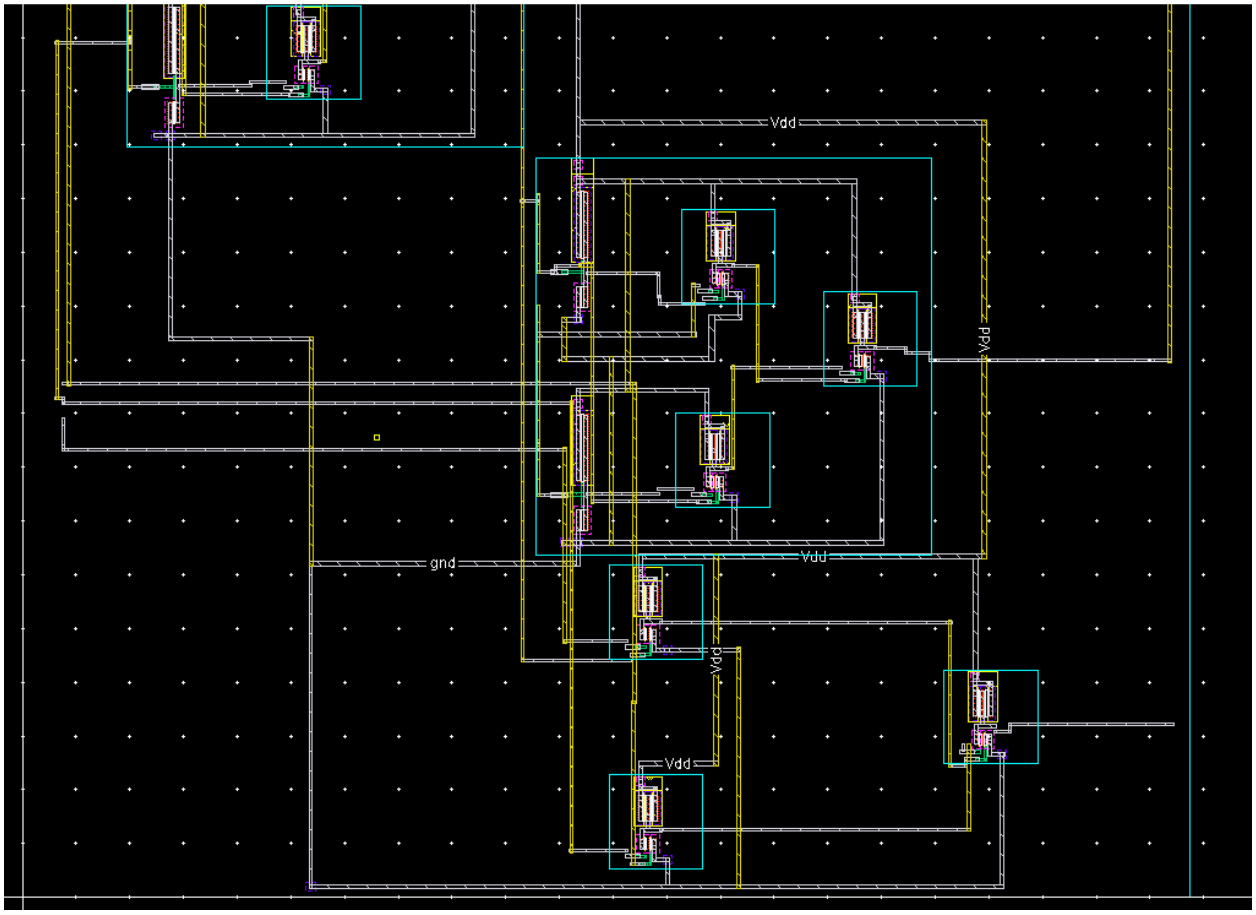
Please refer to the previous sections for signal outputs for various input values

Layout

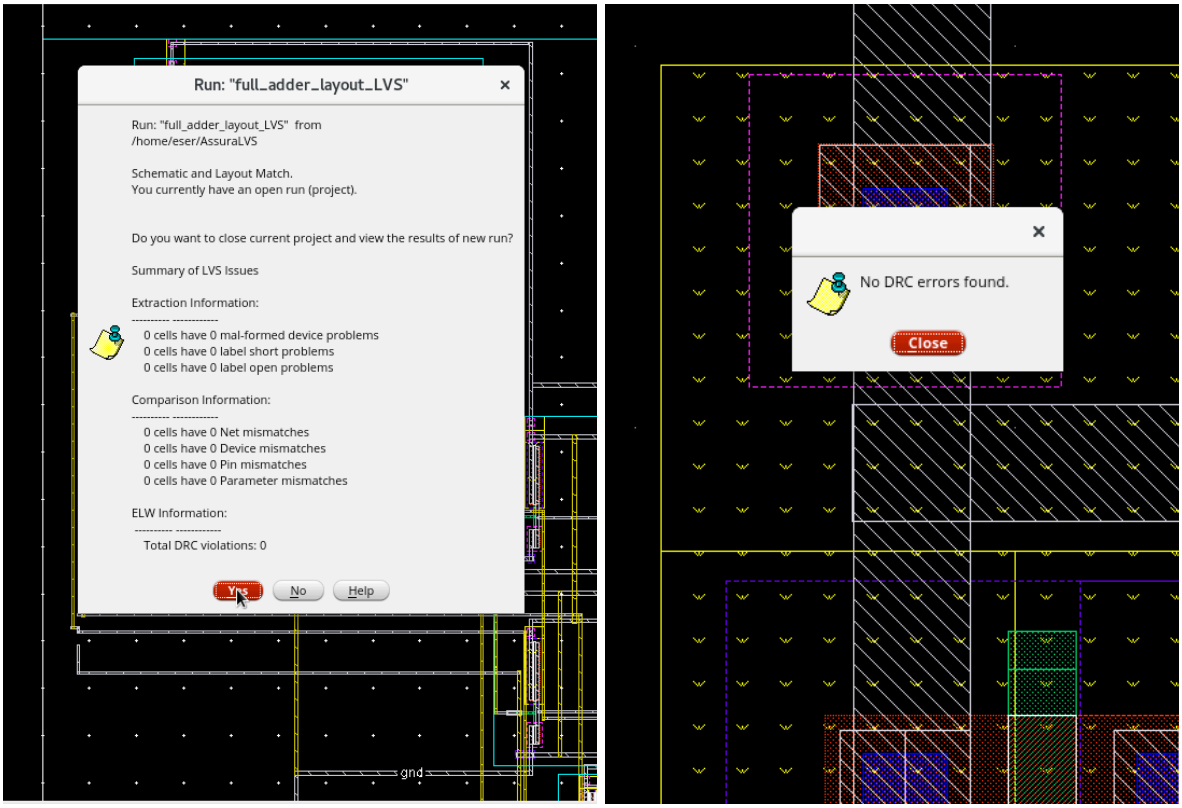
I chose to use my own layout cells from the previous lab instead of starting from scratch. You may find the layout screen accompanied by DRC and LVS pass screenshots below.



The overall layout of the full adder



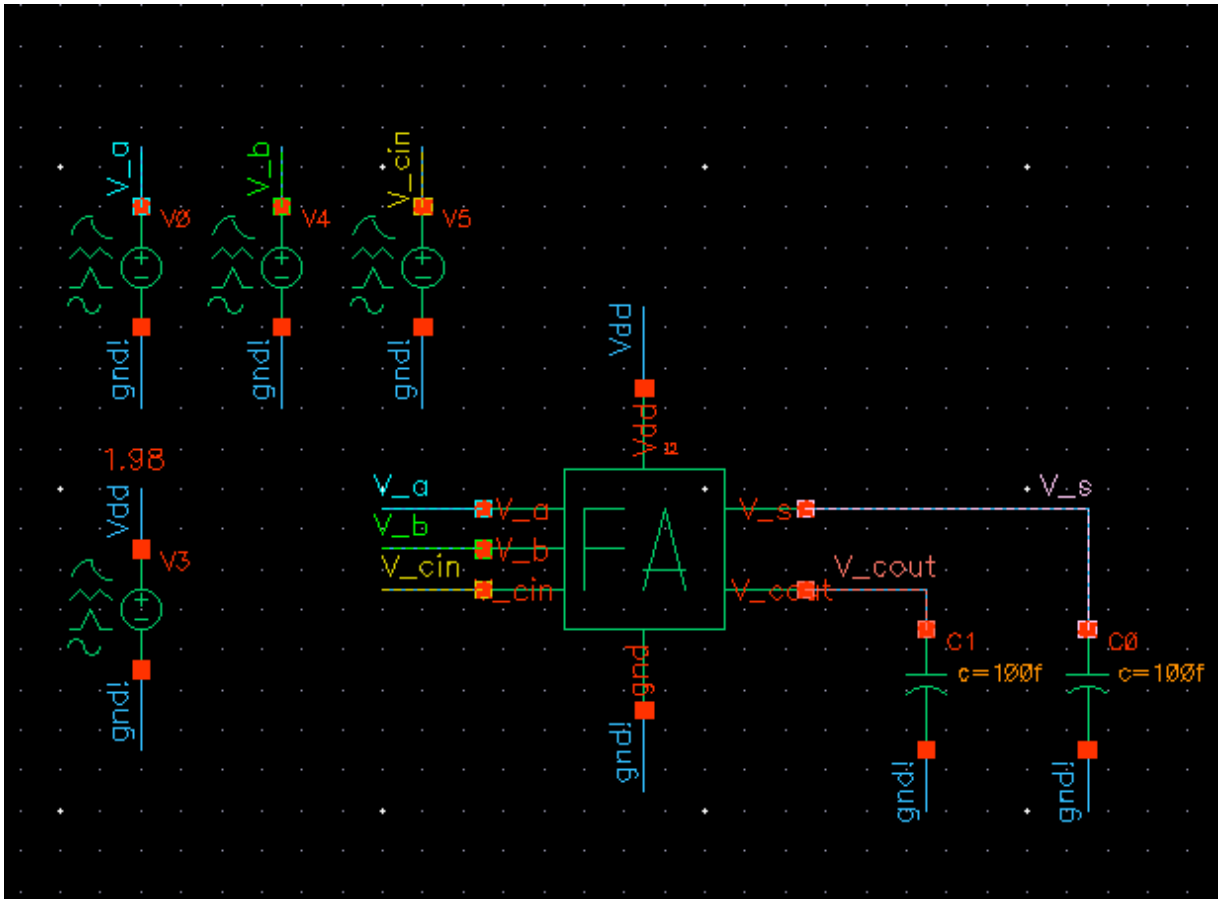
Full Adder layout focusing on the 2nd XOR gate and the NAND gates.



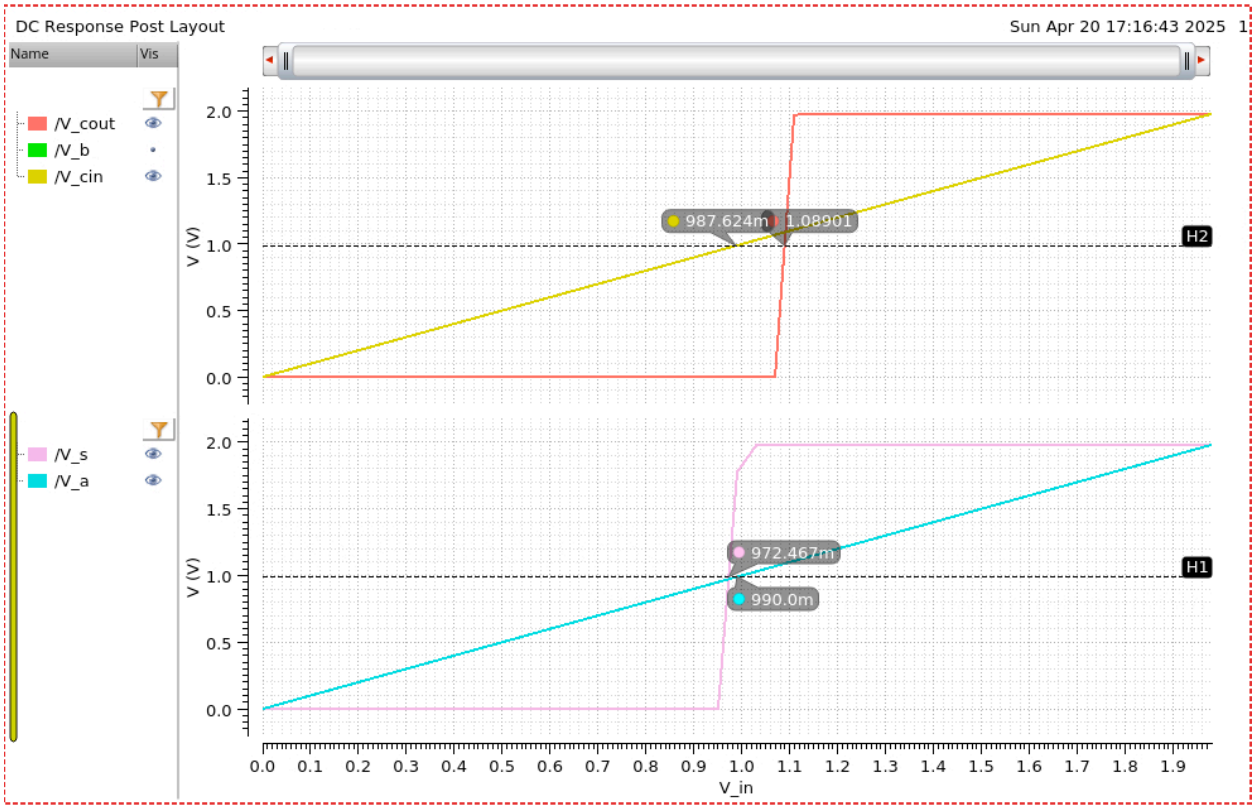
Layout check pass screens

Symbol and Post-layout Simulation

Provided below is the symbol I picked for the full adder as well as the post layout simulation setup.

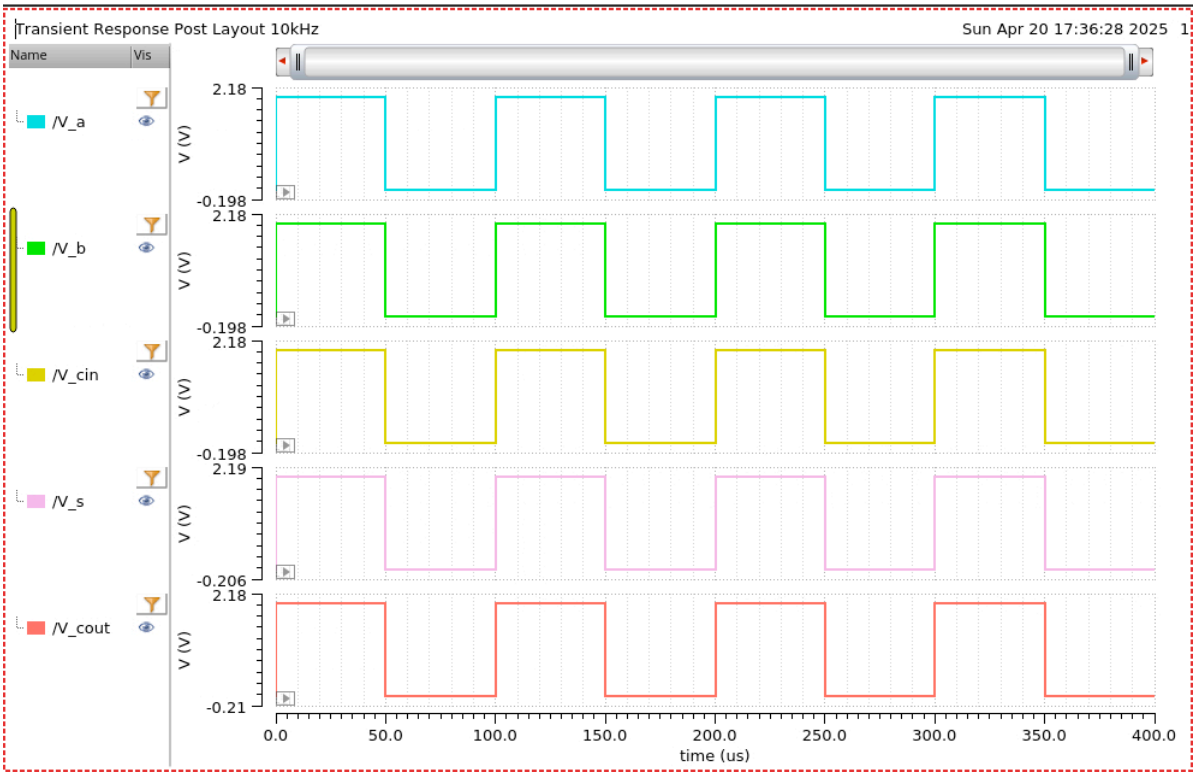


VTC - DC Simulation

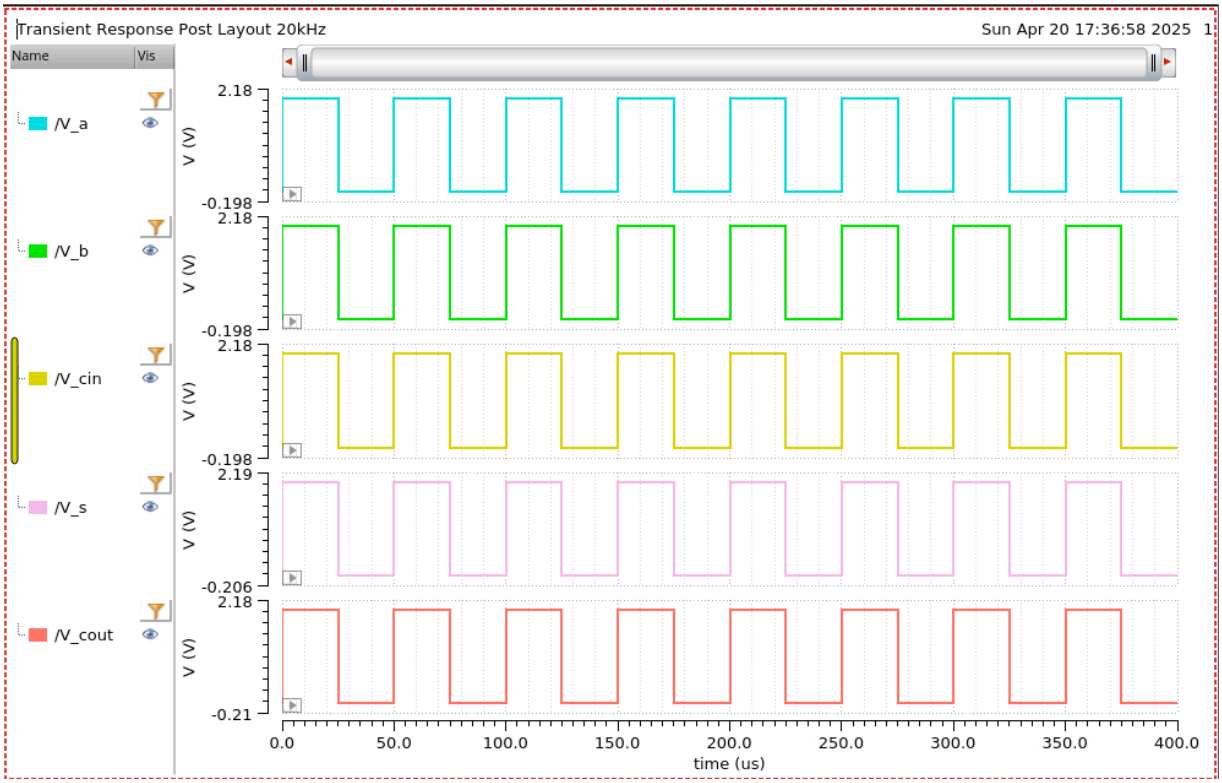


The VTC of V_{cout} improved with the layout by a small margin while the V_{th} of V_s dropped by 20mV post-layout.

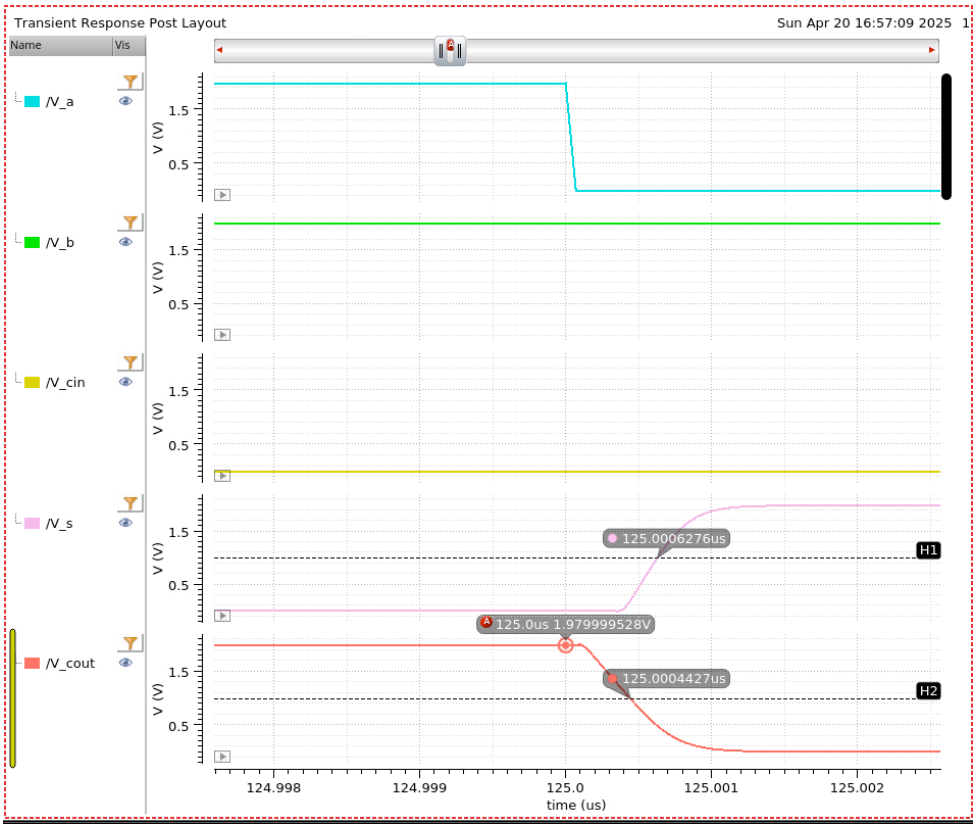
Propagation Delays - Transient Simulation



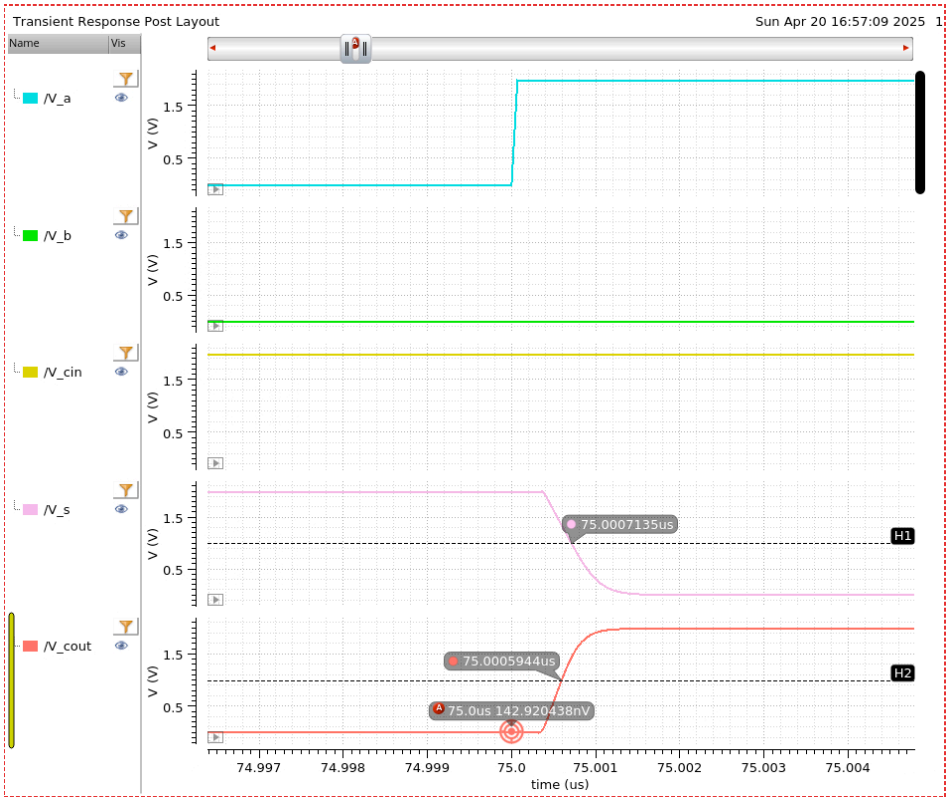
Post layout transient simulation with inputs at 10kHz



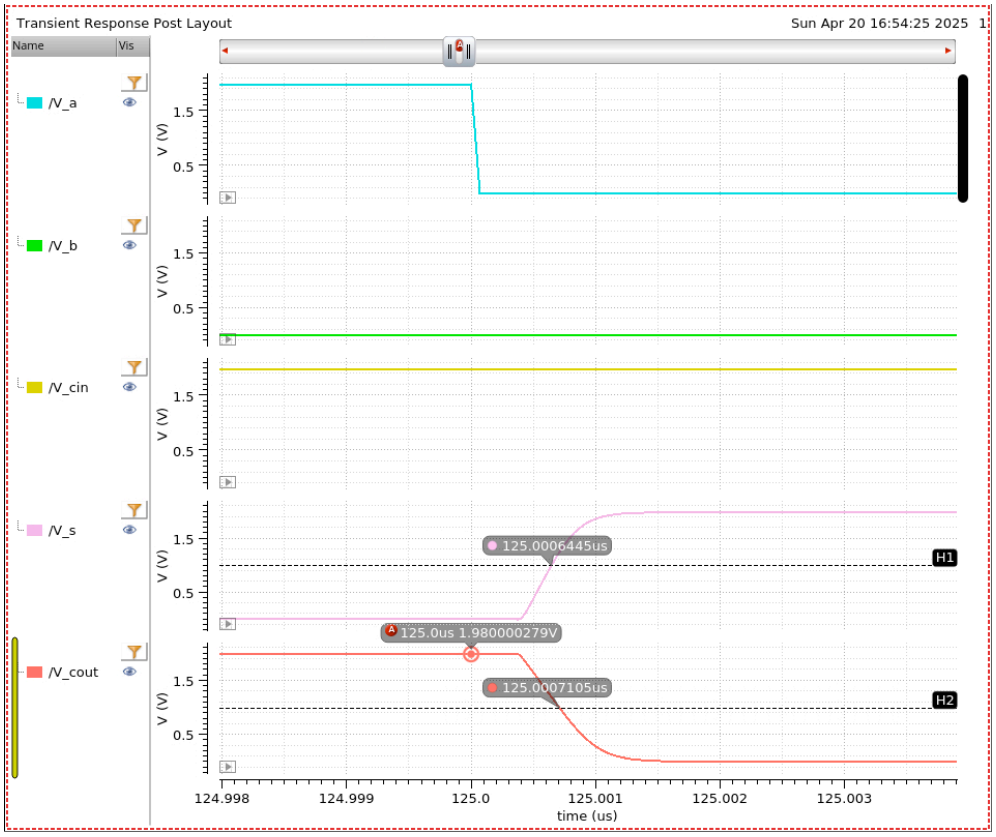
Post layout transient simulation with inputs at 20kHz



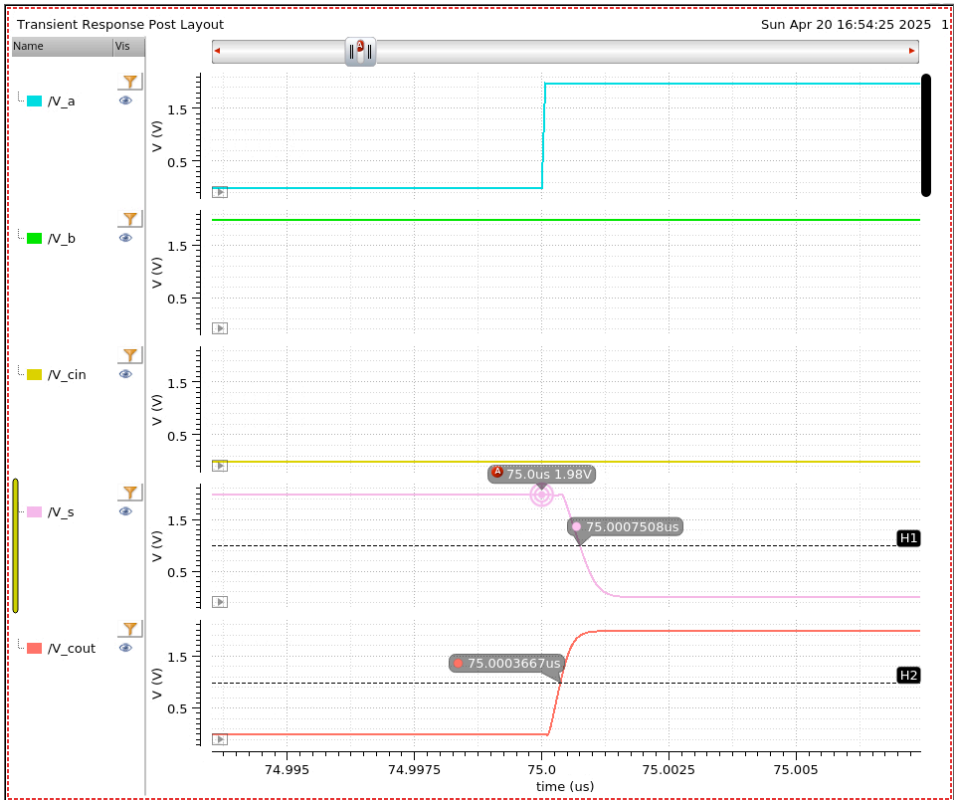
Propagation delay for Vs: 627ps. Propagation delay for Vcout: 443ps.



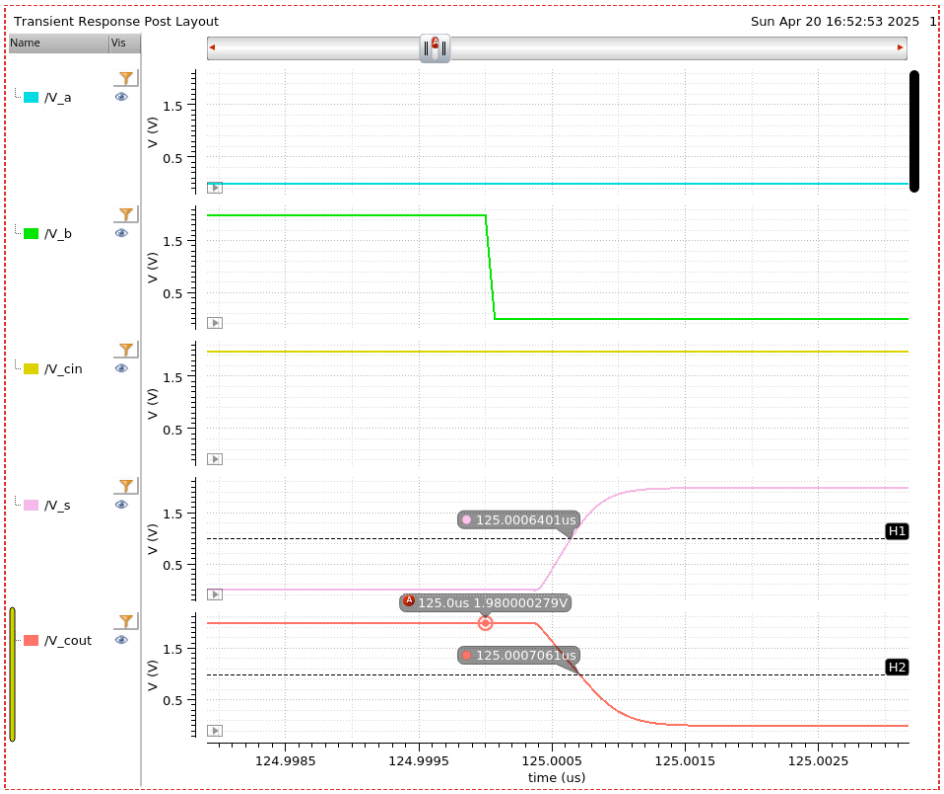
Propagation delay for Vs: 714ps. Propagation delay for Vcout: 594ps.



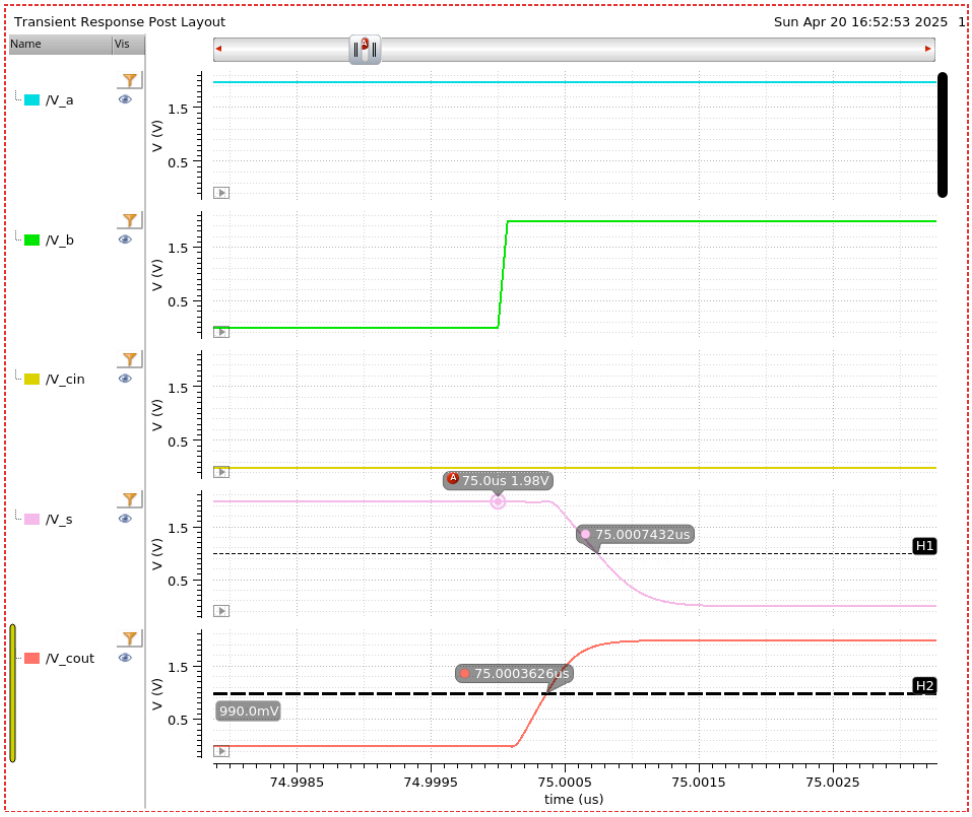
Propagation delay for Vs: 645ps. Propagation delay for Vcout: 711ps.



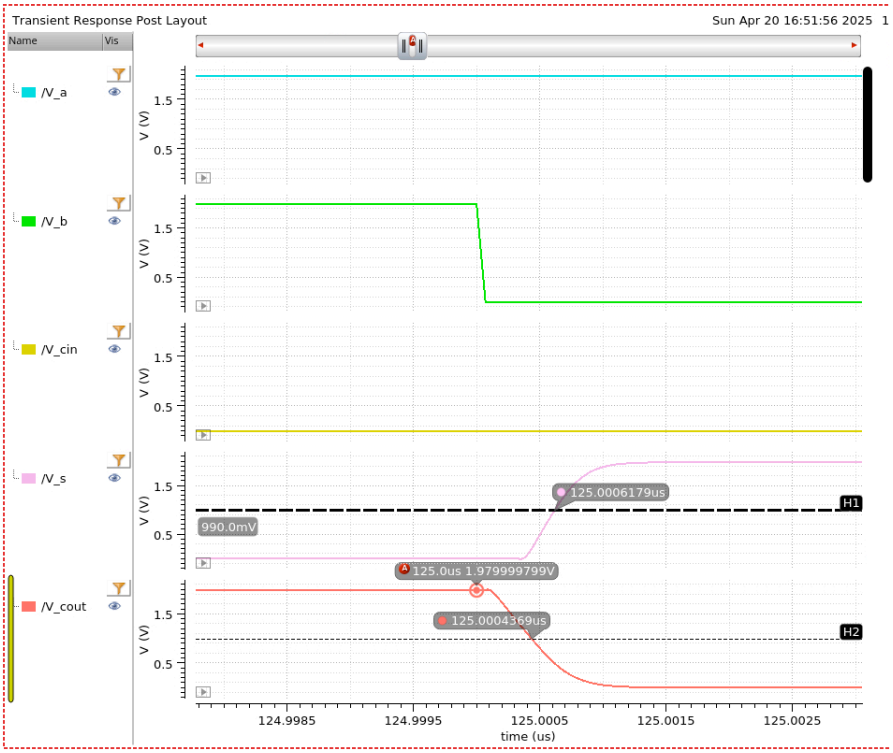
Propagation delay for Vs: 751ps. Propagation delay for Vcout: 367ps.



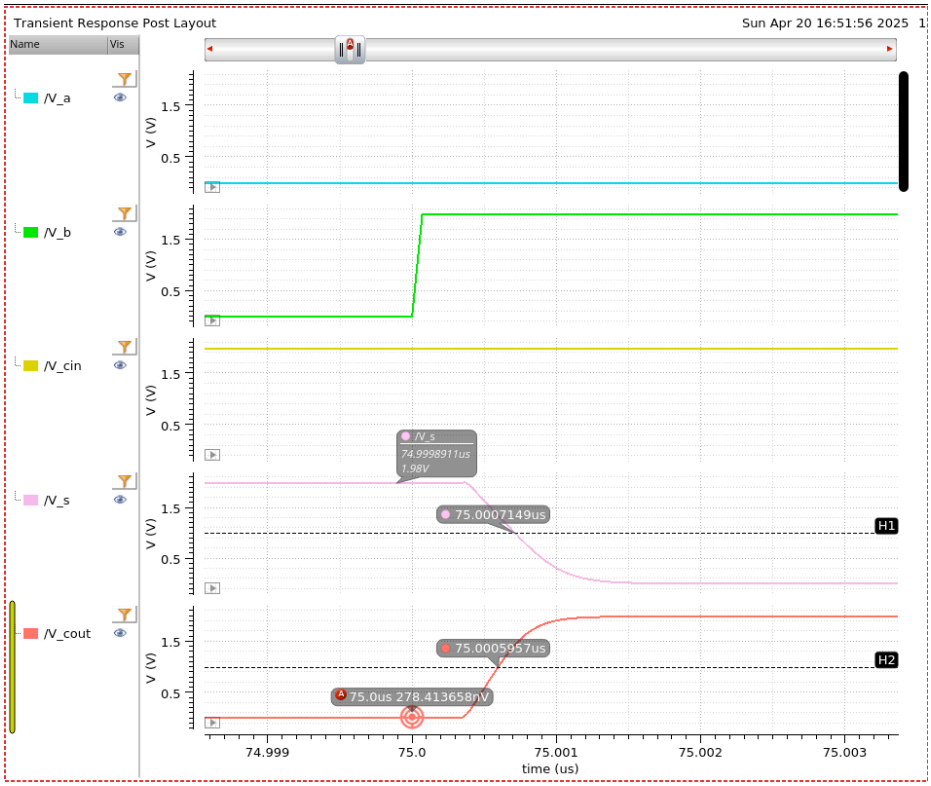
Propagation delay for Vs: 640ps. Propagation delay for Vcout: 706ps.



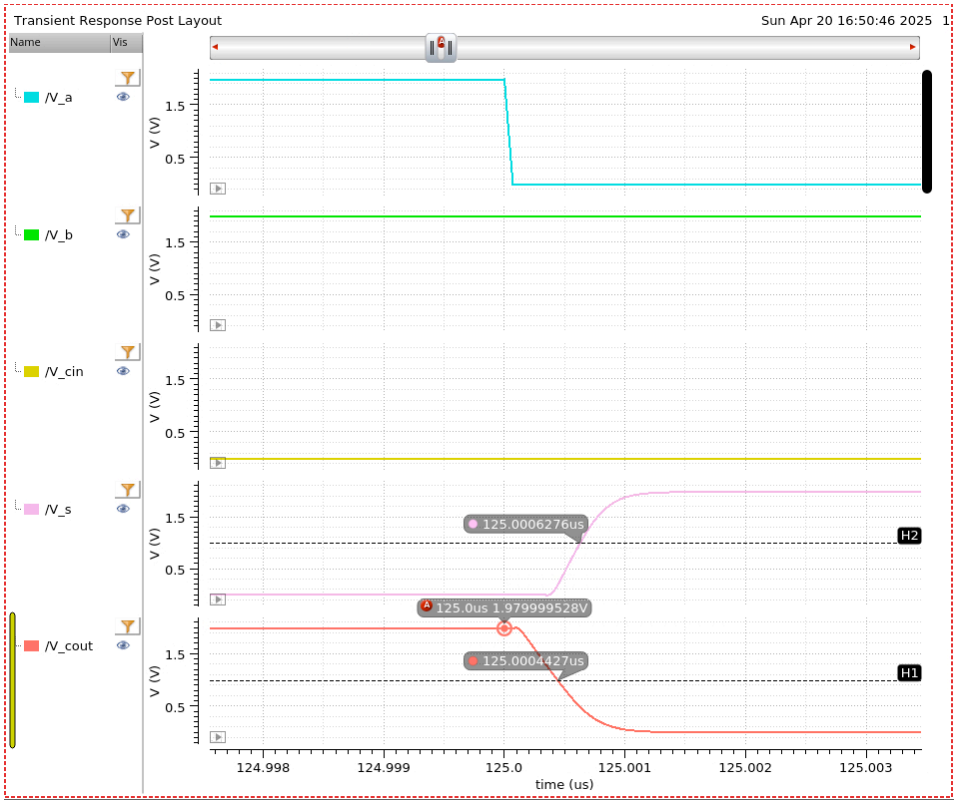
Propagation delay for Vs: 743ps. Propagation delay for Vcout: 363ps.



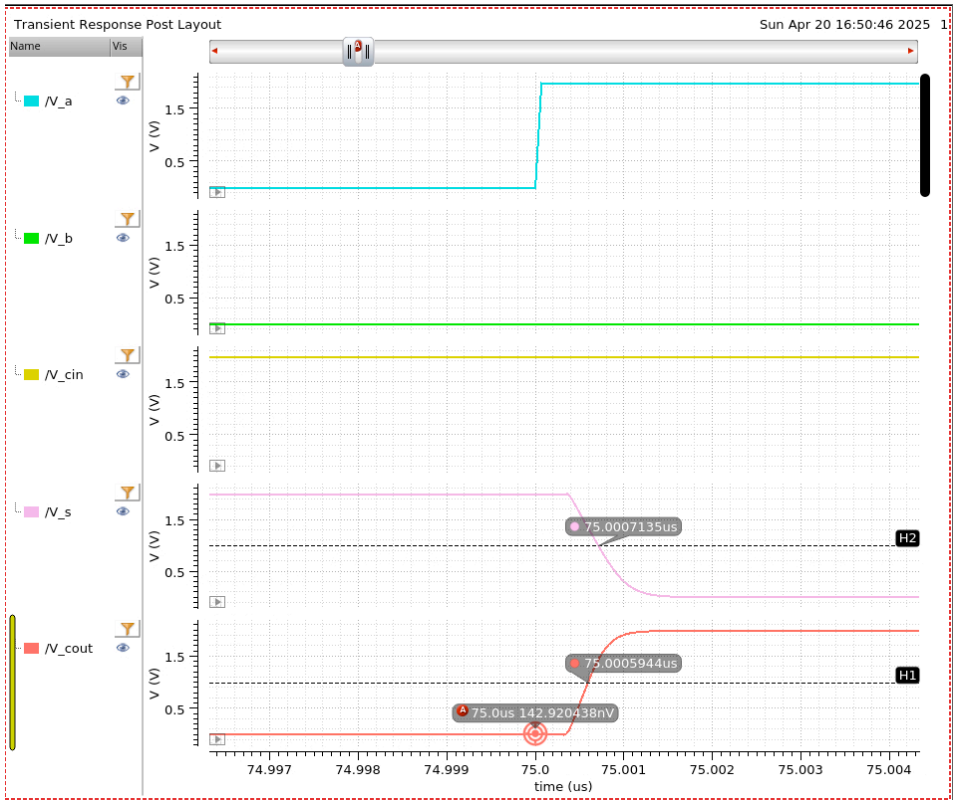
Propagation delay for Vs: 618ps. Propagation delay for Vcout: 437ps.



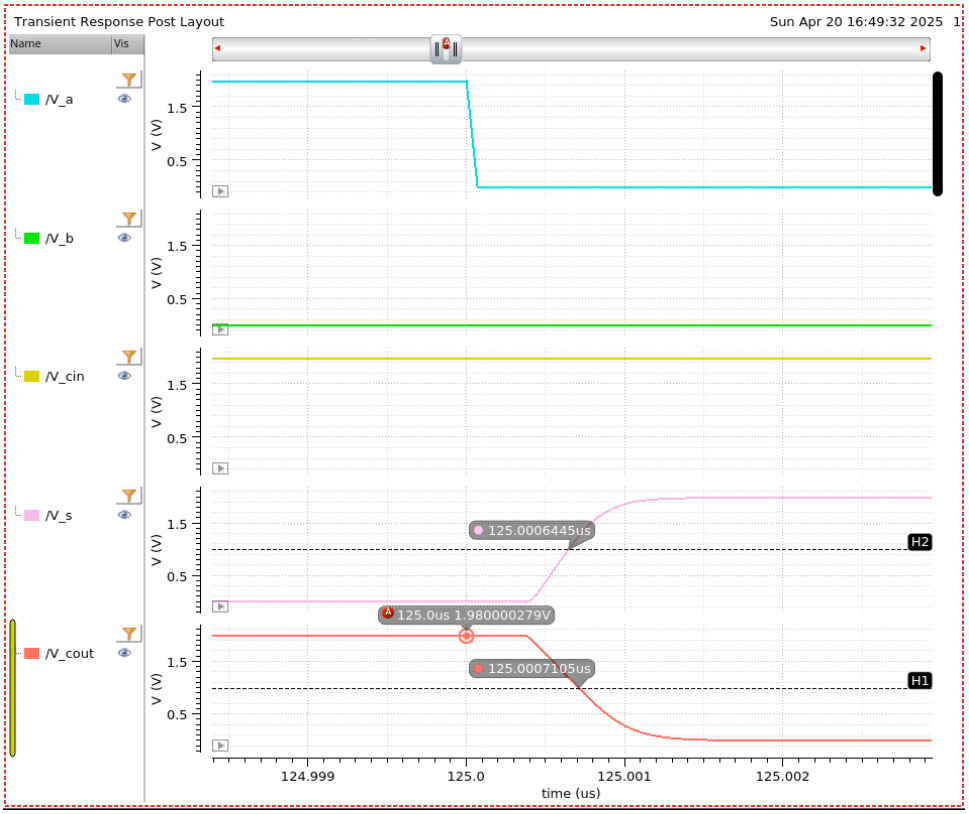
Propagation delay for Vs: 715ps. Propagation delay for Vcout: 596ps.



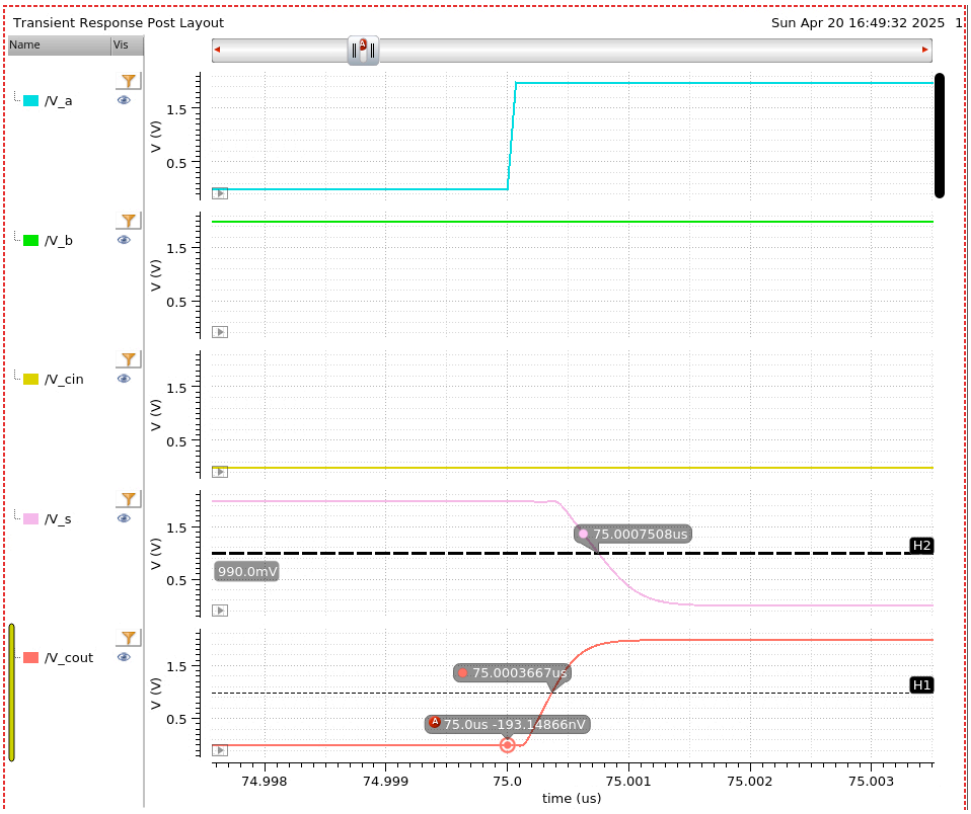
Propagation delay for Vs: 628ps. Propagation delay for Vcout: 443ps.



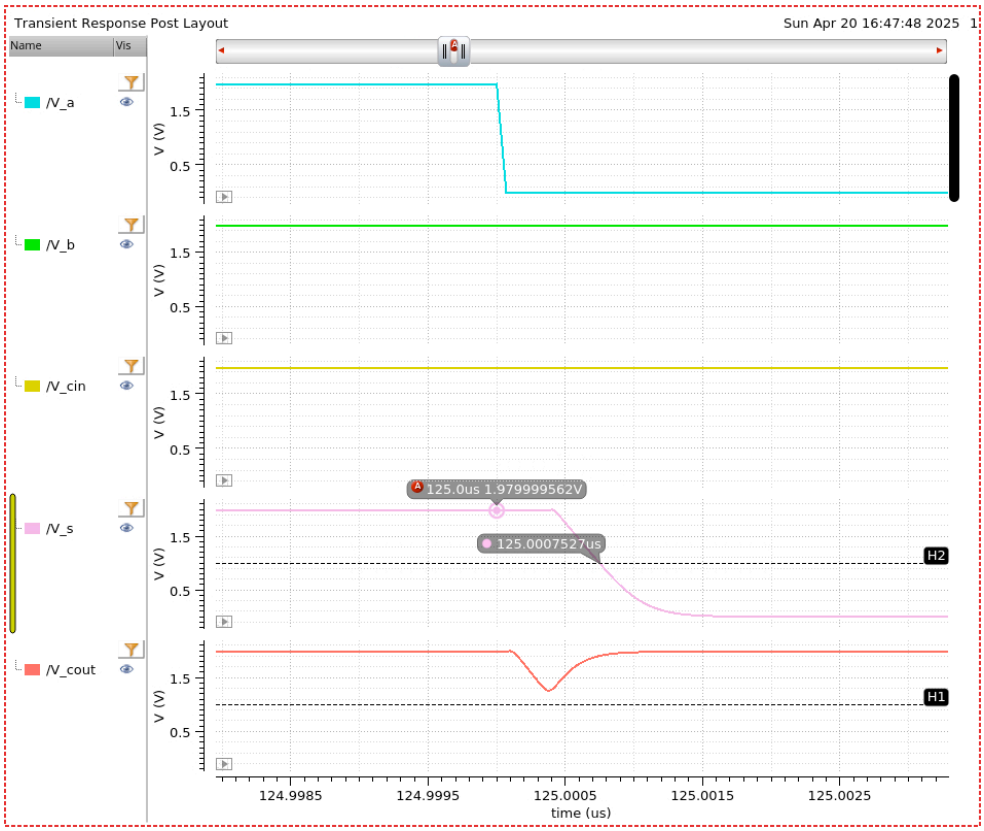
Propagation delay for Vs: 714ps. Propagation delay for Vcout: 594ps.



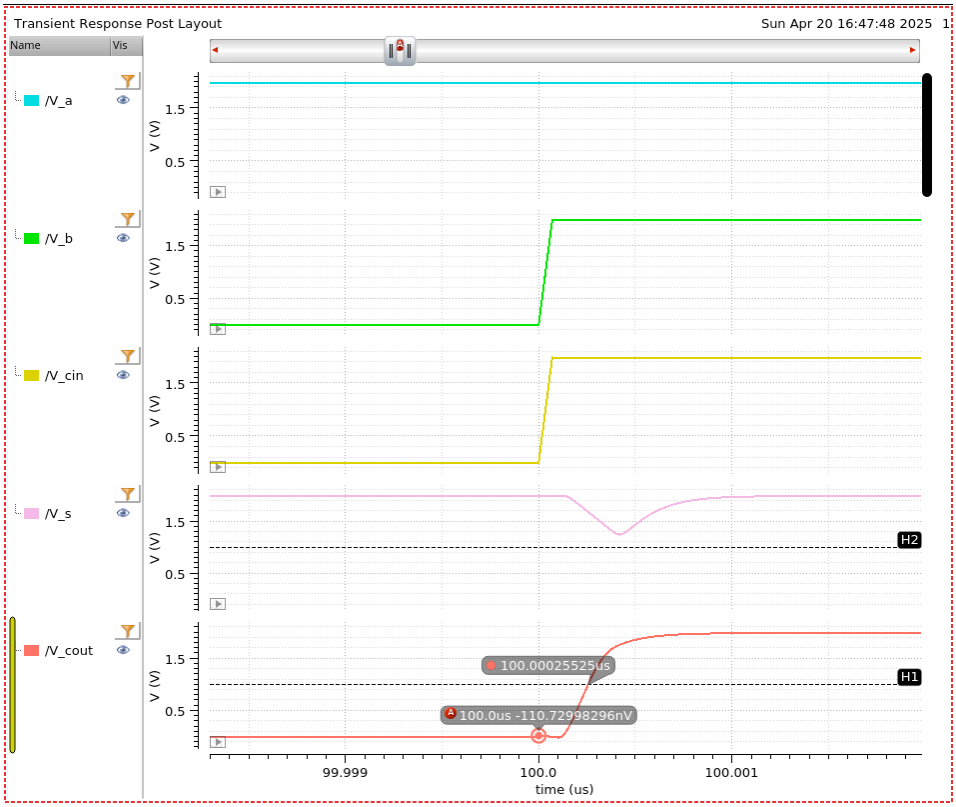
Propagation delay for Vs: 645ps. Propagation delay for Vcout: 711ps.



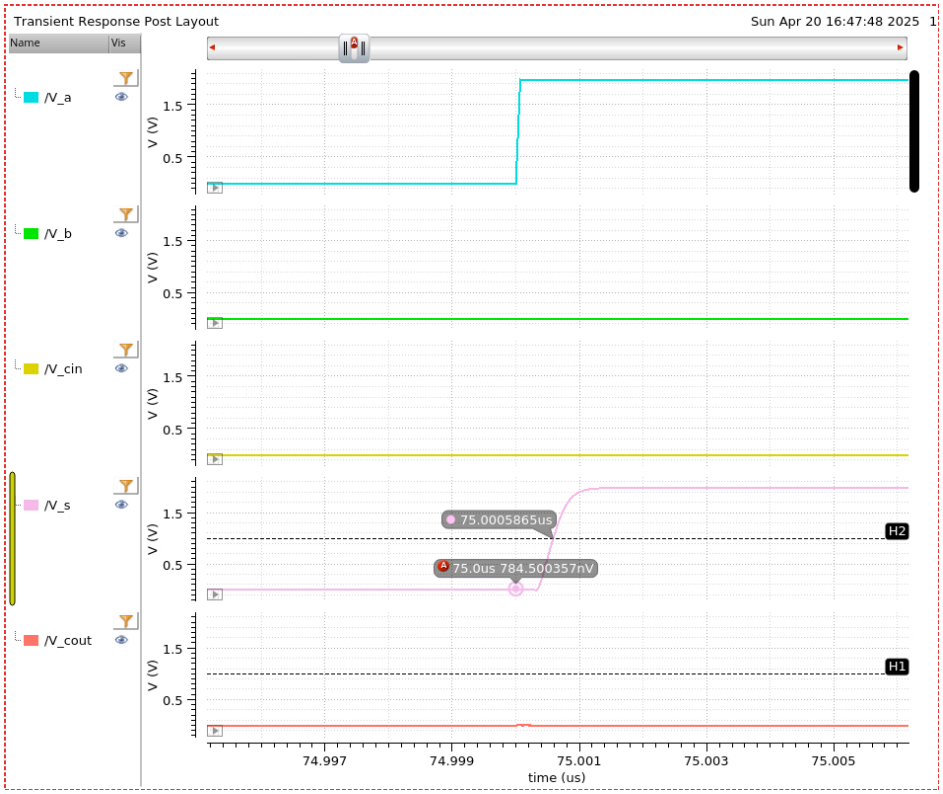
Propagation delay for Vs: 751ps. Propagation delay for Vcout: 367ps.



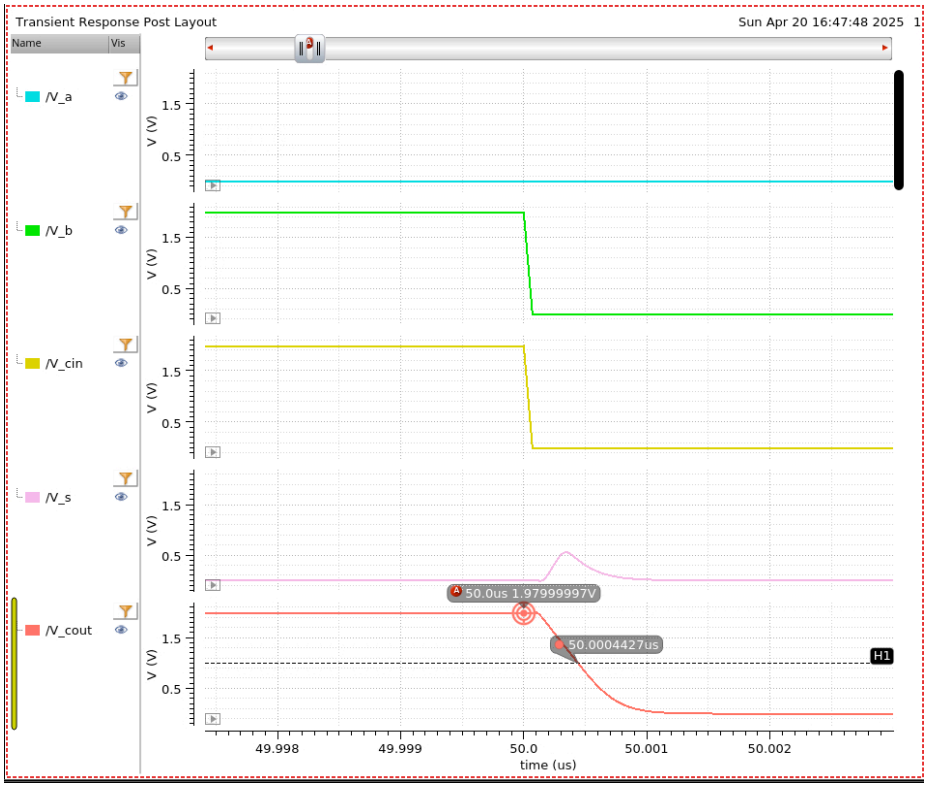
Propagation delay for Vs: 753ps.



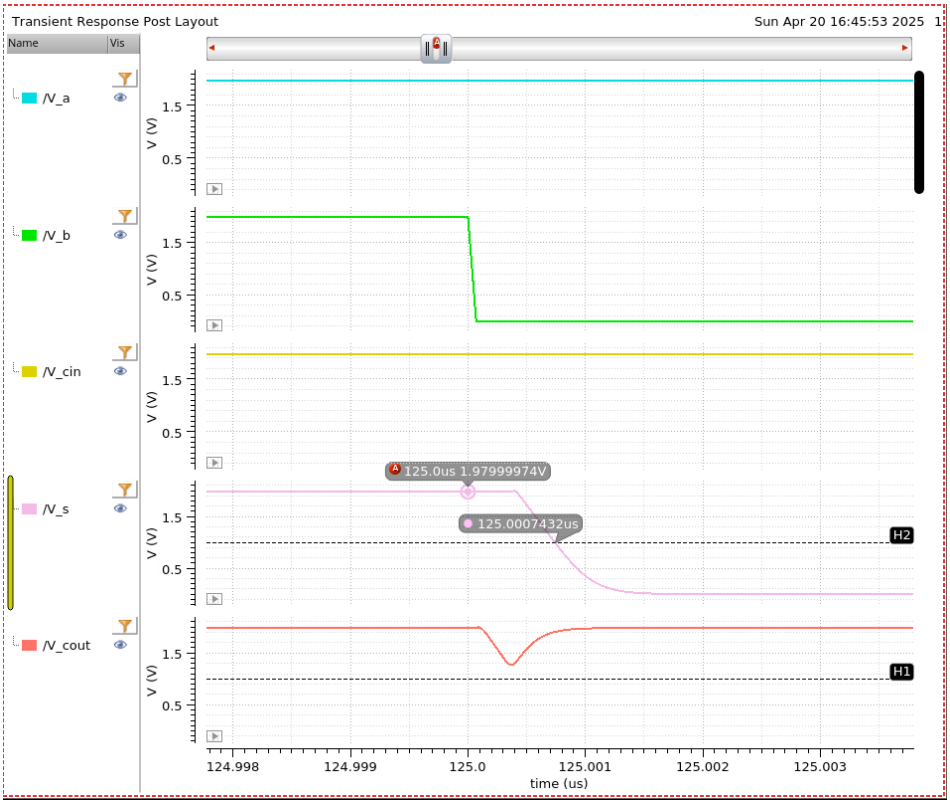
Propagation delay for Vcout: 255ps.



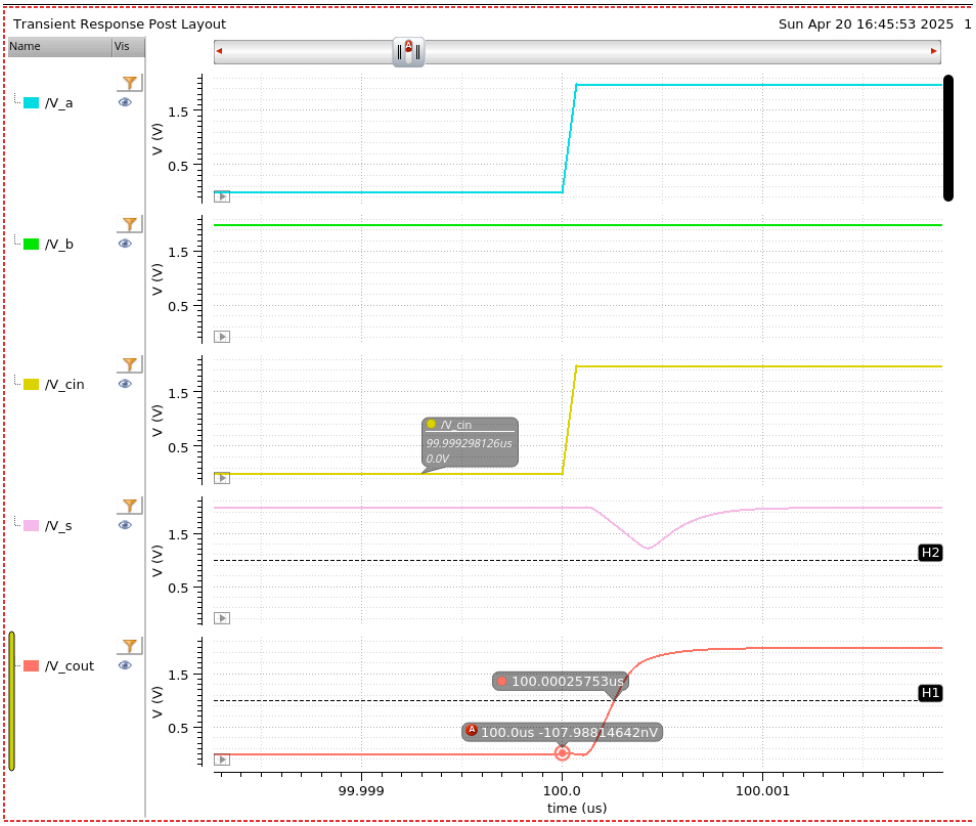
Propagation delay for Vs: 587ps.



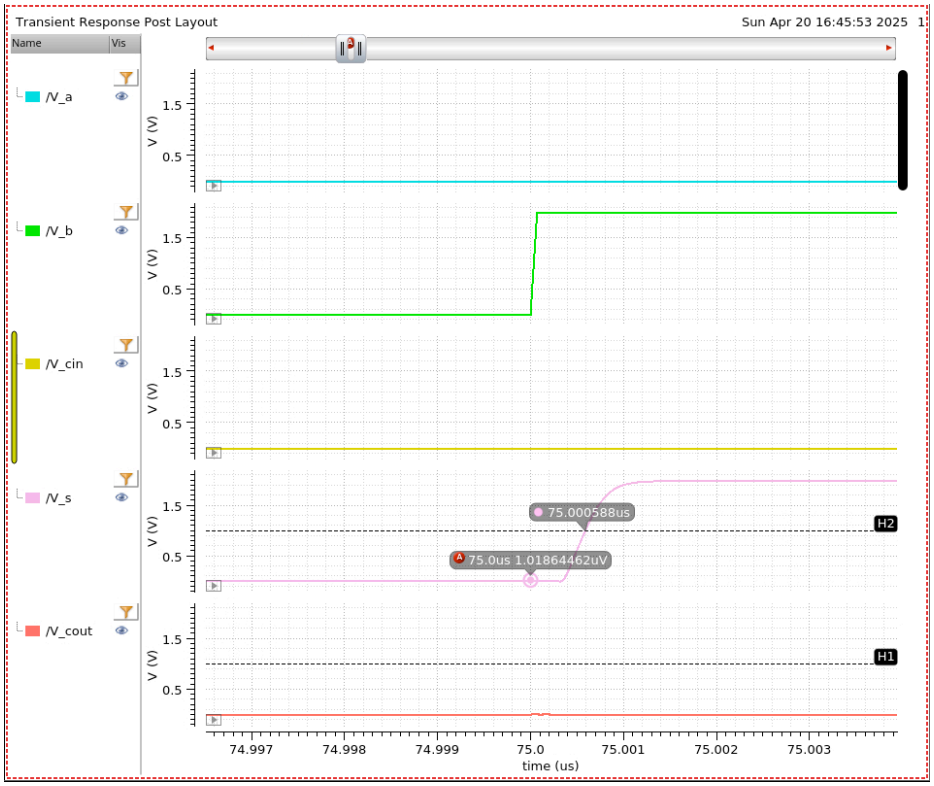
Propagation delay for Vcout: 443ps.



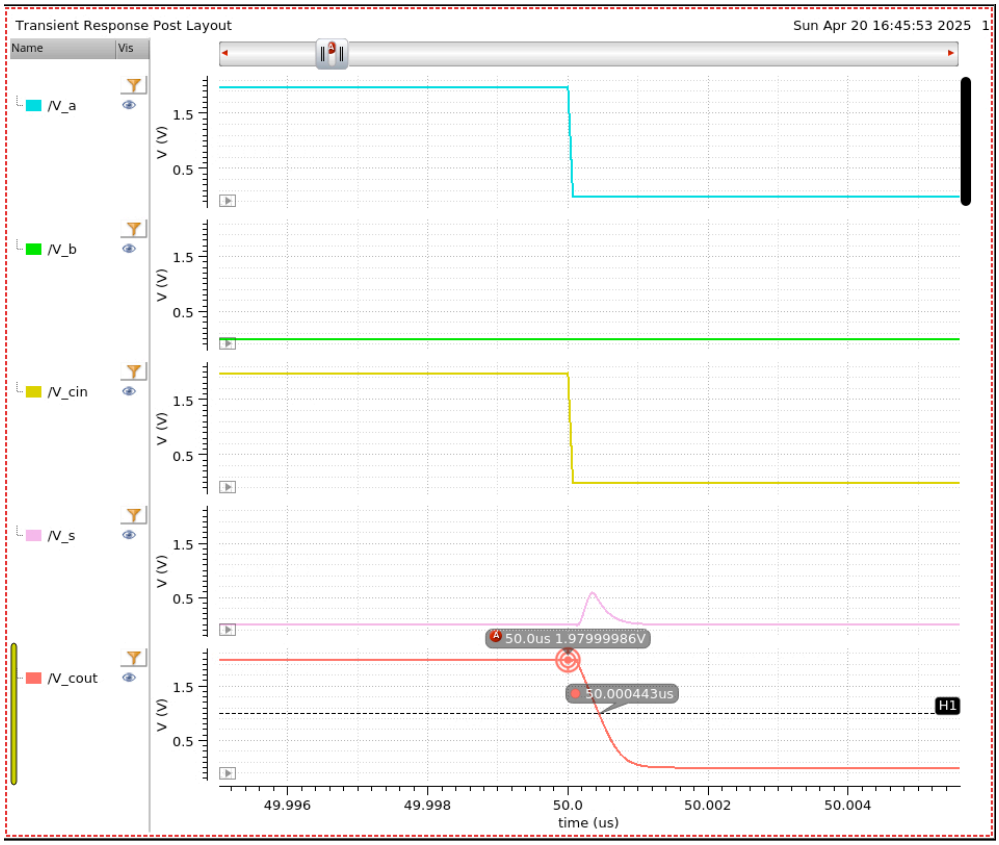
Propagation delay for Vs: 743ps.



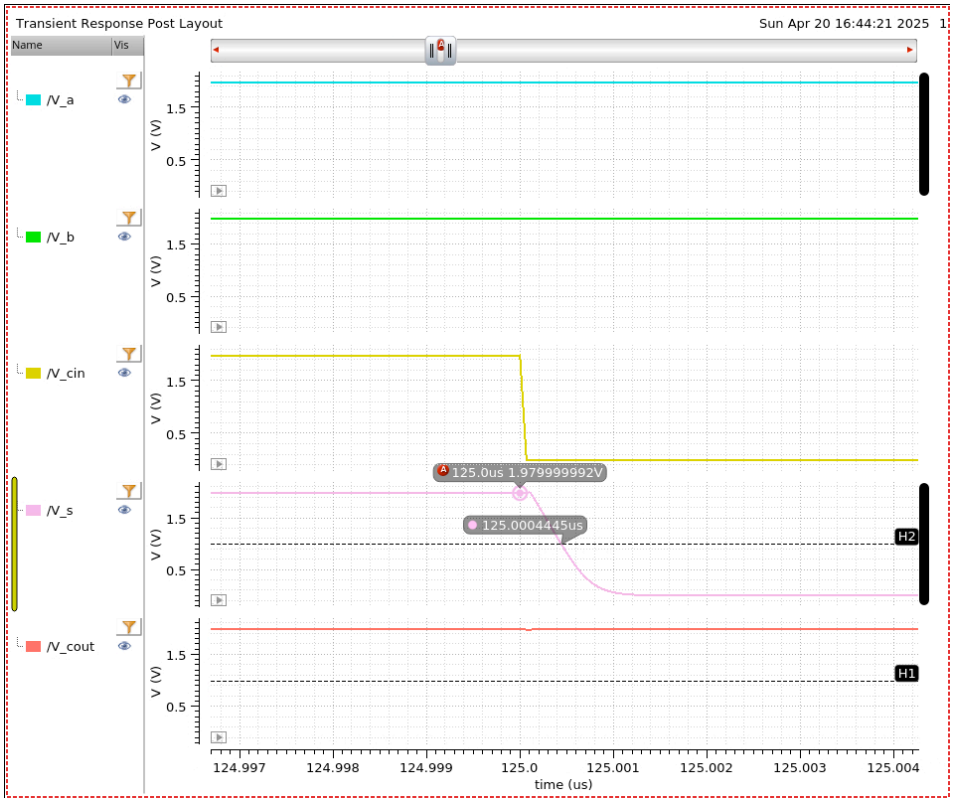
Propagation delay for Vcout: 257ps.



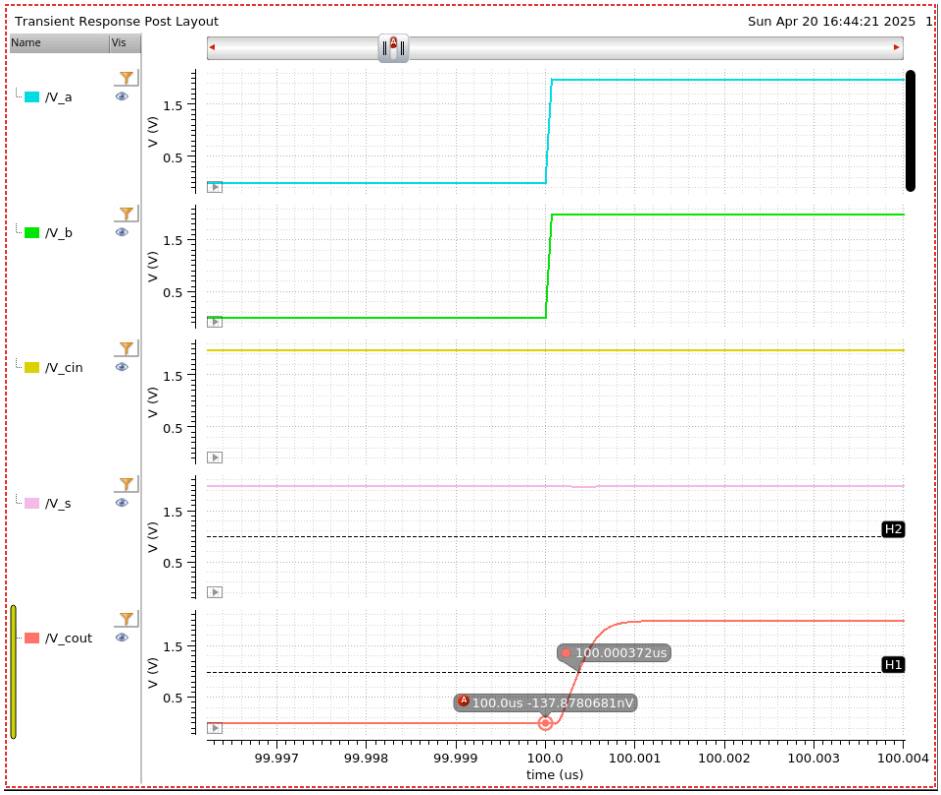
Propagation delay for Vs: 588ps.



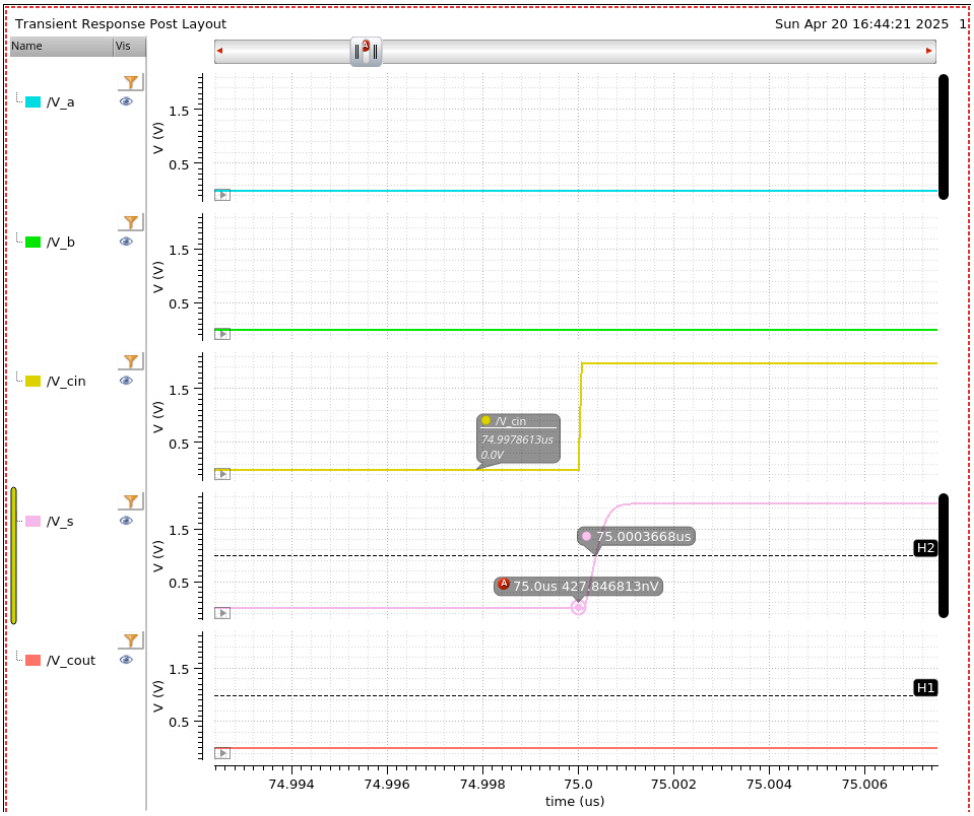
Propagation delay for Vcout: 443ps.



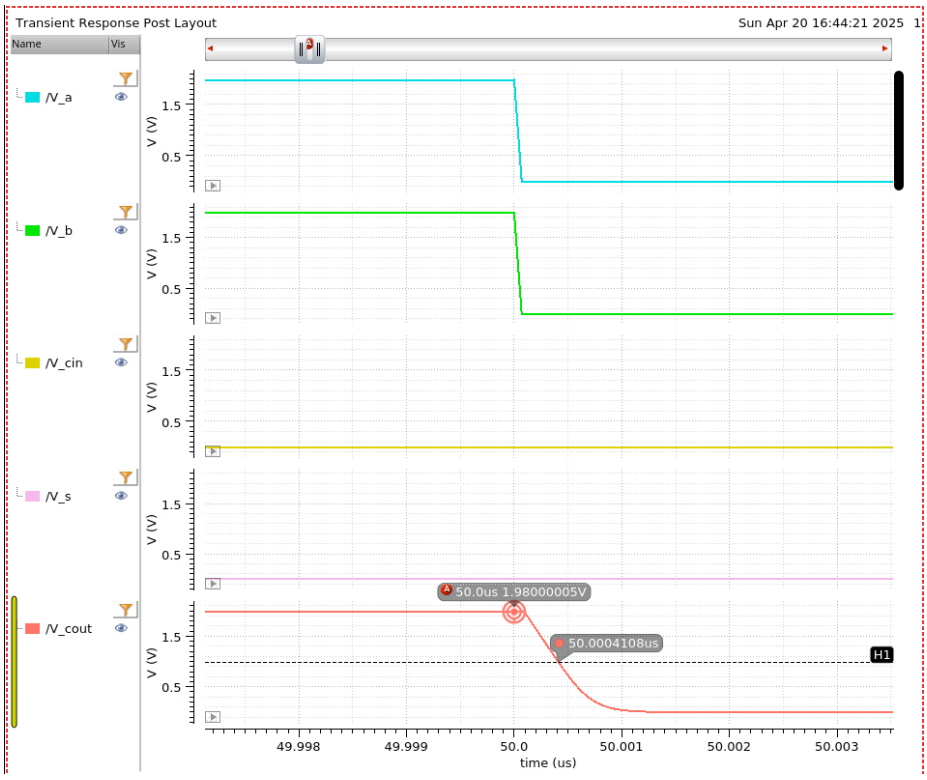
Propagation delay for Vs: 445ps.



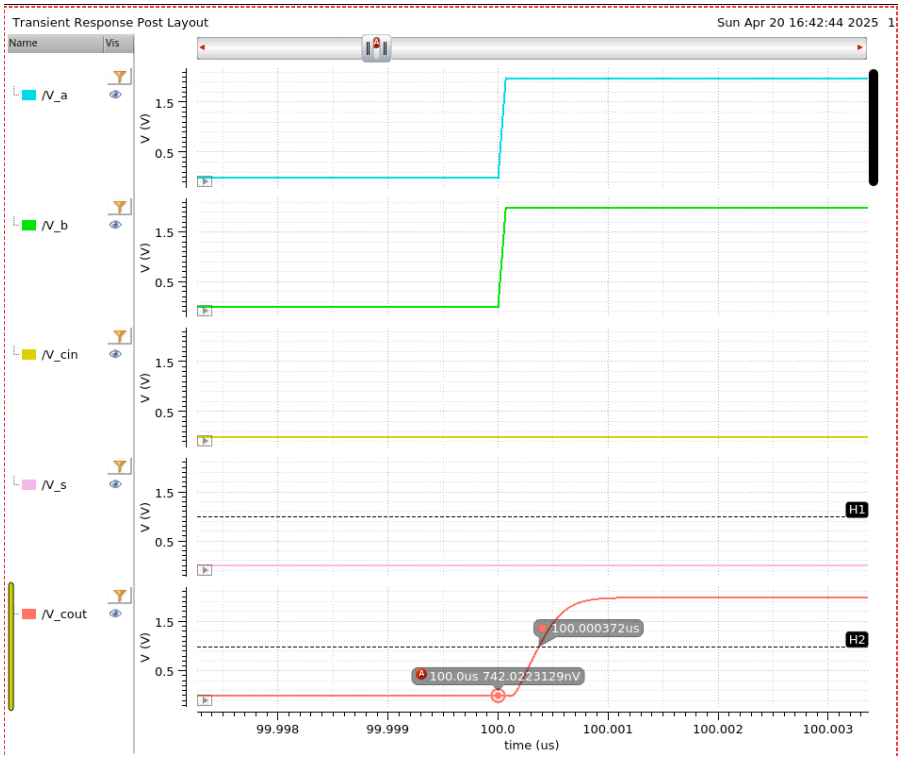
Propagation delay for Vcout: 372ps.



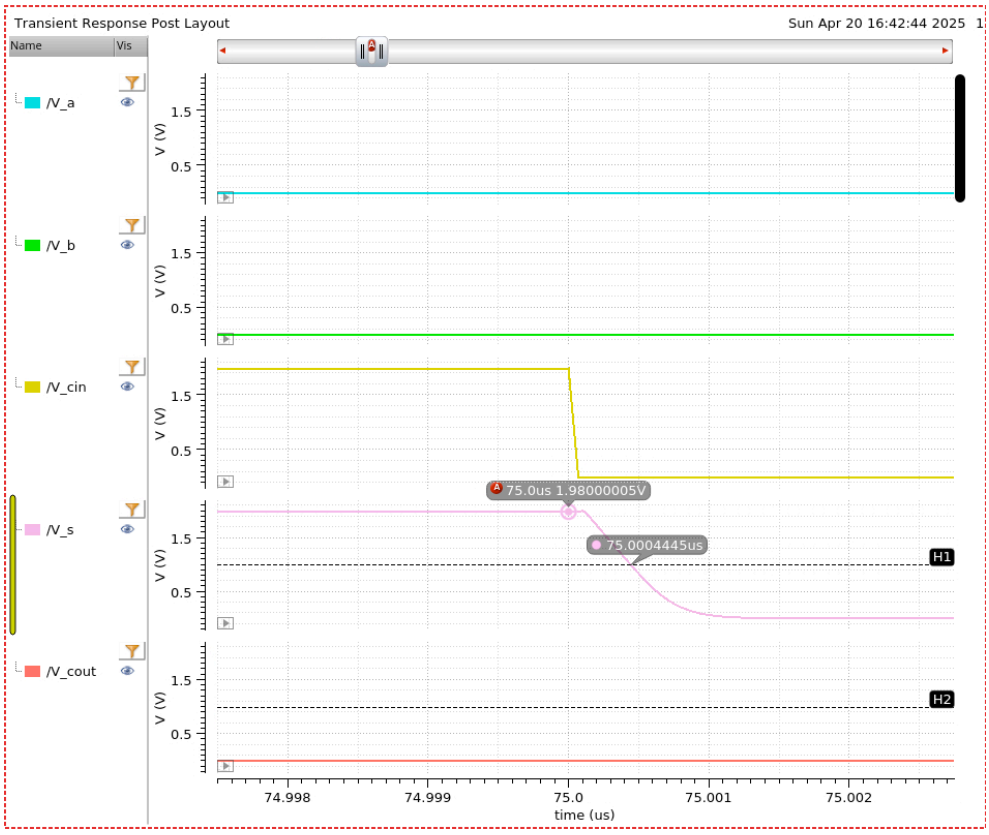
Propagation delay for Vs: 367ps.



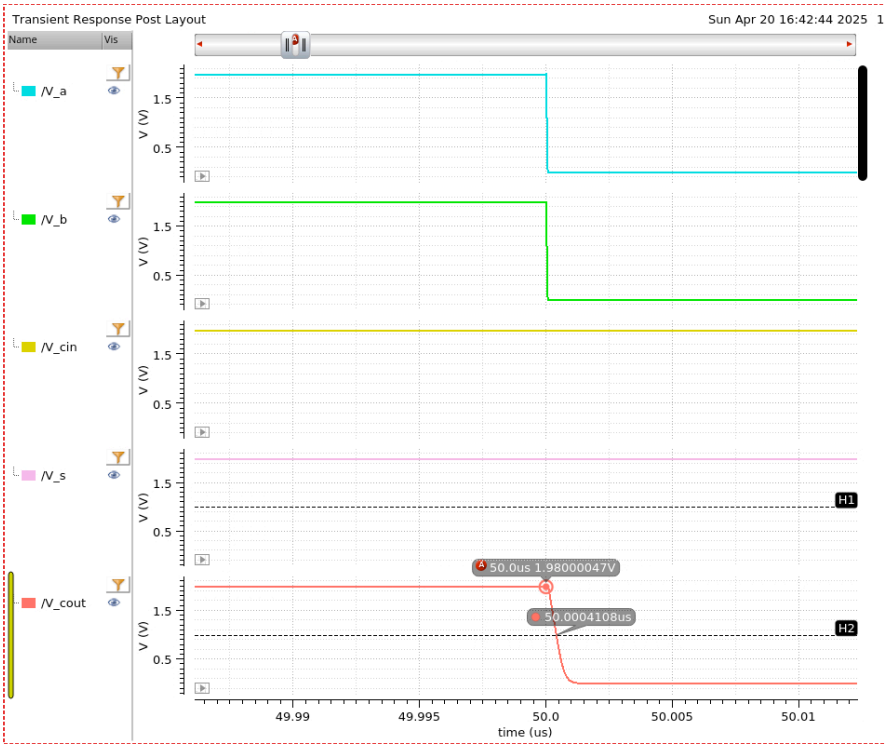
Propagation delay for Vcout: 411ps.



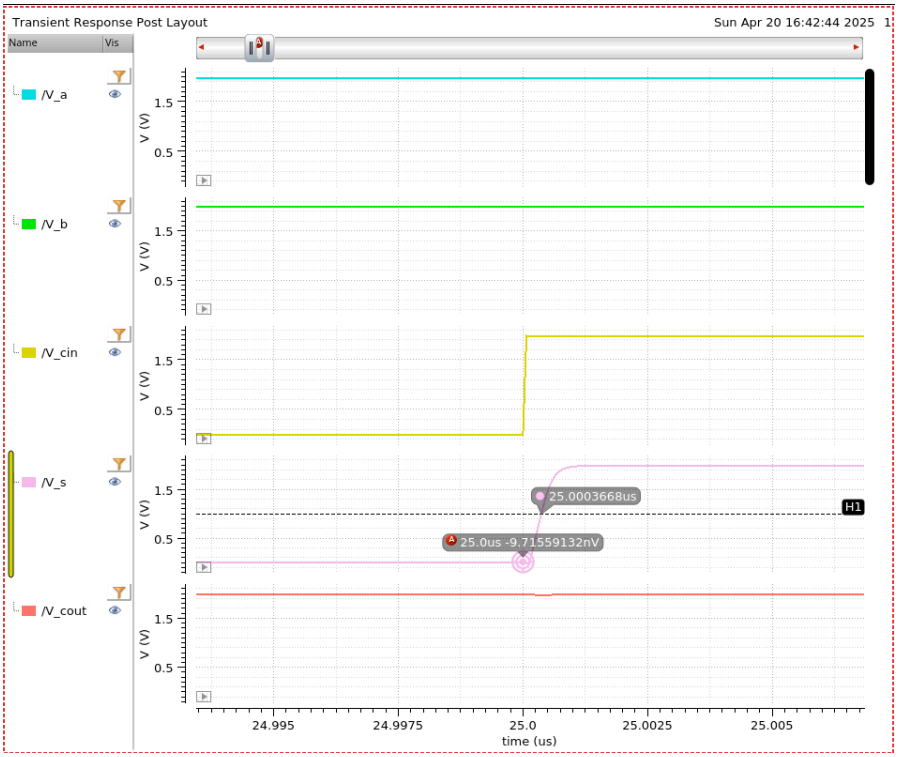
Propagation delay for Vcout: 372ps.



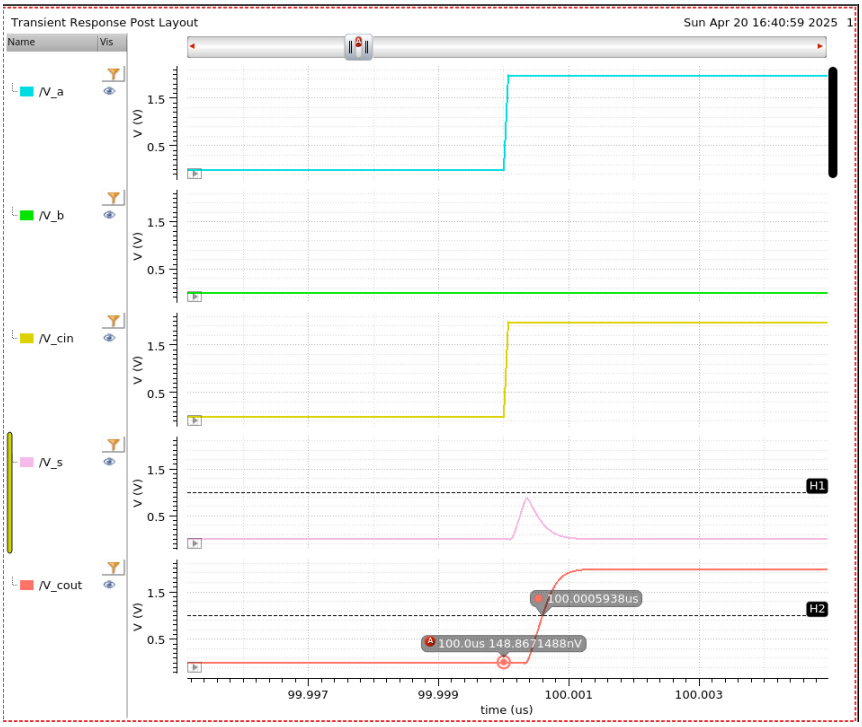
Propagation delay for Vs: 445ps.



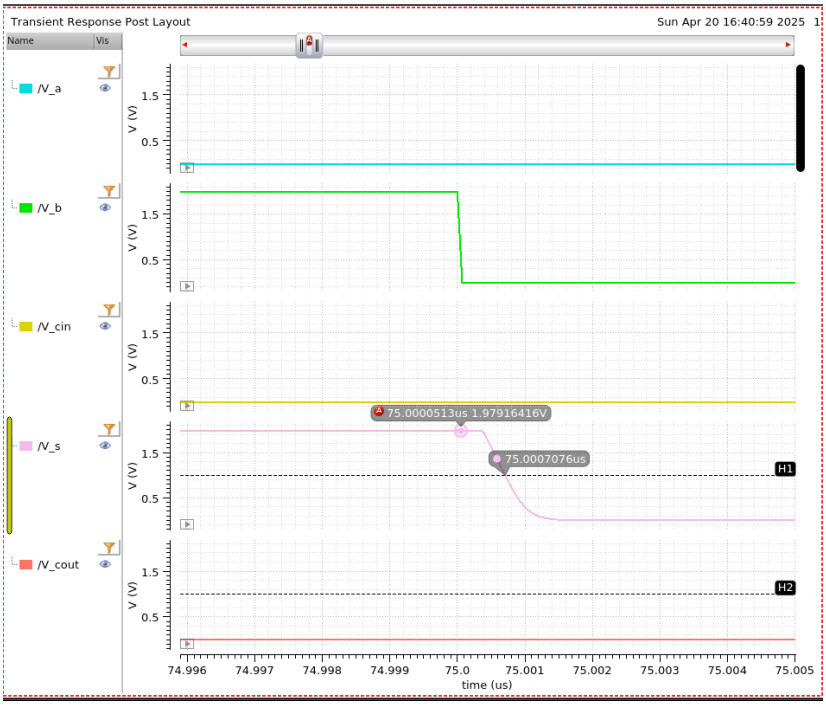
Propagation delay for Vcout: 411ps.



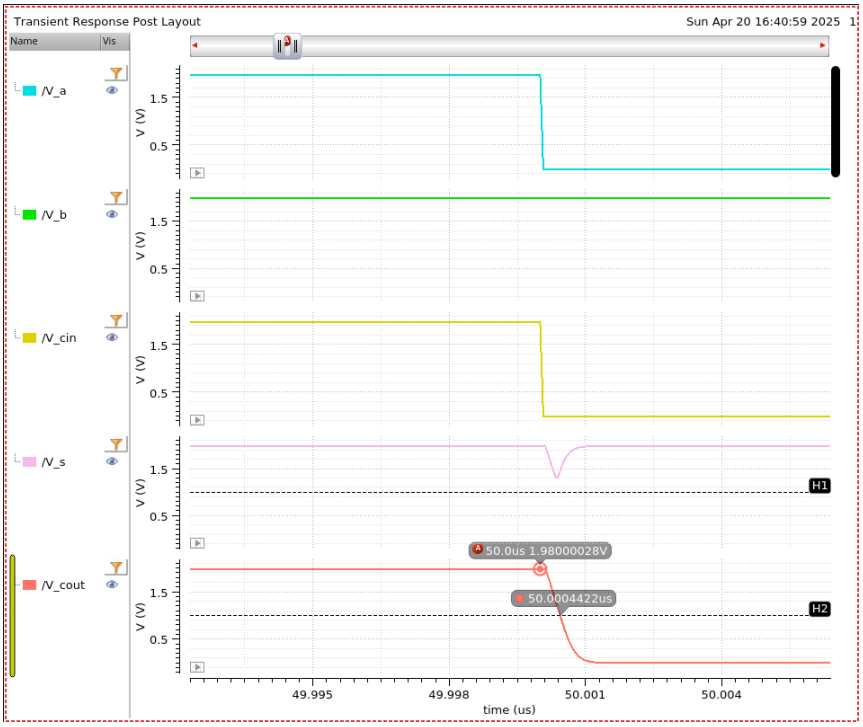
Propagation delay for Vs: 367ps.



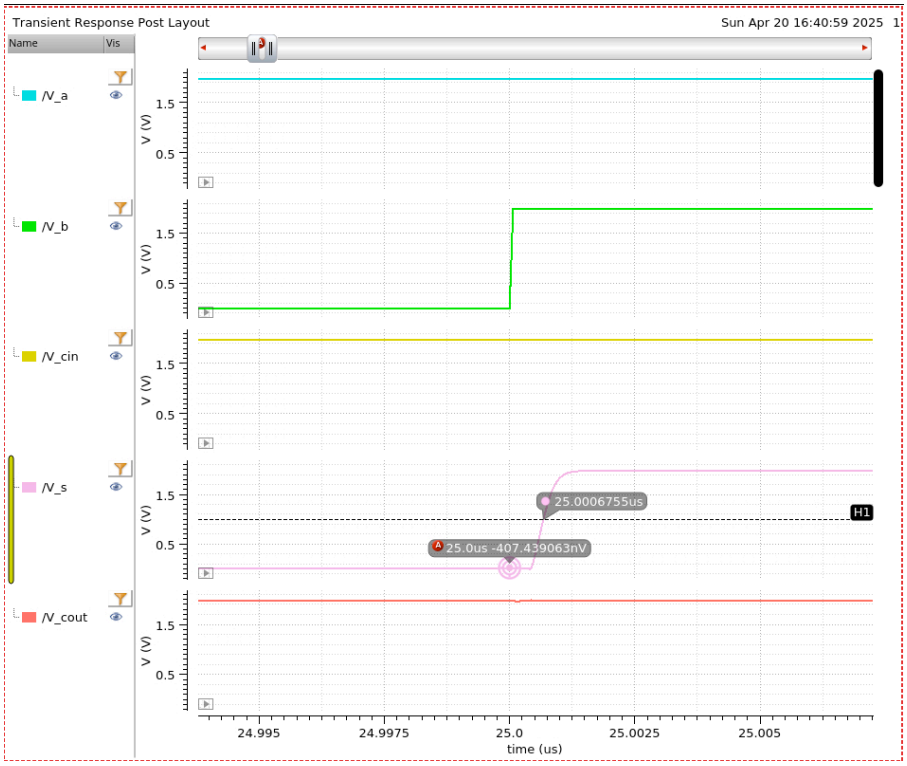
Propagation delay for Vcout: 594ps.



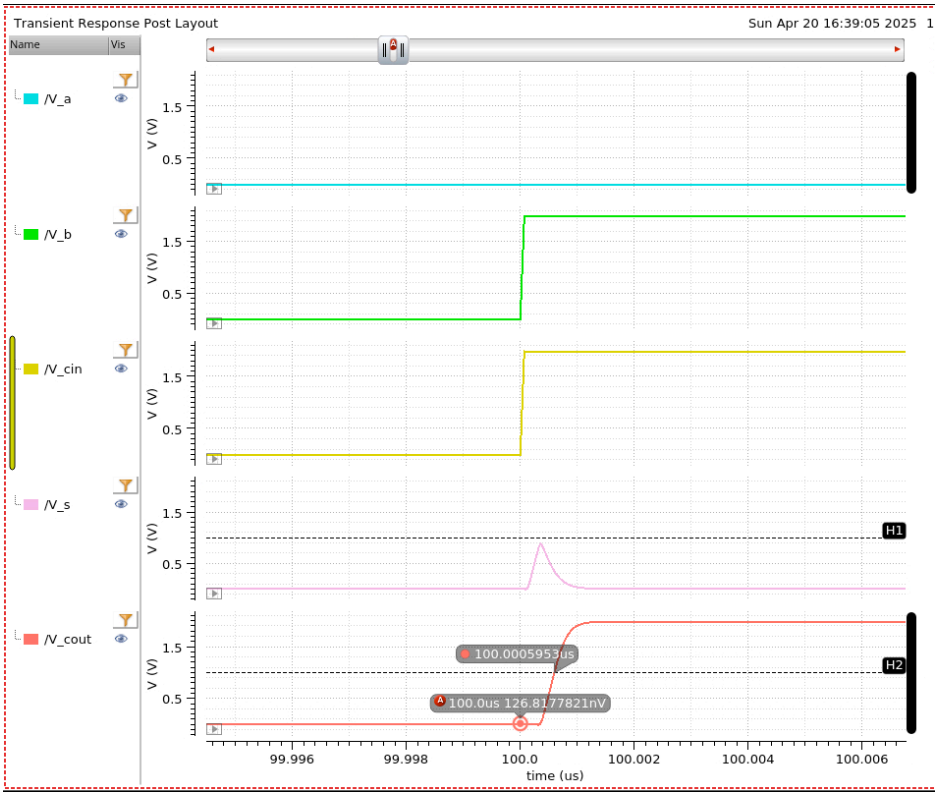
Propagation delay for Vs: 708ps.



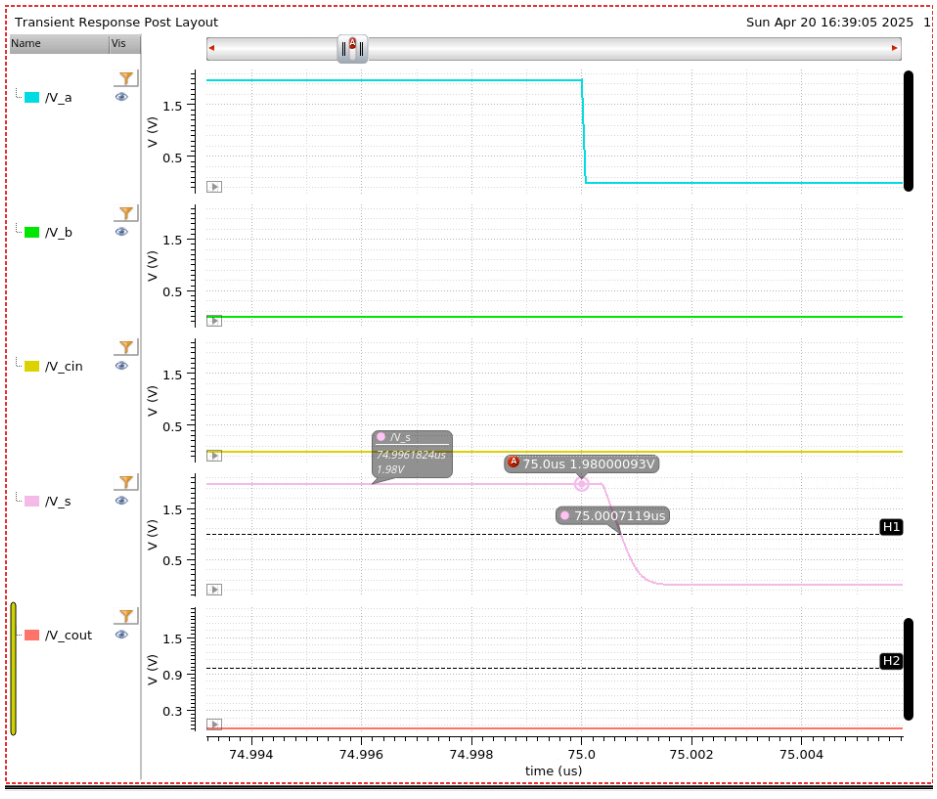
Propagation delay for Vcout: 442ps.



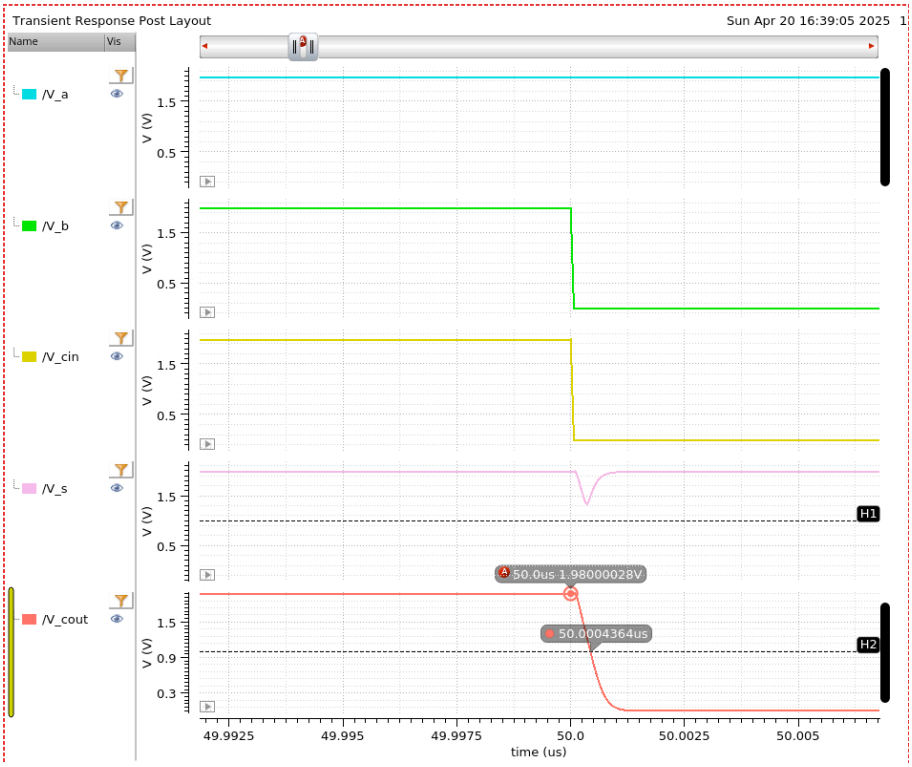
Propagation delay for Vs: 676ps.



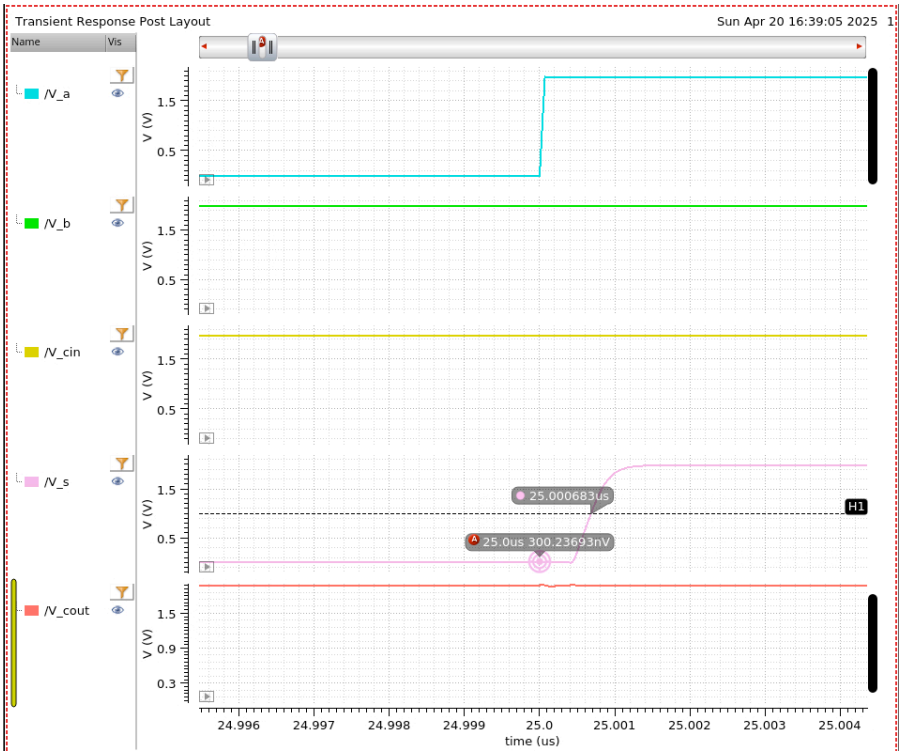
Propagation delay for Vcout: 595ps.



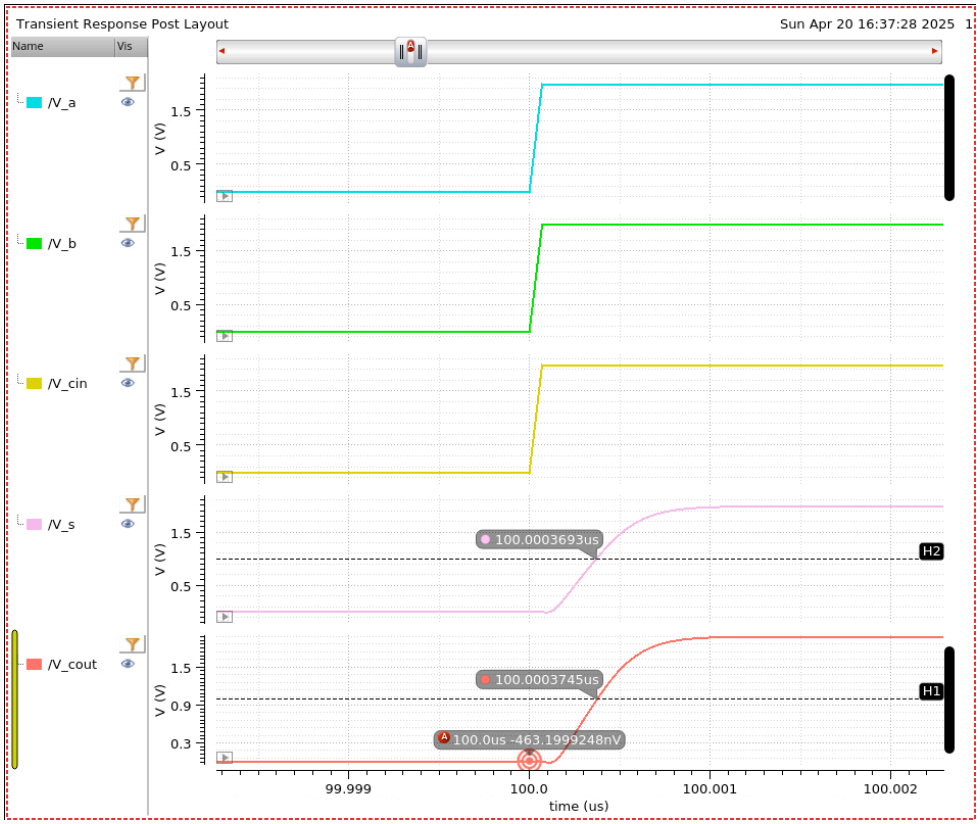
Propagation delay for Vs: 712ps.



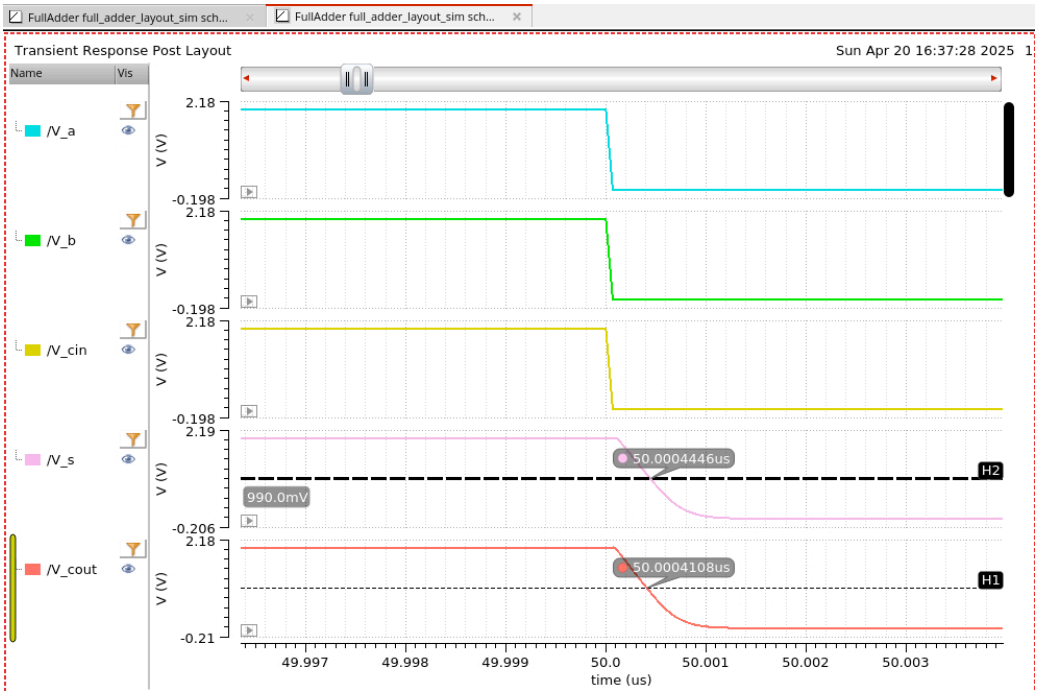
Propagation delay for Vcout: 436ps.



Propagation delay for Vs: 683ps.



Propagation delay for Vs: 369ps.
Propagation delay for Vcout: 375ps.



Propagation delay for Vs: 445ps.
Propagation delay for Vcout: 411ps.

Worst Case Propagation Delays

The worst case high to low propagation delay for Vs was found as 753ps. While the worst case low to high propagation delay was 683ps.

The worst case high to low propagation delay for Vcout was found as 711ps. While the worst case low to high propagation delay was 596ps.

It is worth noting that the layout effects did increase the propagation delays on average and that all worst case propagation delays have increased by ~10 ps on average.