

EE302 Spring 2025

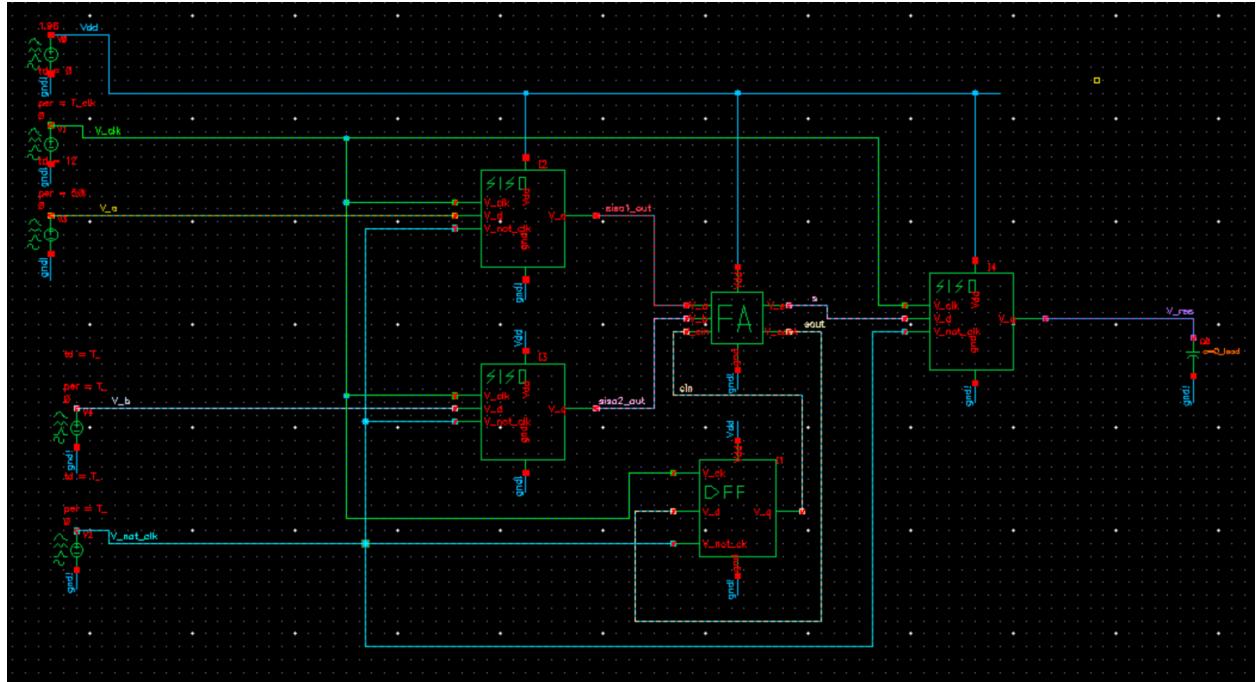
Lab 6 Report

04/06/2025

4 Bit Serial Adder

Schematic

The schematic for the 4 bit serial adder is provided below. The serial adder was constructed fully from modules implemented in the previous labs. It should be noted that the memory elements (DFF and SISO registers) are all negative edge triggered.

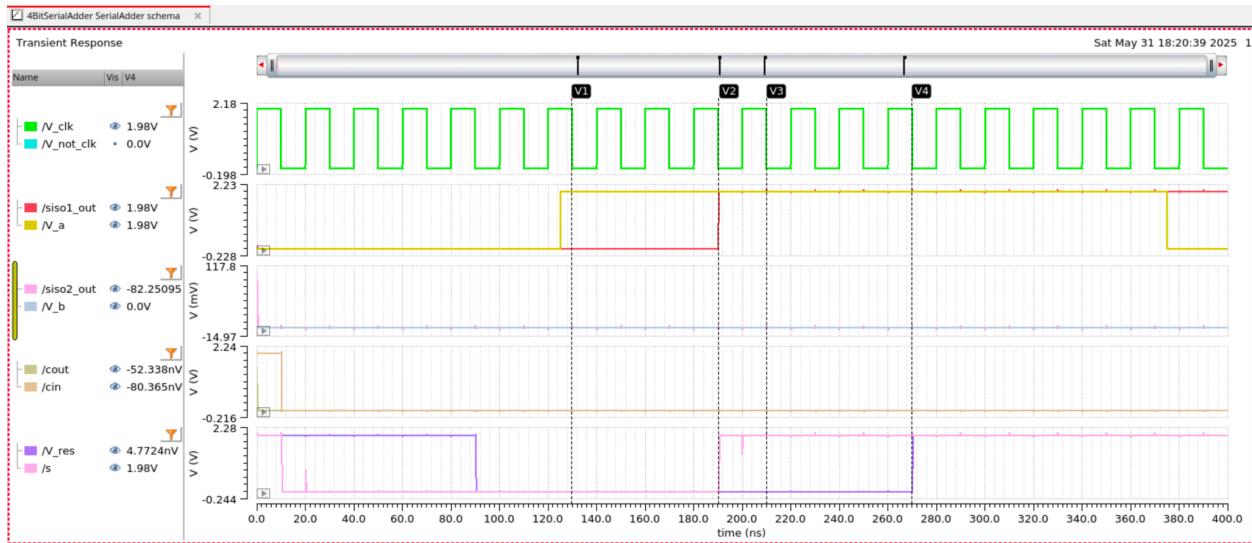


Transient Simulation

Transient simulation results for $C_{load} = 100f\text{ F}$ are provided below:

Test Case #1

Transient simulation results for a: 1111 and b: 0000 could be found below:

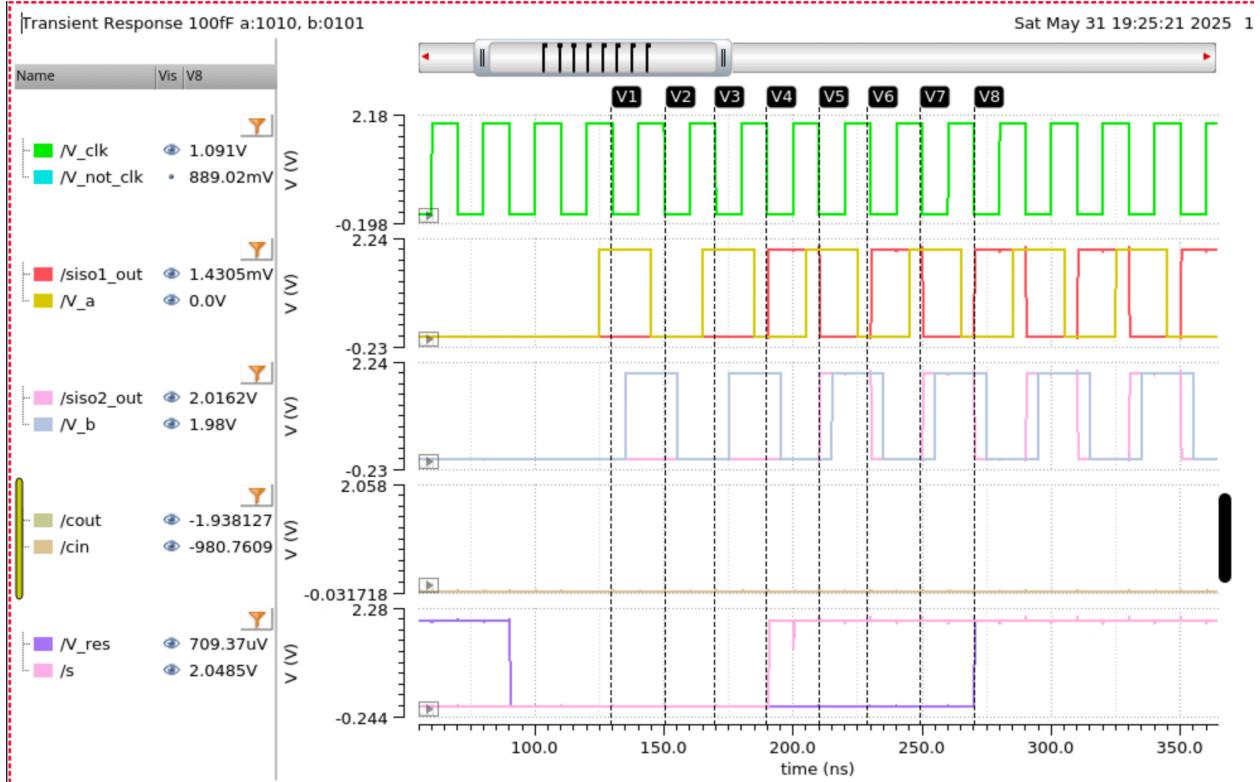


Since we haven't extracted the symbol yet, we can view the values of wires that would otherwise be contained inside the symbol (hence inaccessible from the outside). We can observe that the all positive input sequence for V_a appears at $/iso1_out$ after 4 clock cycles and $/V_{res}$ follows 4 clock cycles after that (8 cycles after V_a flips to 1 for the first time). This demonstrates that the operation of the serial adder is correct. The result for this sequence of inputs is 1111 at the output which is correct.

It should be noted that the initial state of the flip flop cannot be known before simulation, hence we had to wait for the circuit to process a sequence of all 0 inputs and reset itself before we could move on with the test cases.

Test Case #2

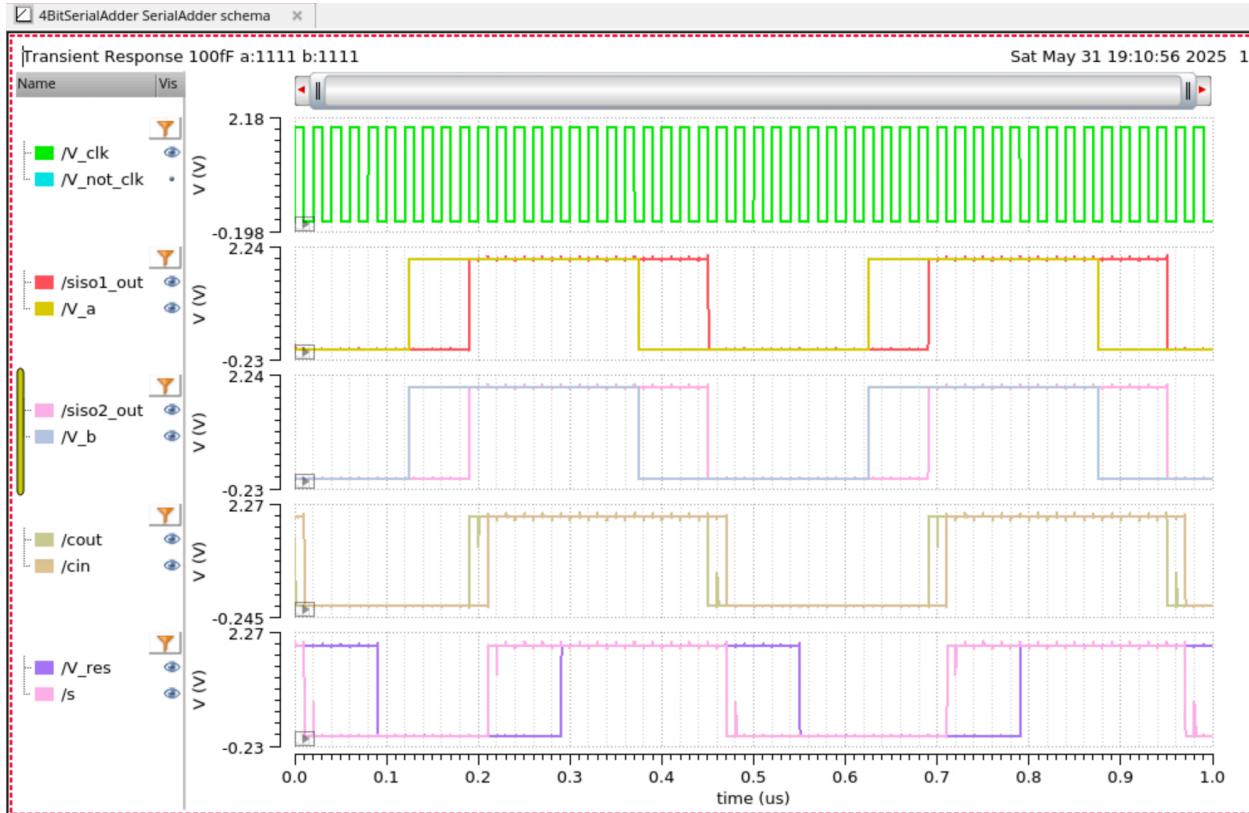
Transient simulation results for a: 1010 and b: 0101 could be found below:



As expected the inputs reach the dequeuing ends of their SISOs at the end of the 4th negative edge and a change in the output sequence occurs 4 negative edges later (8 negative edges after the input sequence is provided). The output produced for these input sequences is 1111 which is correct.

Test Case #3 & 4

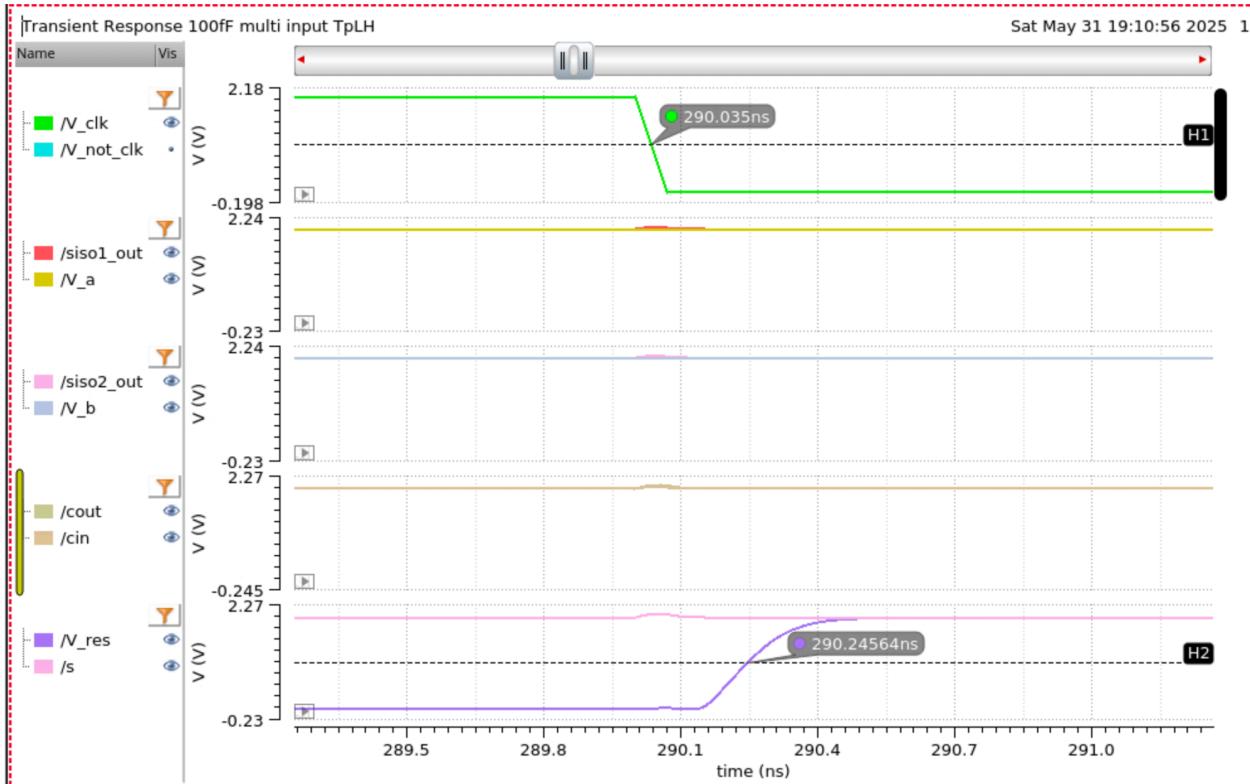
Transient simulation results for a: 1111 and b: 1111 (test case #3) and a:0000, b:0000 (test case #4) could be found below:



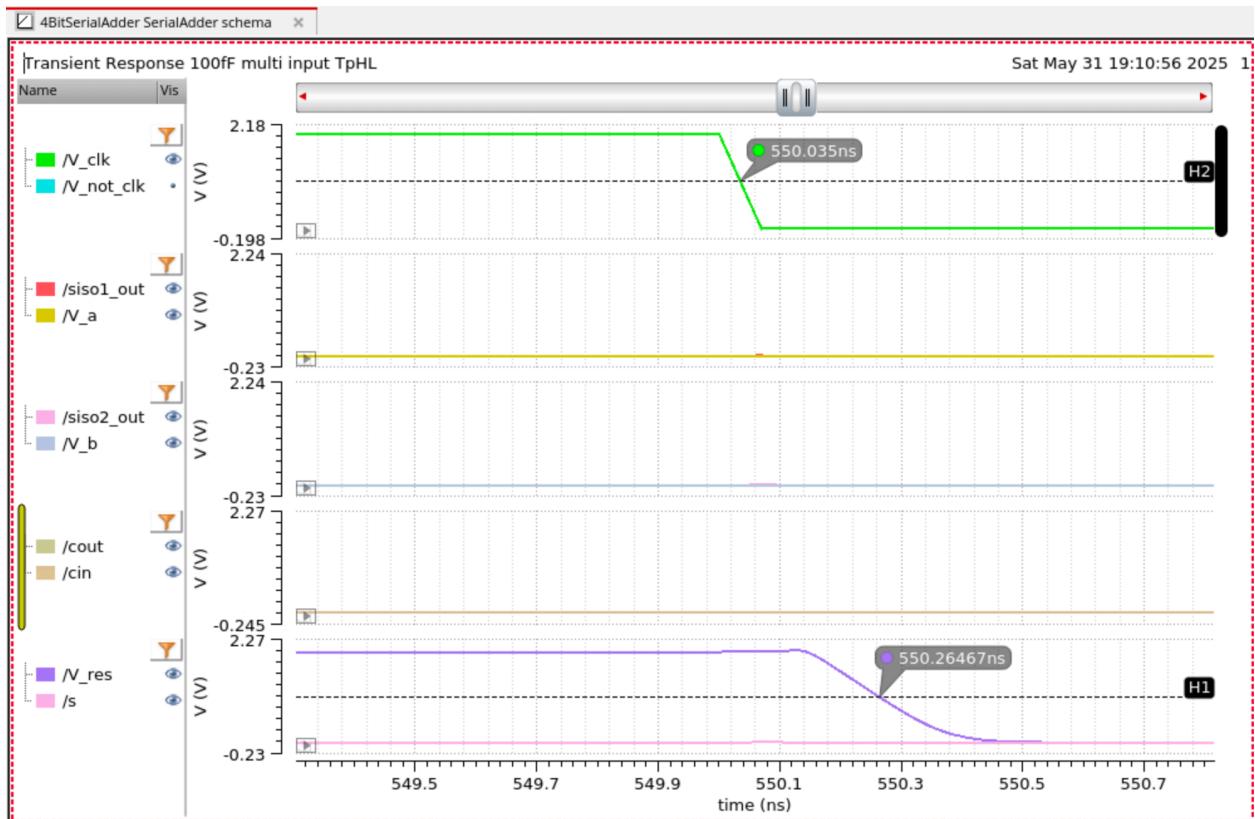
Similarly a sequence of 0s at both inputs produces changes in the outputs of the input SISOs 4 negative edges later. It takes a total of 8 negedges for a change in the input sequences to propagate to the output, which confirms that the circuit functions as specified.

Propagation Delays

Transient simulation results showing pre-layout propagation delays are provided below:



Low to high propagation delay was calculated as the time between the output passing $V_{50\%}$ and the input passing $V_{50\%}$. τ_{PLH} was measured as 210ps.

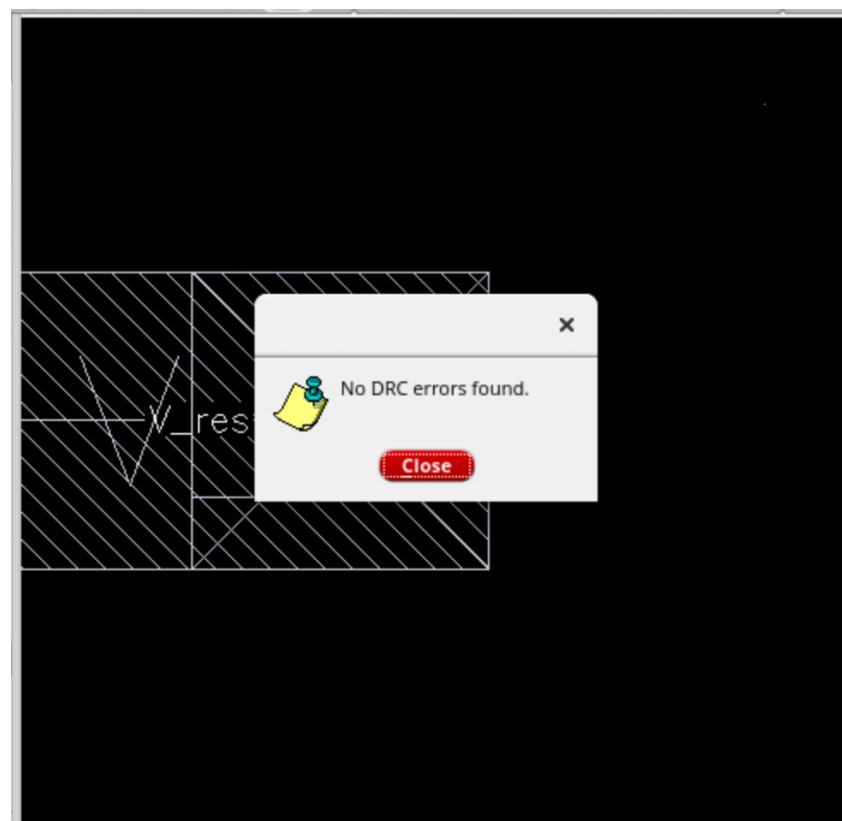
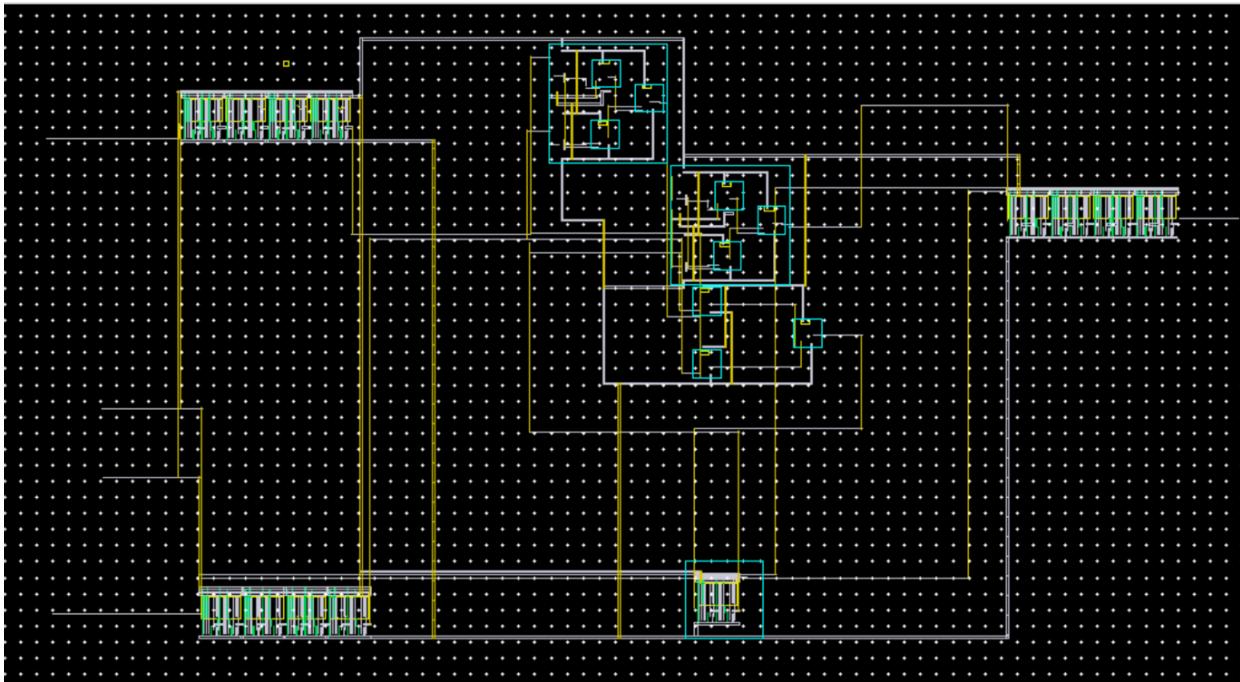


Similarly pre-layout τ_{PLH} was determined as 230ps.

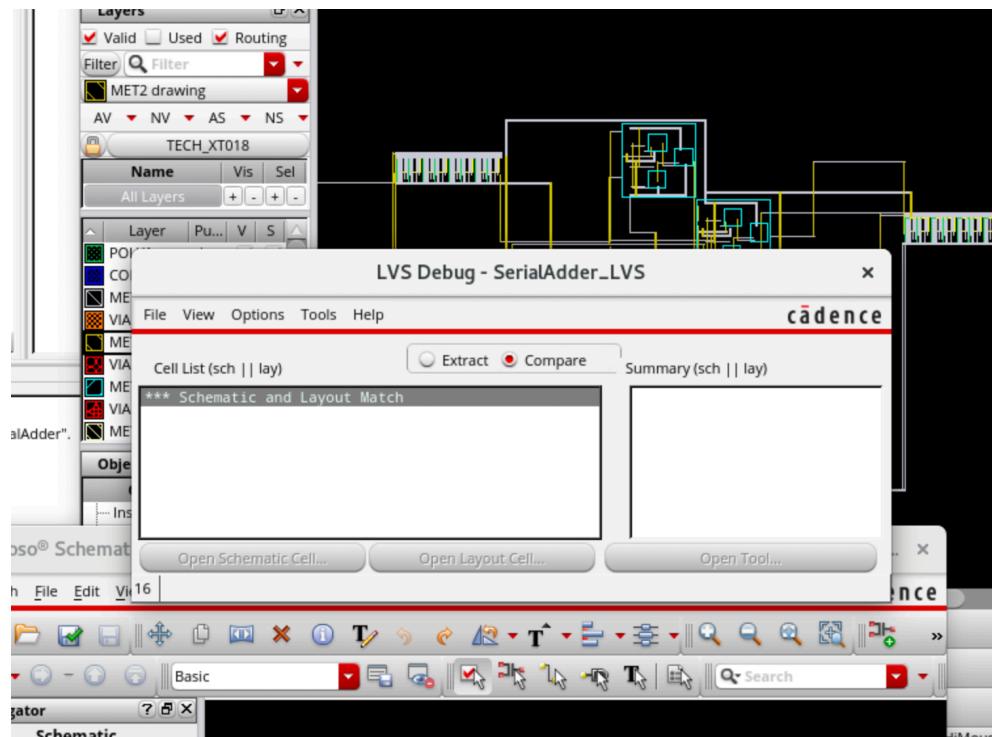
Delay Type	Delay Value
τ_{PLH} (low to high)	210ps
τ_{PHL} (high to low)	230ps

Layout & Symbol Extraction

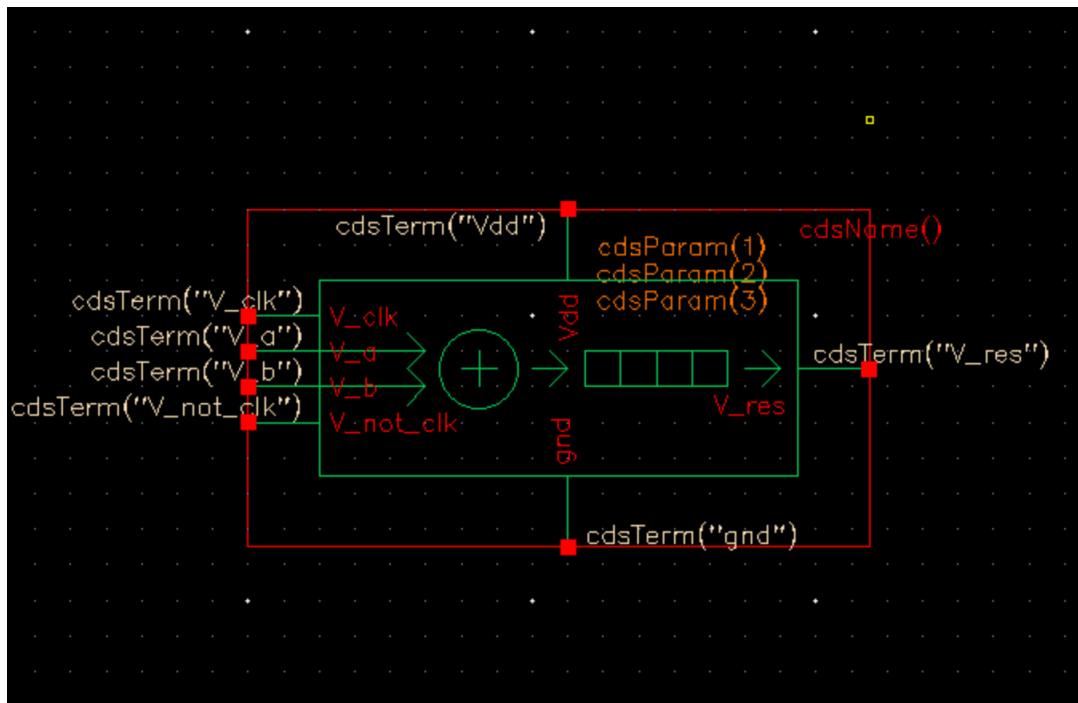
The layout of the serial adder is provided below. Due to the length of the interconnect wiring, I expect propagation delays to increase significantly post-layout.



Successful DRC check screen



Successful LVS check screen

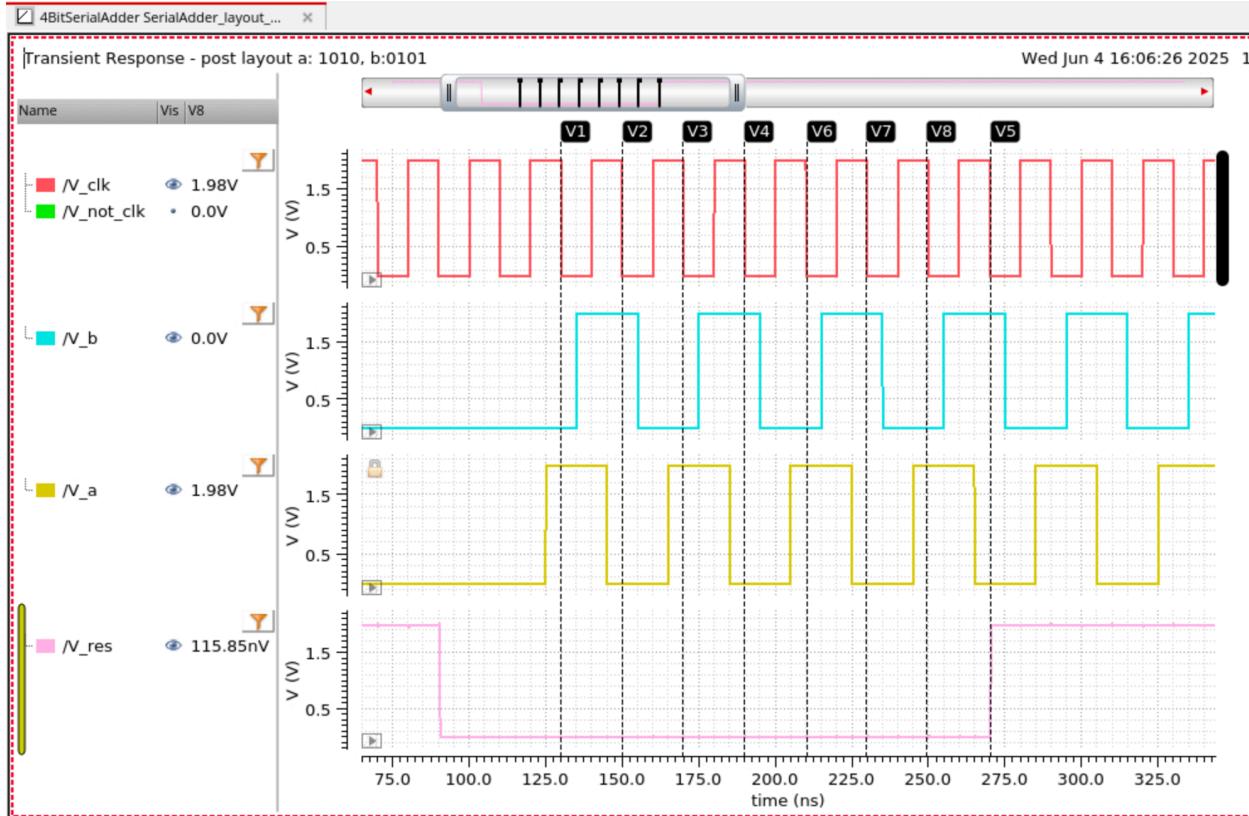


I chose the symbol to reflect the internals of the serial adder circuit. I had to remove the input SISO registers in order to limit the symbol's length.

Post-layout Transient Simulation

Test Case #1

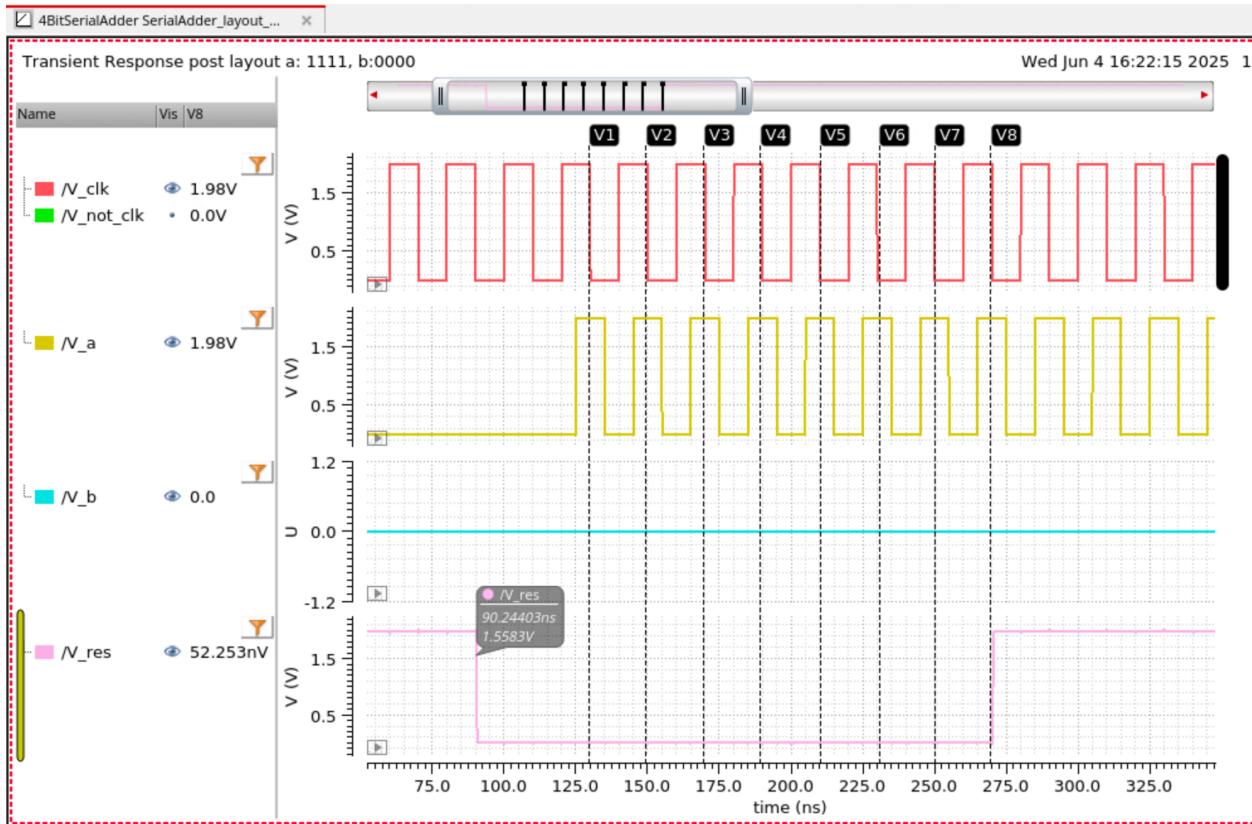
Transient simulation results for input sequences a: 1010, b:0101 are provided below:



As expected, the results of the input sequences are reflected at the output 8 negative clock edges later (4 negedges for the input SISOs, 4 negedges for the output SISOs). The output sequence 1111 is emitted for the input sequences provided which is correct.

Test Case #2

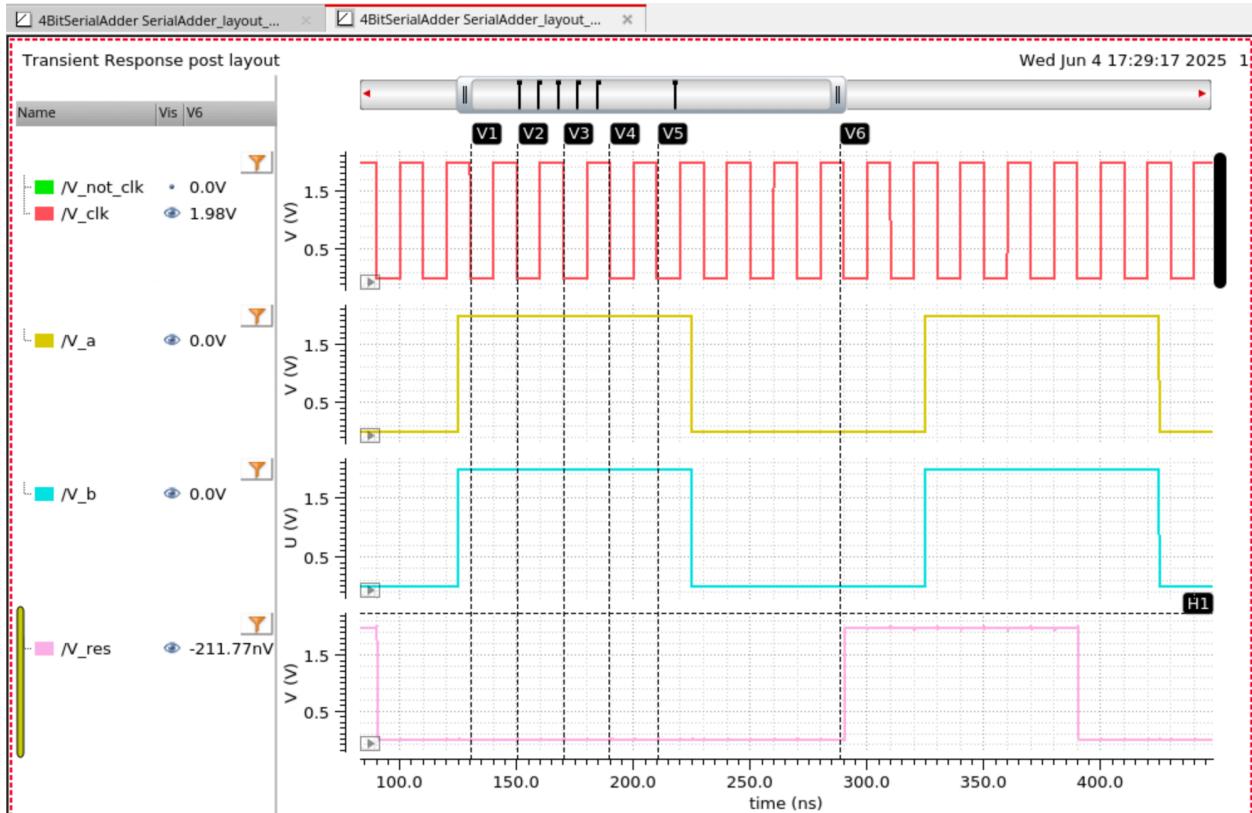
Transient simulation results for input sequences a: 1111, b:0000 are provided below:



As expected, the results of the input sequences are reflected at the output 8 negative clock edges later (4 negedges for the input SISOs, 4 negedges for the output SISOs). The output sequence 1111 is emitted for the input sequences provided which is correct.

Test Case #3 and #4

Simulation results for the input sequences a:1111, b:1111 (test case #3) followed by a:0000, b:0000 (test case #4) are provided below:

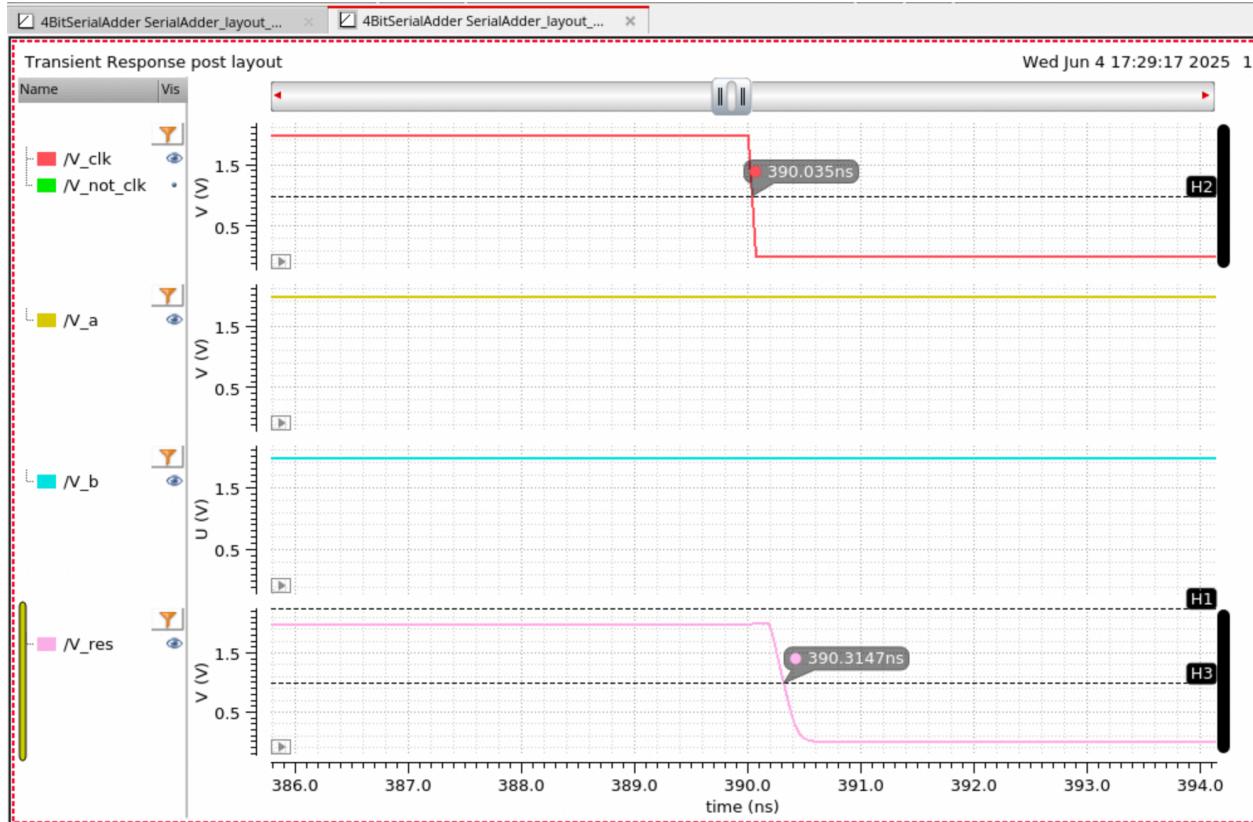


We can observe that the output produces the sequence 1111 for test case #3 exactly 8 clock cycles after the first bit of the sequence is provided. One should note that we provide 5 positive bits in the inputs before flipping them to 0 instead of 4 and count accordingly.

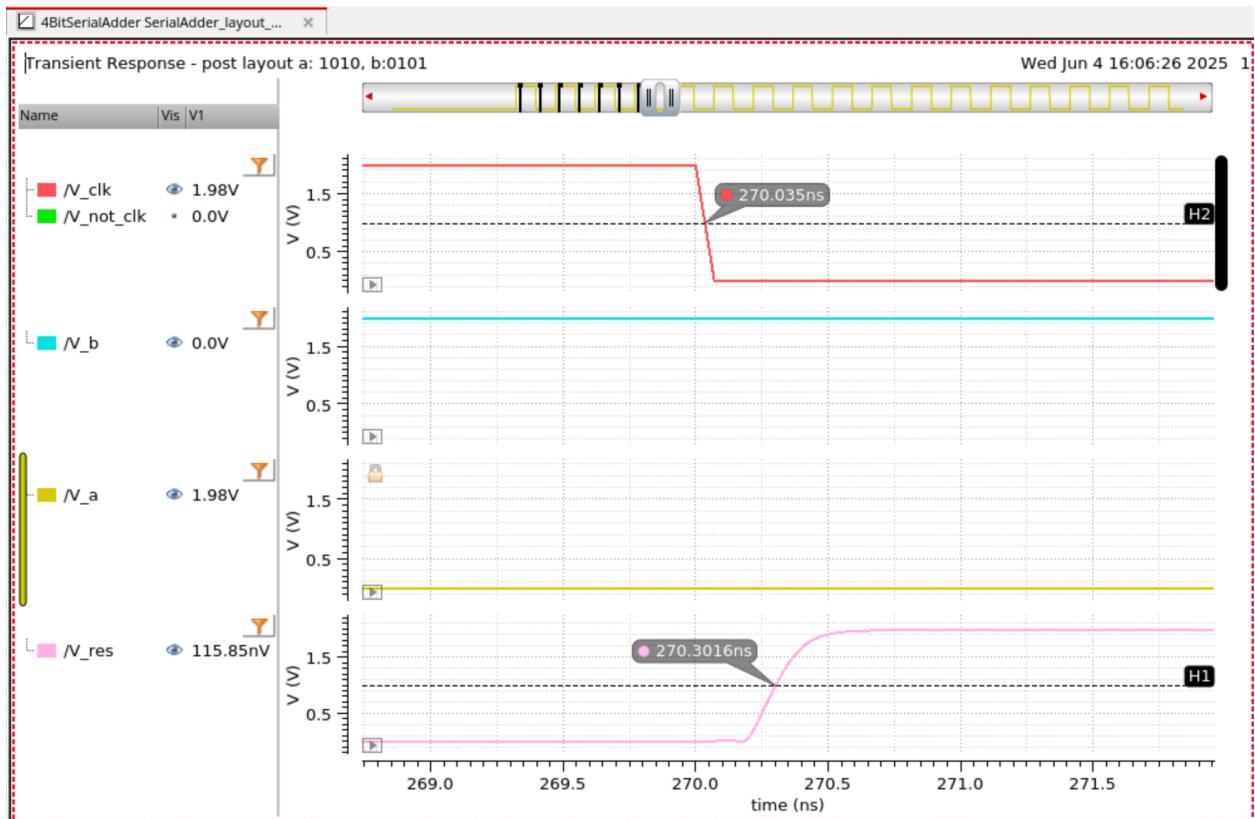
Similarly 8 clock cycles after the first 0 bit input following a series of positive inputs, we can observe that the output sequence 0000 is produced. Both test cases' results are correct.

Propagation Delays

Post layout transient simulation results are provided below:



The high to low propagation delay was measured as 280ps. Interconnection effects increased the propagation delay by 50ps which is equivalent to around 7/6 of the pre-layout simulation value.



Low to high propagation delay was measured as 267ps. We observe a 57ps increase compared to the pre-layout simulation results.

Delay Type	Delay Value
τ_{PLH} (low to high)	267ps
τ_{PHL} (high to low)	280ps