EE302 Spring 2025 Lab 2 Report

16/04/2025

Nand Gate Design

Hand Calculations

Using the equivalent inverter approach we get the formula for the threshold voltage:

$$V_{th} = \frac{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} - V_{T,p})}{1 + 2*\sqrt{\frac{k_p}{k_n}}}$$

Plugging in the parameters and solving for $\frac{k_p}{k_n}$ we get $\frac{k_p}{k_n} = 0.088$, hence $\frac{W_p}{W_n} = 0.248$. This ratio must be obtained for the NAND gate to have a V_{th} of 990mV.

We know that:

$$\frac{W_n}{L_n} = \frac{C_{load}}{\tau_{PHL} * 0.5 * \mu_n C_{ox}(V_{DD} - V_{T,n})}\left(\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right)$$

The k_n of the inverter equivalent of a NAND gate is 0.5 times the actual k_n, which we take into account when pluging values into the formula. In order to account for the variations of k_n with transistor sizing, I chose to take τ as 450ps instead of the 500 provided to us in the constraints. The formula yields: $\left(\frac{W_n}{L_n}\right)_{min} = 3.07$

Similarly evaluating:

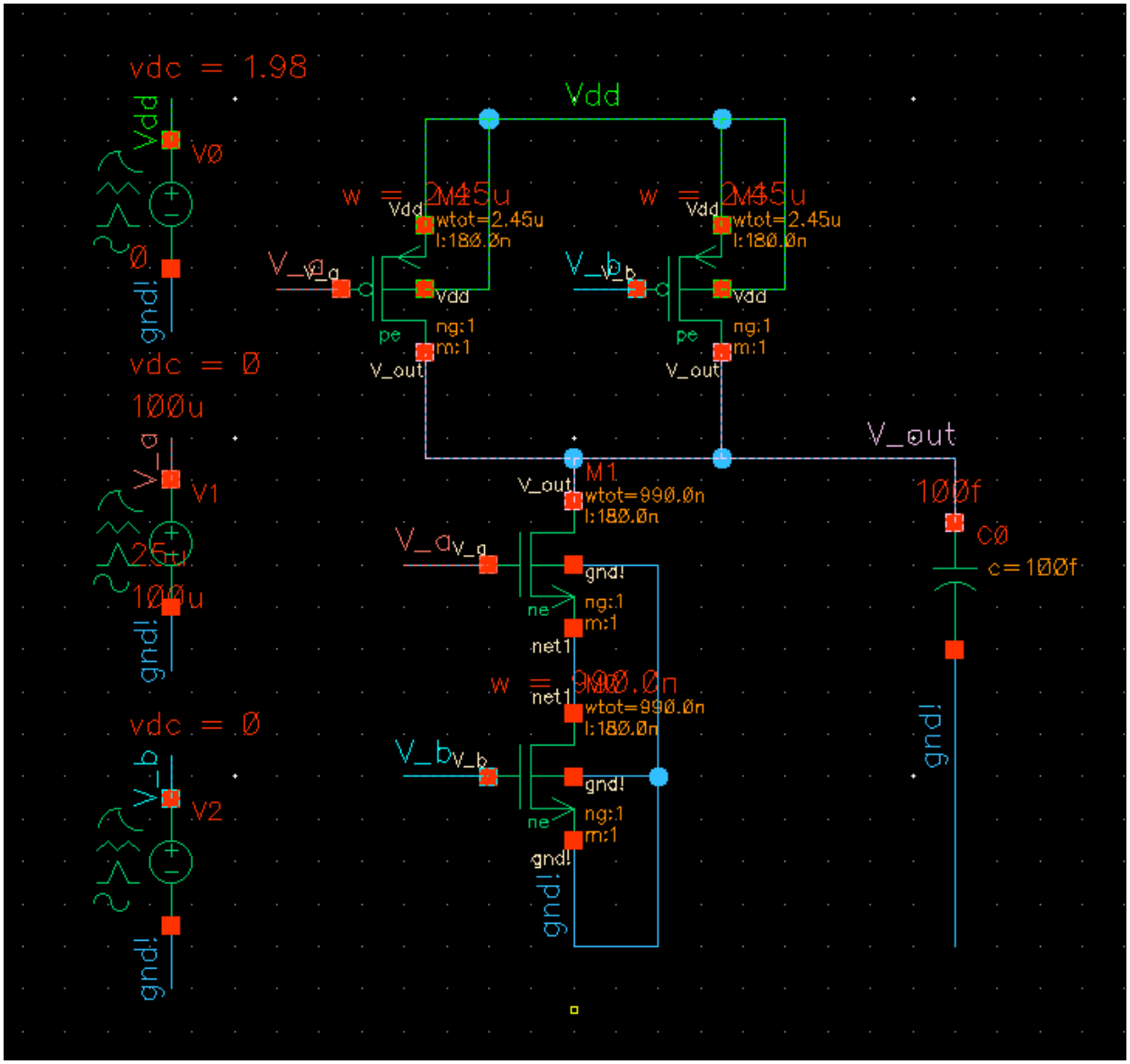
$$\frac{W_p}{L_p} = \frac{C_{load}}{\tau_{PLH} * 2 * \mu_p C_{ox}(V_{DD} - |V_{T,p}|)}\left(\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + ln\left(\frac{4(V_{DD} - |V_{T,p}|}{V_{DD}} - 1\right)\right)$$

with the new k_p value as 2 * the old k_p value (due to the equivalent inverter approach), we get $\left(\frac{W_p}{L_p}\right)_{min} = 1.363$

I began evaluating the circuit with W_n and W_p set to 990 nm and 245 nm respectively. However the circuit did not meet the V_{th} constraint which meant that further tuning would be necessary.

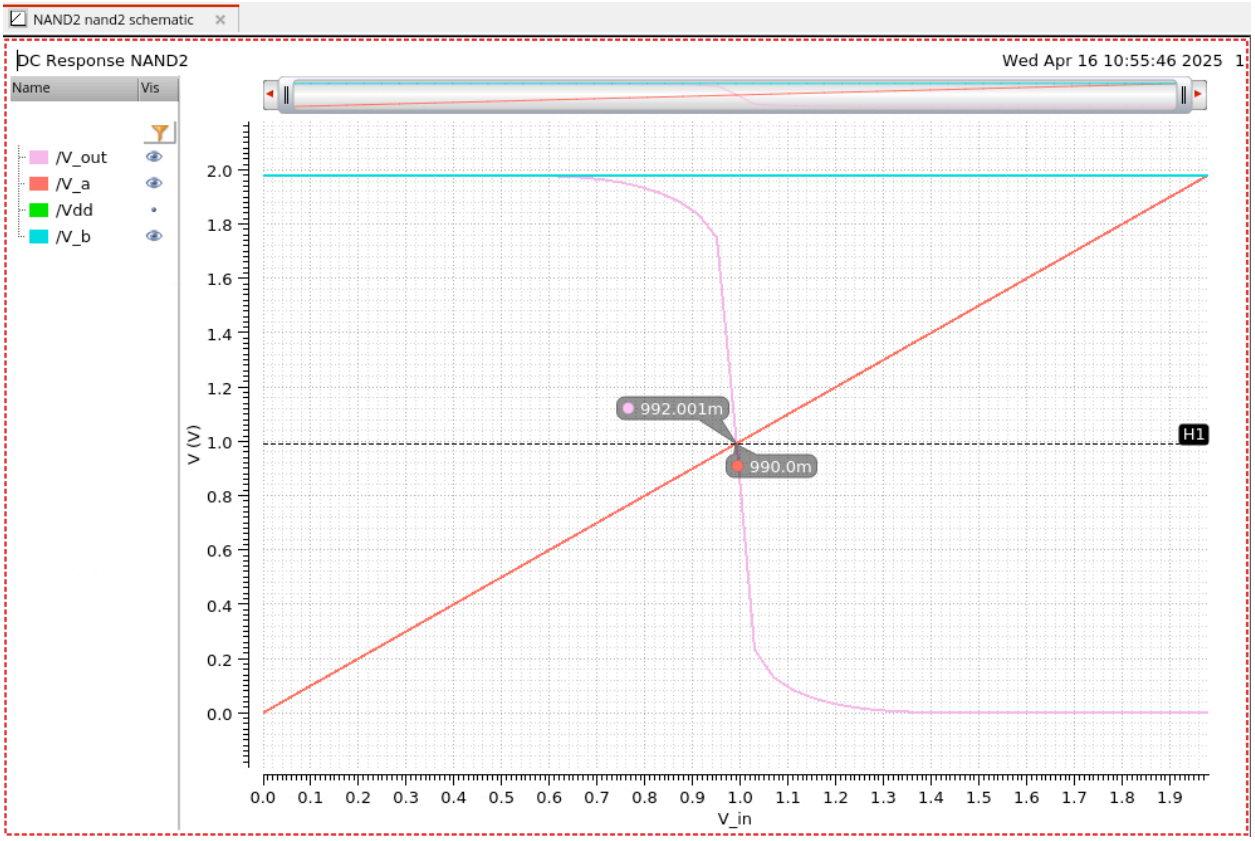
Transistor Size Tuning and Schematic

Gradually adjusting the transistor widths, I finally concluded that W_n = 990nm and W_p = 2.45um is the best setting for the transistors.



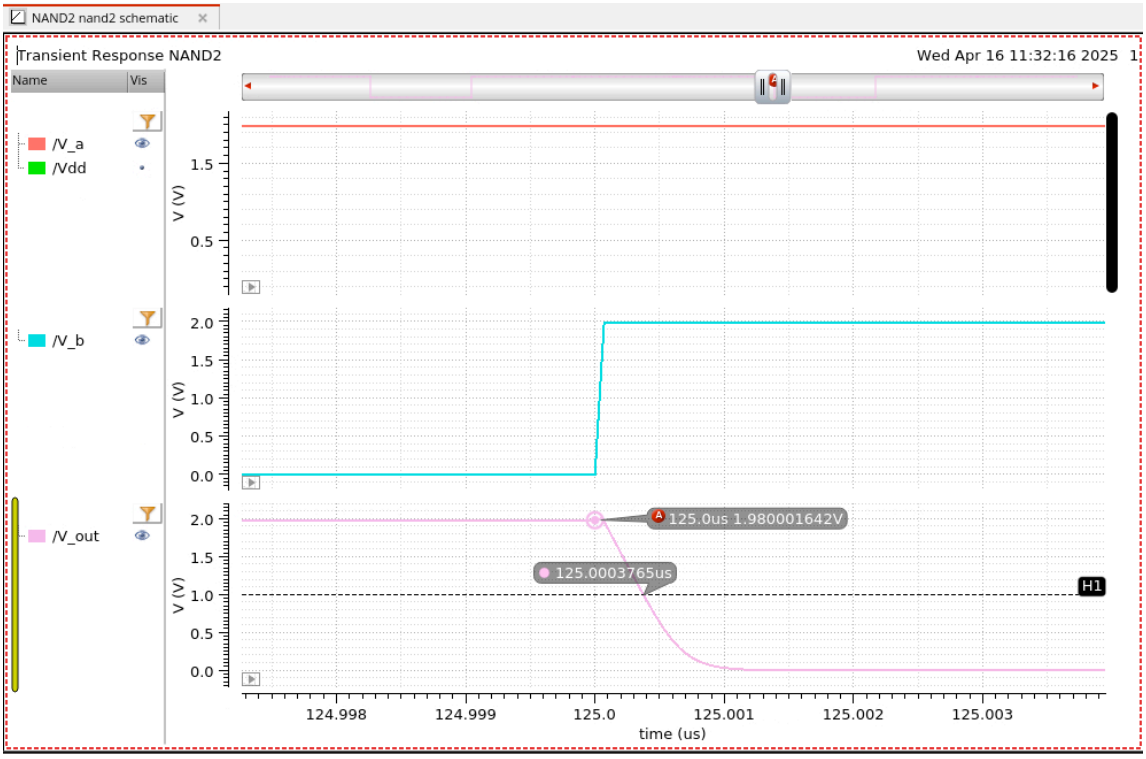
Simulation Results

VTC - DC Simulation

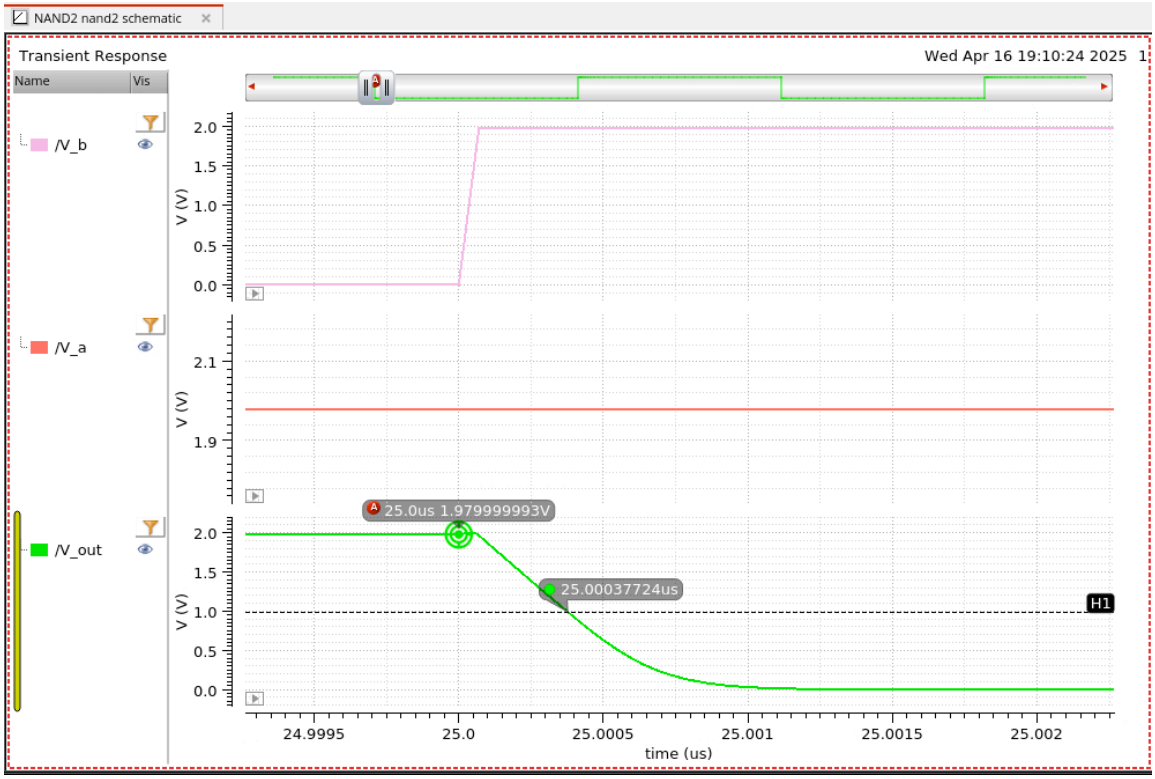


The VTC Curve for the nand gate is provided above. The threshold point is very slightly off 990mV but by a very small margin.

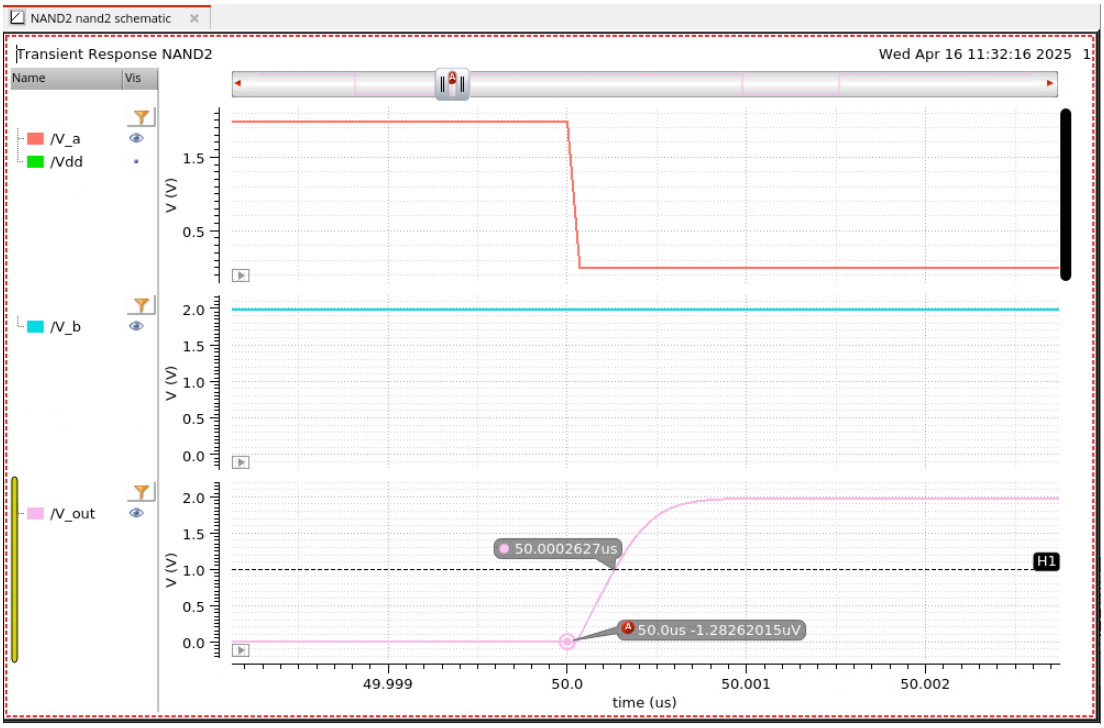
Propagation Delays - Transient Simulation



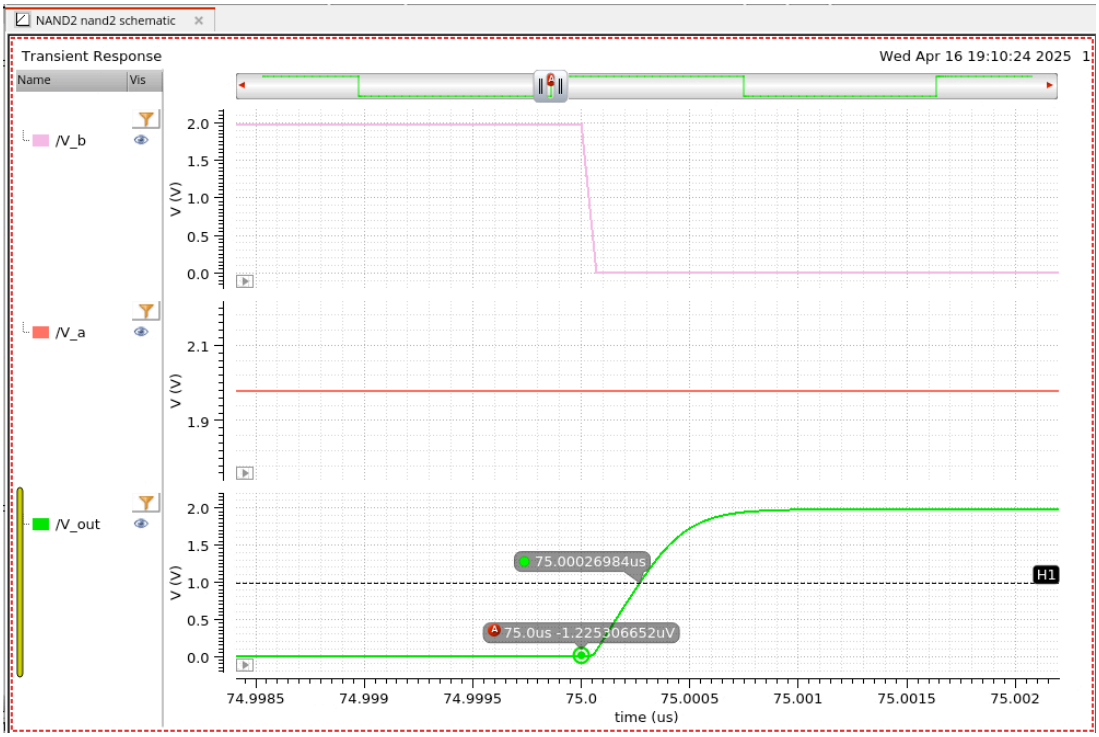
High to low propagation delay for a single changing input (input a) was found as 376.5ps



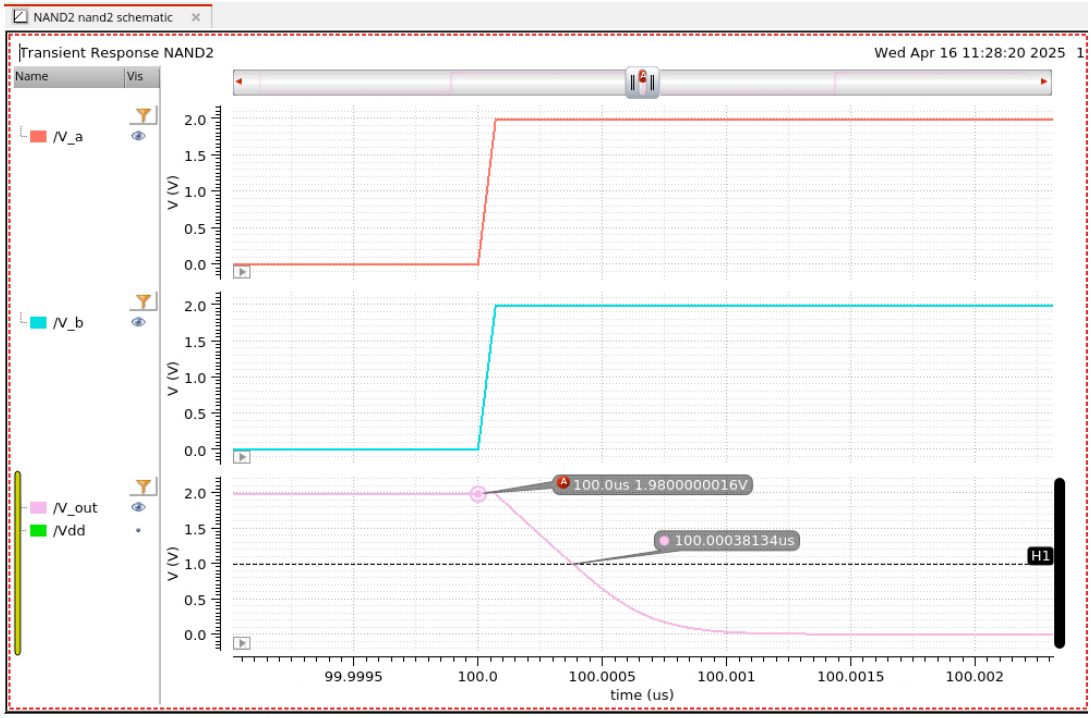
High to low propagation delay for a single changing input (input b) was found as 377.7ps



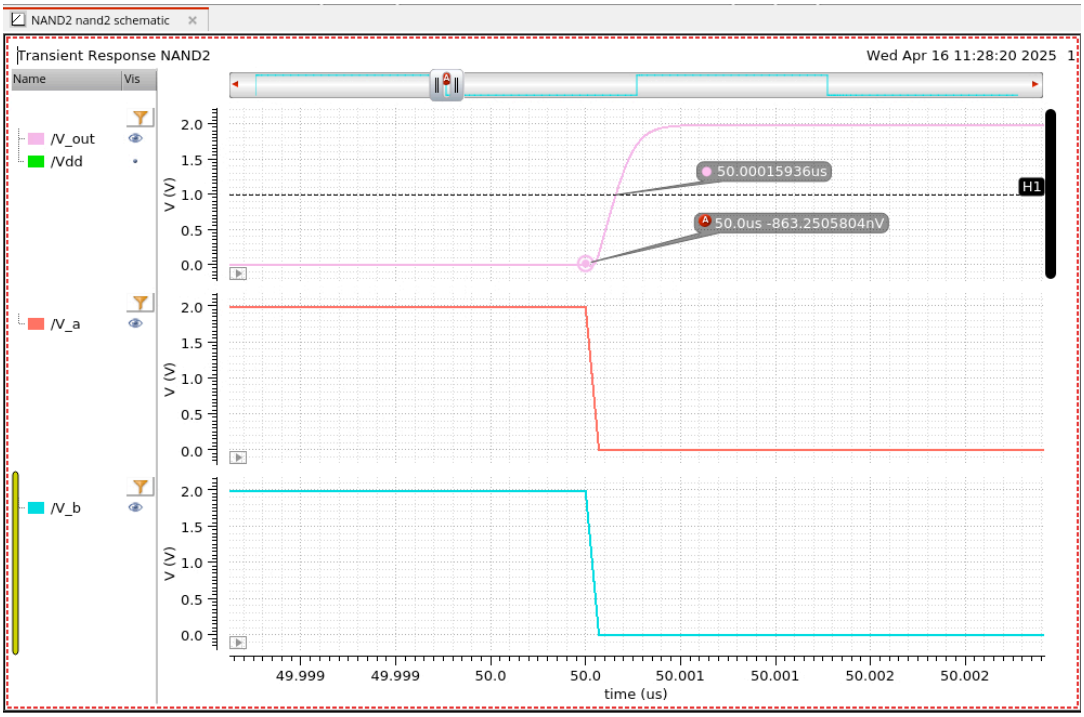
Low to high propagation delay for one changing input (input a) was found as 262.7ps.



Low to high propagation delay for one changing input (input b) was found as 269.8ps.



High to low propagation delay for two changing inputs was found as 381.3ps.

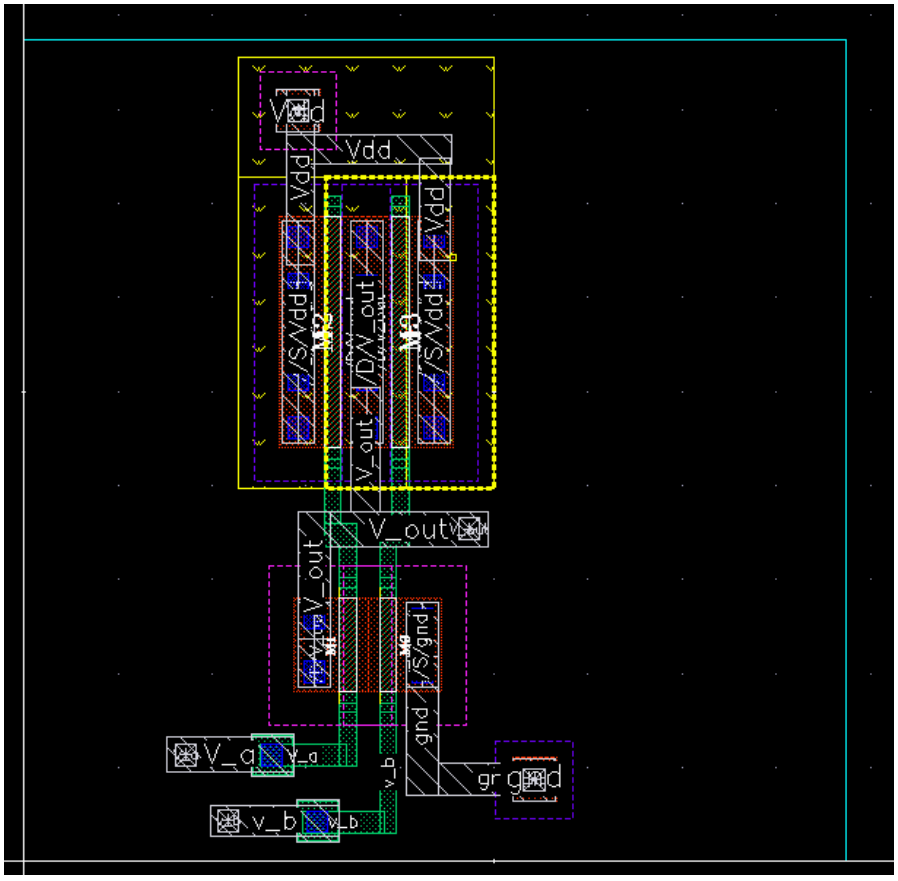


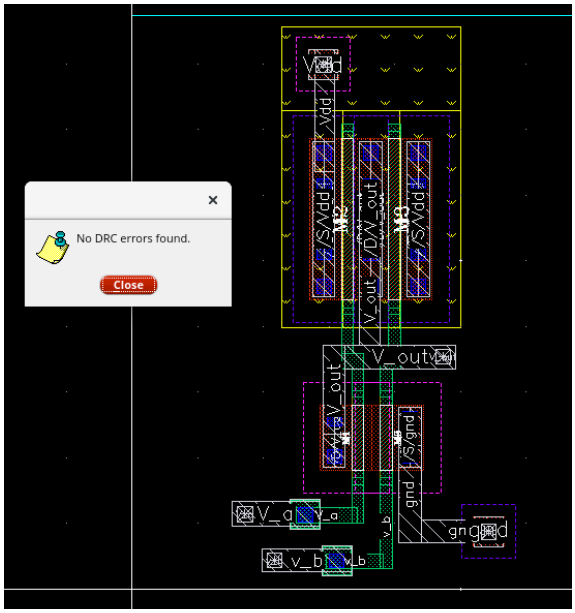
Low to high propagation delay for two changing inputs was found as 159.4ps.

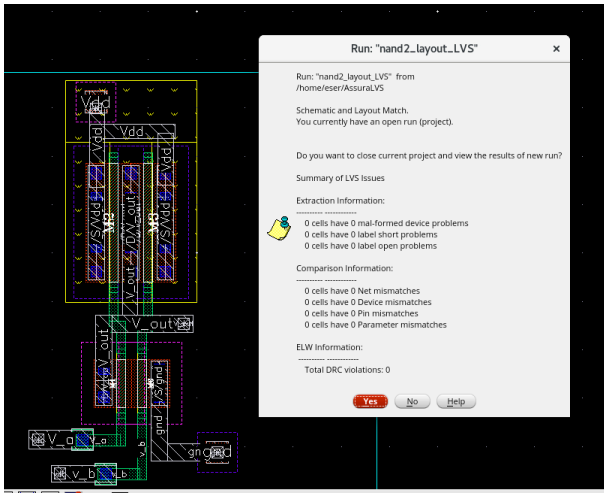
All of the propagation delay measurements above meet the design constraints. The worst case high to low propagation delay was found as 381.3ps. While the worst case low to high propagation delay was 269.8ps.

Layout

I followed the examples in the book and used overlapping transistors for the NMOS and PMOS networks. This allowed for a more compact layout.

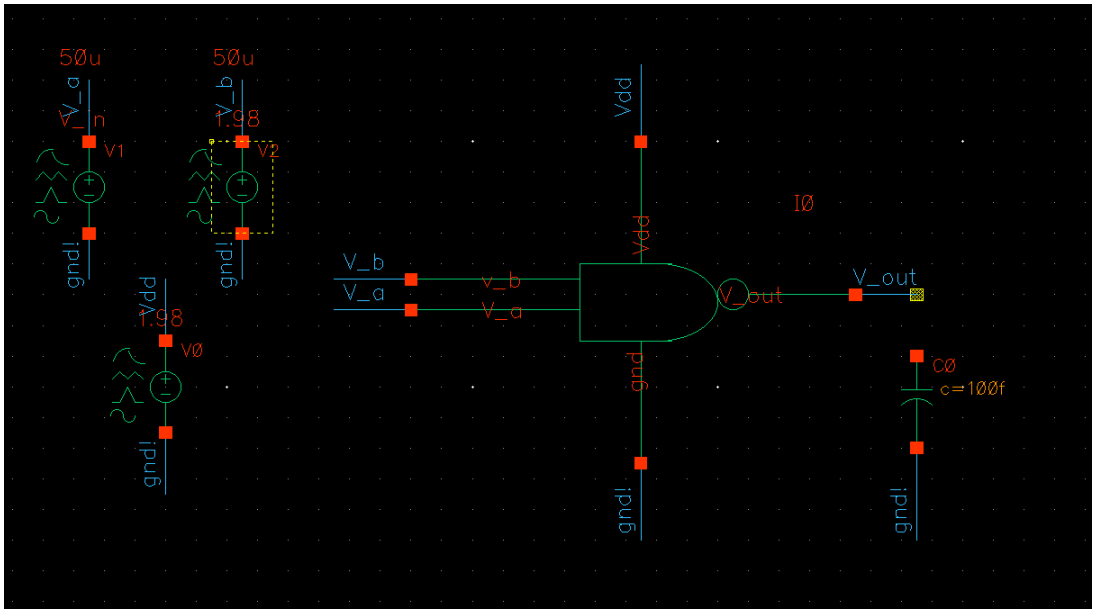




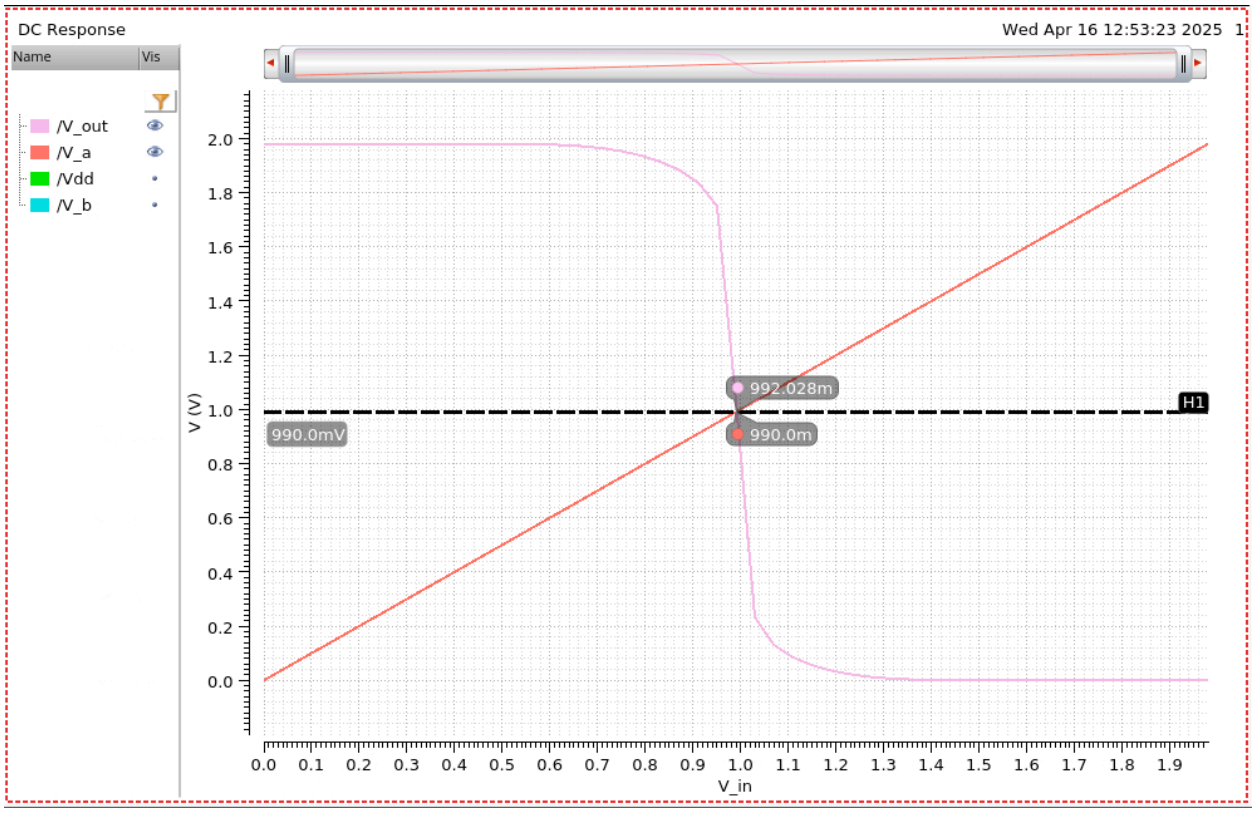


Symbol and Post-layout Simulation

Provided below is the symbol I picked for the NAND gate as well as the post layout simulation setup.

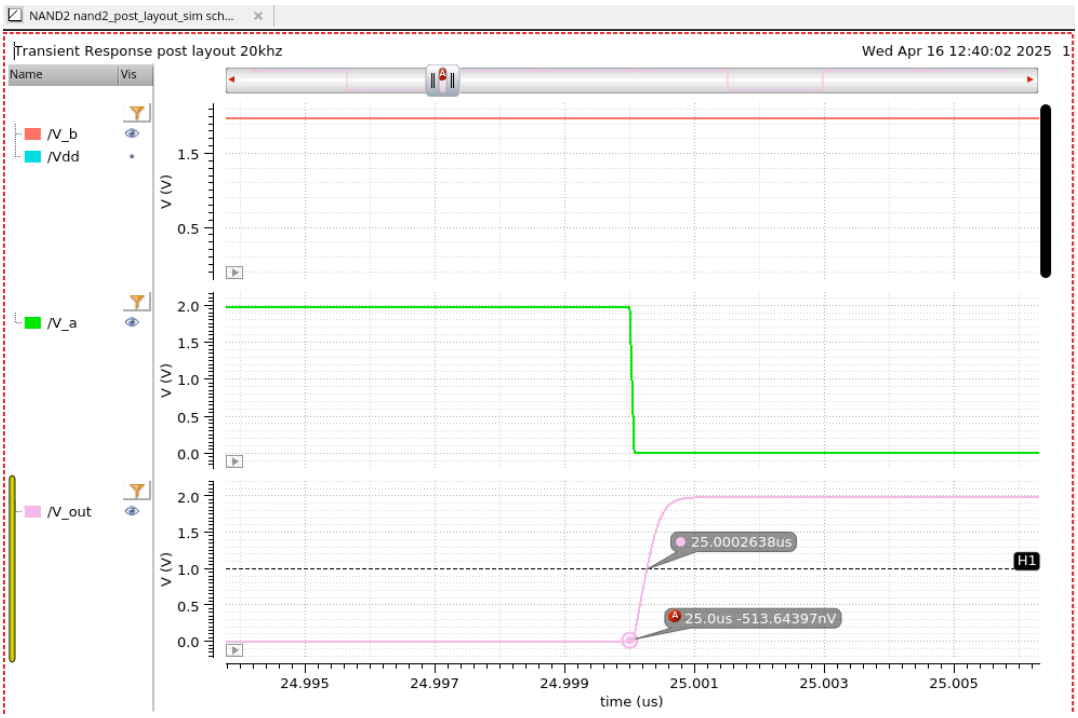


VTC - DC Simulation

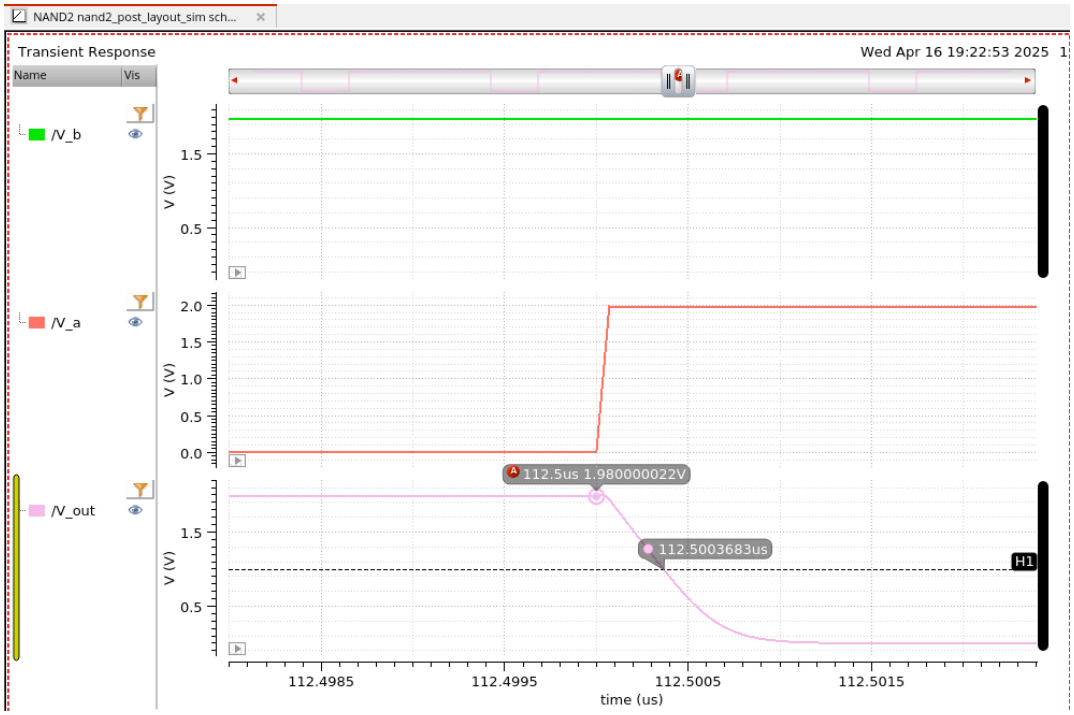


The post layout VTC is identical to the pre-layout VTC apart from a small error margin. The discrepancy between 990mV and the actual threshold voltage is still negligible.

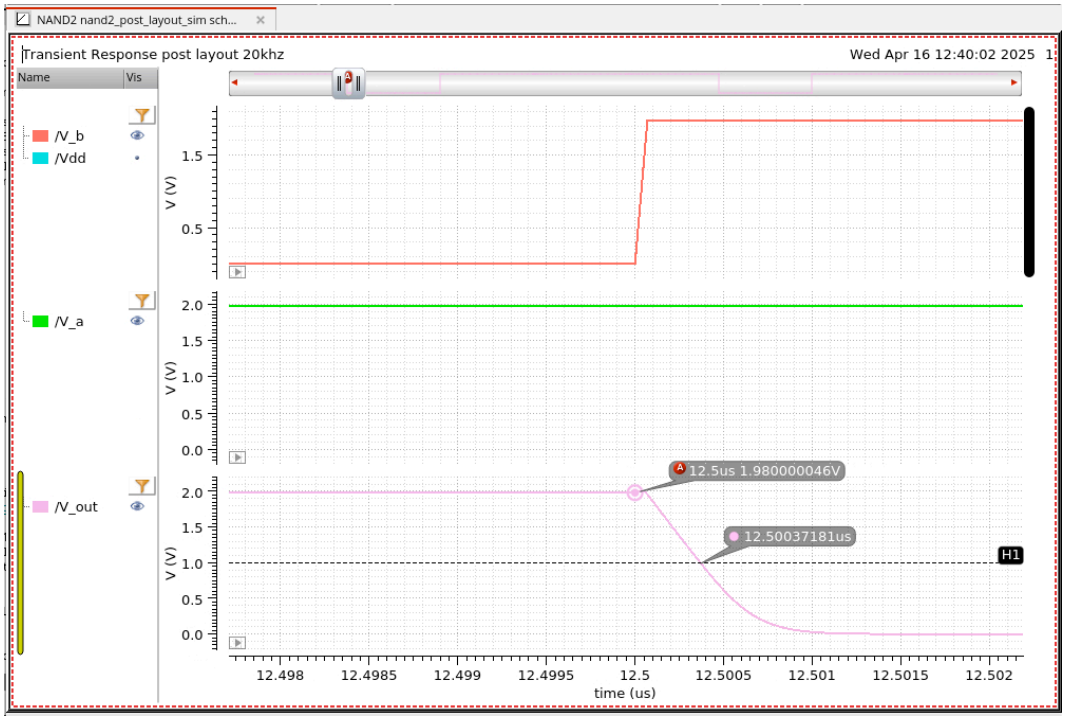
Propagation Delays - Transient Simulation



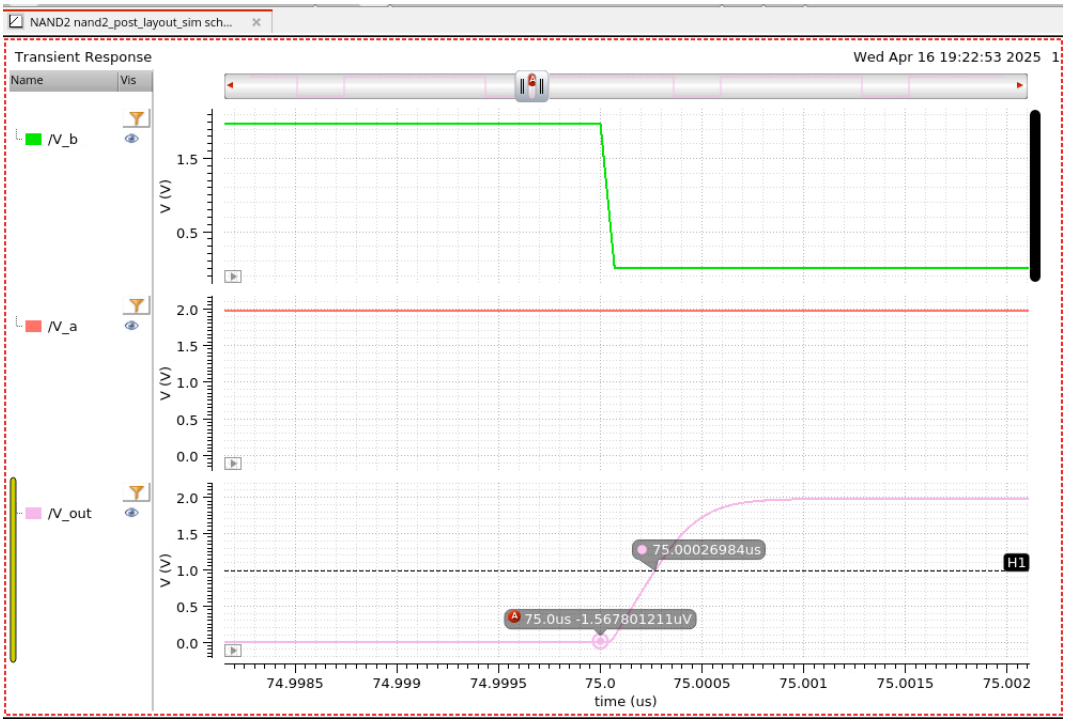
Low to high propagation delay for changing input a was found as 263.8ps



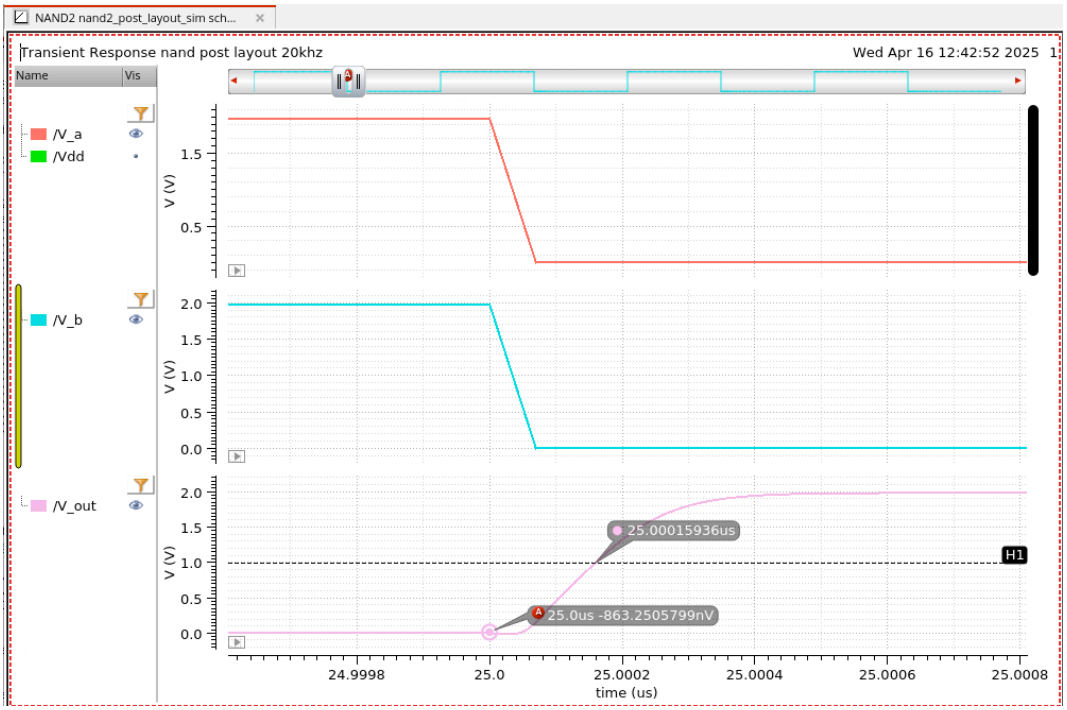
High to low propagation delay for changing input a was found as 368.ps



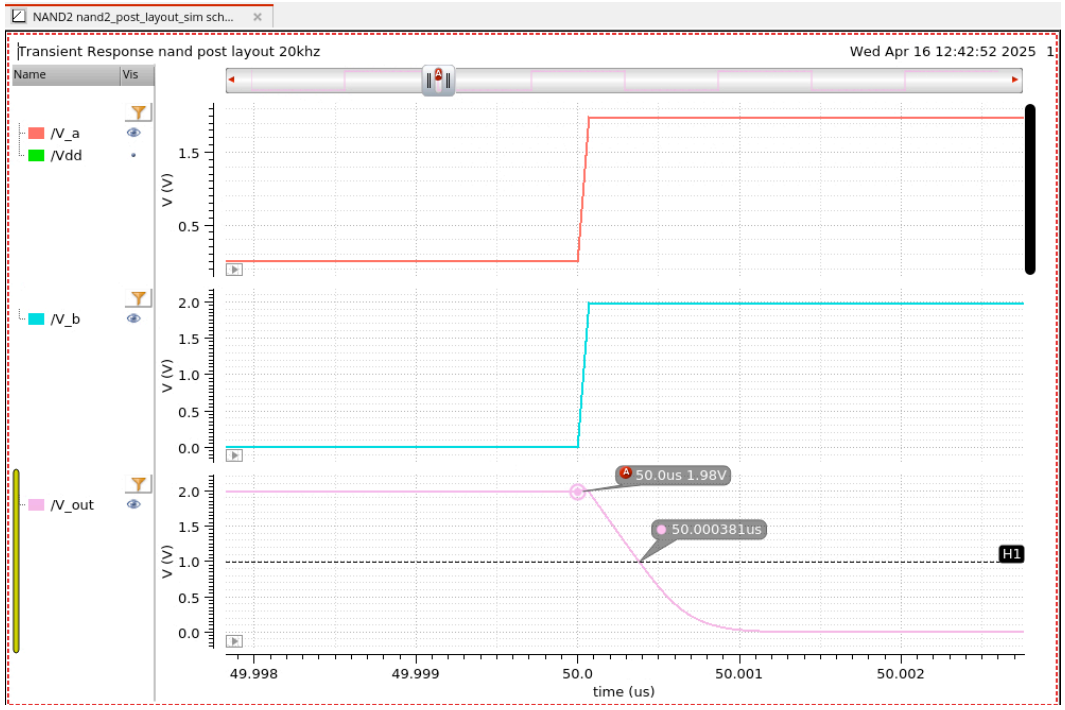
High to low propagation delay for changing input b was found as 371.8ps



Low to high propagation delay for changing input b was found as 269.8ps



Low to high propagation delay for both inputs changing was found as 159.4ps



High to low propagation delay for both inputs changing was found as 381ps

The worst case high to low propagation delay was determined as 381ps for both rising inputs. Worst case low to high propagation delay was determined as 269.8ps for falling input b. All propagation delays are within the tolerable

Nor Gate Design

Hand Calculations

Using the equivalent inverter approach we get the formula for the threshold voltage:

$$V_{th} = \frac{V_{T,n} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}(V_{DD} - V_{T,p})}{1 + \frac{1}{2} * \sqrt{\frac{k_p}{k_n}}}$$

Plugging in the parameters and solving for $\frac{k_p}{k_n}$ we get $\frac{k_p}{k_n} = 0.088$, hence $\frac{W_p}{W_n} = 3.98$. This ratio must be obtained for the NOR gate to have a V_{th} of 990mV.

We know that:

$$\frac{W_n}{L_n} = \frac{C_{load}}{\tau_{PHL} * 2 * \mu_n C_{ox}(V_{DD} - V_{T,n})} \left(\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right)$$

The k_n of the inverter equivalent of a NAND gate is 2 times the actual k_n, which we take into account when pluging values into the formula. In order to account for the variations of k_n with transistor sizing, I chose to take τ as 450ps instead of the 500 provided to us in the constraints. The formula yields: $\left(\frac{W_n}{L_n}\right)_{min} = 0.614$

Similarly evaluating:

$$\frac{W_p}{L_p} = \frac{C_{load}}{\tau_{PLH} * 0.5 * \mu_p C_{ox}(V_{DD} - |V_{T,p}|)} \left(\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + ln\left(\frac{4(V_{DD} - |V_{T,p}|}{V_{DD}} - 1\right)\right)$$

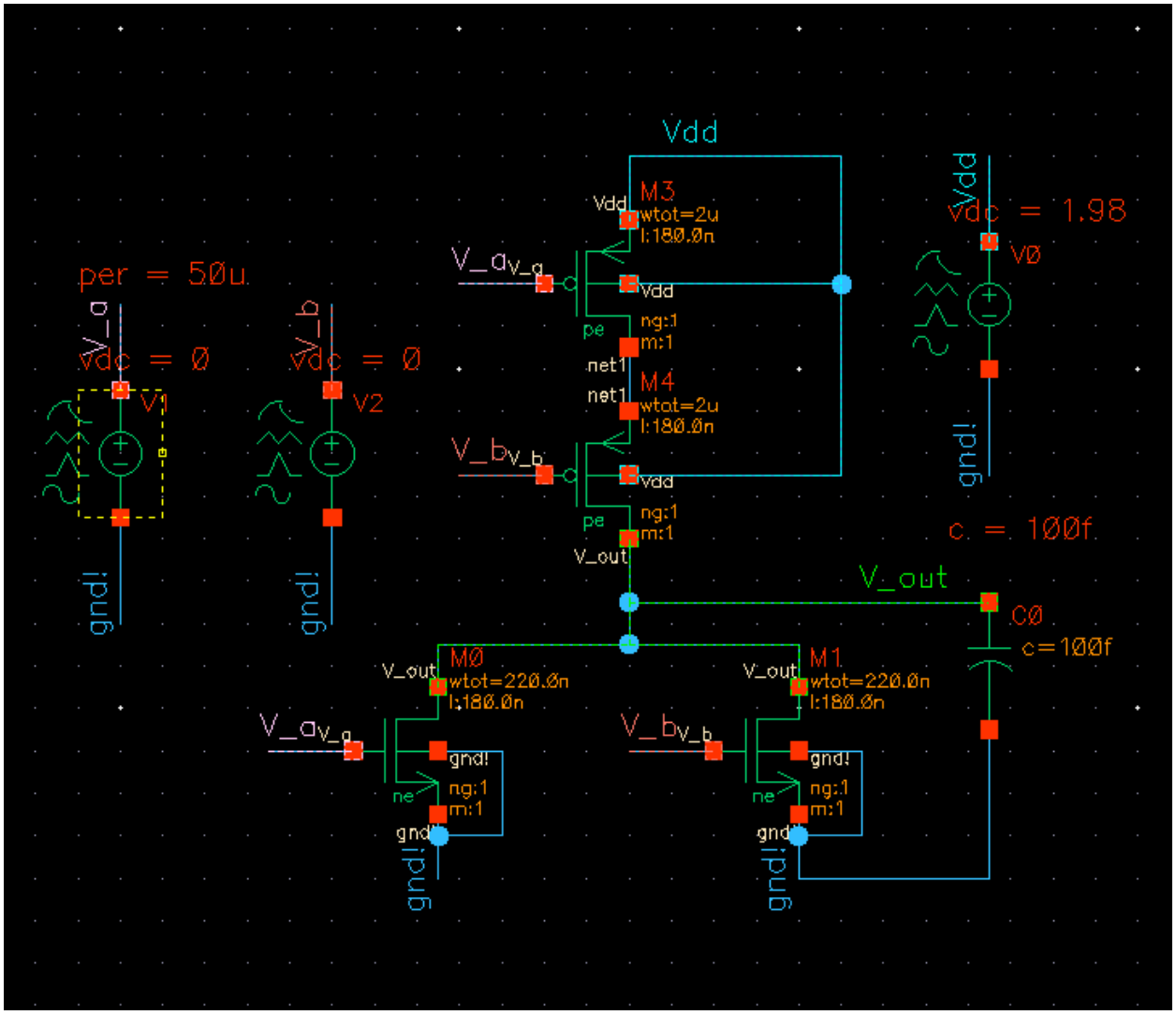
with the new k_p value as 0.5 times the old k_p value (due to the equivalent inverter approach), we get $\left(\frac{W_p}{L_p}\right)_{min} = 4.91$

I began evaluating the circuit with W_n and W_p set to 900 nm and 220 nm respectively. However the circuit did not meet the V_{th} constraint which meant that further tuning would be necessary.

Transistor Size Tuning and Schematic

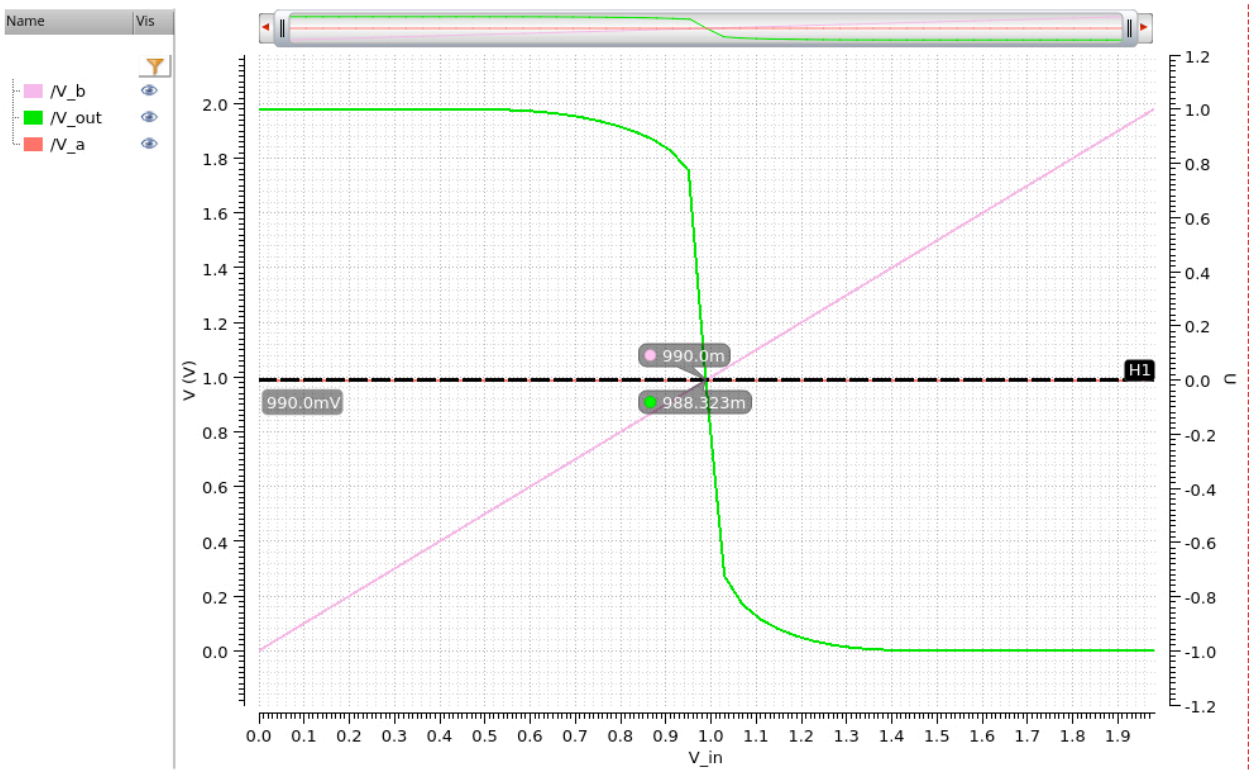
Gradually adjusting the transistor widths, I finally concluded that W_n = 220nm and W_p = 2um is the best setting for the transistors. The NOR gate, while demonstrating adequately fast

propagation delays, fails to meet the propagation delay constraints for two specific switching cases (listed in the simulations section).



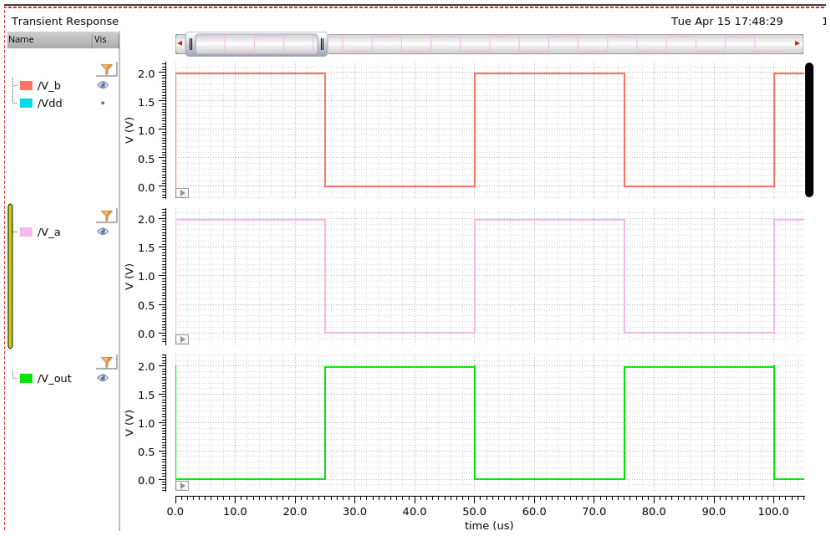
Simulation Results

VTC - DC Simulation Results

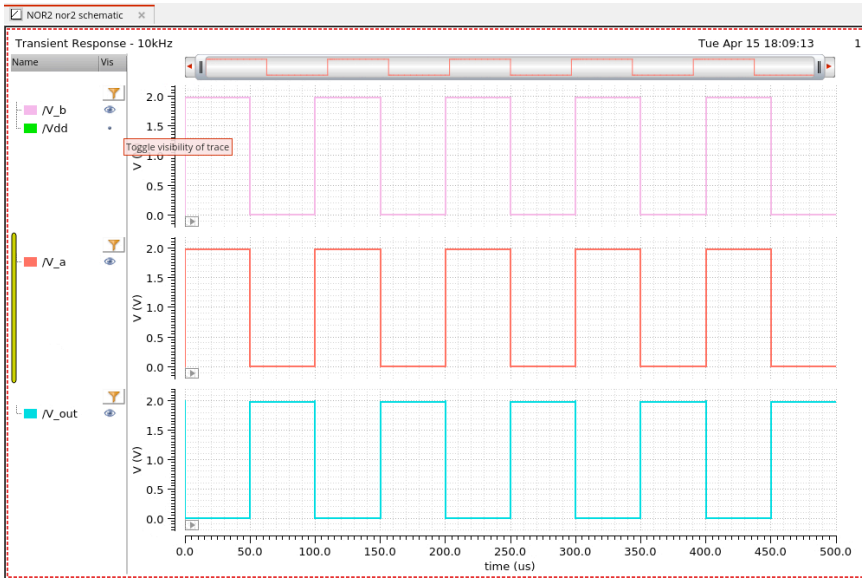


The threshold voltage shows only a slight difference between the ideal value of 990mV with the output voltage being equal to 990mV at input voltage equals 988.3mV on the equivalent inverter.

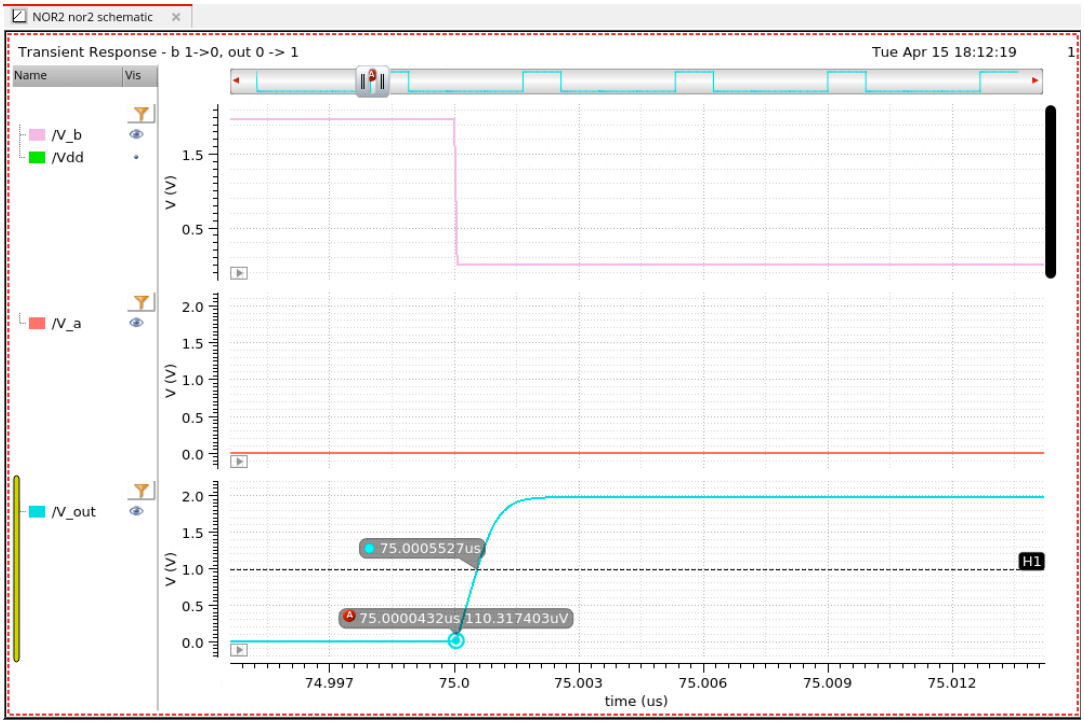
Propagation Delays - Transient Simulation



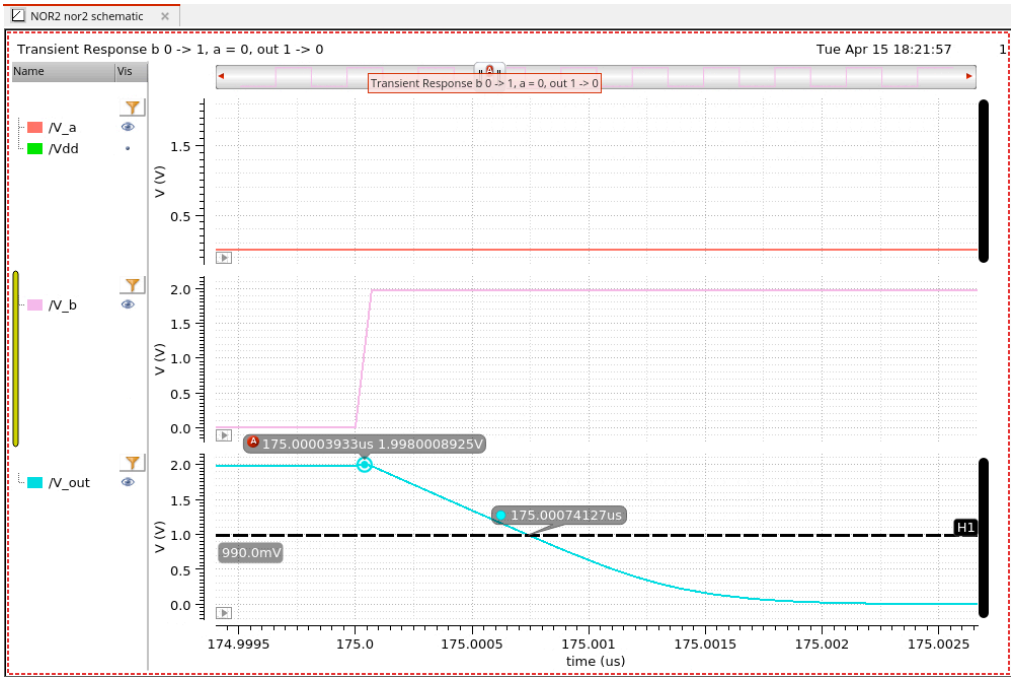
Transient simulation with two 20khz inputs



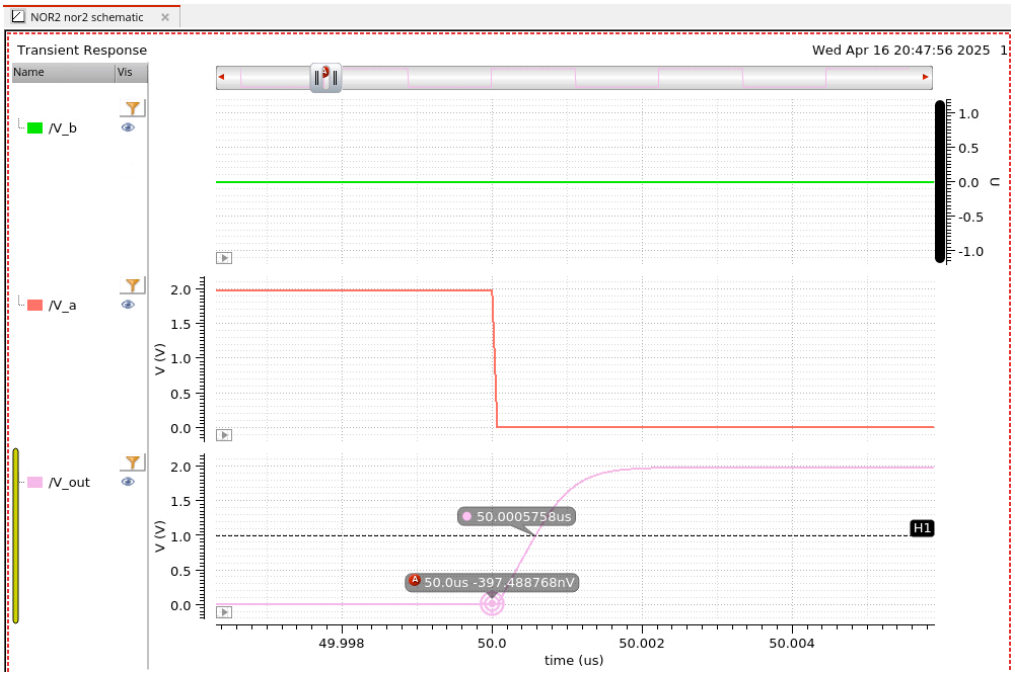
Transient simulation with two 10khz inputs



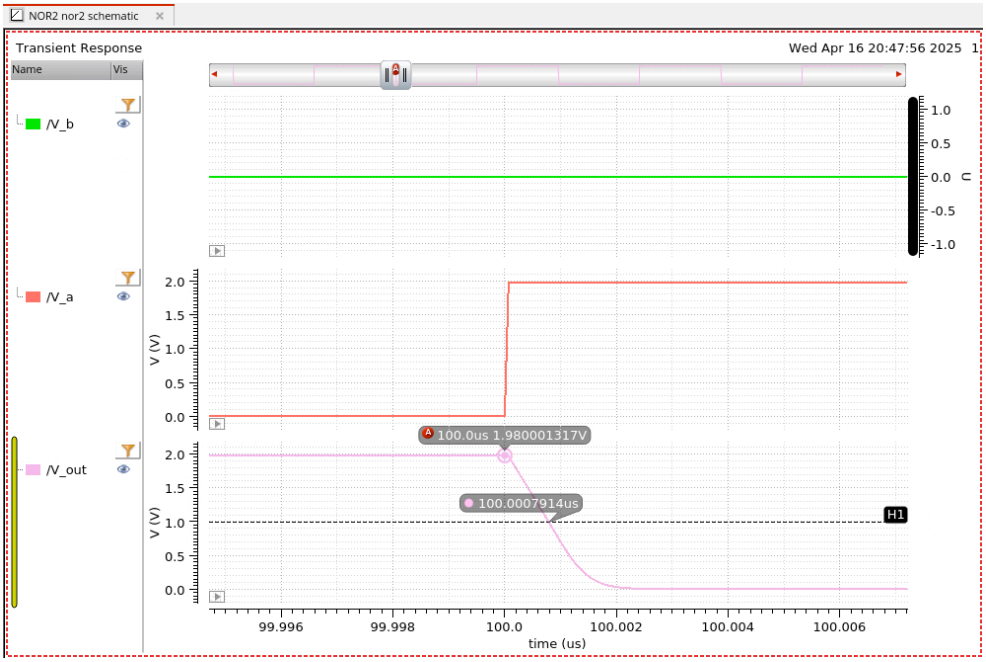
Low to high propagation delay for falling input b was found as 553ps.



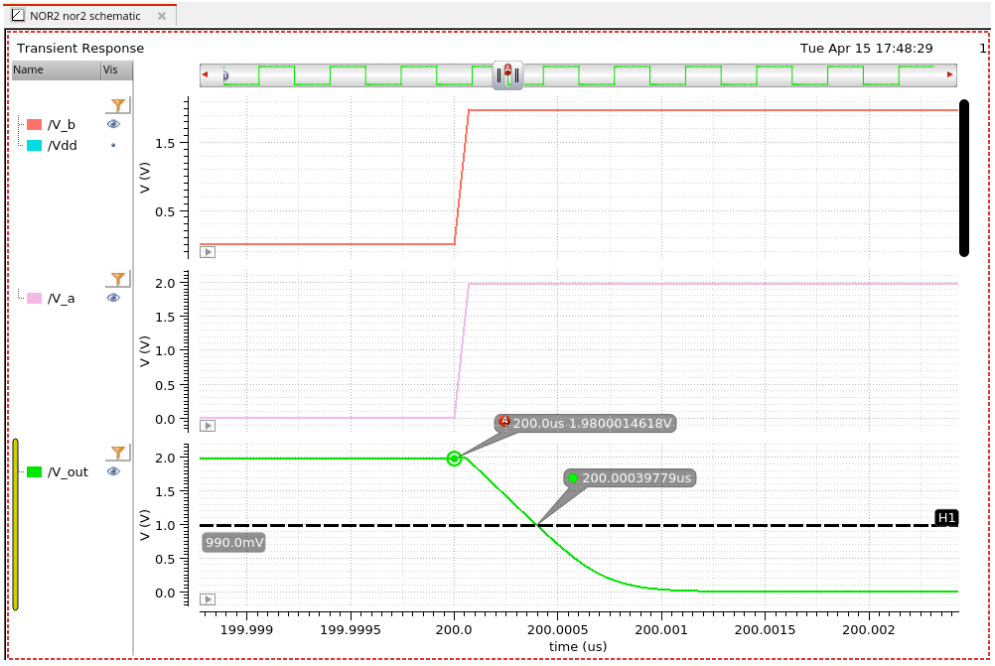
High to low propagation delay for rising input b was found as 741.3ps which fails the design constraints.



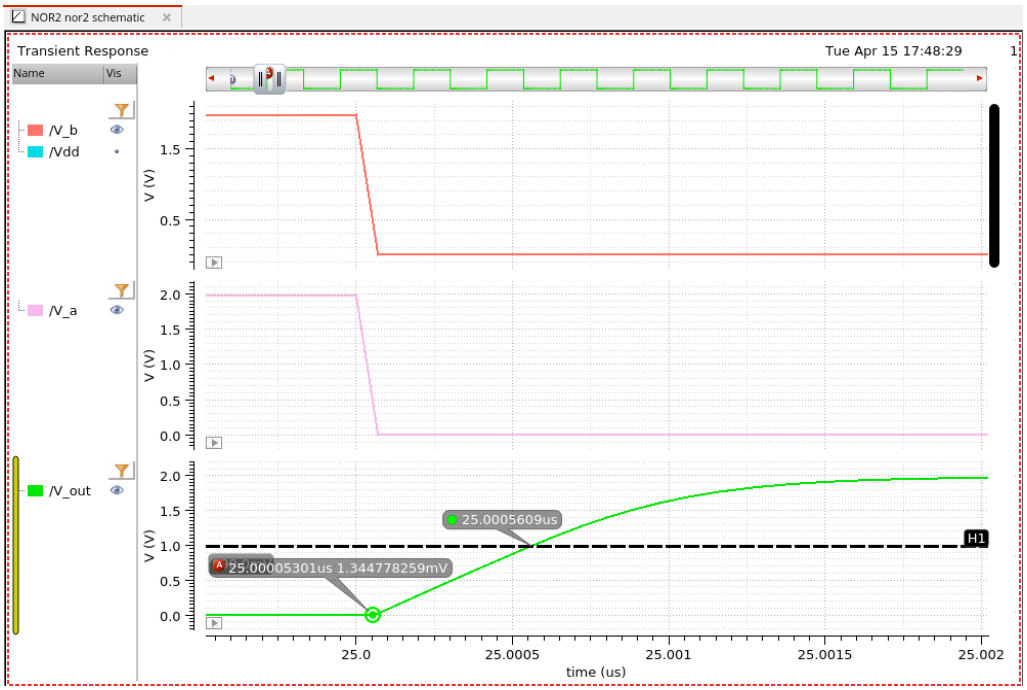
Low to high propagation delay for falling input a was found as 575ps which is slightly above the delay specified by the delay constraints.



High to low propagation delay for rising input a was found as 791.4ps which fails the design constraints.

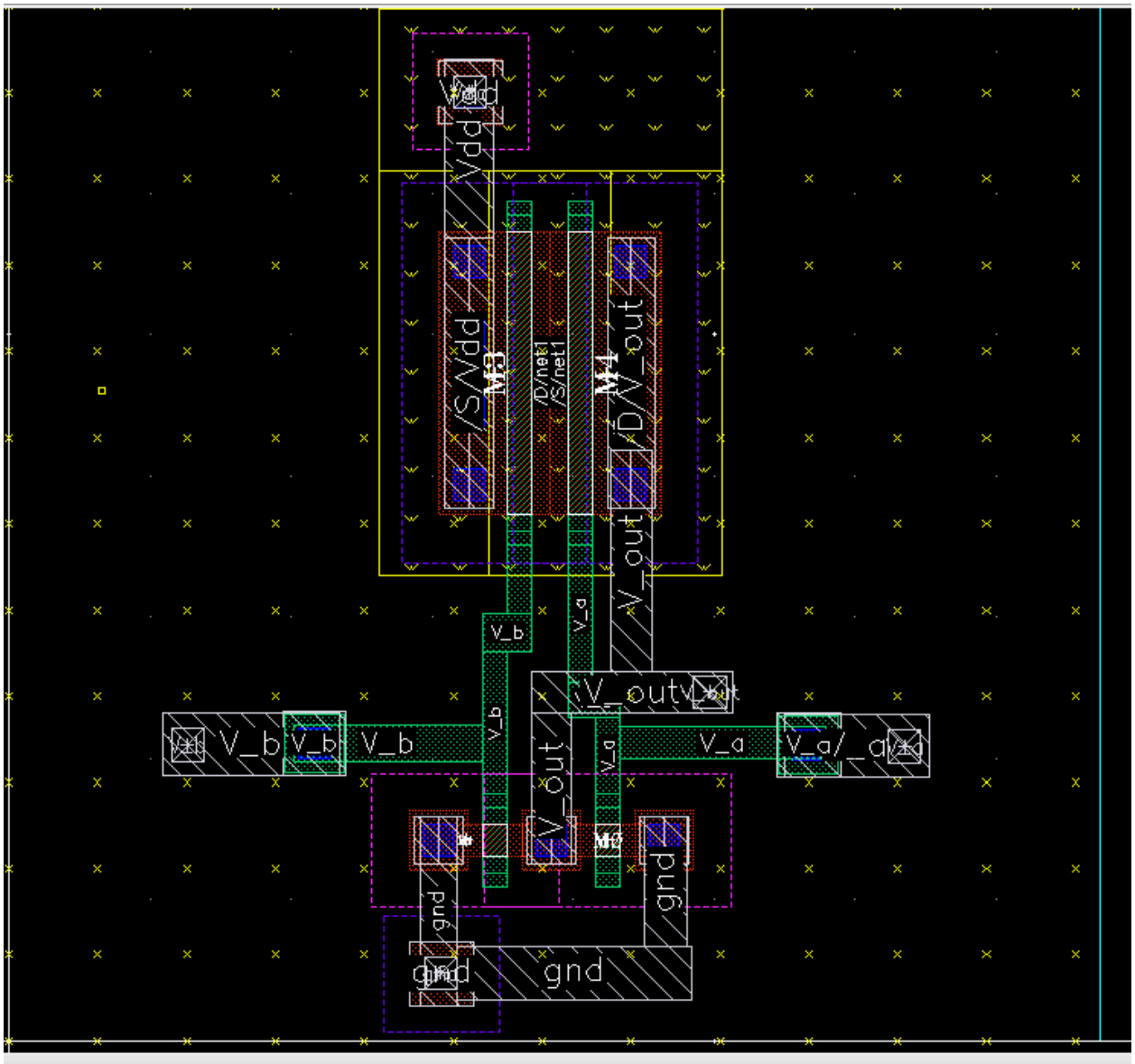


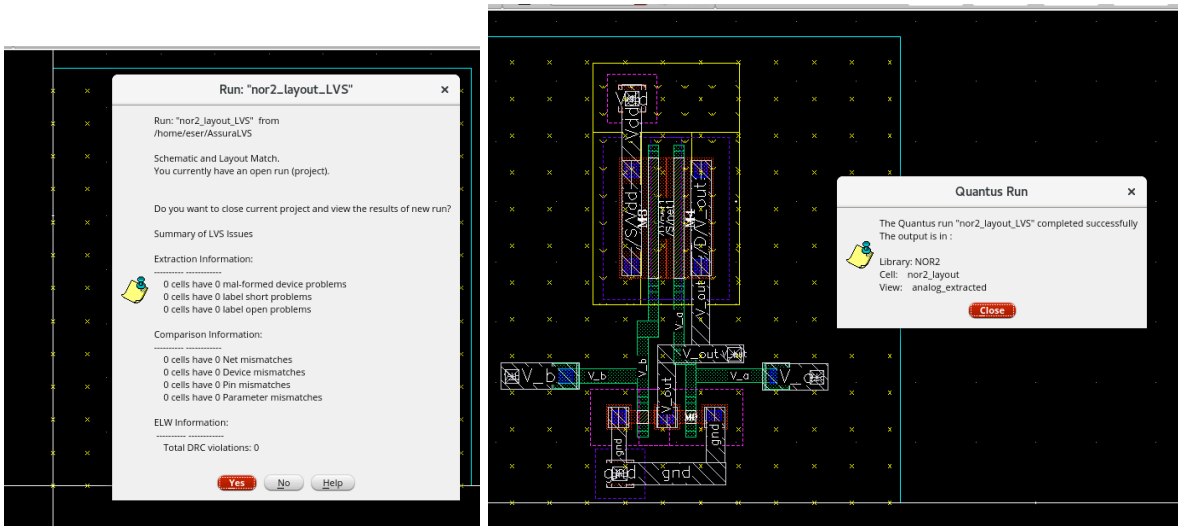
High to low propagation delay for two changing inputs was found to be 397.8ps.



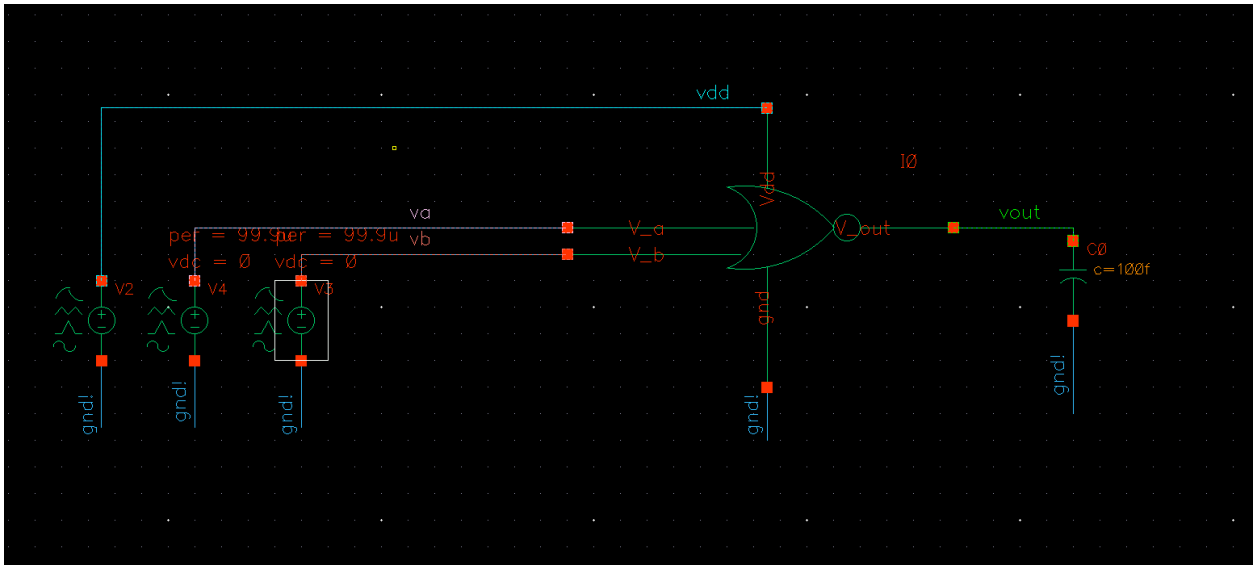
Low to high propagation delay for two falling inputs was found as 560ps which is slightly above the design constraints.

Layout

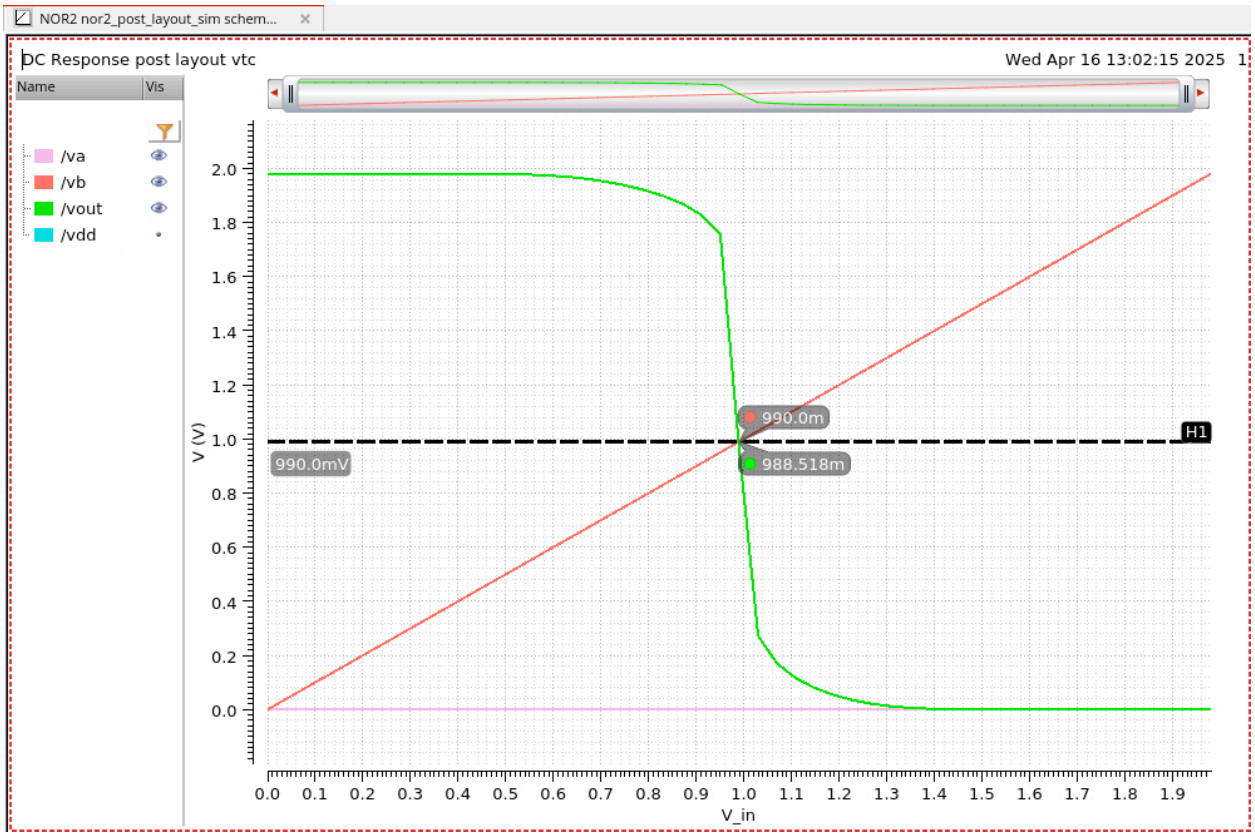

Vdd
S/Vdd
M5
D/net1
S/net1
M4
D/V_out
V_out
V_a
V_b
V_out
V_b
V_b
V_b
V_a
V_a
V_a
V_out
M6
gnd
gnd
gnd



Symbol and Post-layout Simulation

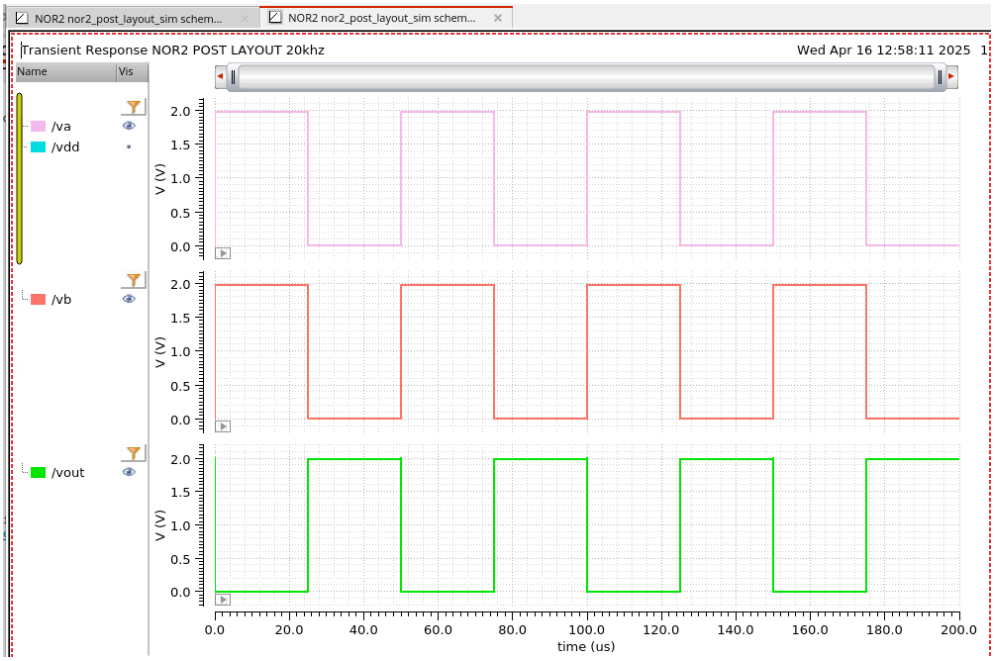


VTC - DC Simulation

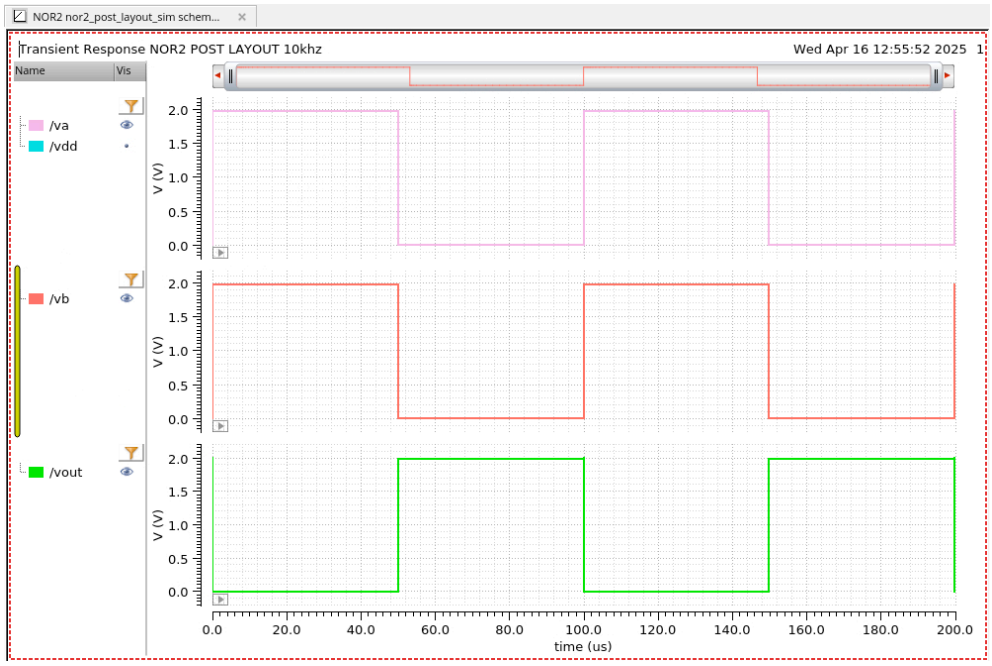


The post layout VTC of the NOR gate is provided above. There is a negligible variation in the threshold voltage value with the VTC reaching 990mv at the output when 988mV is present at the input.

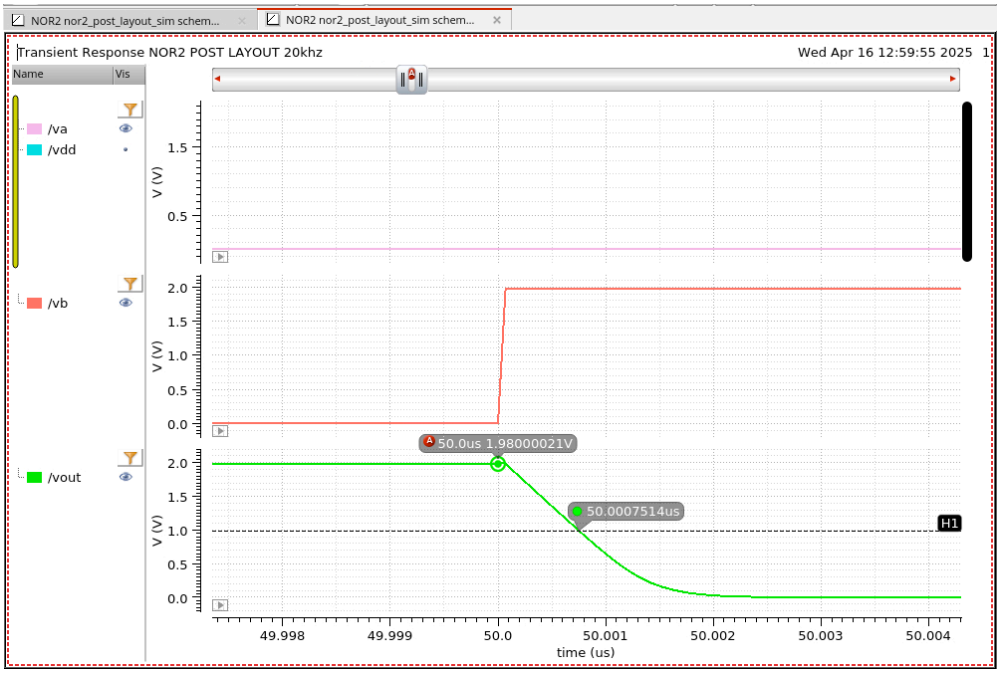
Propagation Delays - Transient Simulation



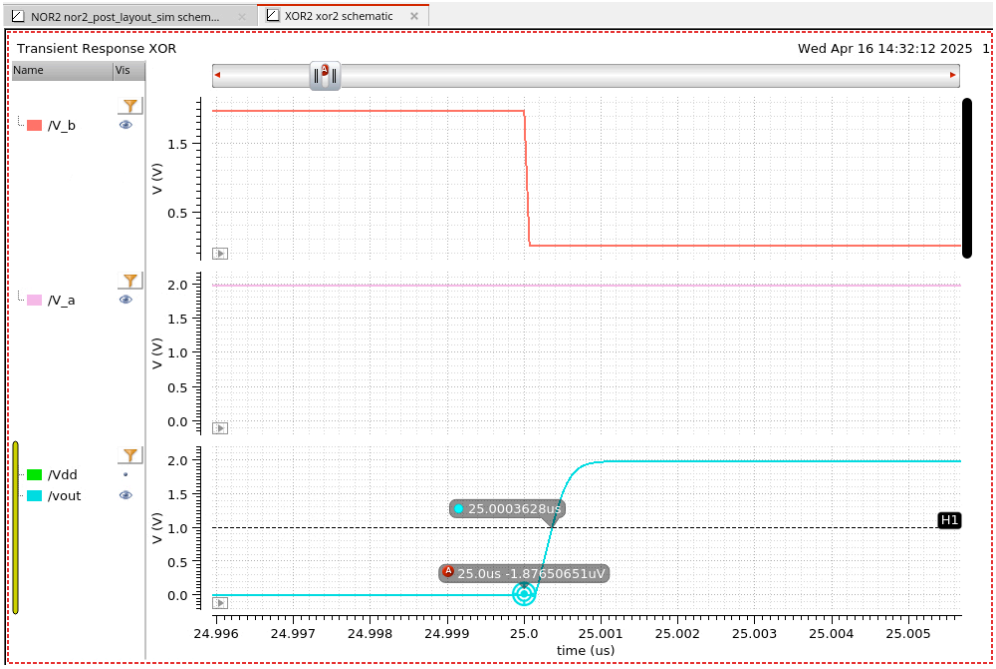
20khz inputs



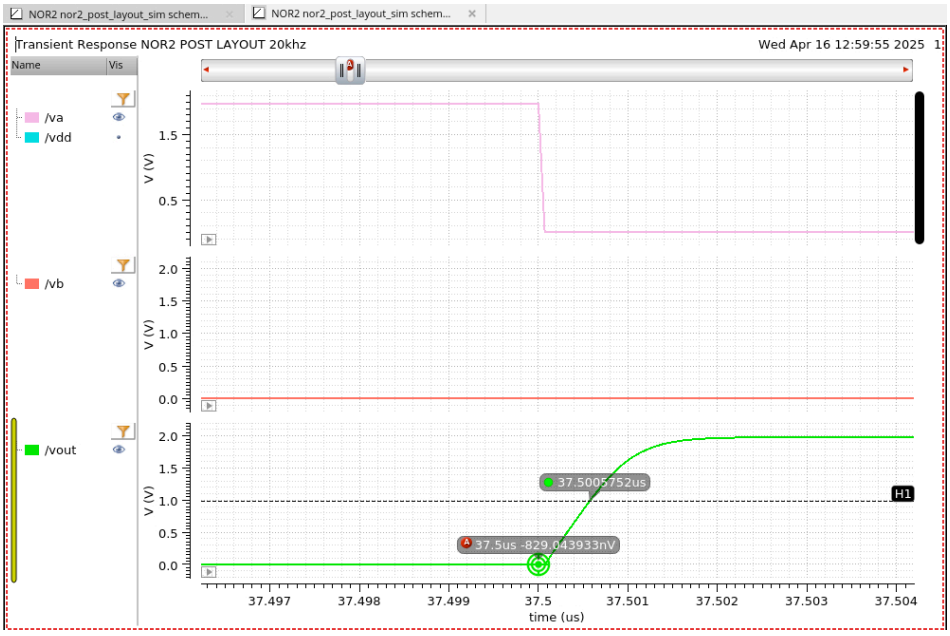
10khz inputs



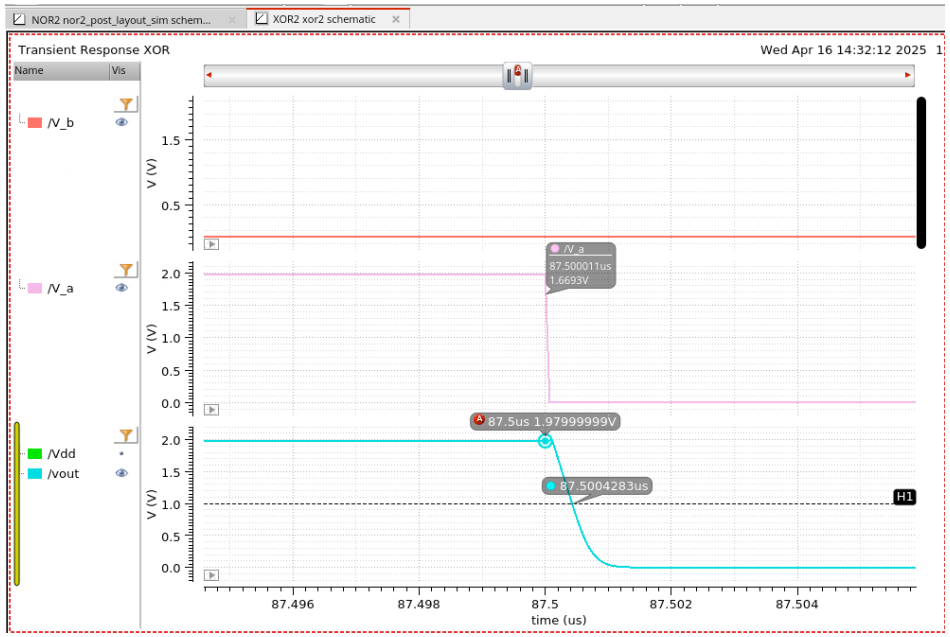
High to low propagation delay for changing input b was found as 751ps which fails the design constraints.



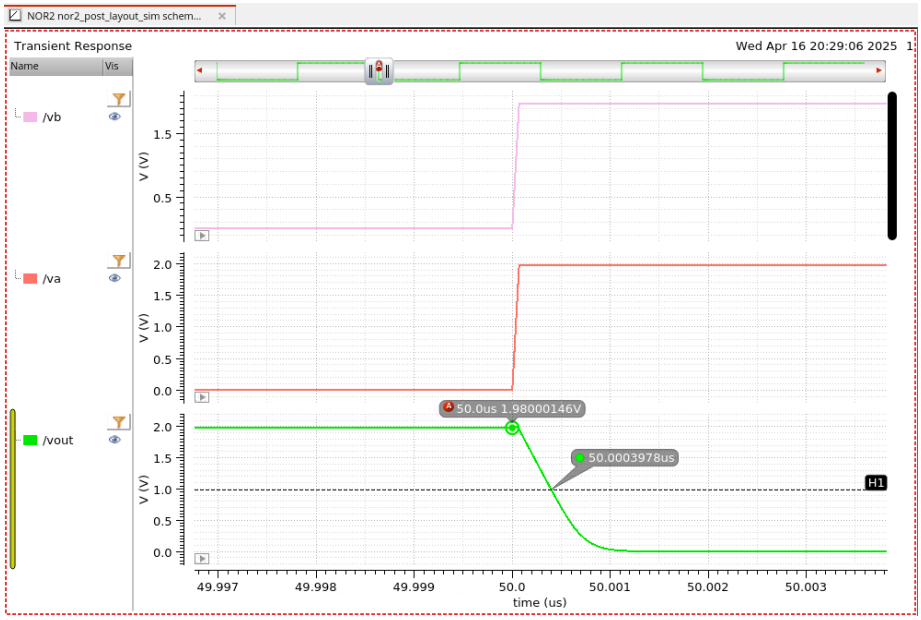
Low to high propagation delay for changing input b was found as 362.8ps.



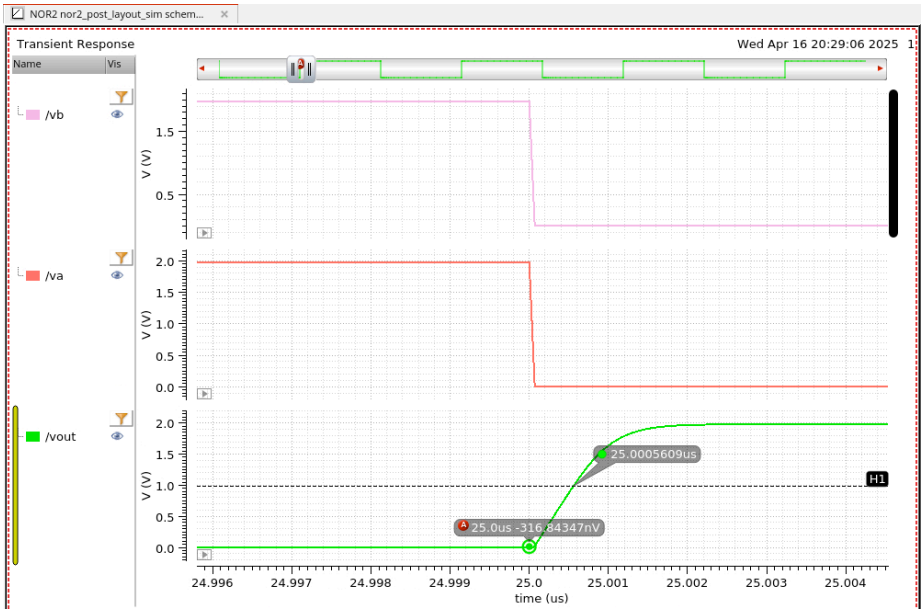
Low to high propagation delay for changing input a was found as 575.2ps



High to low propagation delay for changing input a was found as 428.3ps



High to low propagation delay for two changing inputs was found as 397.8ps



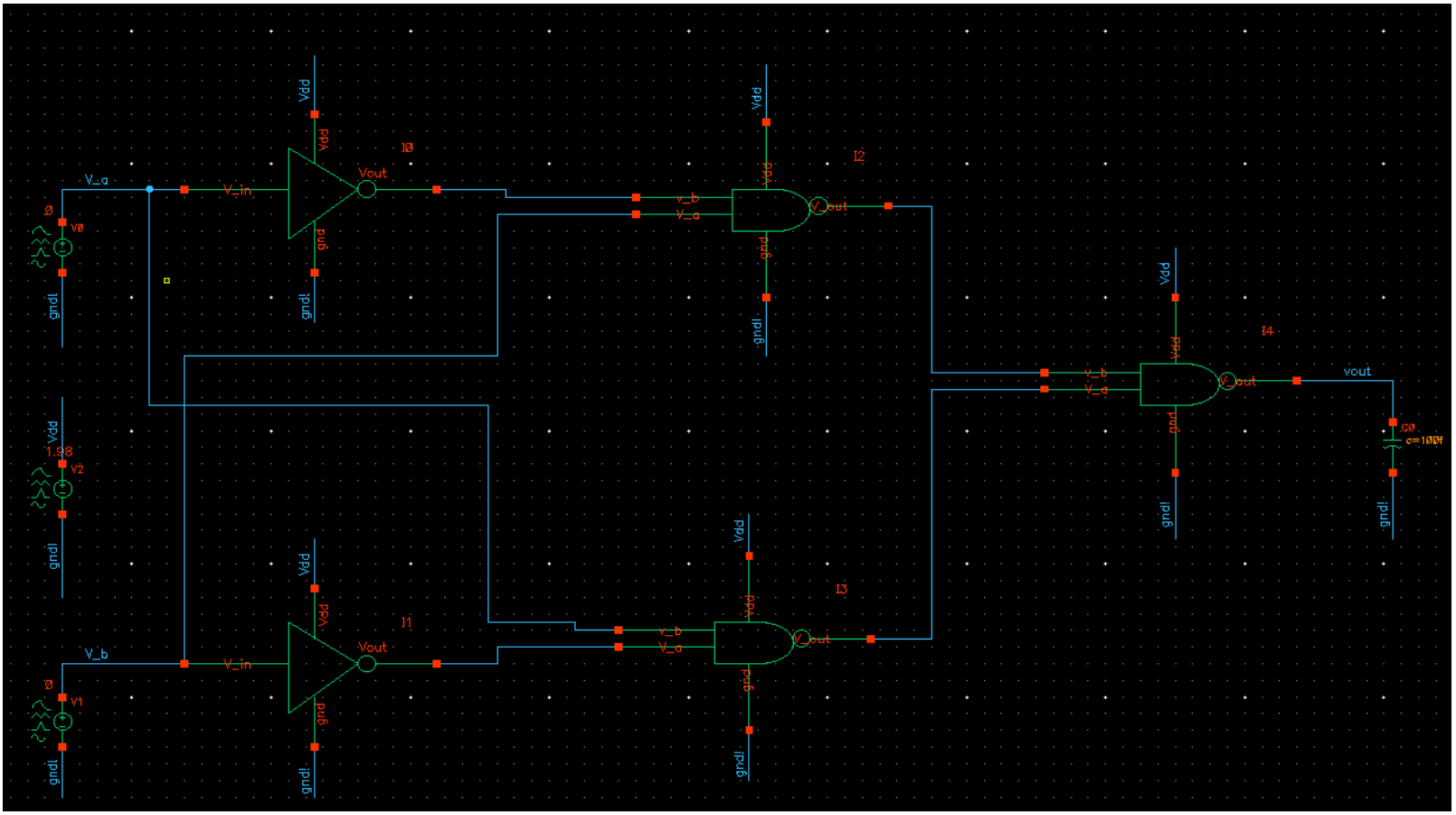
Low to high propagation delay for two changing inputs was found as 561ps

The worst case high to low propagation delay was found as 751ps. It should be noted that the rest of the propagation delays do not fail the design constraints by a significant margin. The only propagation delays that fail the constraints are this one and the very last plot. The worst case low to high propagation delay was found as 561ps which is longer than the design constraint by a small margin.

Xor Gate Design

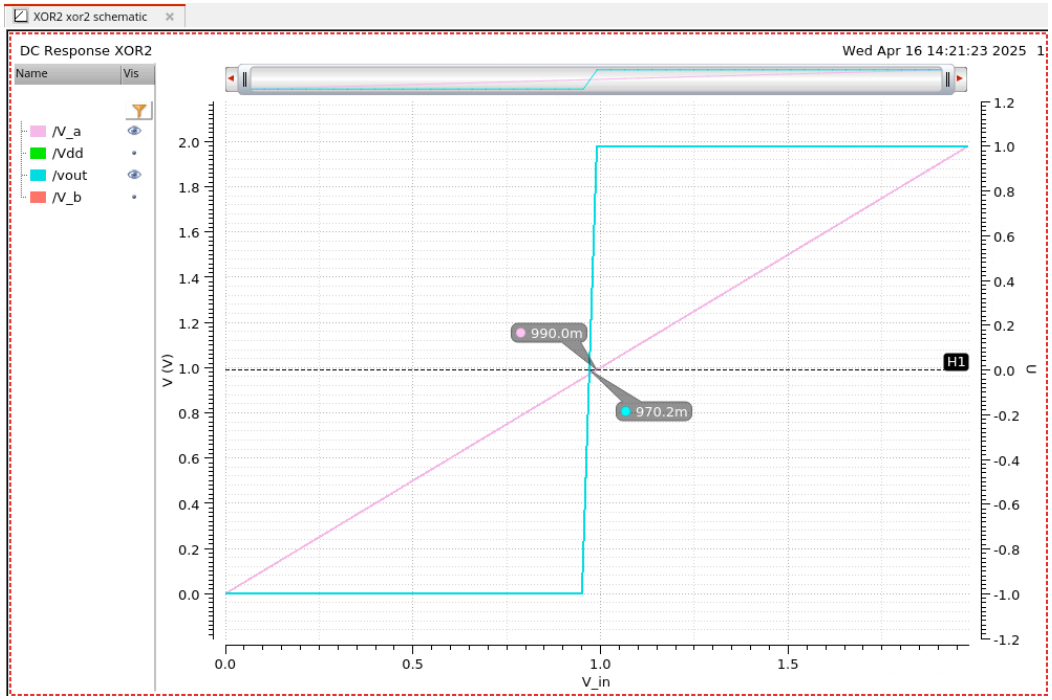
Schematic

XOR gate did not involve any hand calculations since I used my own NOT and NAND gates. The schematic is provided below:



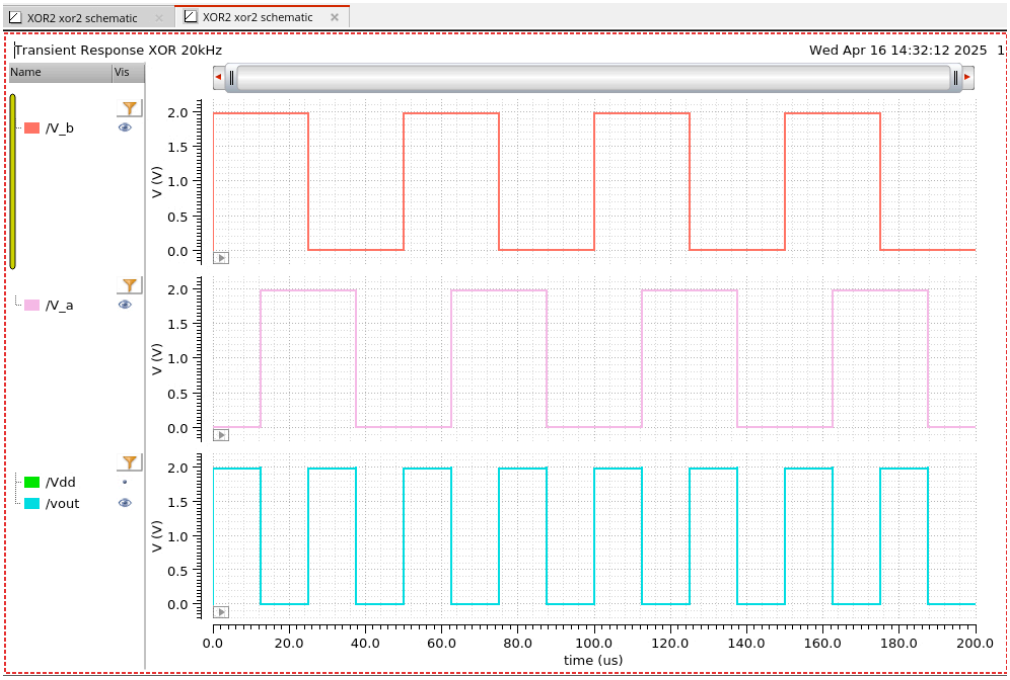
Simulation Results

VTC - DC Simulation

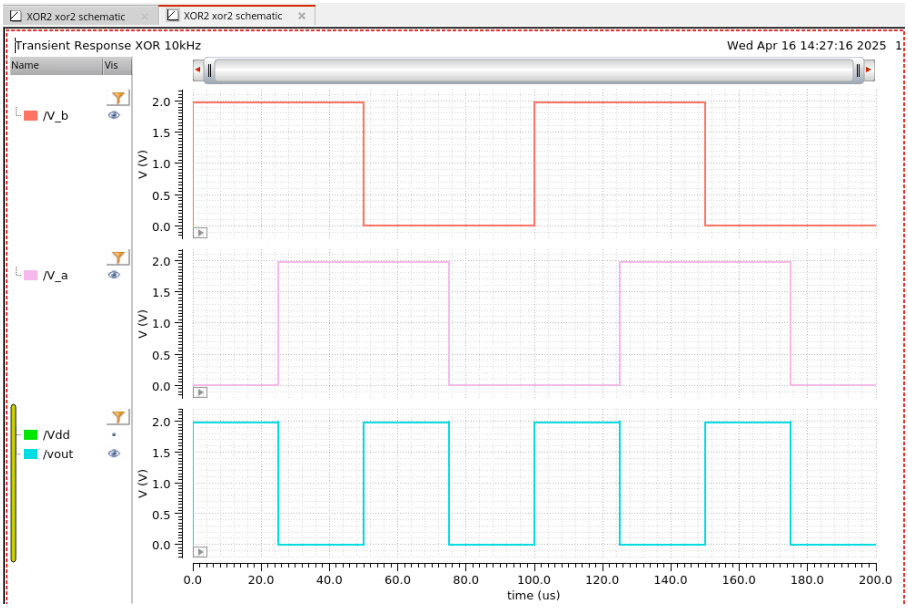


There is only a minute difference between post layout Vth and pre-layout Vth values. Both values are slightly off the 50% point of 990mV despite both the NAND and NOT gates being used having threshold voltages of around 990mV.

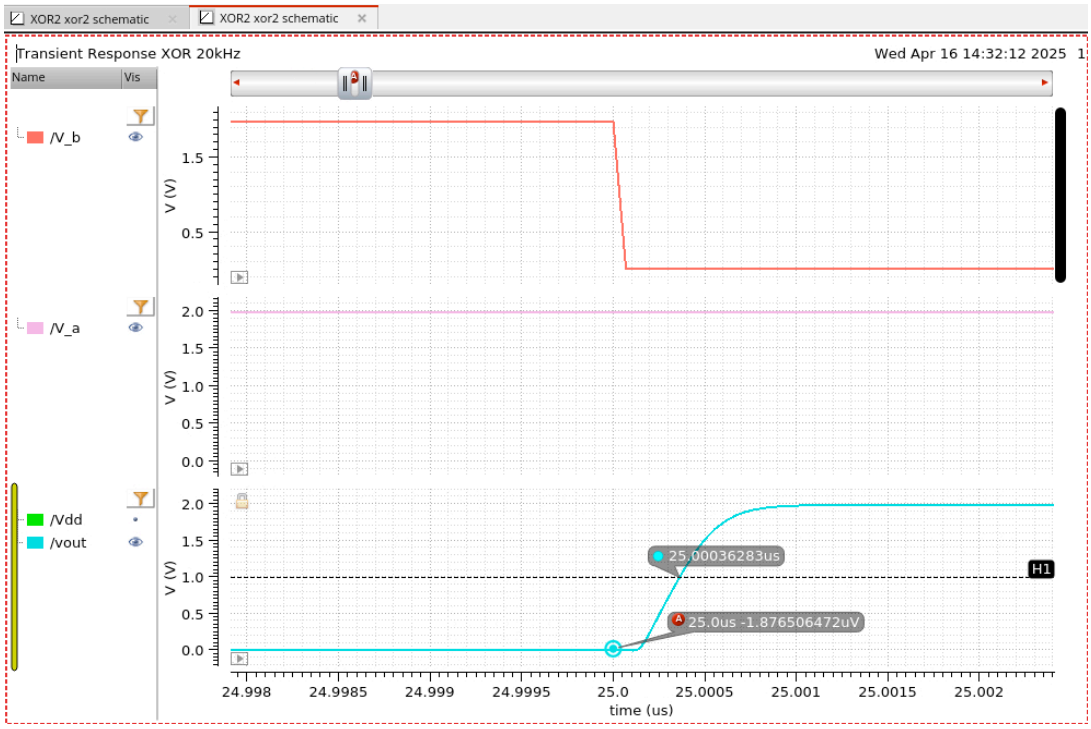
Propagation Delay - Transient Simulation



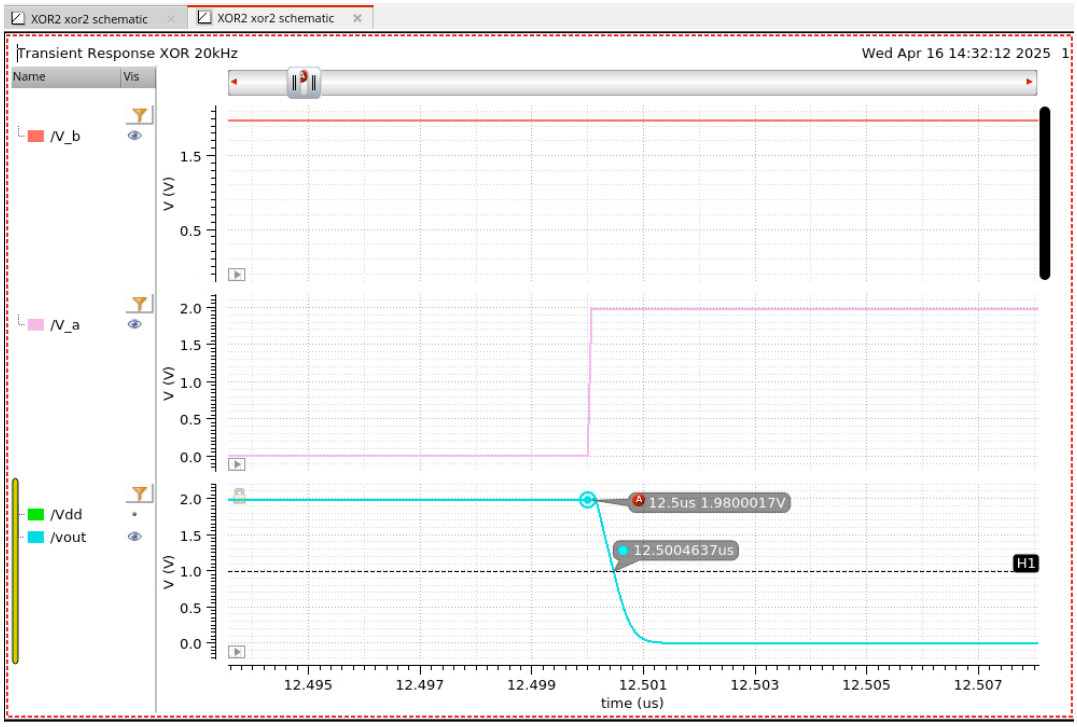
20 kHz inputs 12.5us apart



10 kHz inputs 25us apart



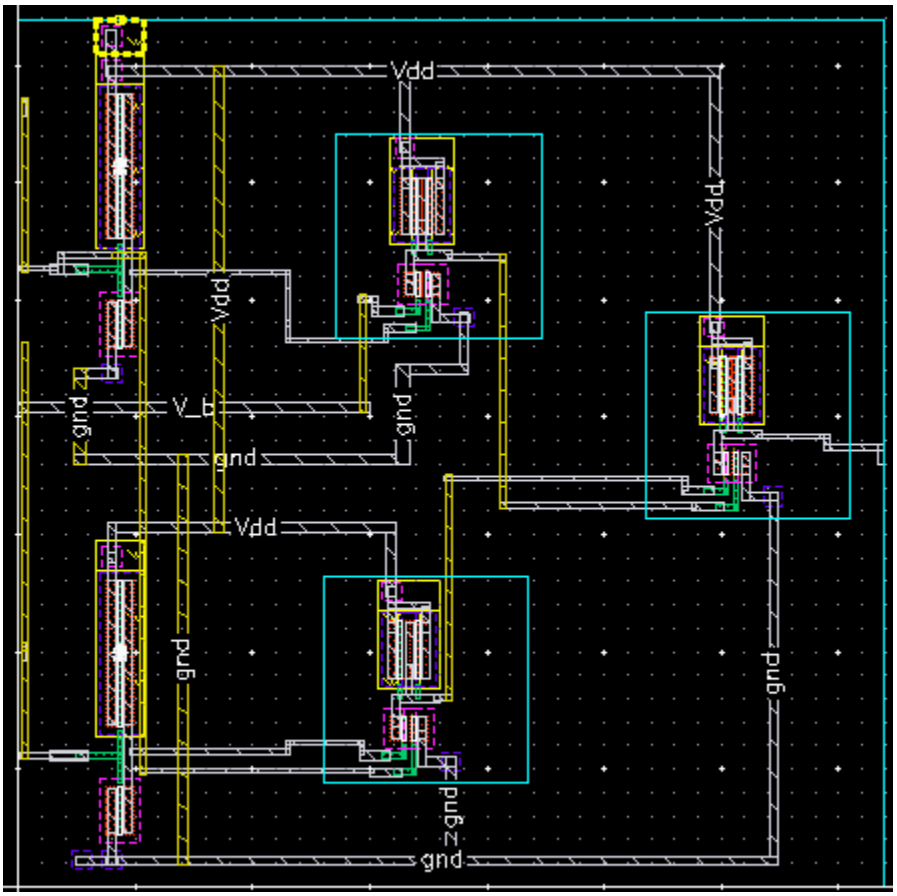
Low to high propagation delay was measured as 362.8ps which meets the design requirements

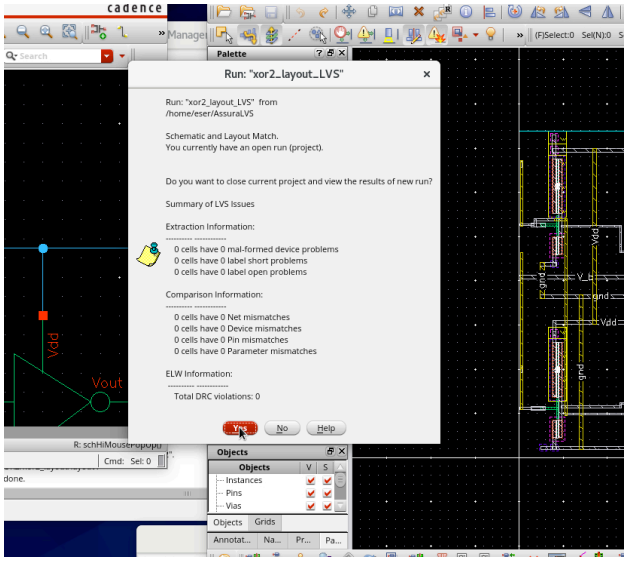


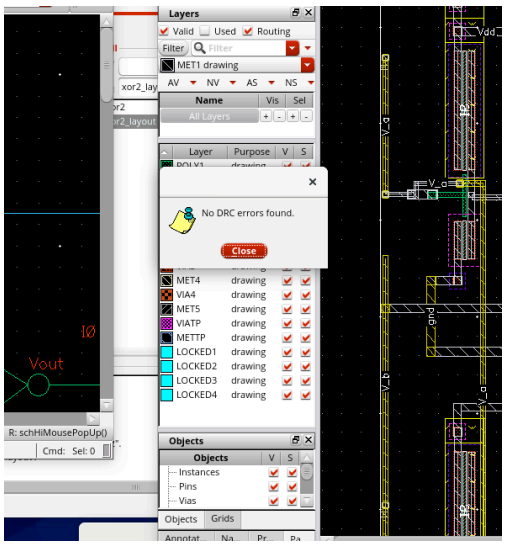
High to low propagation delay was measured as 463.7ps which meets the design requirements.

Layout

I used my NAND gate and my NOT gate designs from previous labs. You may find the layout below above the DRC and LVS check results. I took care to place the pins at accessible points in order to make my life easier in Lab 3.

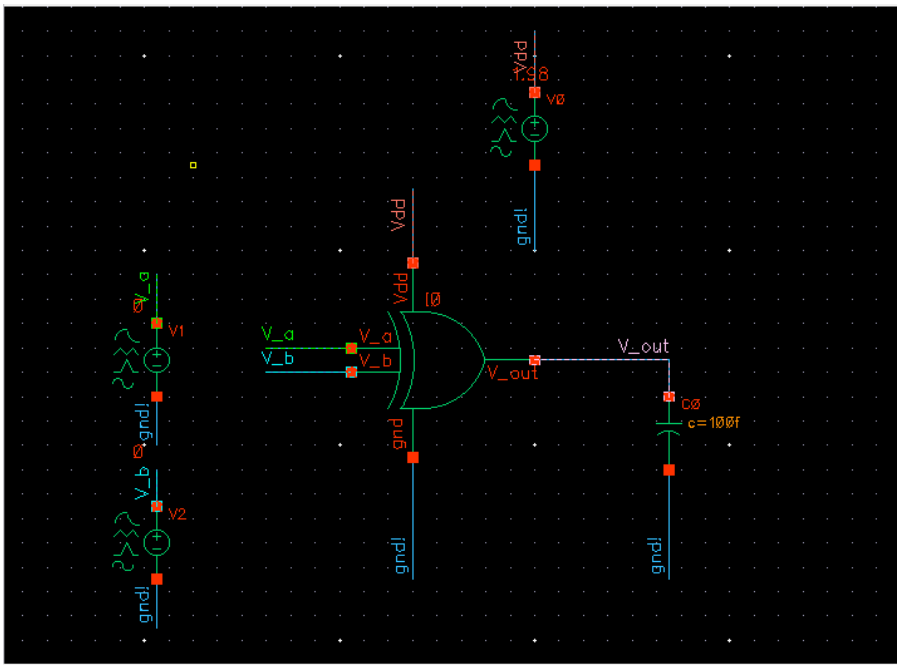




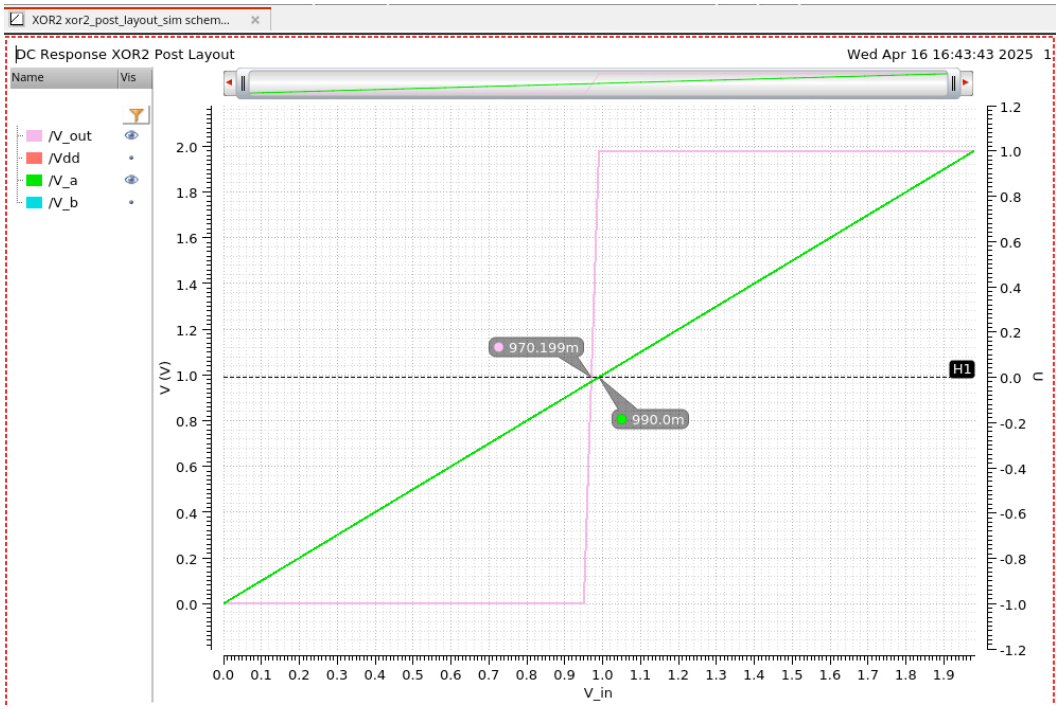


Symbol and Post-layout Simulation

You may find the extracted symbol below. I used the classic xor gate symbol to represent the layout.

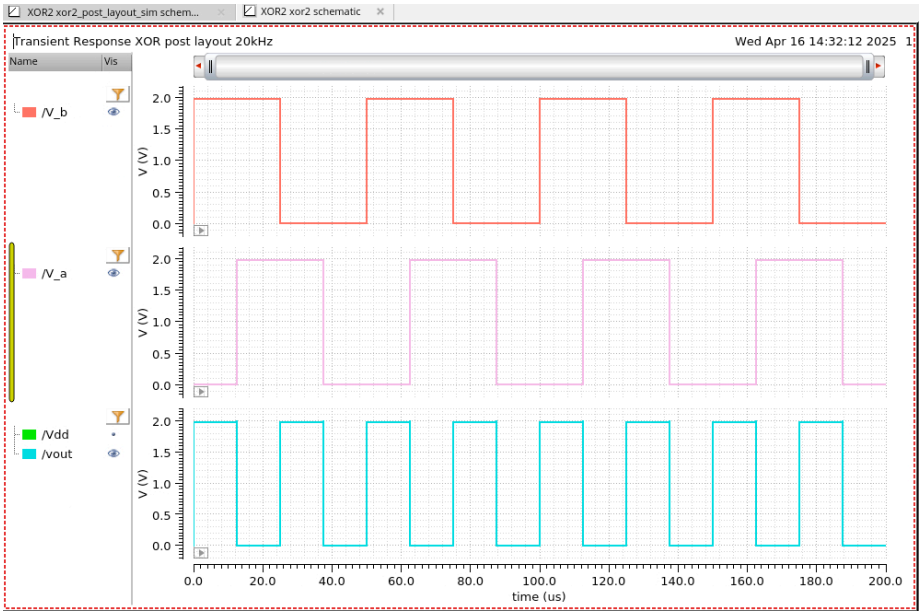


VTC - DC Simulation

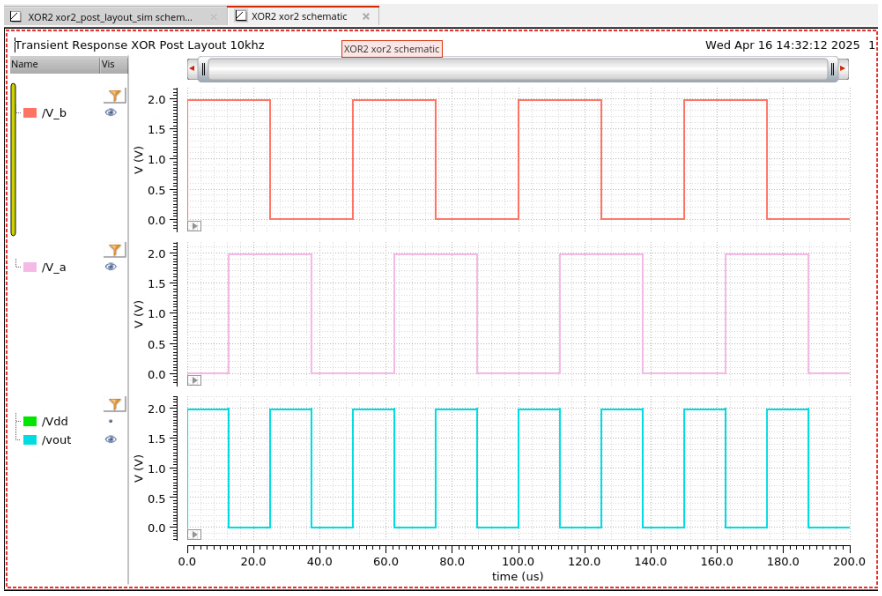


There is only a minute difference between post layout Vth and pre-layout Vth values. Both values are slightly off the 50% point of 990mV despite both the NAND and NOT gates being used having threshold voltages of around 990mV.

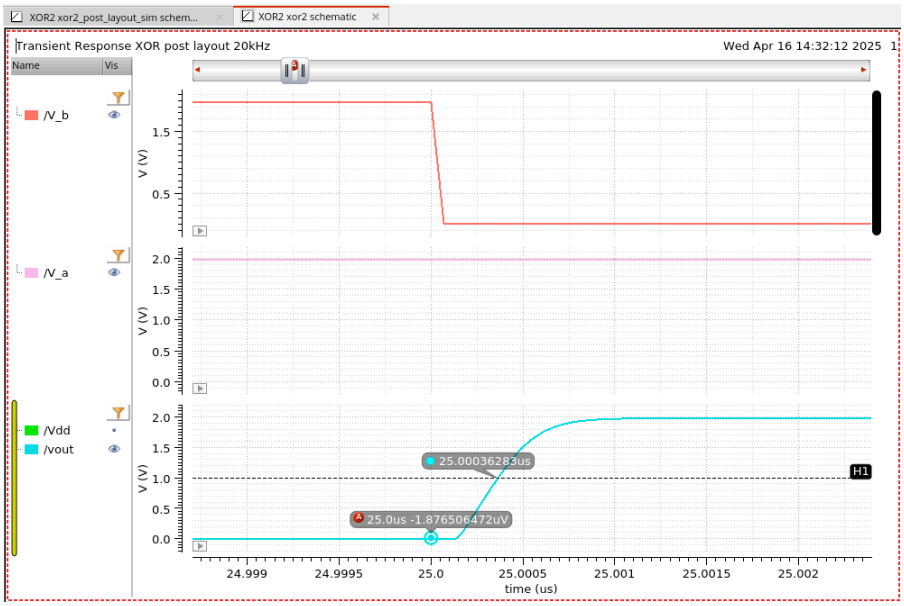
Propagation Delays - Transient Simulation



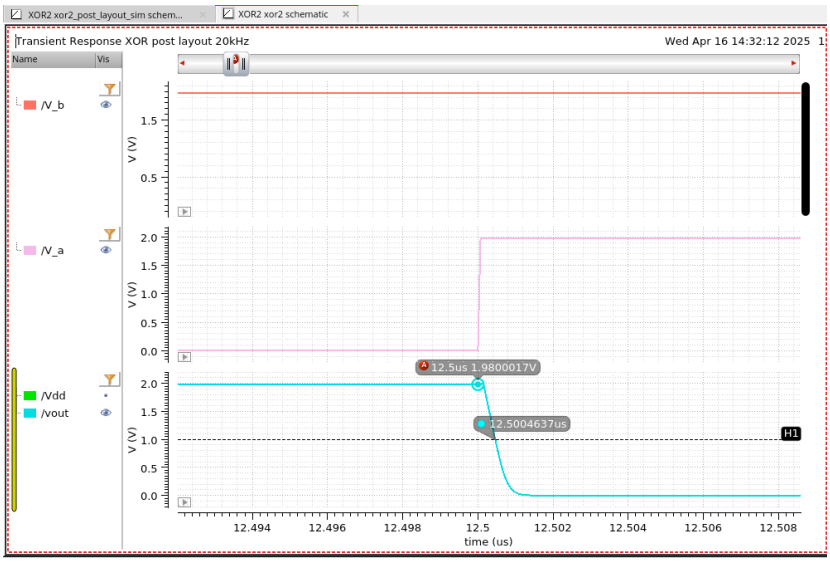
20kHz simulation with inputs 12.5us apart



10kHz simulation with inputs 25us apart



Measured low to high propagation delay is 362.8ps which satisfies the design constraints.



Measured high-to-low propagation delay is 463.7 ps which satisfies the design constraints.