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# Practical UVM

Step by Step with IEEE 1800.2

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All code within this text was compiled and simulated with Synopsys® VCS P-2019.06 using Accellera UVM and the IEEE-1800.2 release.

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*This book is dedicated to:  
The ONE by whose Grace,  
A mute can speak eloquently,  
A lame person can climb a mountain,  
And for whom, nothing is impossible.  
Our families and friends for supporting us  
on this incredible journey.*



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# Please Read! Important Note for the IEEE Edition

Dear Reader:

Thank you for purchasing this book, created to offer knowledge, theories, and practical examples to advance your knowledge and effective usage of SystemVerilog and UVM. This book is both current and rare; few publications support verification and other advancements related to the Universal Verification Methodology.

This book is the result of "blood, sweat and tears" from many, including the author, graphic designers, editors and many in the UVM community on the inner workings of UVM. It has been prepared with considerable effort for your benefit with an effort spanning multiple years. I would greatly appreciate any feedback, suggestions, or comments; you have about this book - please send me your contribution to me via email, which is provided on the inside of the book cover. It shall be gratefully acknowledged.

The greatest profit to receive from the purchases of this book is donating all funds available after recovering the costs of creating this book and its distribution, to those in real need: *Those who suffer economic hardship with insufficient food for themselves and their children, and often without a place to call home or an opportunity to better themselves.*

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I hope you will join me in this endeavor. Together, we can all make this world a better place.

Thank You  
Srivatsa Vasudevan  
Summer 2019