LM27762 Low-Noise Positive and Negative Output Integrated Charge Pump Plus LDO

1 Features

- Generates Low-Noise Adjustable Positive Supply Voltage Between 1.5 V and 5 V and Negative Supply Voltage Between –1.5 V and –5 V
- Input Voltage Range 2.7 V to 5.5 V
- ±250-mA Output Current
- Inverting Charge Pump Followed by Negative LDO
- 2-MHz Low-Noise Fixed-Frequency Operation
- 2.5-Ω Inverter Output Impedance, V_{IN} = 5 V
- Negative LDO Dropout Voltage 30 mV at 100 mA, V_{OUT} = –5 V
- Positive LDO with 45-mV Dropout Voltage at 100 mA, V_{OUT} = 5 V
- 390-µA Quiescent Current (Typical)
- Shutdown Quiescent Current to 0.5 µA (Typical)
- Current Limit and Thermal Protection
- Power Good Pin (Active Low)

2 Applications

- Hi-Fi Audio Headphone Amplifiers
- Operational Amplifier Power Biasing
- Powering Data Converters
- Wireless Communication Systems
- Interface Power Supplies
- Handheld Instrumentation

3 Description

The LM27762 delivers very low-noise positive and negative outputs that are adjustable between ±1.5 V and ±5 V. Input-voltage range is from 2.7 V to 5.5 V, and output current goes up to ±250 mA. With an operating current of only 390 µA and 0.5-µA typical shutdown current, the LM27762 provides ideal performance for power amplifier and DAC bias and other high-current, low-noise negative voltage needs. The device provides a small solution size with few external components.

Negative voltage is generated by a regulated inverting charge pump followed by a low-noise negative LDO. The inverting charge pump of the LM27762 device operates at 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. Positive voltage is generated from the input by a low-noise positive LDO.

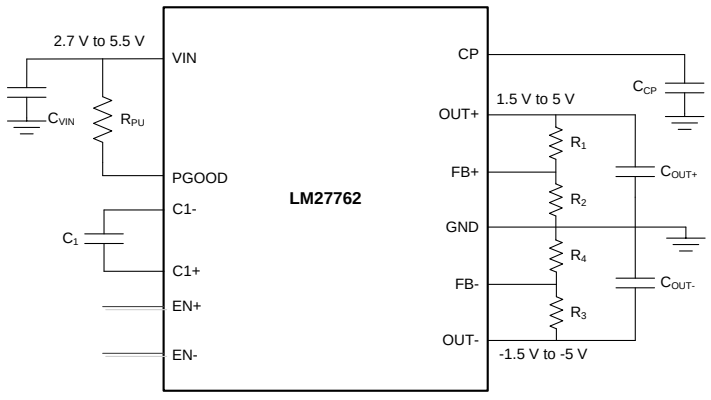
Positive and negative outputs of LM27762 have dedicated enable inputs. These outputs support independent timing for the positive and negative rails for specific system power-sequence needs. Enable inputs can be also shorted together and connected to the input voltage. The LM27762 has an optional Power Good feature.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM27762	WSON (12)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to Revision A	Page
• Changed "Switched Capacitor" to "Charge Pump" in title	1
• Changed "Generates Low-Noise Adjustable Positive and Negative Supply Voltages From ±1.5 V and ±5 V" to "Generates Low-Noise Adjustable Positive Supply Voltages Between 1.5 V and 5 V and Negative Supply Voltages From –1.5 V to –5 V" in *Features*	1

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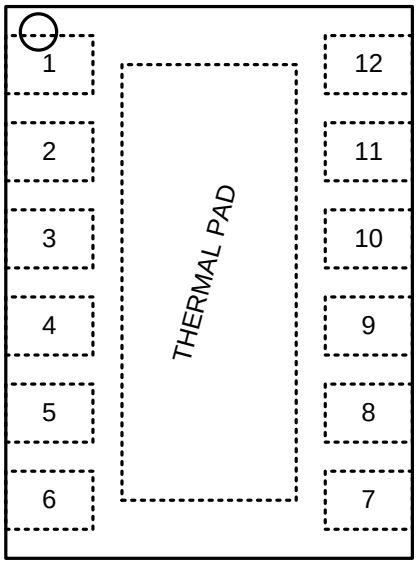
5 Pin Configuration and Functions

DSS Package
12-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
C1+	10	Power	Positive terminal for C_1
C1–	9	Power	Negative terminal for C_1
CP	5	Power	Negative unregulated output voltage
EN+	12	Input	Enable input for the positive LDO, Active high
EN–	8	Input	Enable input for the charge pump and negative LDO, Active high
FB+	2	Power	Feedback input. Connect FB+ to an external resistor divider between OUT+ and GND. **DO NOT** leave unconnected.
FB–	7	Power	Feedback input. Connect FB– to an external resistor divider between OUT– and GND. **DO NOT** leave unconnected.
GND	4	Ground	Ground
OUT+	11	Power	Regulated positive output voltage
OUT–	6	Power	Regulated negative output voltage
PGOOD	1	Output	Power Good flag; open drain; Logic 0 = power good, Logic 1 = power not good. Connect to ground if not used.
VIN	3	Power	Positive power supply input
Thermal Pad	—	Ground	Ground. **DO NOT** leave unconnected.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN to GND or GND to VOUT		5.8	V
EN+, EN-	GND − 0.3	V_{IN}	V
CPOUT, OUT+ and OUT- , continuous output current		300	mA
OUT+, OUT- short-circuit duration to GND(3)		1	s
Continuous power dissipation(4)	Internally limited		
T_{JMAX}(4)		150	°C
Operating input voltage, V_{IN}	2.7	5.5	V
Operating output current, I_{OUT}	0	250	mA
Operating ambient temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to VIN may damage the device and must be avoided. Also, for temperatures above T_A = 85°C, V_{OUT} must not be shorted to GND or VIN or device may be damaged.
(4) Internal thermal shutdown circuitry protects the device from damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM27762 DSS (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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6.5 Electrical Characteristics

Typical limits apply for T_A = 25°C; minimum and maximum limits apply over the full temperature range. Unless otherwise specified V_{IN} = 5 V, C_{IN} = C_{OUT+} = C_{OUT-} = 2.2 µF, C_1 = 1 µF, C_{POUT} = 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Supply current	Open circuit, no load, EN+, EN– connected to VIN. (1)		390		µA
I_{SD}	Shutdown supply current			0.5	5	µA
f_{SW}	Switching frequency	V_{IN} = 3.6 V	1.7	2	2.3	MHz
R_{NEG}	Output resistance to C_{POUT}	V_{IN} = 5.5 V, I_L = 100 mA		2.5		Ω
V_{LDO-}	LDO dropout voltage	I_L = 100 mA, V_{OUT-} = −5 V		30		mV
PSRR	Power supply rejection ratio, OUT–	I_L = 100 mA, V_{OUT-} = −1.8 V, 10 kHz		50		dB
V_N–	Output noise voltage	I_L = 80 mA, 10 Hz to 100 kHz		22		μV_{RMS}
V_{FB-}	Feedback pin reference voltage		–1.238	–1.22	–1.202	V
V_{OUT-}	Adjustable output voltage	5.5 V ≥ V_{IN} ≥ 2.7 V	–5		–1.5	V
	Load regulation	0 to 250 mA, V_{OUT} = –1.8 V		34		µV/mA
	Line regulation	5 V ≥ V_{IN} ≥ 2.7 V, I_L = 50 mA		1.5		mV/V
V_{LDO+}	LDO dropout voltage	I_L = 100 mA, V_{OUT} = 5 V		45		mV
PSRR	Power supply rejection ratio, OUT+	I_L = 100 mA, V_{OUT+} = 1.8 V, 10 kHz		43		dB
V_{N+}	Output noise voltage	I_L = 80 mA, 10 Hz to 100 kHz		22		μV_{RMS}
V_{FB+}	Feedback pin reference voltage		1.182	1.2	1.218	V
V_{OUT+}	Adjustable output voltage	5.5 V ≥ V_{IN} ≥ 2.7 V	1.5		5	V
	Load regulation	0 to 250 mA, V_{OUT} = 1.8 V		11		µV/mA
	Line regulation	5 V ≥ V_{IN} ≥ 2.7 V, I_L = 50 mA		1.9		mV/V
V_{IH}	Enable pin input voltage high	5.5 V ≥ V_{IN} ≥ 2.7 V	1.2			V
V_{IL}	Enable pin input voltage low	5.5 V ≥ V_{IN} ≥ 2.7 V			0.4	V

(1) When VIN = 5.5V charge pump may enter PWM mode in hot conditions.

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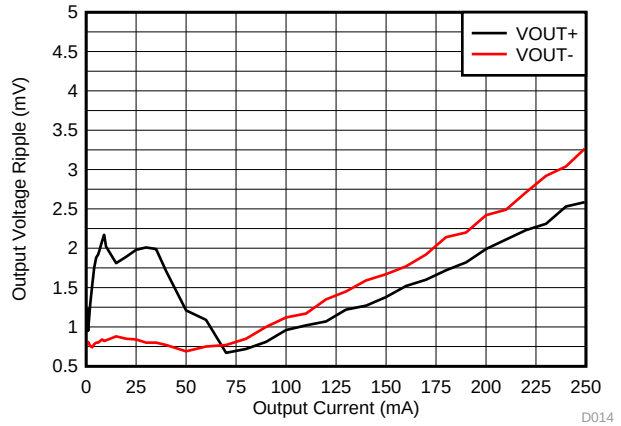
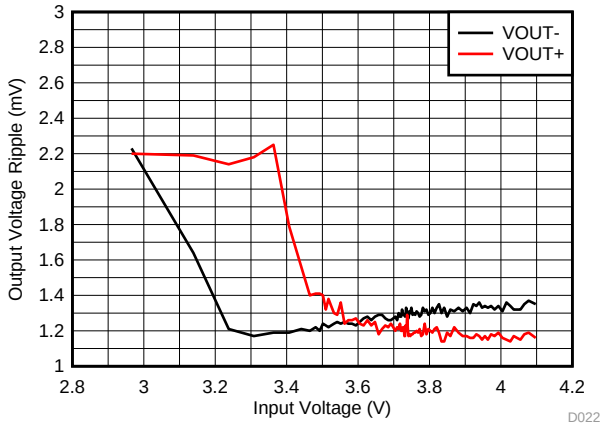
6.6 Typical Characteristics



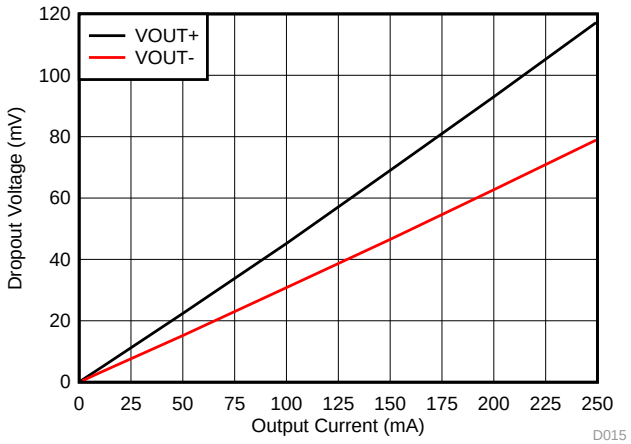
V_{IN} = 3.7 V V_{OUT} = ±3 V

Figure 1. Output Voltage Ripple vs Output Current



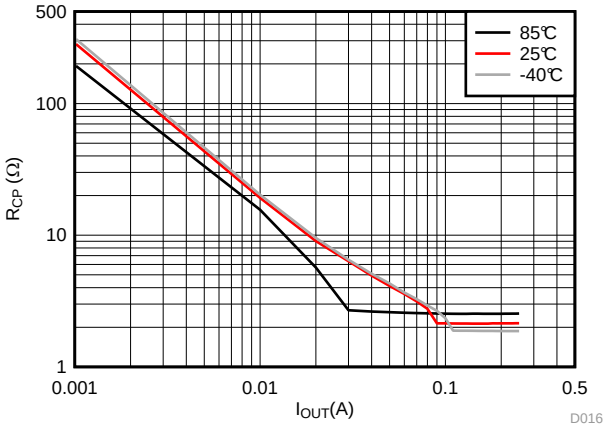
V_{OUT} = ±3 V I_{OUT} = ±100 mA

Figure 2. Output Voltage Ripple vs Input Voltage



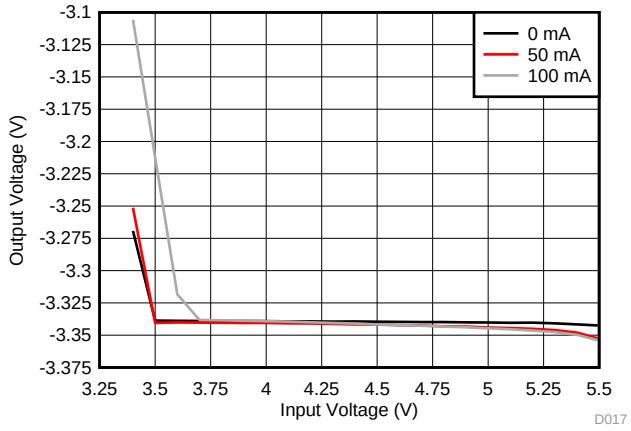
V_{OUT} = ± 3.3 V

Figure 3. LDO Dropout Voltage vs Output Current



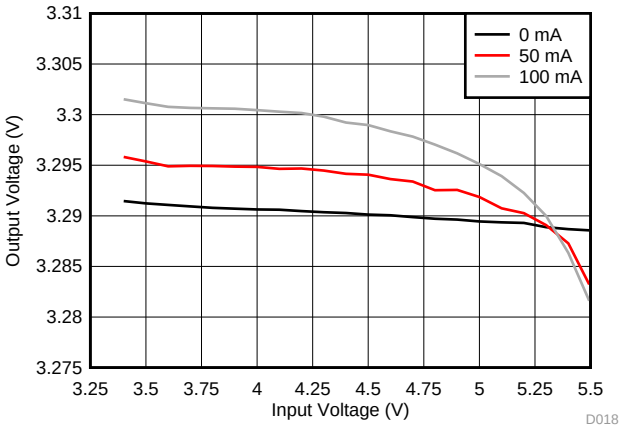
V_{IN} = 5.5 V

Figure 4. Charge Pump Output Resistance vs Output Current



V_{OUT} = –3.3 V

Figure 5. Line Regulation for OUT-



V_{OUT} = 3.3 V

Figure 6. Line Regulation for OUT+

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Typical Characteristics (continued)

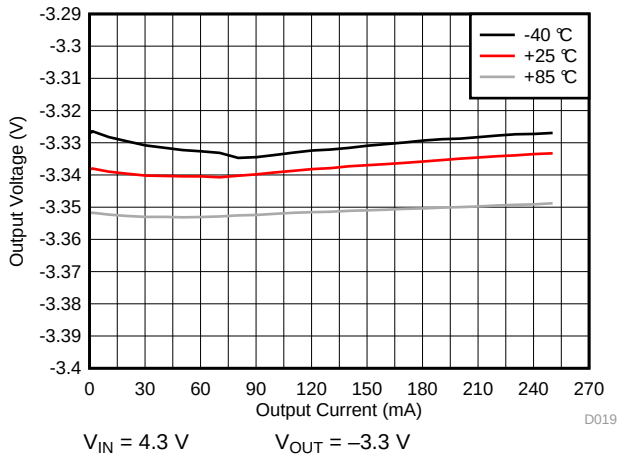

Figure 7. Load Regulation for OUT-

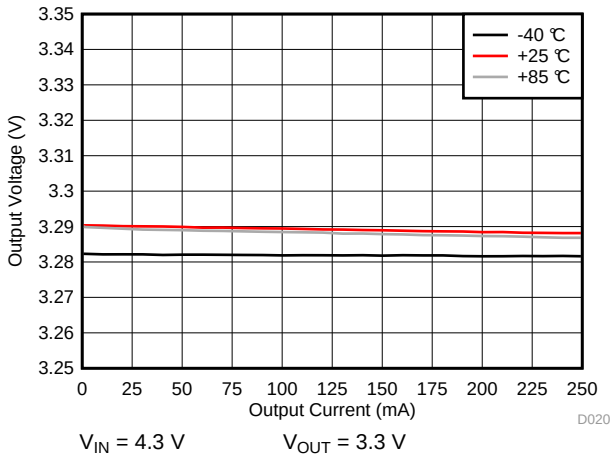

Figure 8. Load Regulation for OUT+

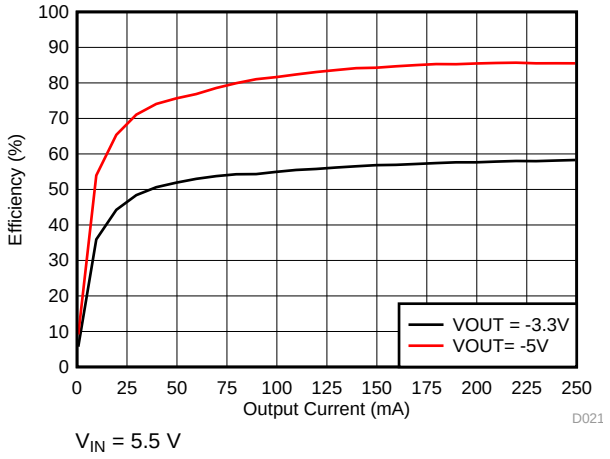

Figure 9. Efficiency for OUT–

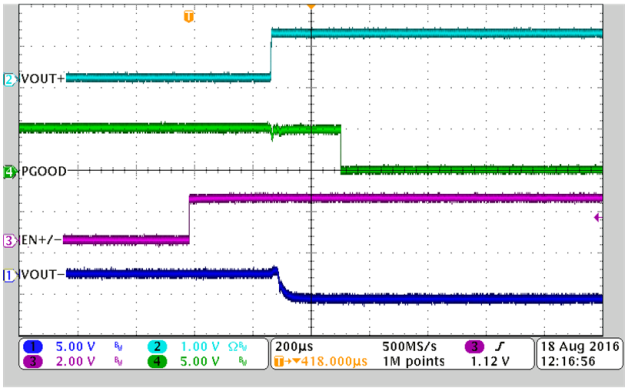

Figure 10. Start-Up

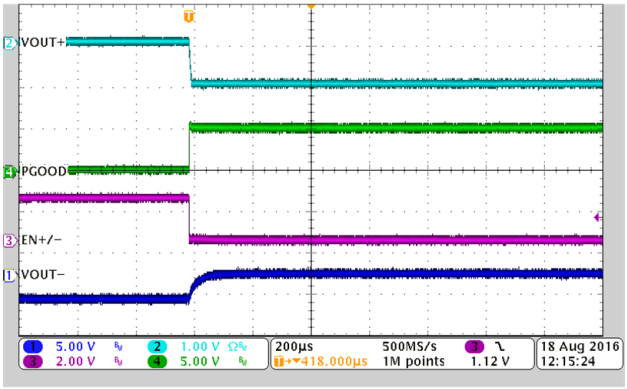

Figure 11. Shutdown

7 Detailed Description

7.1 Overview

The LM27762 low-noise inverting charge pump with both positive and negative LDOs delivers very low-noise adjustable positive and negative outputs between ±1.5 V and ±5 V. The output voltage levels of the positive and negative LDO are independently controllable with external resistors. Input voltage range of LM27762 is from 2.7 V to 5.5 V. Five low-cost capacitors are used in this circuit to provide up to ±250 mA of output current. The LM27762 operates at 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. With an typical operating current of only 390 µA and 0.5-µA typical shutdown current, the LM27762 provides ideal performance for power amplifiers and DAC bias and other high-current, low-noise negative voltage needs.

The LM27762 device has an enable input (EN+) for the positive LDO and another enable input (EN–) for the negative charge pump and LDO. This supports independent timing for the positive and negative rails in system power sequence. Enable inputs can be also shorted together and connected to VIN. When LDO is disabled, output of the positive LDO has 50-kΩ pulldown to ground, and output of the negative LDO has 50-kΩ pullup to ground. The LM27762 has power good monitoring for OUT+ and OUT– outputs. The PGOOD pin is an open-drain output and requires an external pullup resistor. When Power Good feature is not used, PGOOD pin can be connected to ground.

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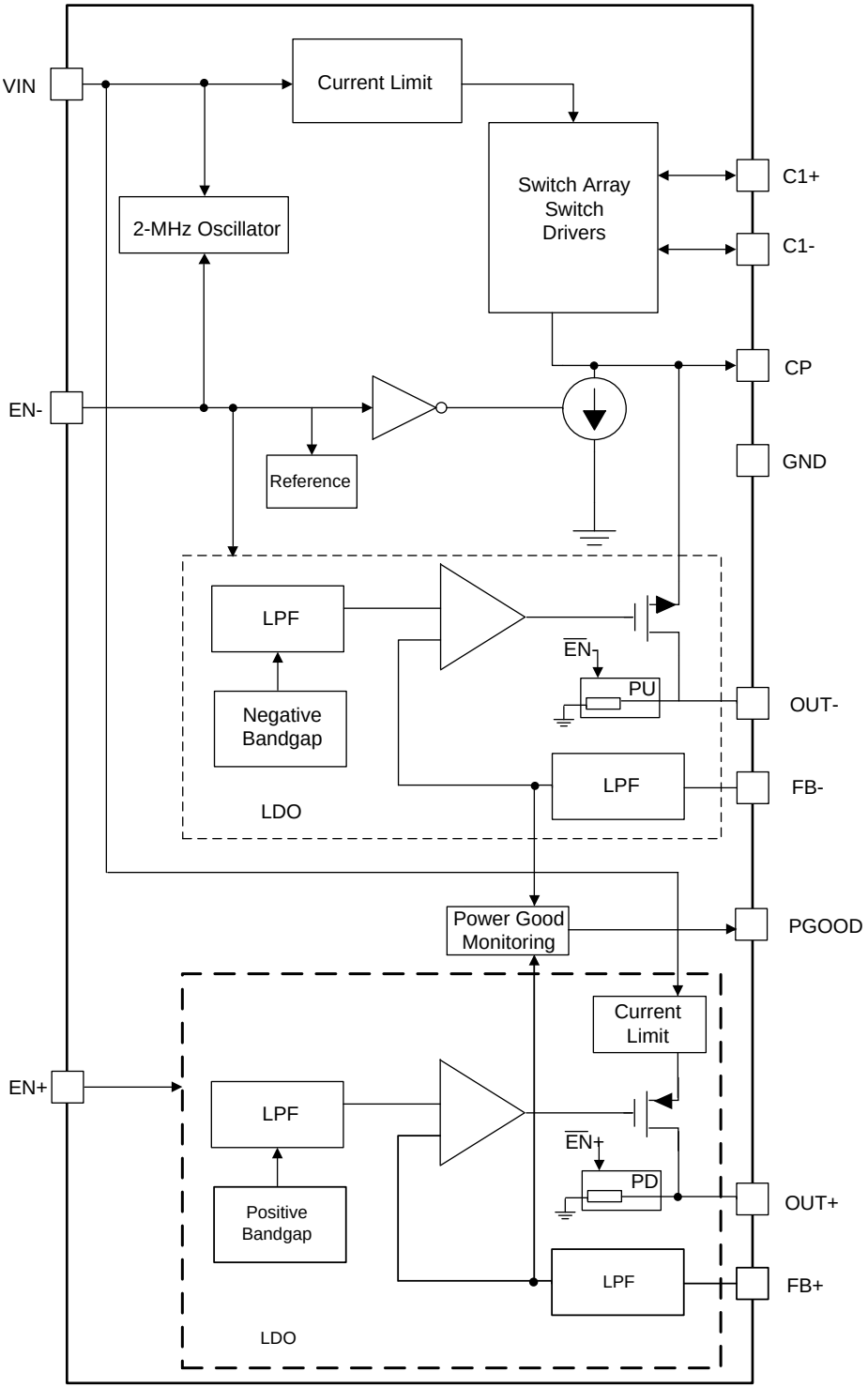
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Undervoltage Lockout

The LM27762 has an internal comparator that monitors the voltage at V_{IN} and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM27762 resumes normal operation.

7.3.2 Input Current Limit

The LM27762 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The charge pump and positive LDO both have 500 mA (typical) input current limit when the output is shorted directly to ground. When the LM27762 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

7.3.3 PFM Operation

To minimize quiescent current during light load operation, the LM27762 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is low, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-2-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency in the LM27762 is 2 MHz.

7.3.4 Output Discharge

In shutdown, the LM27762 actively pulls down on the outputs (OUT+, OUT–) of the device until the output voltage reaches GND.

7.3.5 Power Good Output (PGOOD)

The LM27762 has monitoring for the OUT+ and OUT– output voltage levels and open-drain PGOOD output.

Table 1. PGOOD (Active Low) Operation

EN+	EN–	OUT+	OUT–	PGOOD
Low	Low	Don't care	Don't care	High
High	Low	< 95% of target value	Don't care	High
High	Low	> 95% of target value	Don't care	Low
Low	High	Don't care	< 95% of target value	High
Low	High	Don't care	> 95% of target value	Low
High	High	< 95% of target value	Don't care	High
High	High	Don't care	< 95% of target value	High
High	High	> 95% of target value	> 95% of target value	Low

7.3.6 Thermal Shutdown

The LM27762 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the device switches into shutdown mode. The LM27762 releases thermal shutdown when the junction temperature is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. The LM27762 device power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped by reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the device.

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7.4 Device Functional Modes

7.4.1 Shutdown Mode

When enable pins (EN+, EN–) are low, both positive and negative outputs of LM27762 are disabled, and the device is in shutdown mode reducing the quiescent current to minimum level. In shutdown, the outputs of the LM27762 are pulled to ground (internal 50 kΩ between each OUT pin and ground).

7.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN+ pin enables the positive LDO. Applying a voltage greater than 1.2 V to the EN– pin enables the negative CP and LDO. When enabled, the positive and negative output voltages are equal to levels set by external resistors. Care must be taken to both the positive LDO and the inverting charge pump followed by negative LDO have enough headroom. Power Good ouput PGOOD indicates the status of OUT+ and OUT– voltage levels.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM27762 input voltage range is from 2.7 V to 5.5 V. The positive LDO provides a positive voltage configurable with external gain setting resistors R_1, R_2. The low-noise charge-pump voltage converter inverts the input voltage V to a negative output voltage. Charge pump is followed by the negative LDO which regulates a negative output voltage configurable with external gain setting resistors R_3, R_4. Output voltage range is ± 1.5 V to ± 5 V. When selecting input (VIN) and output (OUT+, OUT-) voltages ranges, headroom required by the charge pump and LDOs must to be considered. Charge-pump minimum headroom can be estimated based on the maximum load current and charge pump output resistance.

The device uses five low-cost capacitors to provide up to 250 mA of output current. The LM27762 operates at a 2-MHz oscillator frequency to reduce charge-pump output resistance and voltage ripple under heavy loads. When using the optional open-drain PGOOD feature, connect a 10-kΩ pullup resistor (R_{PU}) to VIN. Connect pin to ground if PGOOD is not used.

8.2 Typical Application

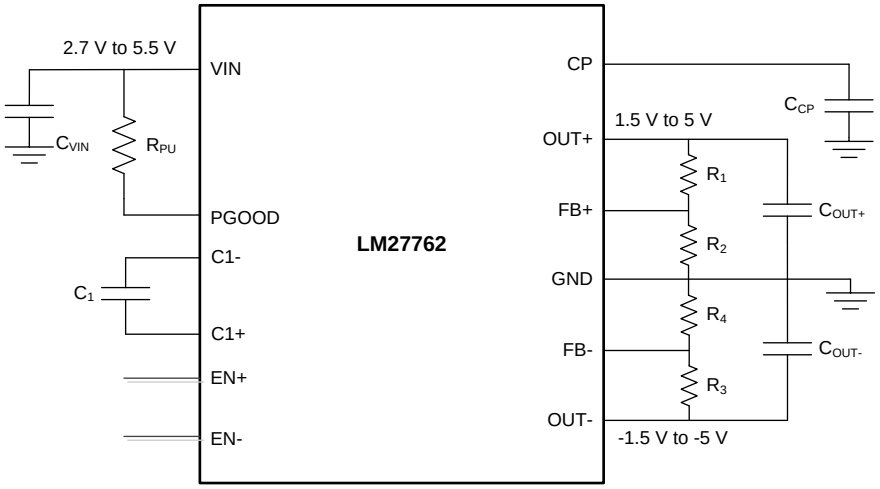

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Figure 12. LM27762 Typical Application

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Typical Application (continued)

8.2.1 Design Requirements

The following example describes powering an amplifier driving high impedance headphones. Input voltage is from a smart-phone battery. Amplifier is driving 2-V_{RMS} to 600-Ω stereo headphones.

Table 2. Application Example Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V to 4.2 V
Output voltage	±3 V
Output current	10 mA (LM27762 capability 250 mA maximum)
C_{VIN}, C_{OUT+}, $C_{OUT–}$	2.2 µF
C_{CP}	4.7 µF
R_{PU}	10 kΩ (optional, connect PGOOD pin to ground if feature is not used)

8.2.2 Detailed Design Procedure

8.2.2.1 Positive Low-Dropout Linear Regulator and OUT+ Voltage Setting

LM27762 features a low-dropout, linear positive voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The positive output voltage of the LM27762 is externally configurable. The value of R_1 and R_2 determines the output voltage setting. The output voltage can be calculated using Equation 1:

$$V_{OUT} = 1.2\ V \times (R_1 + R_2) / R_2 \quad (1)$$

The value for R_2 must be no less than 50 kΩ.

8.2.2.2 Charge-Pump Voltage Inverter

The main application of the LM27762 is to generate a regulated negative supply voltage. The voltage inverter circuit uses only three external capacitors, and the LDO regulator circuit uses one additional output capacitor.

The voltage inverter portion of the LM27761 contains four large CMOS switches which are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 13 shows the voltage switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, and C_1 is charging C_{CP}. After a number of cycles, the voltage across C_{CP} is pumped into V_{IN}. Because the anode of C_{CP} is connected to ground, the output at the cathode of C_{CP} equals –(V_{IN}) when there is no load current. When a load is added, the output voltage drop is determined by the parasitic resistance (R_{DSON} of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between the capacitors.

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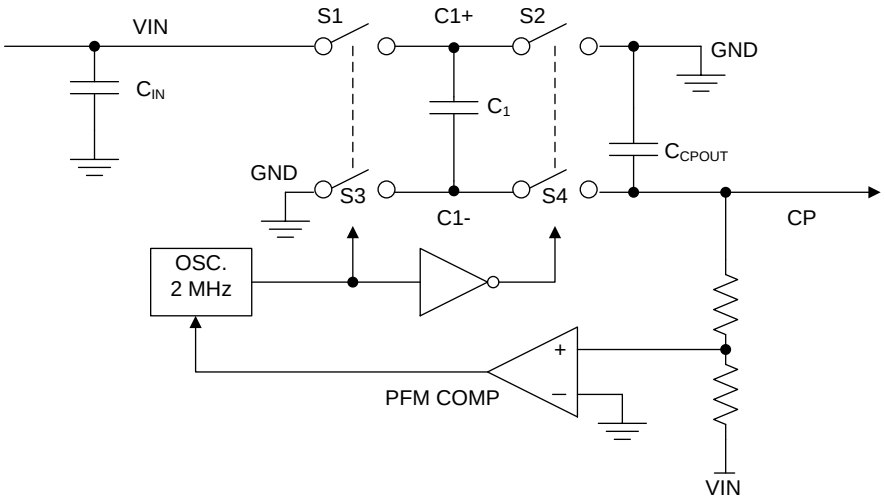

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Figure 13. Voltage Inverting Principle

The output characteristic of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals $–(V_{IN})$. The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance, and the ESR of C_1 and C_{CP}. Because the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The charge-pump output capacitor C_{CP} is charging and discharging at a current approximately equal to the output current; therefore, its ESR only counts once in the output resistance. A good approximation of charge-pump R_{OUT} is shown in Equation 2:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C_1)] + (4 \times ESR_{C1}) + ESR_{CCP} \quad (2)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 13.

High capacitance and low-ESR ceramic capacitors reduce the output resistance.

8.2.2.3 Negative Low-Dropout Linear Regulator and OUT– Voltage Setting

At the output of the inverting charge-pump the LM27762 features a low-dropout, linear negative voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This negative LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The negative output voltage of the LM27762 is externally configurable. The value of R_3 and R_4 determines the output voltage setting. The output voltage can be calculated using Equation 1:

$$V_{OUT} = –1.22\ V \times (R_3 + R_4) / R_4 \quad (3)$$

The value for R_4 must be no less than 50 kΩ.

8.2.2.4 External Capacitor Selection

The LM27762 requires 5 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low ESR (≤ 15 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM27762 due to their high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferable for use with the LM27762. These capacitors have tight capacitance tolerances (as good as ±10%) and hold their value over temperature (X7R: ±15% over –55°C to +125°C; X5R ±15% over –55°C to +85°C).

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Using capacitors with a Y5V or Z5U temperature characteristic is generally not recommended for the LM27762. These capacitors typically have wide capacitance tolerance (80%, ….20%) and vary significantly over temperature (Y5V: 22%, –82% over –30°C to +85°C range; Z5U: 22%, –56% over 10°C to 85°C range). Under some conditions a 1-µF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27762.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower-than-expected capacitance on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. TI strongly recommends that the LM27762 circuit be evaluated thoroughly early in the design-in process with the mass-production capacitor of choice. This helps ensure that any such variability in capacitance does not negatively impact circuit performance.

8.2.2.4.1 Charge-Pump Output Capacitor

In typical applications, Texas Instruments recommends a 4.7-µF low-ESR ceramic charge-pump output capacitor (C_{CP}). Different output capacitance values can be used to reduce charge pump ripple, shrink the solution size, and/or cut the cost of the solution. However, changing the output capacitor may also require changing the flying capacitor or input capacitor to maintain good overall circuit performance.

In higher-current applications, a 10-µF, 10-V low-ESR ceramic output capacitor is recommended. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2-µF capacitance is recommended. For example, 10-µF, 10-V output capacitor in a 0402 case size typically has only 2-µF capacitance when biased to 5 V.

8.2.2.4.2 Input Capacitor

The input capacitor (C2) is a reservoir of charge that aids in a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. It also filters noise on the input pin, keeping this noise out of the sensitive internal analog circuitry that is biased off the input line.

Input capacitance has a dominant and first-order effect on the input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, a 4.7-µF low-ESR ceramic capacitor is recommended on the input. When operating near the maximum load of 250 mA, after taking into the DC bias derating, a minimum recommended input capacitance is 2 µF or larger. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution.

8.2.2.4.3 Flying Capacitor

The flying capacitor (C_1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM27762 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and charge pump output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 0.47-µF or 1-µF 10-V low-ESR ceramic capacitors are recommended for the flying capacitors. Polarized capacitors (tantalum, aluminum, electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM27762 operation.

8.2.2.4.4 LDO Output Capacitor

The LDO output capacitor (COUT+, COUT-) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27762 only requires the use of a 2.2-µF ceramic output capacitor for stable operation. For typical applications, a 2.2-µF ceramic output capacitor located close to the output is sufficient.

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8.2.2.5 Power Dissipation

The allowed power dissipation for any package is a measure of the ability of the device to pass heat from the junctions of the device to the heatsink and the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation can be calculated by Equation 4:

$$P_{D\text{-}MAX} = (T_{J\text{-}MAX} – T_A) / R_{\theta JA} \quad (4)$$

The actual power being dissipated in the device can be represented by Equation 5:

$$P_D = P_{IN} – P_{OUT} = V_{IN} \times (–I_{OUT–} + I_{OUT+} + I_Q) – (V_{OUT+} \times I_{OUT+} + V_{OUT–} \times I_{OUT–}) \quad (5)$$

Equation 4 and Equation 5 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These equations must be used to determine the optimum operating conditions for the device in a given application.

In lower power dissipation applications the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased. In higher power dissipation applications the maximum ambient temperature($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ can be calculated using Equation 6:

$$T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$$

where

- $T_{J\text{-}MAX\text{-}OP}$ = maximum operating junction temperature (125°C)
- $P_{D\text{-}MAX}$ = the maximum allowable power dissipation
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the package (6)

Alternately, if $T_{A\text{-}MAX}$ cannot be derated, the power dissipation value must be reduced. This can be accomplished by reducing the input voltage as long as the minimum V_{IN} is not violated, or by reducing the output current, or some combination of the two.

8.2.3 Application Curves

Refer also to Typical Characteristics

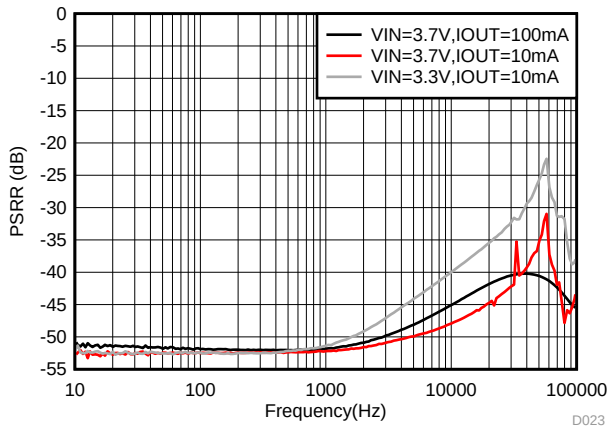

Figure 14. PSRR for OUT-

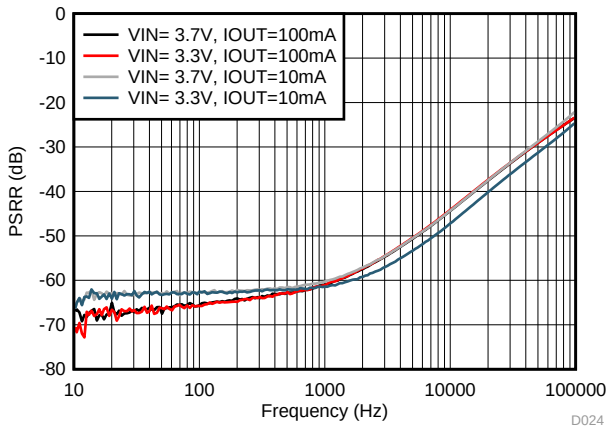

Figure 15. PSRR for OUT+

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9 Power Supply Recommendations

The LM27762 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the LM27762, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM27762 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place C_{IN} on the top layer (same layer as the LM27762) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching, which can corrupt the VIN line.
- Place C_{CPOUT} on the top layer (same layer as the LM27762) and as close as possible to the VOUT and GND pins. The returns for both C_{IN} and C_{CPOUT} must come together at one point, as close as possible to the GND pin. Connecting C_{CPOUT} through short, wide traces reduces the series inductance on the VCPOUT and GND pins that can corrupt the VCPOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C_1 on top layer (same layer as the LM27762) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.
- Place C_{OUT+}, C_{OUT-} on the top layer (same layer as the LM27762) and as close to the respective OUT pin as possible. For best performance the ground connection for C_{OUT} must connect back to the GND connection at the thermal pad of the device.
- Place R_1 to R_4 on the top layer (same layer as LM27762) and as close as possible to the respective FB pin. For best performance the ground connection of R_2, R_4 must connect back to the GND connection at the thermal pad of the device.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

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10.2 Layout Example

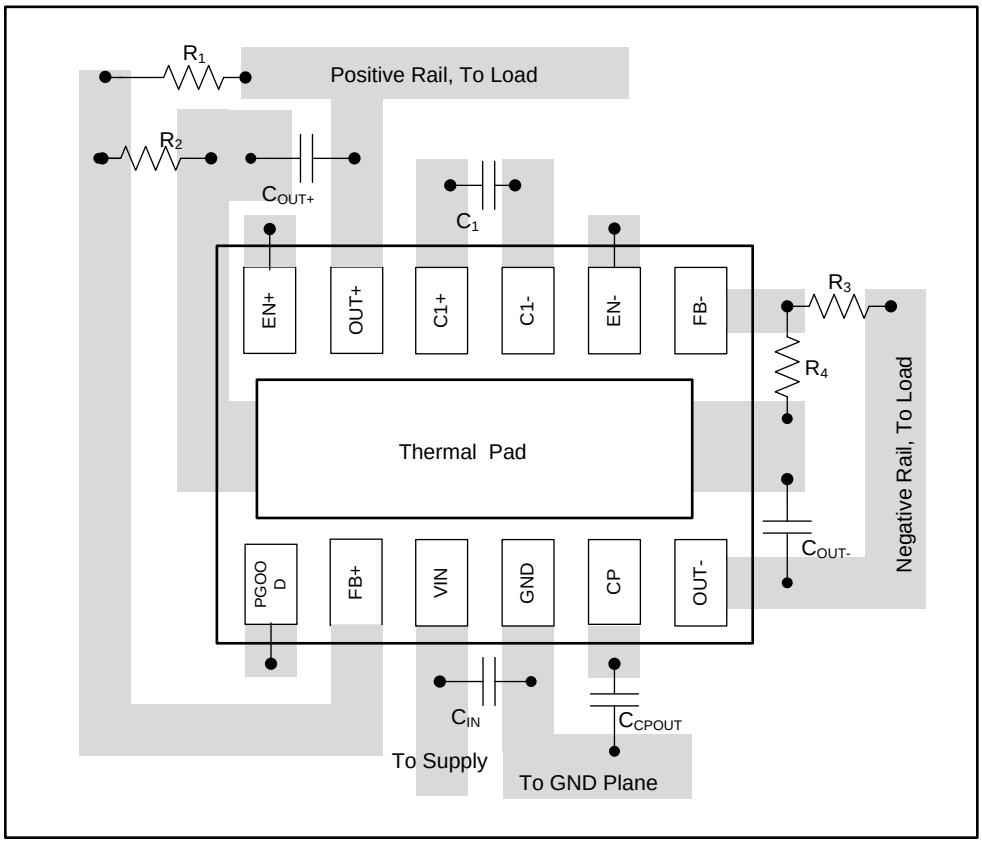

Figure 16. LM27762 Layout Example
(Note: Pullup resistor for PGOOD not shown in example.)

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11 Device and Documentation Support

11.1 Device Support

- *Using the LM27762EVM Evaluation Module*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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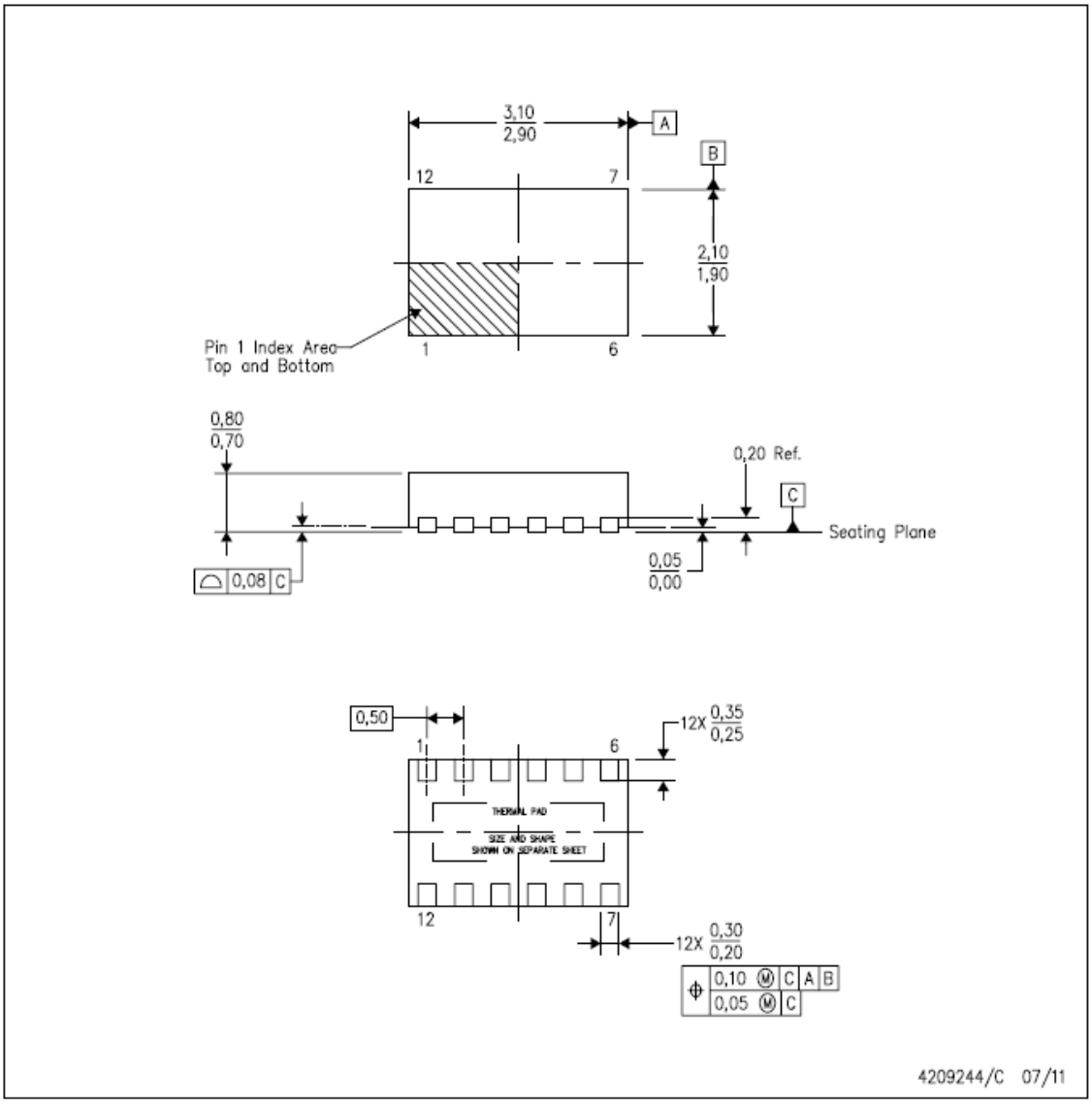
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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THERMAL PAD MECHANICAL DATA

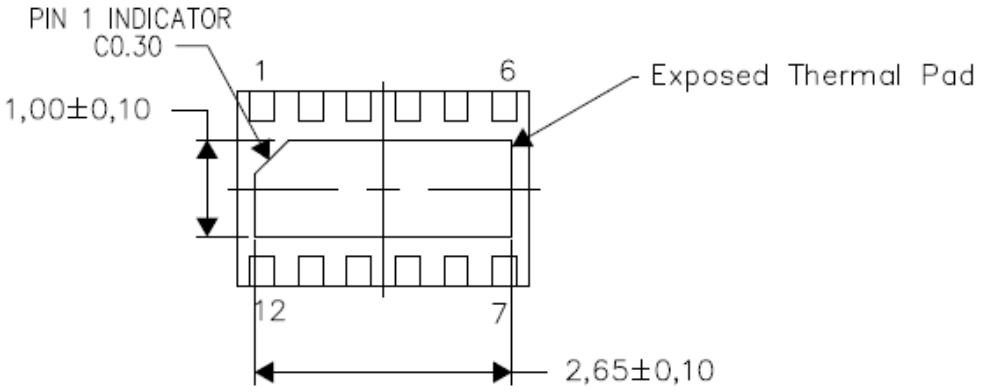
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4210135–3/D 02/16

NOTE: All linear dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27762DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	L27762	Samples
LM27762DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	L27762	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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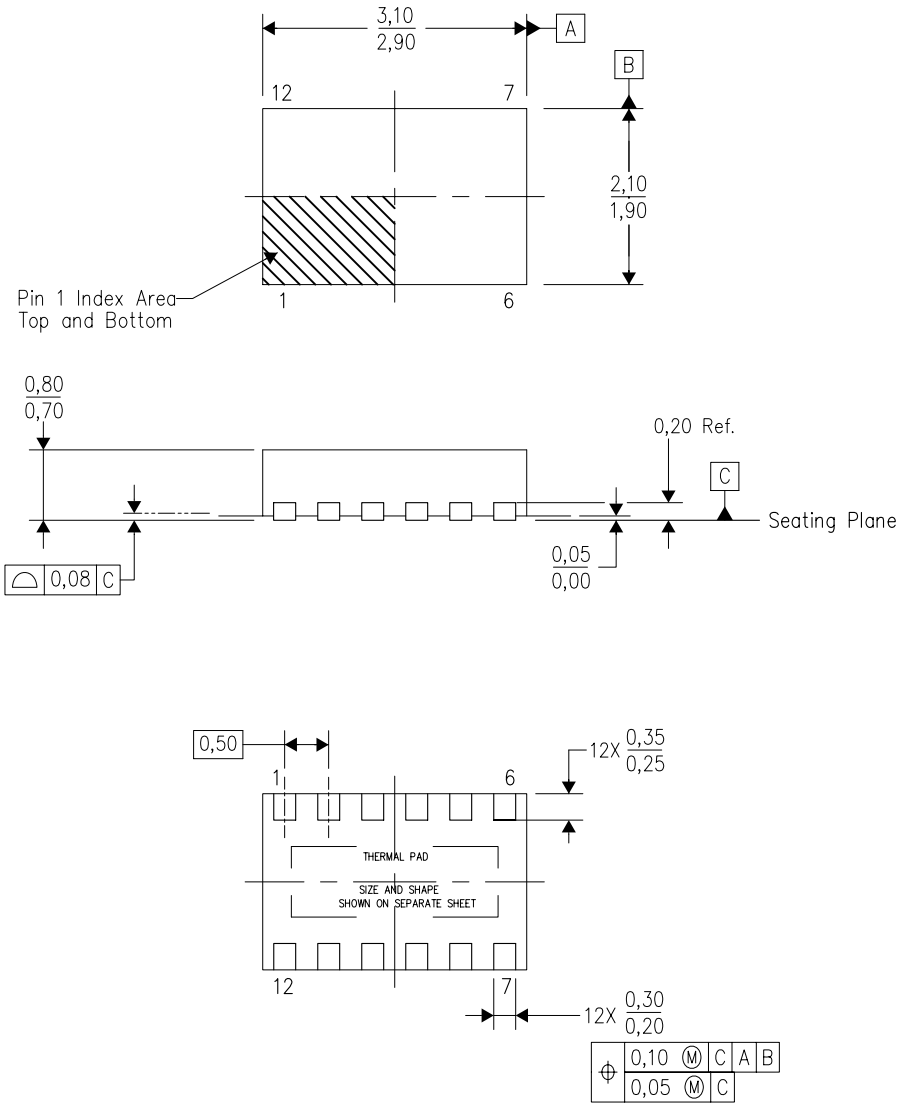

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NOTES:
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