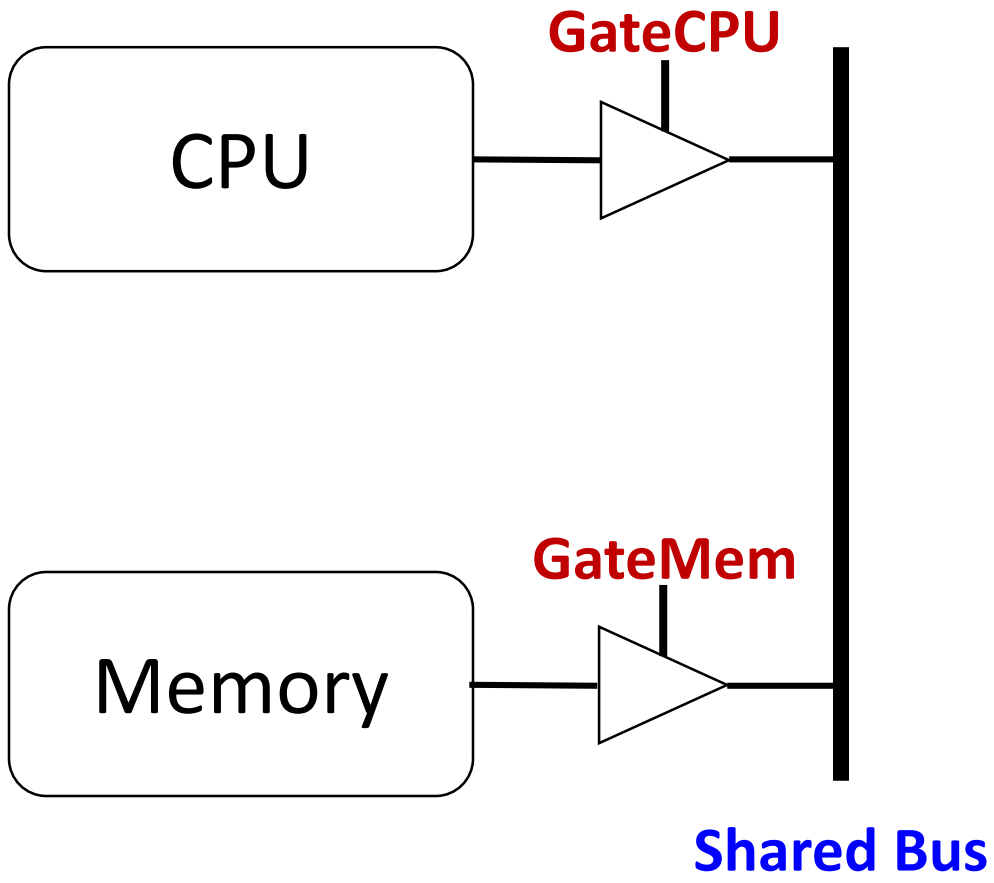
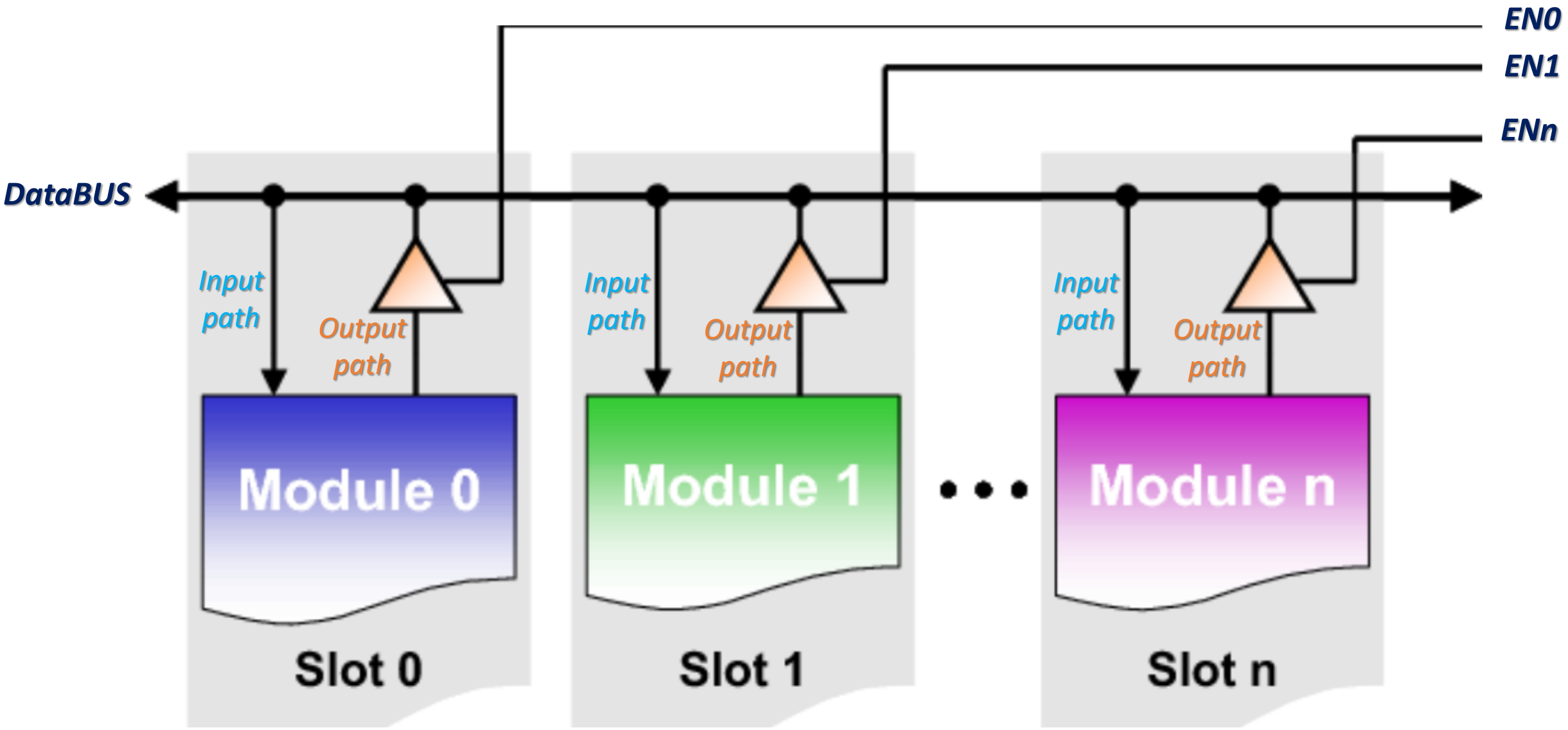
Design with Tri-State Buffers

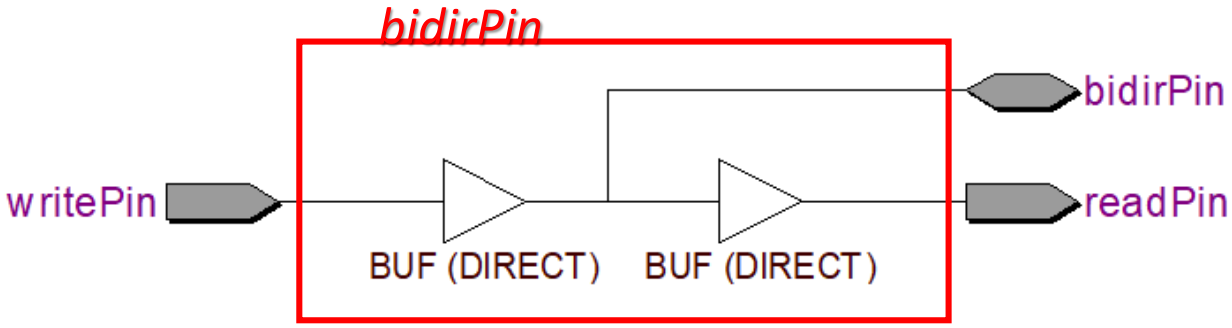


Bi-directional BUS

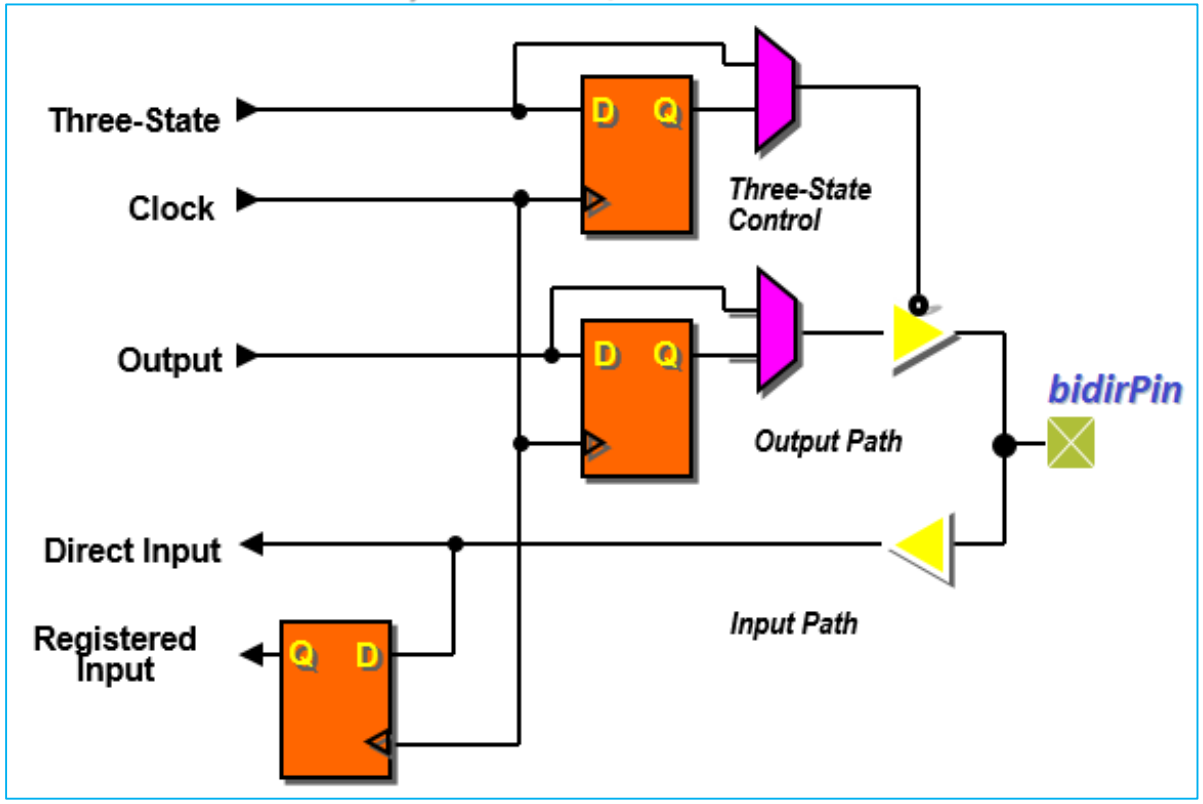


inout Pin synthesis - Bidirectional Pin

```
entity BidirPinBasic is
    port(   writePin: in    std_logic;
            readPin:  out   std_logic;
            bidirPin: inout std_logic
    );
end BidirPin;

architecture comb of BidirPinBasic is
begin

    readPin  <= bidirPin;
    bidirPin <= writePin;

end comb;
```



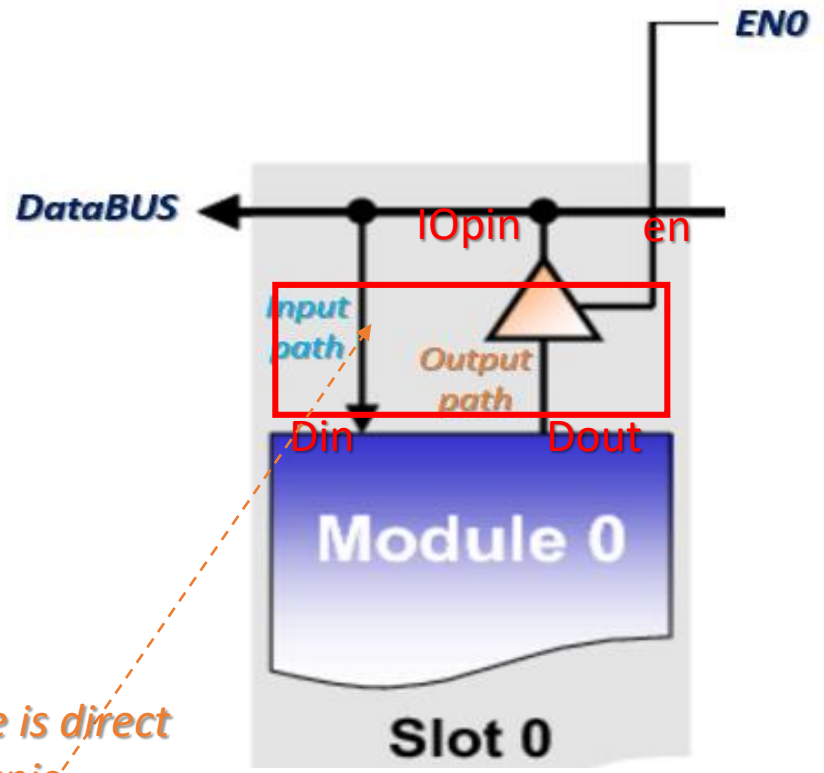
Cyclone II I/O Features



*Reading and writing from **inout** module pin is synthesized via buffer (as shown in the above RTL synthesis)*

Bi-directional BUS

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  ----------------------------------------------------------------
4  entity BidirPin is
5      generic( width: integer:=16 );
6      port(    Dout:   in      std_logic_vector(width-1 downto 0);
7               en:     in      std_logic;
8               Din:    out     std_logic_vector(width-1 downto 0);
9               IOpin:  inout   std_logic_vector(width-1 downto 0)
10     );
11 end BidirPin;
12
13 architecture comb of BidirPin is
14 begin
15
16     Din  <= IOpin;
17     IOpin <= Dout when(en='1') else (others => 'Z');
18
19 end comb;
```



There is direct galvanic connection but via buffer