

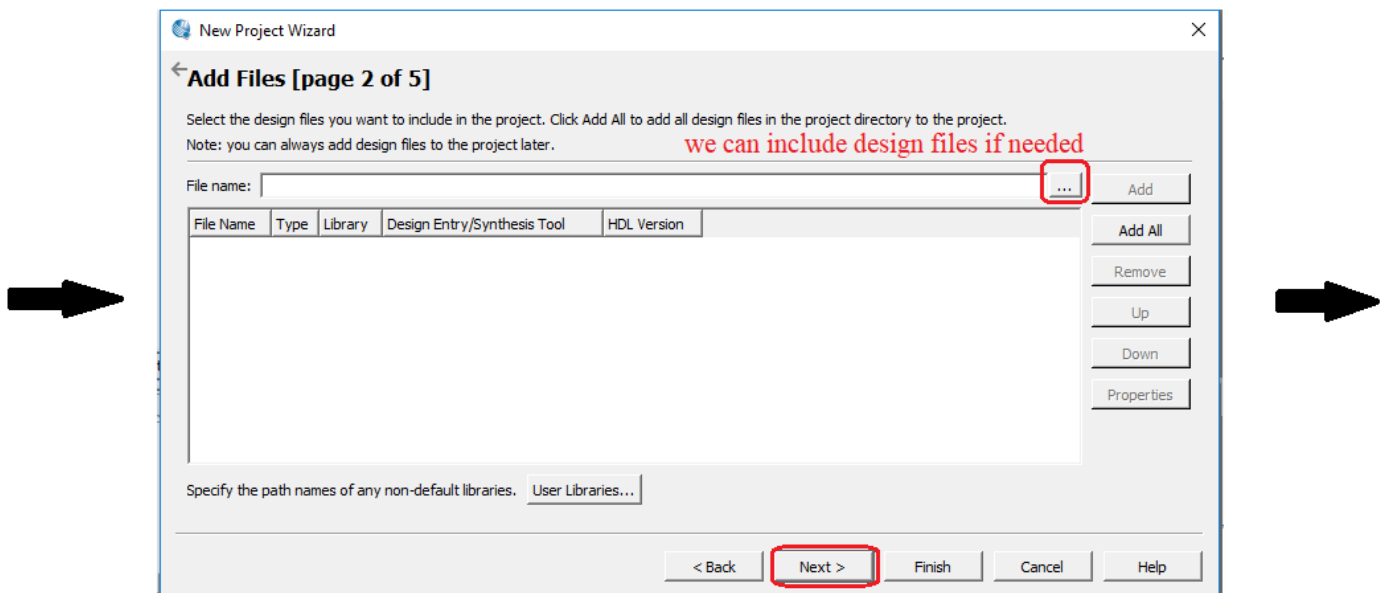
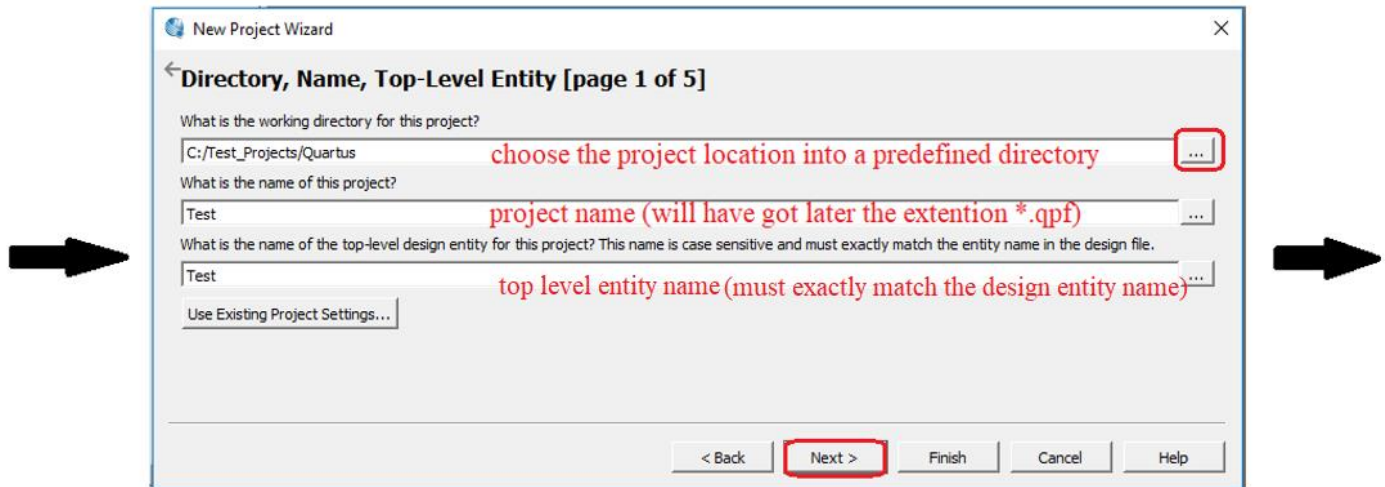
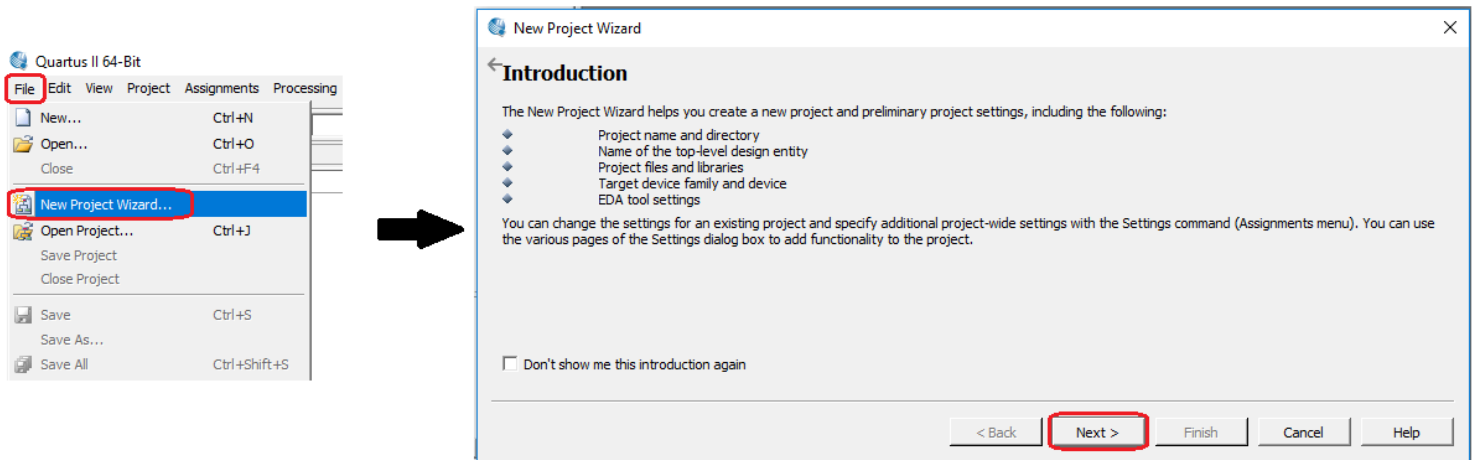
Table of Contents

A. Create a New Project:	2
1. Step 1 – create a new project and add VHDL files:	2
2. Step 2 – Add project files:	4
3. Step 3 – Code compilation:	5
4. Step 4 – Synthesis results:	8
5. Step 5 – Setting system constraints:	9
6. Step 6 – Pin Planner Layout:	10
7. Step 7 – Full compilation (finding of f_{max}):	11
8. Step 8 – Finding The Critical Path Location:	12
i. Technology Map Viewer:	14
ii. Resource Property Editor:	14
iii. Chip Planner:	15
9. Step 9 – Code Programming:	16
B. Verification – Using Signal TAP:	17
1. Block Diagram:	17
2. Using STP with a student activation license:	17
3. Create a new STP file:	18
4. Configurations (after expansion of the previous window):	19
5. Project Compilation and Programming (an eventually the Signals results):	22
C. Changing the VHDL source files of the project:	24
D. Open Existing Project:	24

Quartus - Create or Open a Project

A. Create a New Project:

1. Step 1 – create a new project and add VHDL files:



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: **Cyclone II**

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ **Specific device selected in 'Available devices' list**

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

☒ Show advanced devices ☐ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	G
EP2C20F256C7	1.2V	18752	152	239616	52	4	16
EP2C20F256C8	1.2V	18752	152	239616	52	4	16
EP2C20F256I8	1.2V	18752	152	239616	52	4	16
EP2C20F484C6	1.2V	18752	315	239616	52	4	16
EP2C20F484C7	1.2V	18752	315	239616	52	4	16
EP2C20F484C8	1.2V	18752	315	239616	52	4	16
EP2C20F484IR	1.2V	18752	315	239616	52	4	16

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back **Next >** Finish Cancel Help

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back **Next >** Finish Cancel Help

New Project Wizard

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory: C:/Test_Projects/Quartus

Project name: Test

Top-level design entity: Test

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: Cyclone II

Device: EP2C20F484C7

EDA tools:

Design entry/synthesis: <None> (<None>)

Simulation: ModelSim-Altera (VHDL)

Timing analysis: 0

Operating conditions:

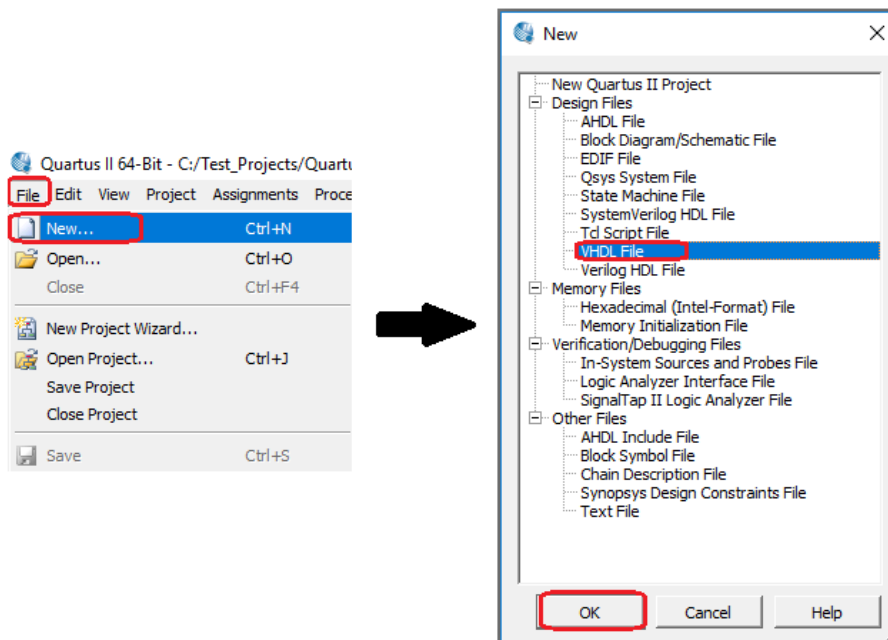
Core voltage: 1.2V

Junction temperature range: 0-85 °C

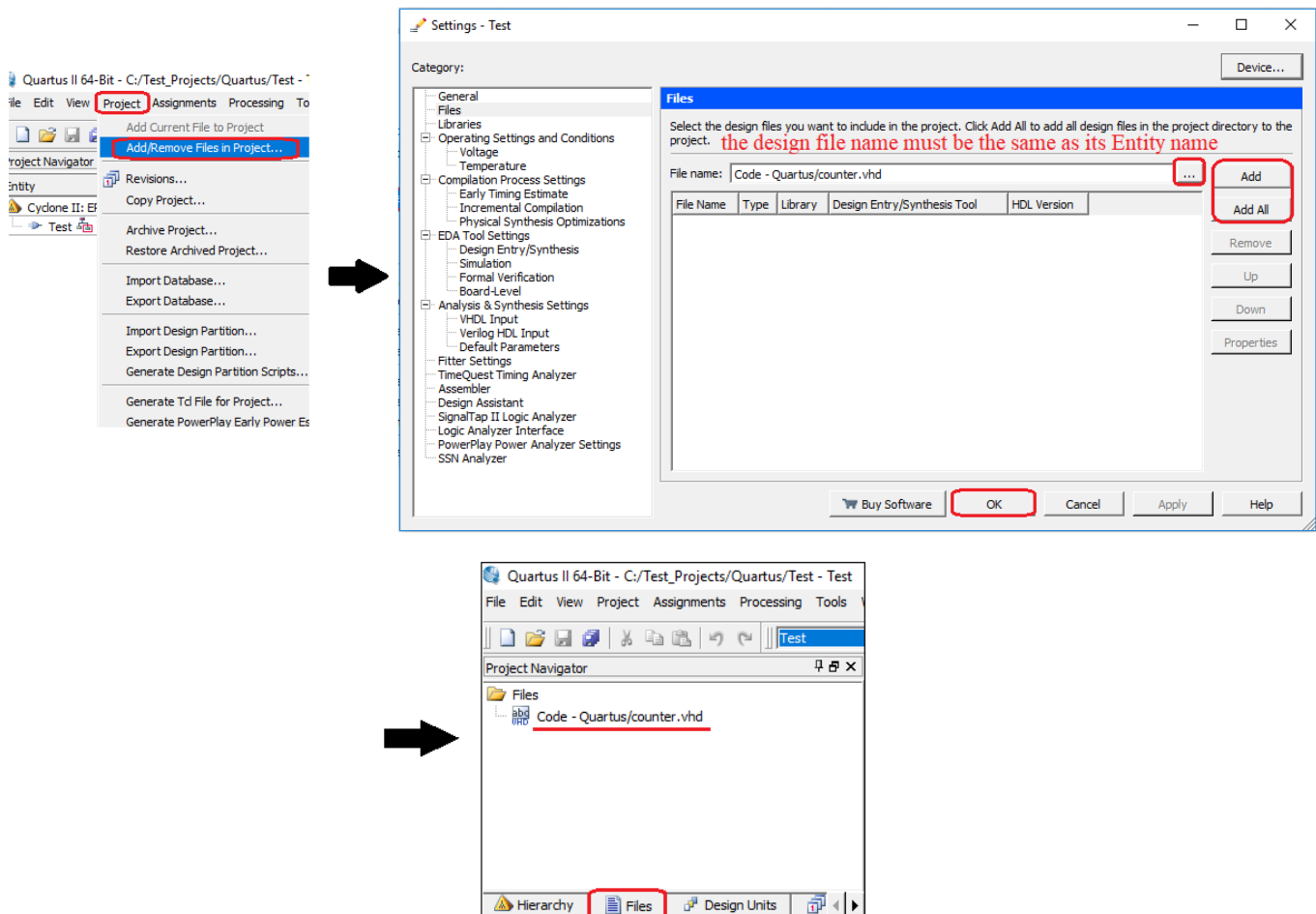
< Back Next > **Finish** Cancel Help

2. Step 2 – Add project files:

- a. In order to open VHDL blank file use the next step (if you're using VHDL existing files, copy these files into project folder and skip to clause b):

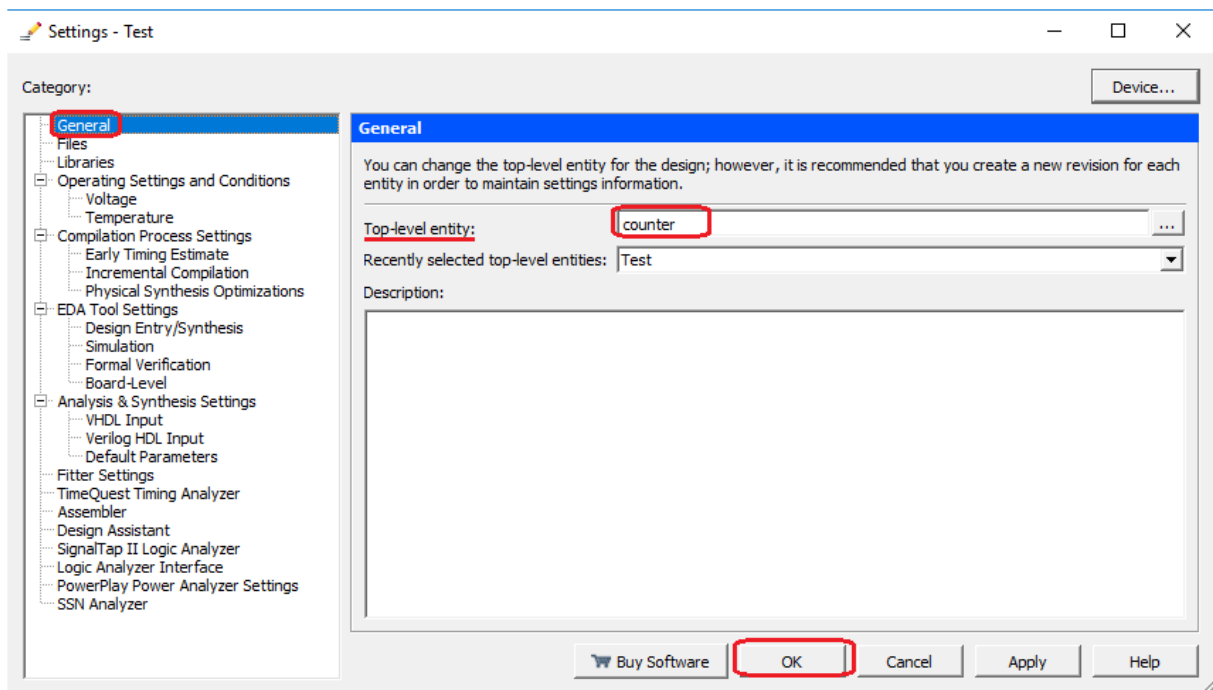
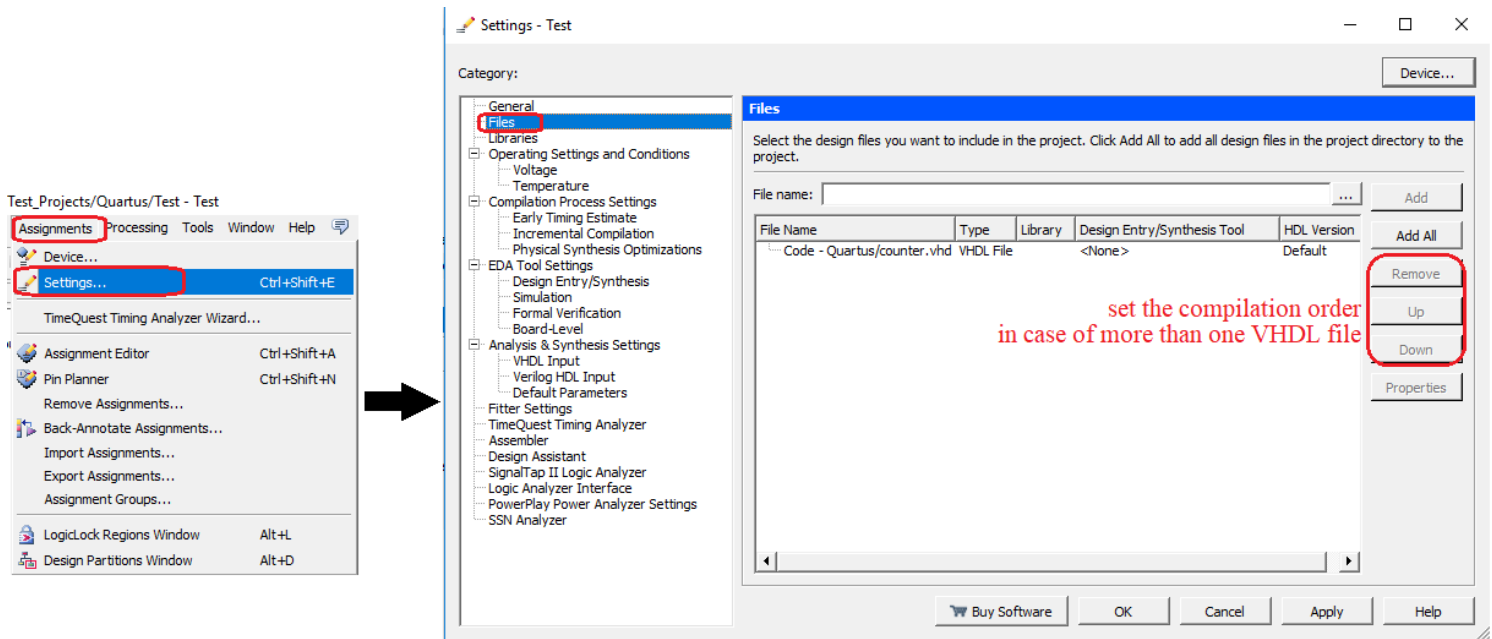


- b. Add the project VHDL existing files:



3. Step 3 – Code compilation:

a. Set the compilation order and top level entity:



counter.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity counter is port (
    clk,enable : in std_logic;
    q          : out std_logic_vector (7 downto 0));
end counter;

architecture rtl of counter is
    signal q_int : std_logic_vector (31 downto 0) :=x"00000000";
begin
    process (clk)
    begin
        if (rising_edge(clk)) then
            if enable = '1' then
                q_int <= q_int + 1;
            end if;
        end if;
    end process;
    q <= q_int(31 downto 24); -- Output only 8MSB
end rtl;
```

Example application:

- 32bit behavioral counter with enable
- 8 MSB connected to green LEDs
- Enable connected to switch
- Clock to 50MHz onboard oscillator

b. Code compilation:

Quartus II 64-bit - C:/Test_Projects/Quartus/Test - Test

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Files

- Code - Quartus/counter.vhd

Tasks

Flow: Compilation Customize...

Task	Status
Compile Design	00
Analysis & Synthesis	00
Fitter (Place & Route)	00
Assembler (Generate programming files)	00
TimeQuest Timing Analysis	00
EDA Netlist Writer	00
Program Device (Open Programmer)	

Compilation Report - Test

Flow Summary

Flow Status: Successful - Tue Mar 26 15:04:19 2019

Quartus II 64-bit Version: 12.1 Build 177 11/07/2012 SJ Web Edition

Revision Name: Test

Top-level Entity Name: counter

Family: Cyclone II

Device: EP2C20F484C7

Timing Models: Final

Total logic elements: 32 / 18,752 (< 1 %)

Total combinational functions: 32 / 18,752 (< 1 %)

Dedicated logic registers: 32 / 18,752 (< 1 %)

Total registers: 32

Total pins: 10 / 315 (3 %)

Total virtual pins: 0

Total memory bits: 0 / 239,616 (0 %)

Embedded Multiplier 9-bit elements: 0 / 52 (0 %)

Total PLLs: 0 / 4 (0 %)

Quartus II

Full Compilation was successful (11 warnings)

OK

c. Start analysis and synthesis:

File Edit View Project Assignments Processing Tools Window Help

Compilation Report - Test

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis

Flow Summary

Flow Status: Successful - Tue Mar 26 15:13:14 2019

Quartus II 64-bit Version: 12.1 Build 177 11/07/2012 SJ Web Edition

Revision Name: Test

Top-level Entity Name: counter

Family: Cyclone II

Device: EP2C20F484C7

Timing Models: Final

Total logic elements: 32

Total combinational functions: 32

Dedicated logic registers: 32

Total registers: 32

Total pins: 10

Total virtual pins: 0

Total memory bits: 0

Embedded Multiplier 9-bit elements: 0

Total PLLs: 0

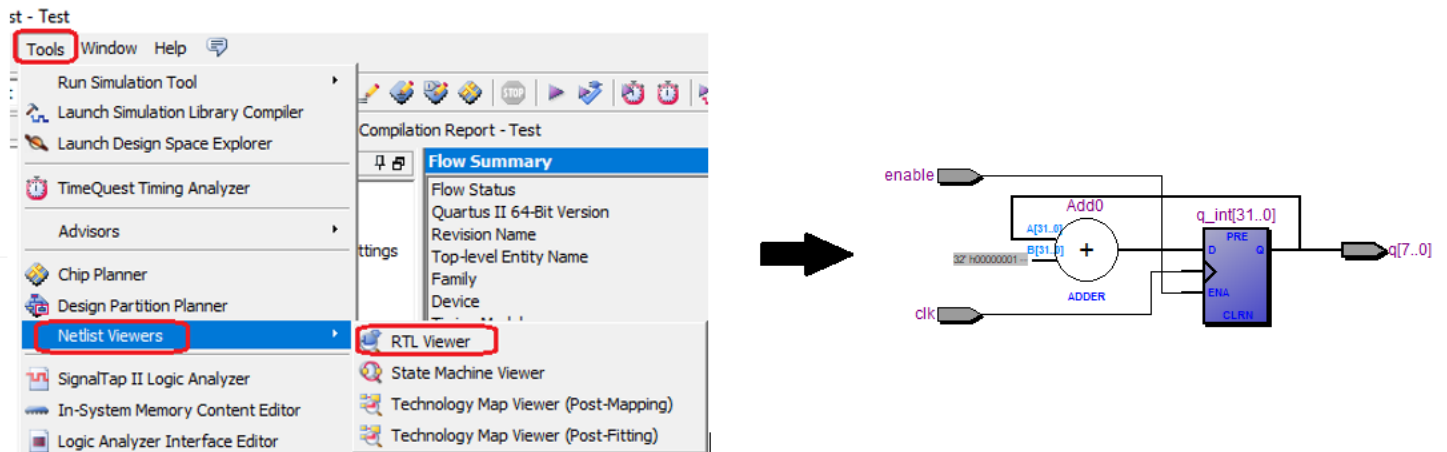
Quartus II

Analysis & Synthesis was successful (1 warning)

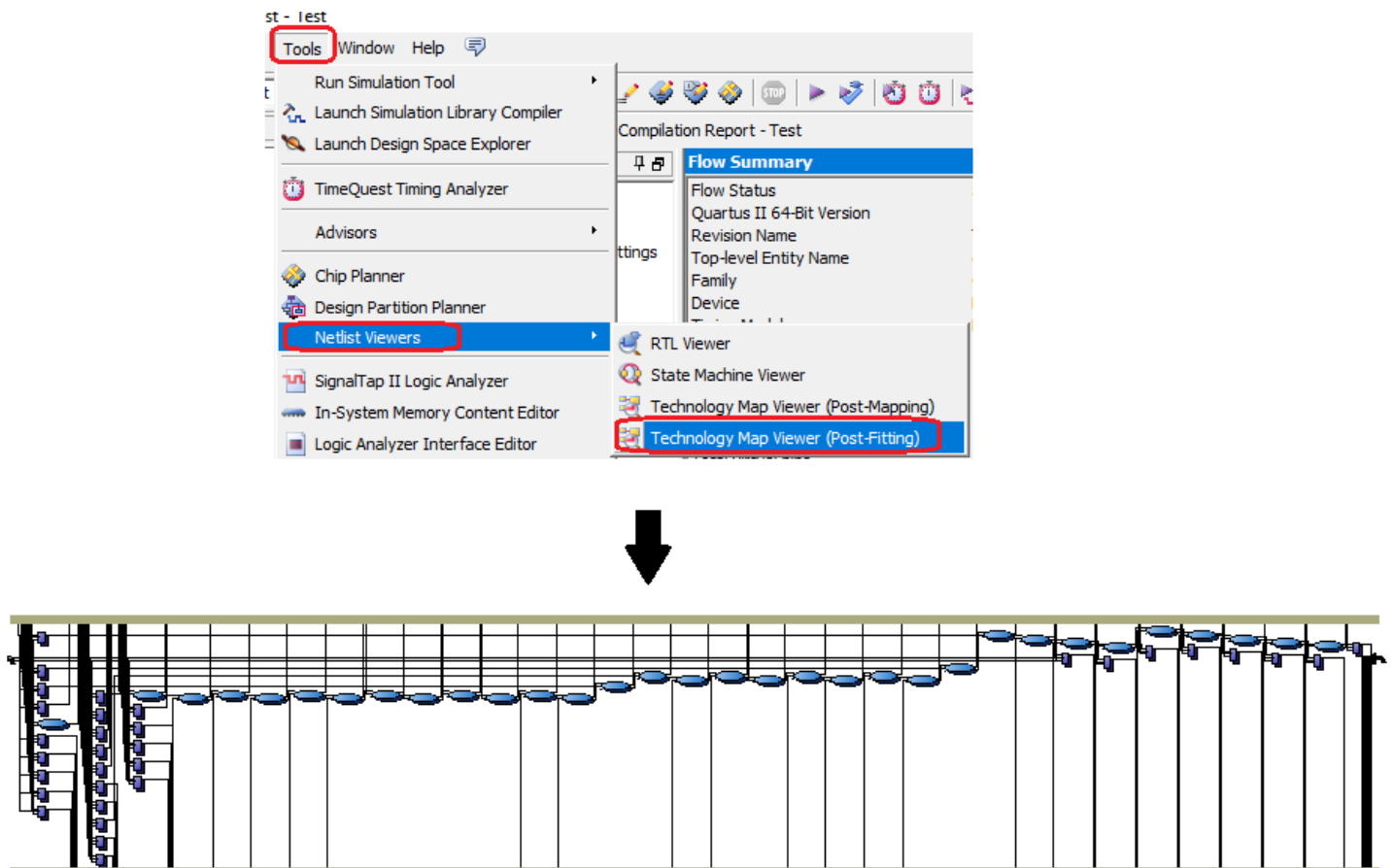
OK

4. Step 4 – Synthesis results:

a. Synthesis RTL viewer:

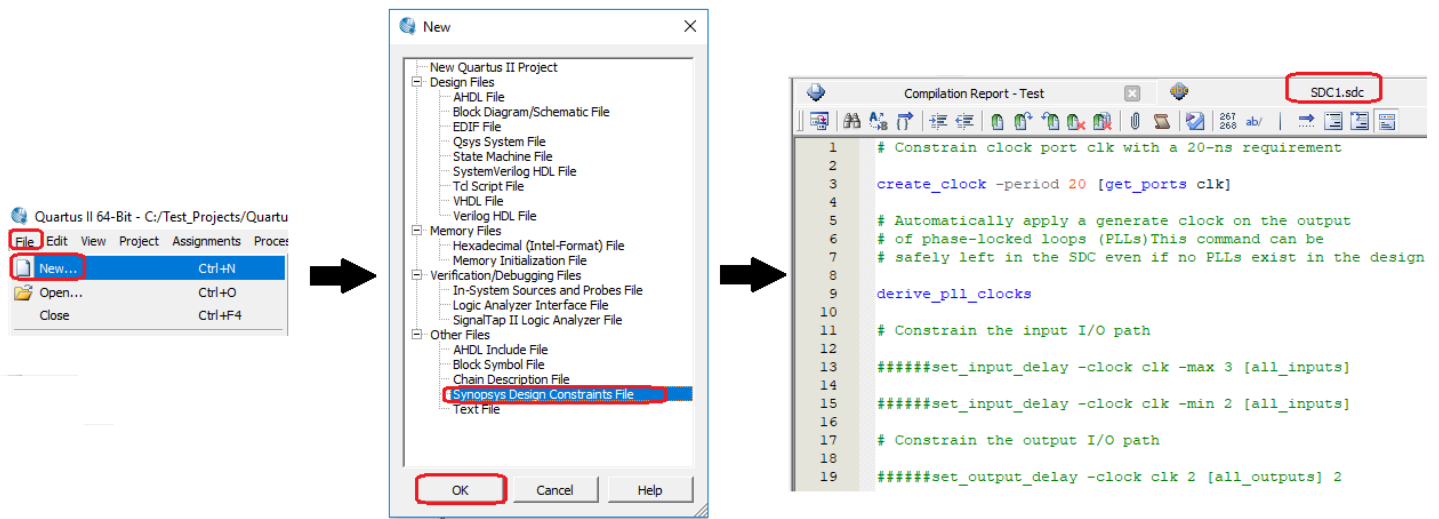


b. Synthesis Map (Post-Fitting) viewer (LEs and FFs combination):

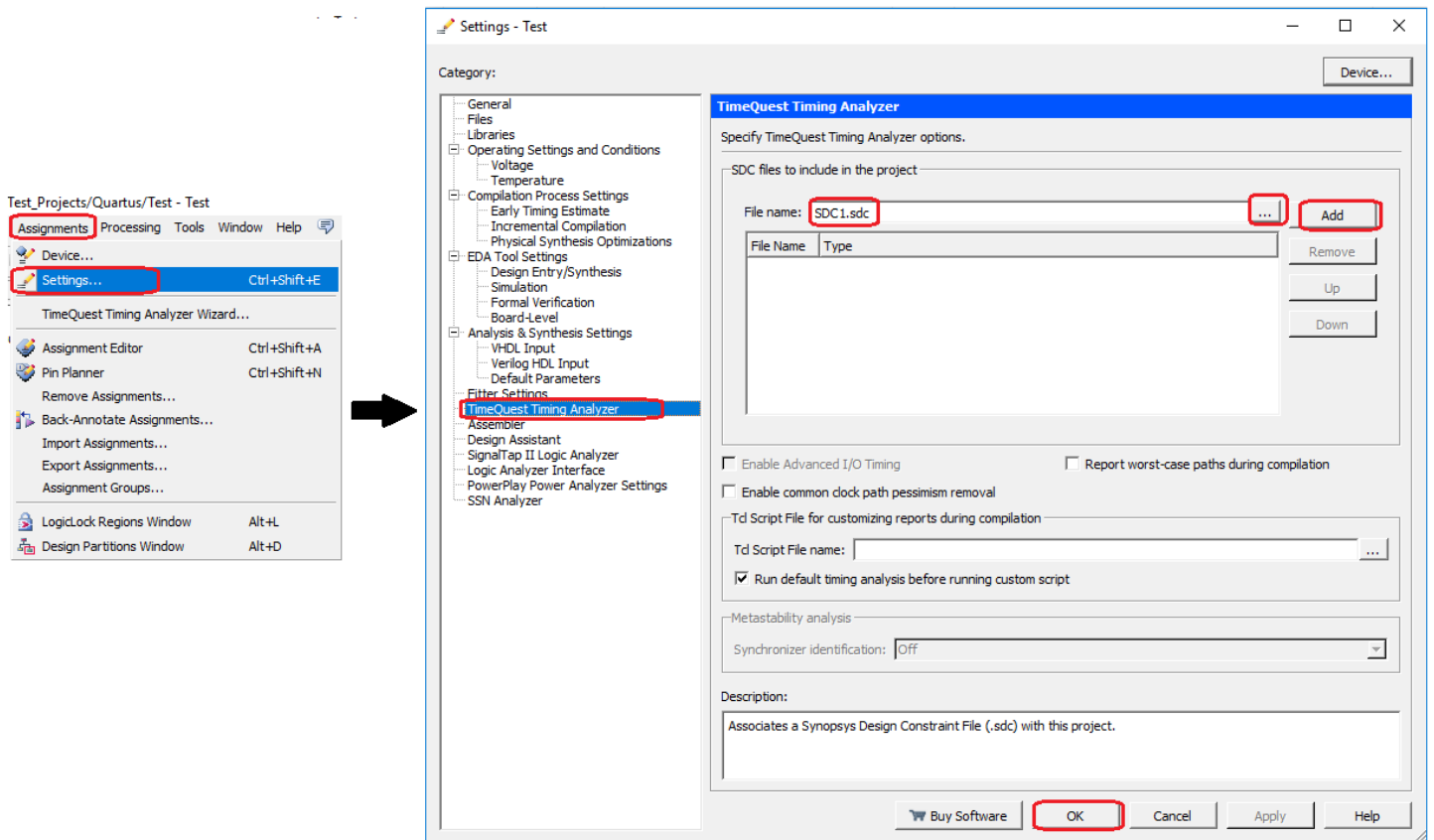


5. Step 5 – Setting system constraints:

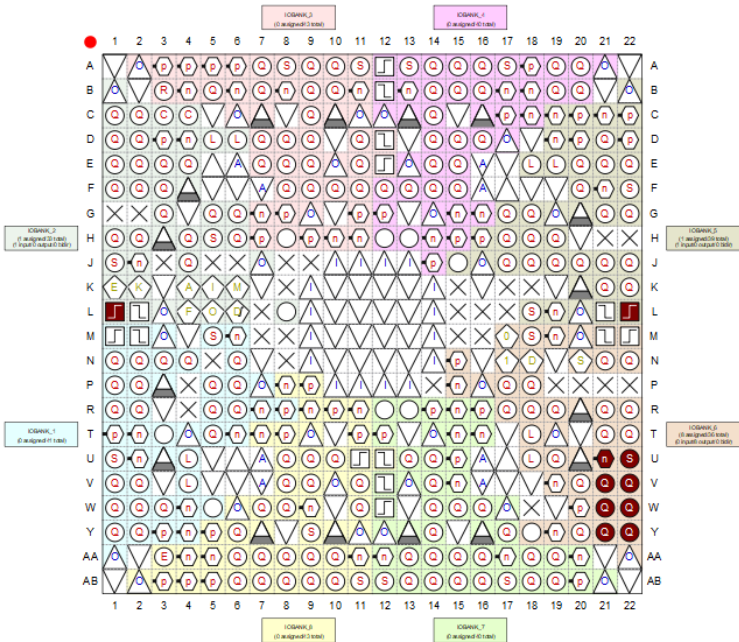
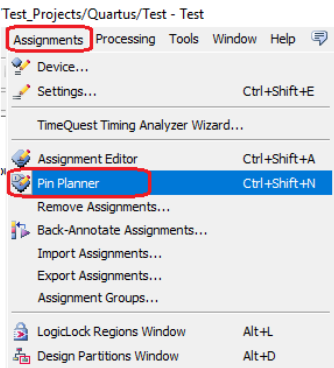
a. Create the system constraints *.sdc file:



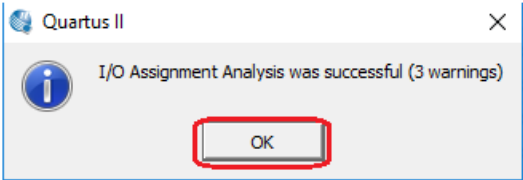
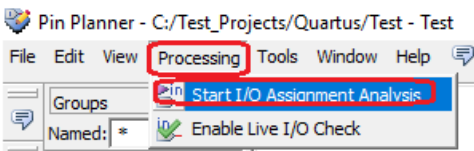
b. Add the *.sdc file to the project:



6. Step 6 – Pin Planner Layout:



Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Differential Pair
clk	Input	PIN_L1	2	B2_N1	3.3-V LVTTTL (default)		24mA (default)	
enable	Input	PIN_L22	5	B5_N1	3.3-V LVTTTL (default)		24mA (default)	
q[7]	Output	PIN_Y21	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[6]	Output	PIN_Y22	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[5]	Output	PIN_W21	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[4]	Output	PIN_W22	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[3]	Output	PIN_V21	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[2]	Output	PIN_V22	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[1]	Output	PIN_U21	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	
q[0]	Output	PIN_U22	6	B6_N1	3.3-V LVTTTL (default)		24mA (default)	



Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D12, PIN_E12	27 MHz clock input
CLOCK_50	PIN_L1	50 MHz clock input
CLOCK_24	PIN_A12, PIN_B12	24 MHz clock input from USB Blaster
EXT_CLOCK	PIN_M21	External (SMA) clock input

Table 4.5. Pin assignments for the clock inputs.

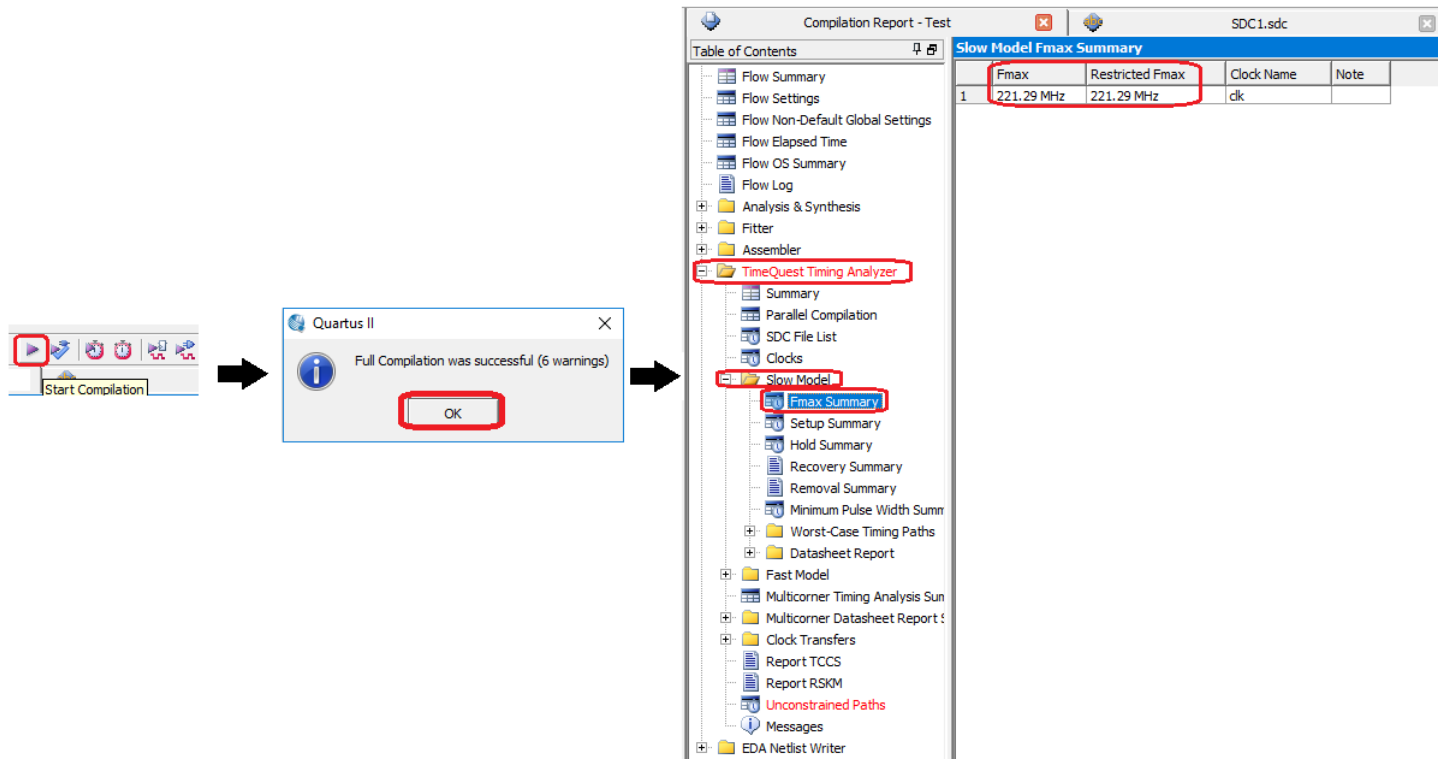
Signal Name	FPGA Pin No.	Description
SW[0]	PIN_L22	Toggle Switch[0]

Table 4.1. Pin assignments for the toggle switches.

LEDG[0]	PIN_U22	LED Green[0]
LEDG[1]	PIN_U21	LED Green[1]
LEDG[2]	PIN_V22	LED Green[2]
LEDG[3]	PIN_V21	LED Green[3]
LEDG[4]	PIN_W22	LED Green[4]
LEDG[5]	PIN_W21	LED Green[5]
LEDG[6]	PIN_Y22	LED Green[6]
LEDG[7]	PIN_Y21	LED Green[7]

Table 4.3. Pin assignments for the LEDs.

7. Step 7 – Full compilation (finding of f_{max}):



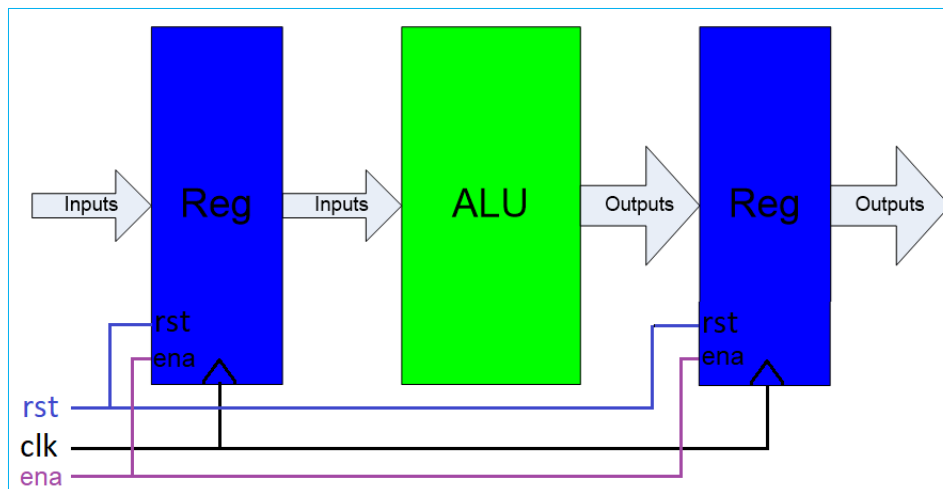
Compilation Report - Test SDC1.sdc

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analyzer
- Summary
- Parallel Compilation
- SDC File List
- Clocks
- Slow Model
- Fmax Summary
- Setup Summary
- Hold Summary
- Recovery Summary
- Removal Summary
- Minimum Pulse Width Summ
- Worst-Case Timing Paths
- Datasheet Report
- Fast Model
- Multicorner Timing Analysis Sun
- Multicorner Datasheet Report !
- Clock Transfers
- Report TCCS
- Report RSKM
- Unconstrained Paths
- Messages
- EDA Netlist Writer

Slow Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	221.29 MHz	221.29 MHz	clk	



Explanation: In order Quartus IDE can calculate f_{max} the logic design parts must be wrapped by registers

8. Step 8 – Finding The Critical Path Location:

The screenshot illustrates the steps to generate a timing report in the TimeQuest Timing Analyzer. On the left, a secondary window shows the 'Tools' menu with 'TimeQuest Timing Analyzer' highlighted. A large black arrow points to the main application window. In the main window, the 'Tasks' pane on the left lists various reports, with 'Report Timing...' selected and a red box around it. A red text label 'Mouse right click' points to this item. A context menu is open over 'Report Timing...', showing 'Start' and 'Start Again' options, with 'Start' highlighted by a red box. The 'Report' pane at the top shows 'Report not available'. The right side of the interface features a 'Getting Started' panel with a 'Welcome' message and sections for 'Report P' and 'Tasks Pa'. The bottom 'Console' pane displays Tcl commands and their outputs, including 'project_open -force "C:/Test_Projects/Quartus/Test.qpf" -revision T'.

TimeQuest Timing Analyzer - C:/Test_Projects/Quartus/Test - Test

File View Netlist Constraints Reports Script Tools Window Help

Report

Report not available

Tasks

Report Setup Summary
Report Hold Summary
Report Recovery Summary
Report Removal Summary
Report Minimum Pulse Width Summary
Report Max Skew Summary
Datasheet
Report Fmax Summary
Report Datasheet
Device Specific
Report TCCS
Report RSKM
Report DDR
Report Metastability
Diagnostic
Report Clocks
Report Clock Transfers
Report Unconstrained Paths
Report SDC
Report Ignored Constraints
Check Timing
Report Partitions
Custom Reports
Report Timing...
Report Minimum P...
Report False Path...
Report Path...
Report Exceptions...
Report Bottlenecks...
Report Net Timing...
Report Skew...
Report Max Skew...

Mouse right click

Start
Start Again

Getting Started

Welcome

The TimeQuest timing performance reporting module provides all timing performance interface features.

Report P

Lists general report pane

Tasks Pa

Lists commands you can perform. You can do click a command to start a process or flow.

Console

assumed to be external and are run using Tcl's "exec" command.
- Type "exit" to exit.
- Type "help" to view a list of Quartus II Tcl packages.
- Type "help <package name>" to view a list of Tcl commands available for the specified Quartus II Tcl package.
- Type "help -tcl" to get an overview on Quartus II Tcl usages.

tcl> project_open -force "C:/Test_Projects/Quartus/Test.qpf" -revision T
tcl>

Report Timing

Clocks
 From clock:
 To clock:

Targets
 From:
 Through:
 To:

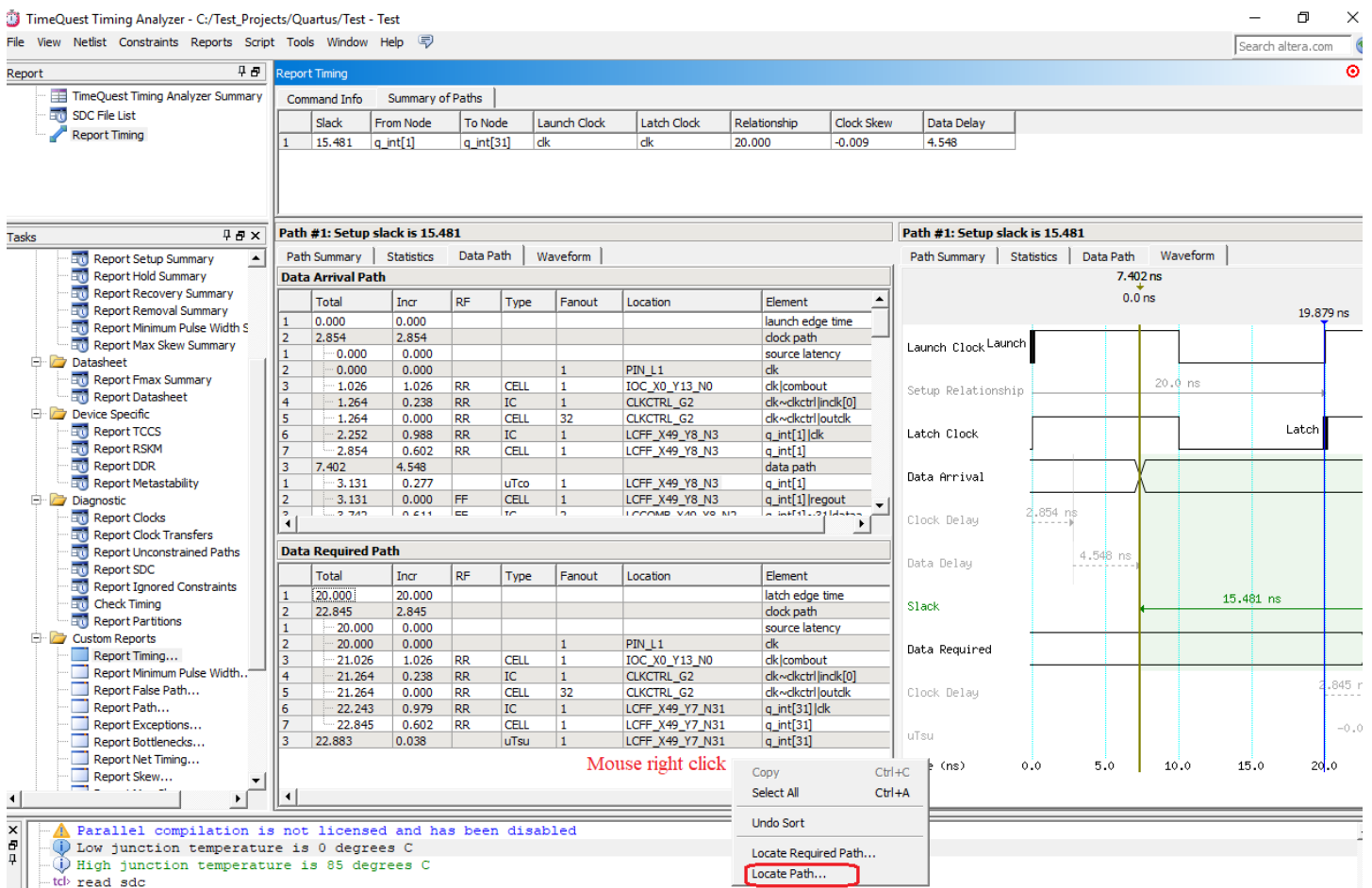
Analysis type
☒ Setup
☐ Hold
☐ Recovery
☐ Removal

Paths
 Report number of paths: 1
 Maximum number of paths per endpoint:
 Maximum slack limit: ns
☐ Pairs only

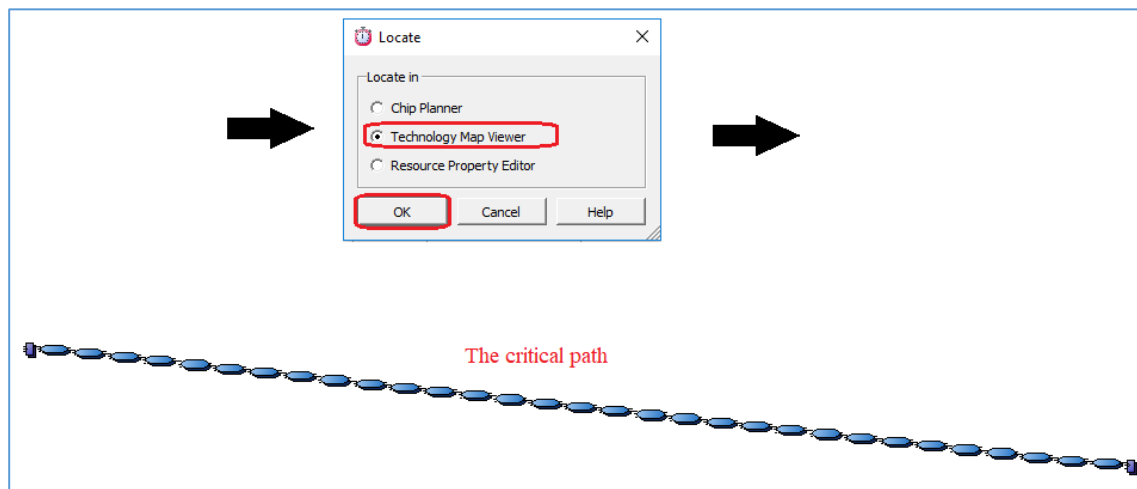
Output
 Detail level: Full path
☐ Show routing
☒ Report panel name: Report Timing
☐ File name:
 File options:
☒ Overwrite ☐ Append
☐ Console
 Open

Td command: report_timing -setup -npaths 1 -detail full_path -panel_name {Report Timing}

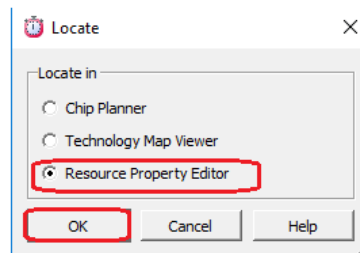
Report Timing Close Help



i. Technology Map Viewer:



ii. Resource Property Editor:



Resource Property Editor - C:/Test_Projects/Quartus/Test - Test

Resource Property Editor - C:/Test_Projects/Quartus/Test - Test

Node Name | Location

Node Name	Location
<input checked="" type="checkbox"/> [counter]q_int[10]~49	LCCOMB_X49_Y8_N20
<input type="checkbox"/> [counter]q_int[11]~51	LCCOMB_X49_Y8_N22
<input type="checkbox"/> [counter]q_int[12]~53	LCCOMB_X49_Y8_N24
<input type="checkbox"/> [counter]q_int[13]~55	LCCOMB_X49_Y8_N26
<input type="checkbox"/> [counter]q_int[14]~57	LCCOMB_X49_Y8_N28
<input type="checkbox"/> [counter]q_int[15]~59	LCCOMB_X49_Y8_N30
<input type="checkbox"/> [counter]q_int[16]~61	LCCOMB_X49_Y7_N0
<input type="checkbox"/> [counter]q_int[17]~63	LCCOMB_X49_Y7_N2
<input type="checkbox"/> [counter]q_int[18]~65	LCCOMB_X49_Y7_N4
<input type="checkbox"/> [counter]q_int[19]~67	LCCOMB_X49_Y7_N6
<input type="checkbox"/> [counter]q_int[1]	LGFF_X49_Y8_N3
<input type="checkbox"/> [counter]q_int[1]~31	LCCOMB_X49_Y8_N2
<input type="checkbox"/> [counter]q_int[20]~69	LCCOMB_X49_Y7_N8
<input type="checkbox"/> [counter]q_int[21]~71	LCCOMB_X49_Y7_N10

Logic Resource(s) | IO_PIN(s) | CLKCTRL(s)

Properties/Modes | Values

Properties/Modes	Values
Sum LUT Mask	SA5F
Carry LUT Mask	SF5F
Operation Mode	arithmetic
Latch Type	none
Sum Equation	A & IC # 1A & (C # 1D)
Carry Equation	1C # 1A

Register | Combinational

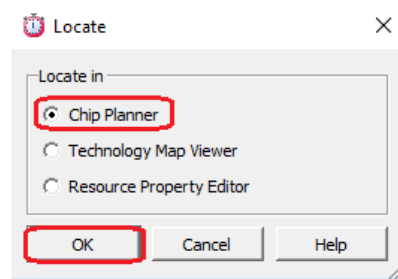
Input Port Name | Signal Name | Inverted

Input Port Name	Signal Name	Inverted
EN	[counter]enable	False
SCLR	<Disconnected>	False
IACLR	<Disconnected>	False
SDATA	<Disconnected>	False
DATAIN	[counter]q_int[10]~49	False
SLOAD	<Disconnected>	False
CLK	[counter]clk~clkctrl	False

Output Port Name | Signal Name

Output Port Name	Signal Name
REGOUT	[counter]q_int[10]
COUT	[counter]q_int[10]~50
COMBOUT	[counter]q_int[10]~49

iii. Chip Planner:



Coordinate: Editing Mode: ECO - EP2C20F484C7

Layers Settings

Basic

- ☒ Background
 - ☐ None
 - ☒ Block Utilization
 - ☐ Design Partition P...
- ☒ LogicLock Regions
 - ☒ User-assigned Lo...
 - ☒ Fitter-placed Logi...
- ☐ Clock Regions
 - ☐ Global Clock Region
 - ☐ Local Clock Region
 - ☐ LVDS Clock Region
 - ☐ Regional Clock R...
 - ☐ Periphery Clock ...
- ☒ Overlay Objects
 - ☒ Connection Lines
 - ☒ Labels
 - ☒ Differential Pin P...
 - ☒ Report Overlay

Layers Settings Color Legend

Properties

Selected elements:

General

Timing

Located Objects

Located 1 paths

Time	Object
15.481	q_int[1] -> q_int[31]
1.026ns	clk -> q_int[1]
0.238ns	clk -> clk~clkctrl
0.000ns	clk~clkctrl -> clk~clkctrl
0.988ns	clk~clkctrl -> q_int[1]
0.602ns	q_int[1] -> q_int[1]
Arrival Data	q_int[1] -> q_int[31]
(Required Clock)	clk -> q_int[31]

9. Step 9 – Code Programming:

Programmer - C:/Test_Projects/Quartus/Test - Test - [output_files/Test.cdf]

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG

☒ Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase
output_files/Test.sof	EP2C20F484	001B38FE	FFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

TDI → EP2C20F484 ← TDO

Programmer - C:/Test_Projects/Quartus/Test - Test - [output_files/Test.cdf]

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Successful)

☒ Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

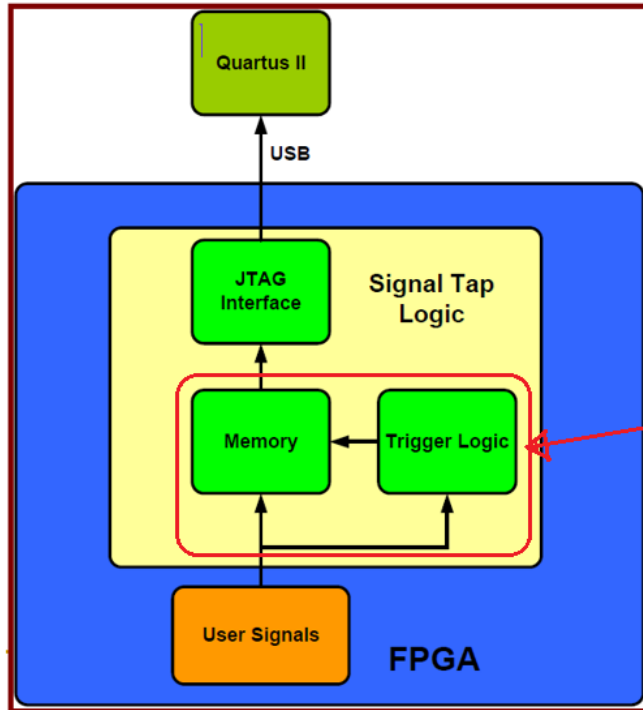
Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/Test.sof	EP2C20F484	001B38FE	FFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

TDI → EP2C20F484 ← TDO

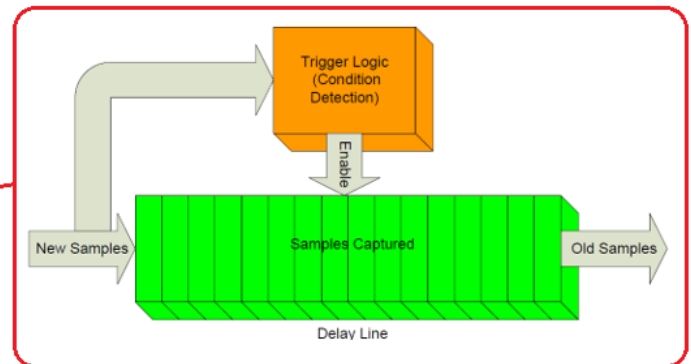
B. Verification – Using Signal TAP:

1. Block Diagram:



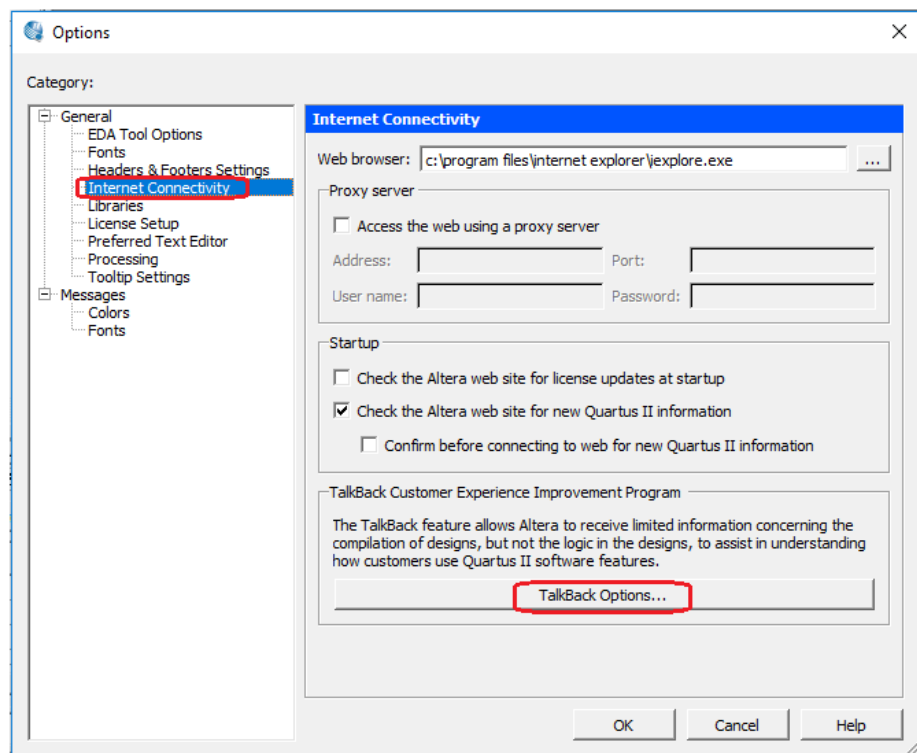
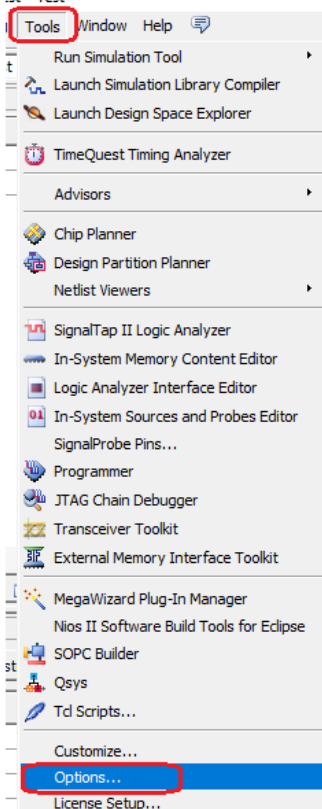
Signal TAP Pros & Cons:

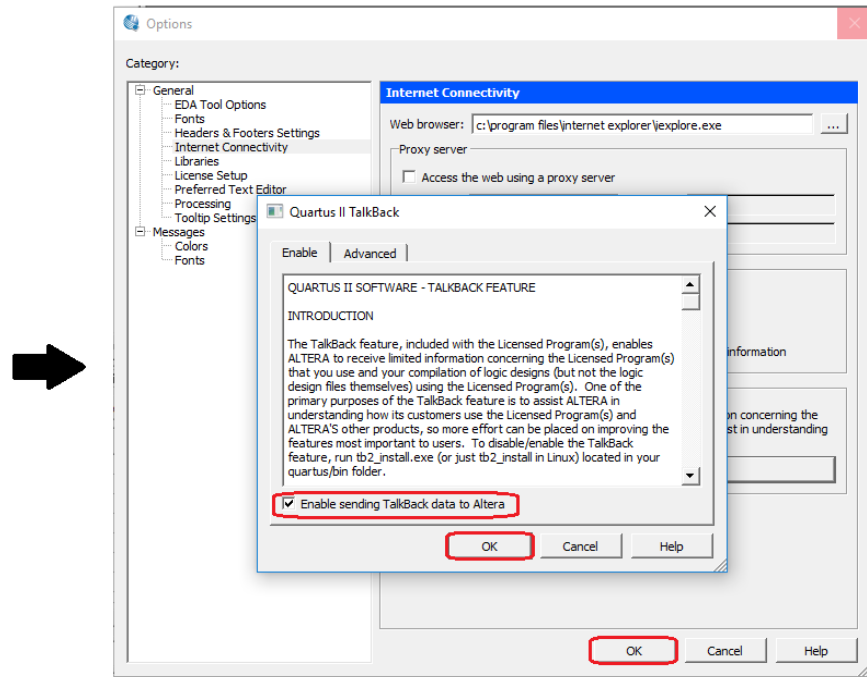
- Captures real time state of FPGA internal signals and pins (up to 200MHz)
- Connects to Quartus II through JTAG
- Do not require huge and expensive equipment
- Uses internal FPGA resources
 - Memory Blocks
 - Logic Elements
- Each time the captured signals list change the design must be recompiled



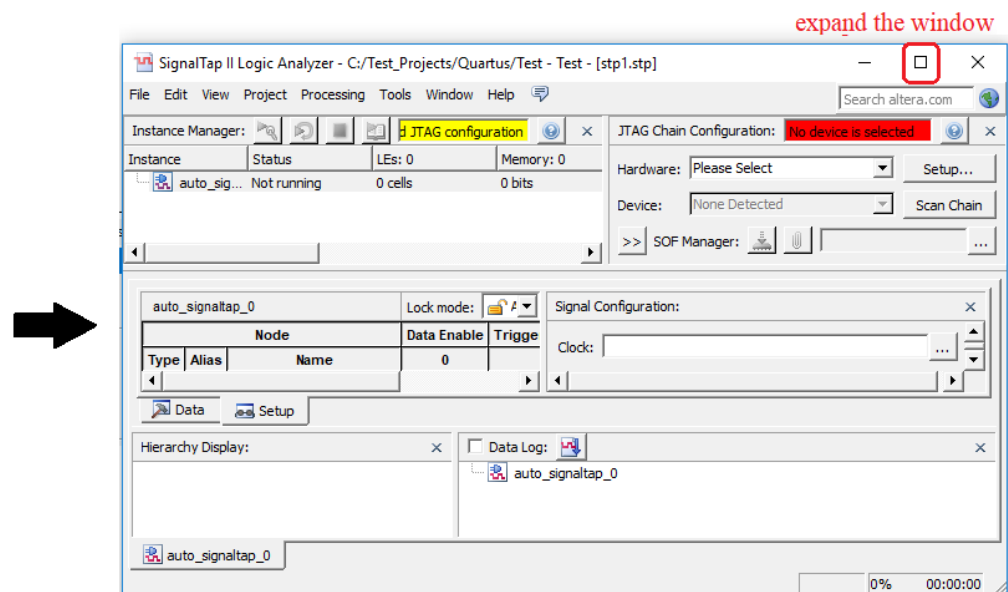
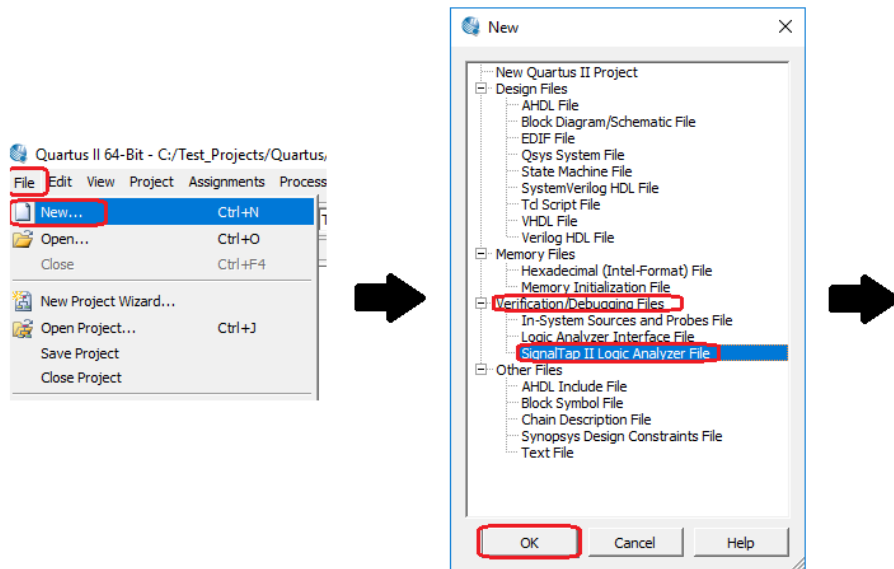
Signal TAP Features:

- Up to 1024 Data Channels
- Multiple Analyzers in One Device
 - Supports Analysis of Multiple Clock Domains
 - Each Analyzer Can Run Simultaneously
- Multiple Analyzers in One Device
- Up to 10 Trigger Levels Per Channel





3. Create a new STP file:



4. Configurations (after expansion of the previous window):

The image displays a sequence of screenshots from the Quartus II software interface, illustrating the configuration process for a signal tap.

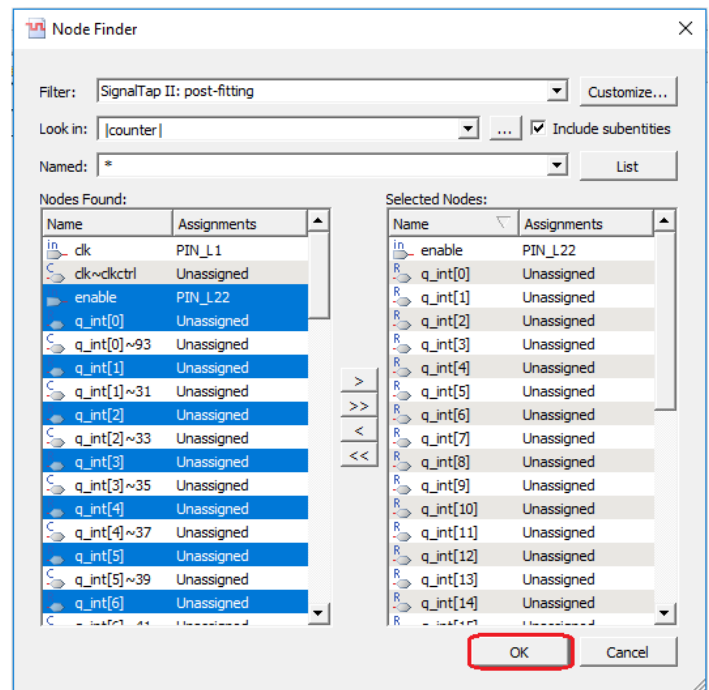
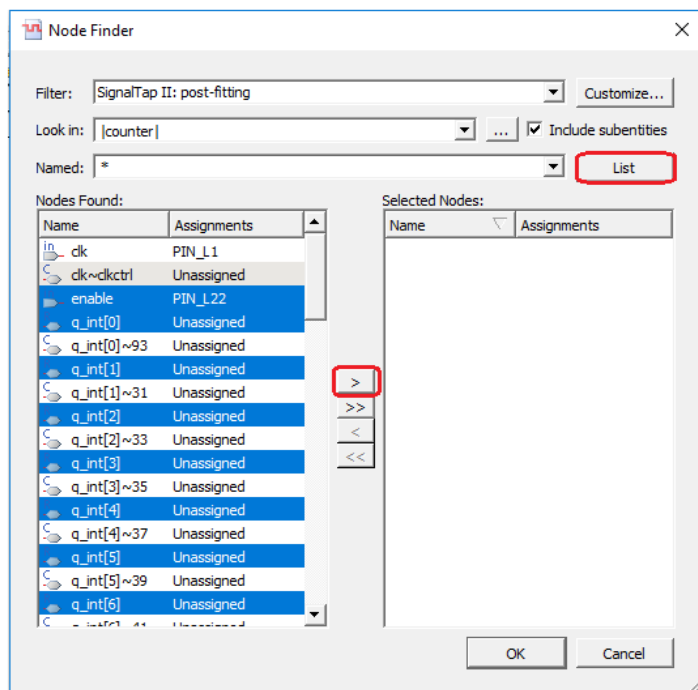
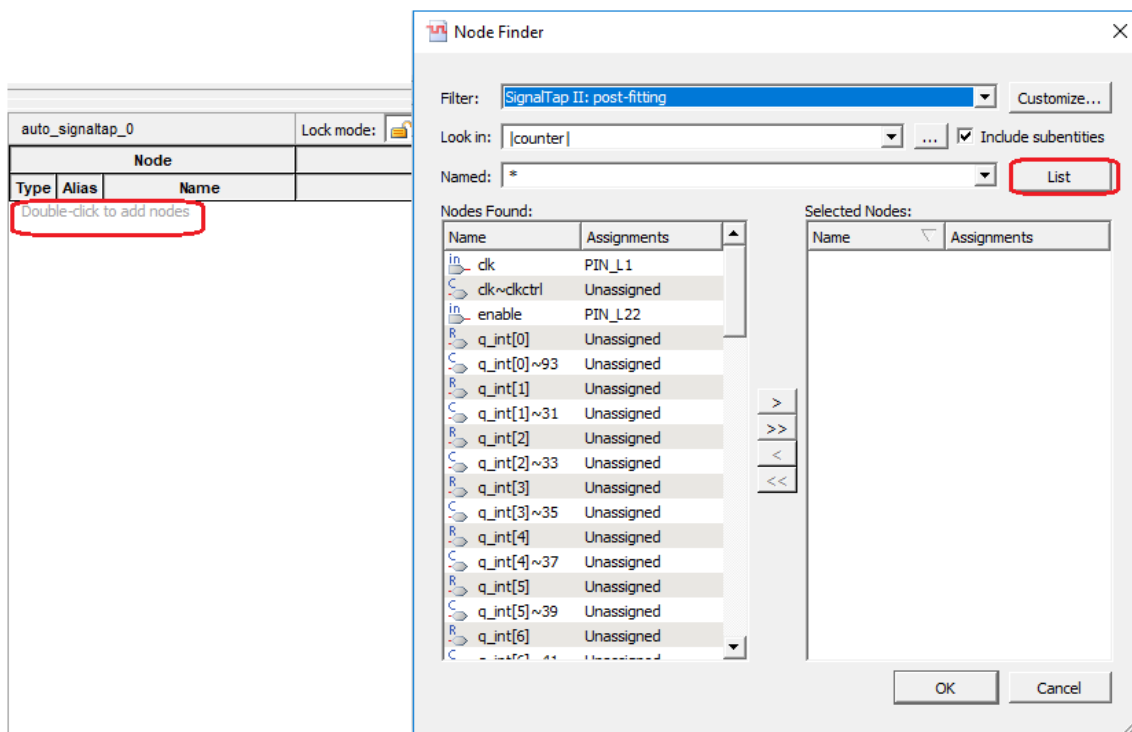
Top Row:

- Node Finder:** The 'Filter' is set to 'SignalTap II: post-fitting'. The 'Look in' dropdown shows 'counter'. The 'List' button is highlighted. The 'Nodes Found' table lists various signals, with 'clk' (PIN_L1) selected. The 'Selected Nodes' table shows 'clk' (PIN_L1) is now selected.
- JTAG Chain Configuration:** The 'Hardware' dropdown is set to 'Please Select'. The 'Device' dropdown is set to 'None Detected'. The 'SOF Manager' button is highlighted.
- Signal Configuration:** The 'Clock' is set to 'clk'. The 'Sample depth' is set to '4 K'. The 'RAM type' is set to 'Auto'. The 'Type' is set to 'Continuous'. The 'Trigger flow control' is set to 'Sequential'. The 'Trigger position' is set to 'Pre trigger position'. The 'Trigger conditions' are set to '1'.

Bottom Row:

- Select Programming File:** The 'Look in' dropdown shows 'C:\Test_Projects\Quartus'. The 'Files of type' is set to 'SRAM Object Files (*.sof)'. The 'output_files' folder is selected.
- Select Programming File:** The 'Look in' dropdown shows 'C:\Test_Projects\Quartus\output_files'. The 'Test.sof' file is selected. The 'Open' button is highlighted.
- JTAG Chain Configuration:** The 'Hardware' dropdown is set to 'USB-Blaster [USB-0]'. The 'Device' dropdown is set to 'None Detected'. The 'SOF Manager' button is highlighted.
- Signal Configuration:** The 'Clock' is set to 'clk'. The 'Sample depth' is set to '4 K'. The 'RAM type' is set to 'Auto'. The 'Type' is set to 'Continuous'. The 'Trigger flow control' is set to 'Sequential'. The 'Trigger position' is set to 'Pre trigger position'. The 'Trigger conditions' are set to '1'.

Red boxes and arrows indicate the flow of the configuration process, highlighting key settings and file selections.



In case of more than one Trigger condition columns:
 1) **Between lines in the same column** the operation is **AND**.
 2) **Between columns** the operation is **OR**.



auto_singaltap_0 Lock mode: Allow all changes

Type	Alias	Name	Data Enable	Trigger Enable	Trigger Conditions
In		enable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	1 Basic
R		q_int[0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[1]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[2]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[3]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[4]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[5]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[6]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[7]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[8]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[9]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[10]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[11]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[12]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[13]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[14]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[15]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[16]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[17]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[18]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[19]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[20]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[21]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[22]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[23]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[24]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[25]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[26]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

mouse right click

Don't Care
 Low
 Falling Edge
Rising Edge
 High
 Either Edge
 Insert Value...

Signal Configuration:

Clock: **clk**

Data

Sample depth: 4 K

☐ Segmented: 2 2

Storage qualifier:

Type: Con

Input port:

☒ Record data disc

☐ Disable storage q

Trigger

Trigger flow control: S

Trigger position:

Trigger conditions: 1

☐ Trigger in

Source: auto_stp_

Pattern: Don't C

☐ Trigger out

Target:

Level: Active

Latency delay:

Data **Setup**



SignalTap II Logic Analyzer - C:/Test_Projec

File Edit View Project Processing Tools W

New File Ctrl+N

Close

Save Ctrl+S

Save As...

Export...

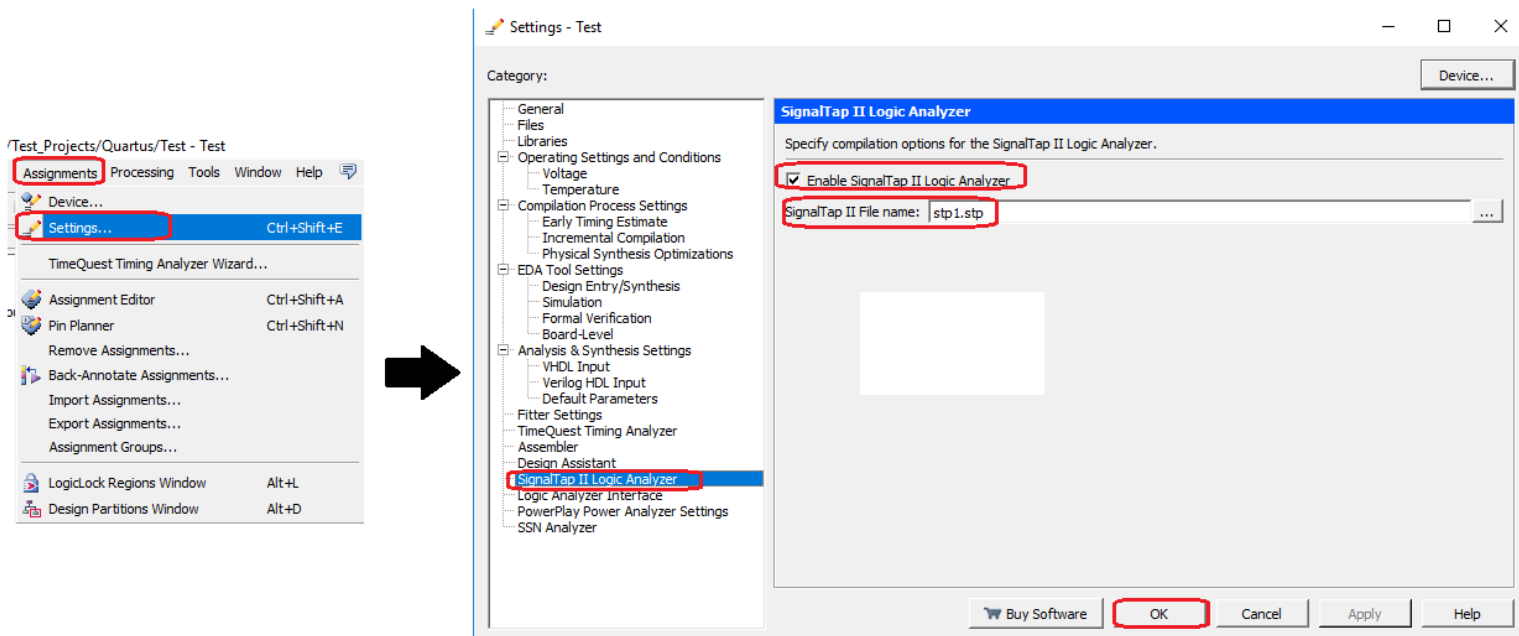
Page Setup...

Print Preview

Print... Ctrl+P

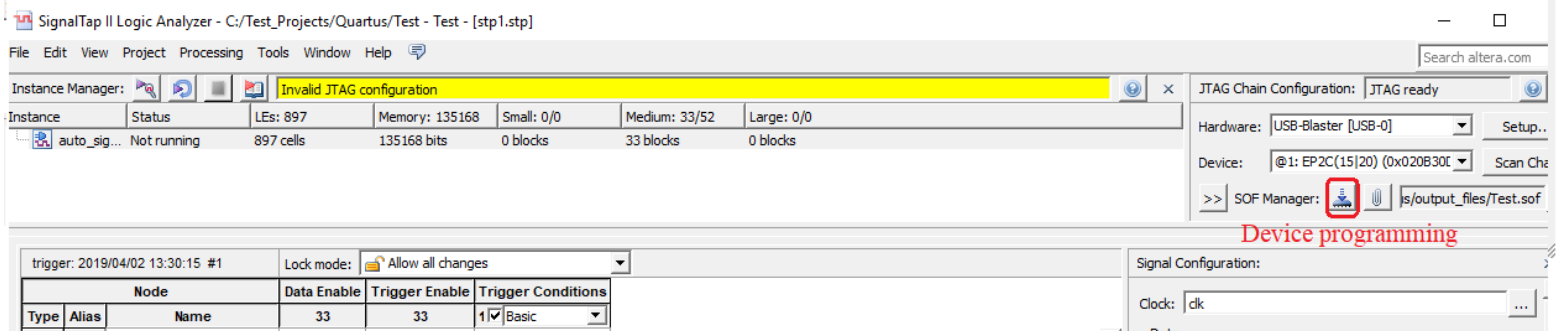
Type	Alias	Name
In		enable
R		q_int[0]

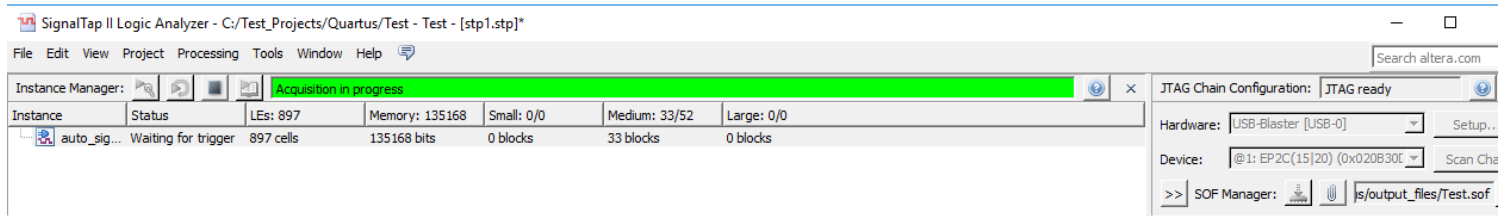
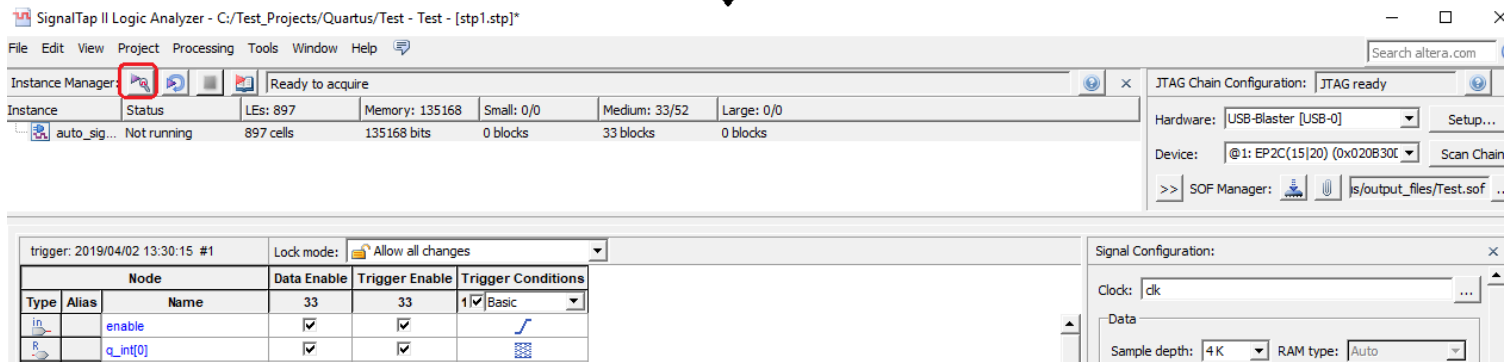
5. Project Compilation and Programming (an eventually the Signals results):



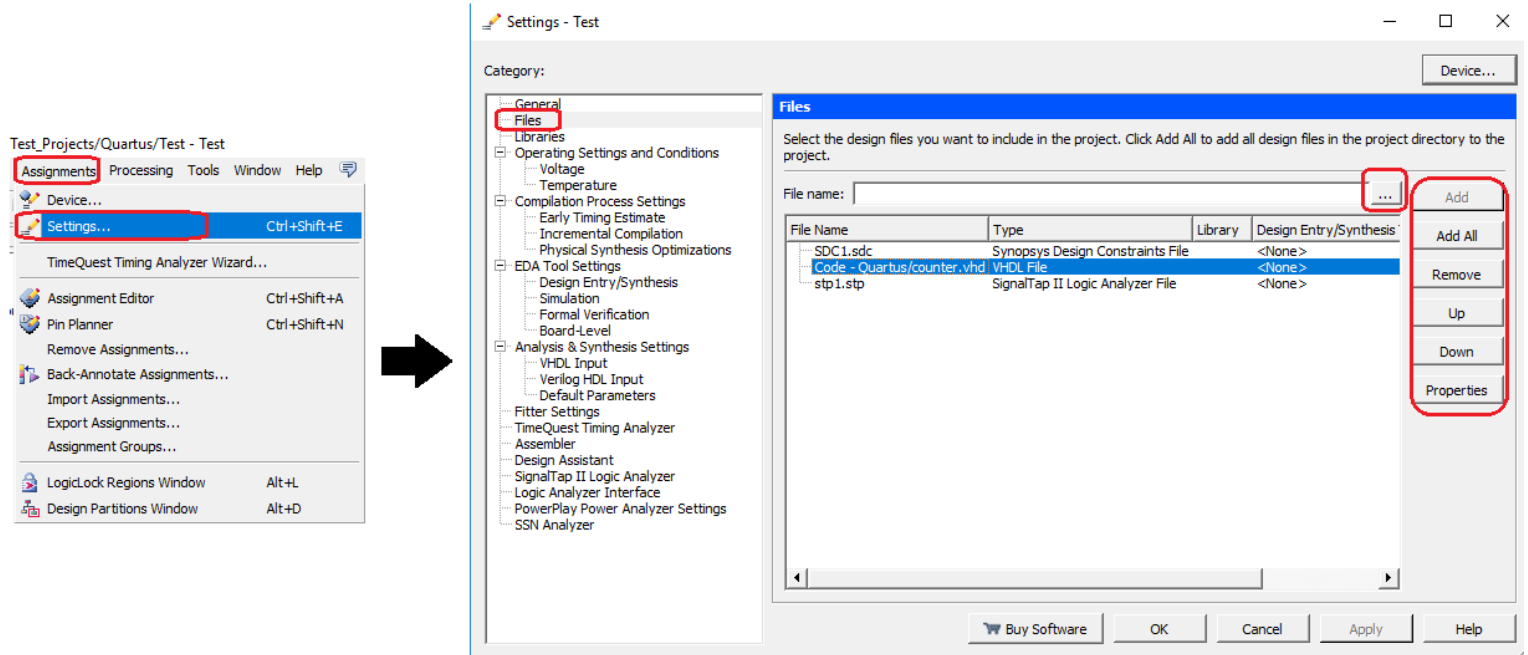
Turn ON the DE1 Board power

Open the STP file





C. Changing the VHDL source files of the project:



D. Open Existing Project:

