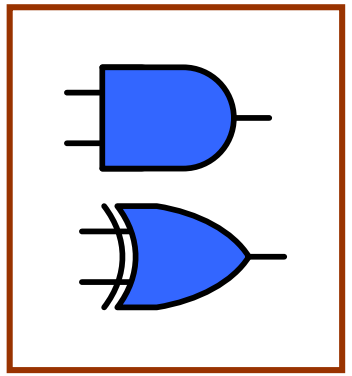
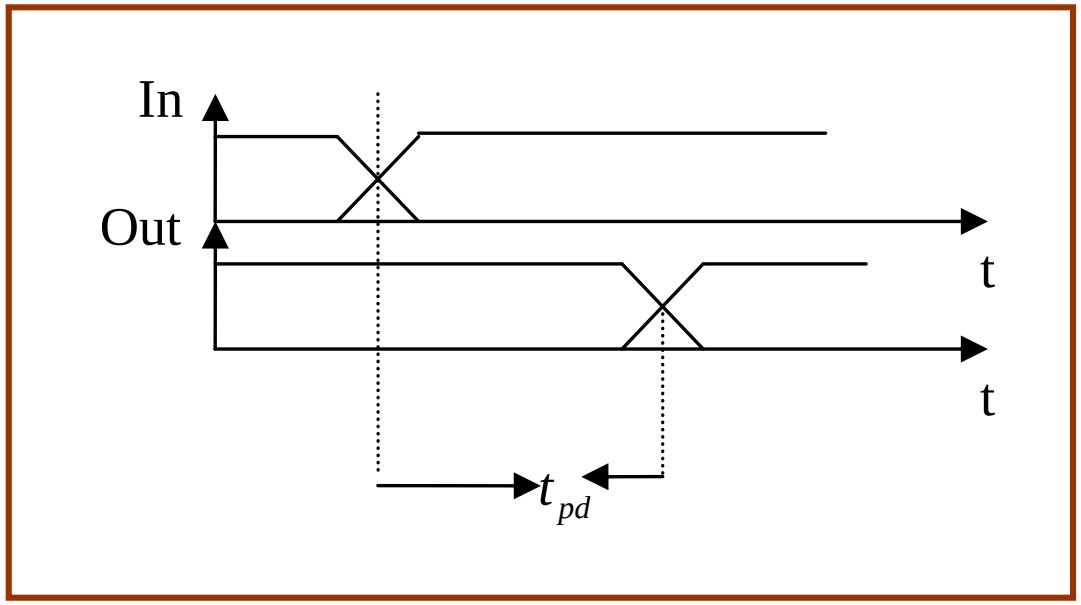
Combinational Circuits Timing Analysis

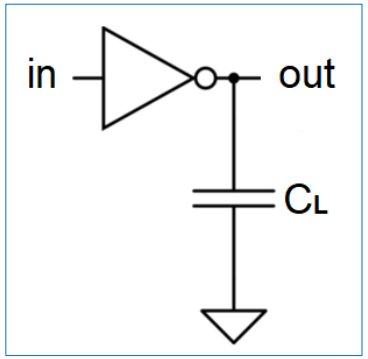
Logic Gates Timing

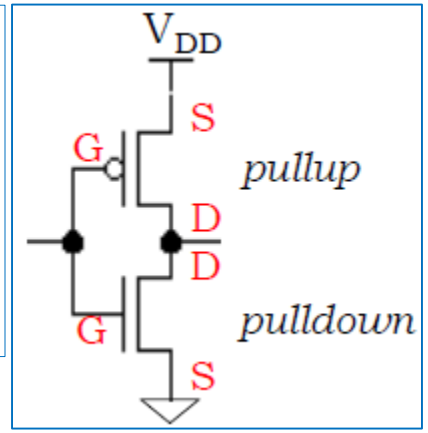
t_{pd}: Time from state change at input to state change at output

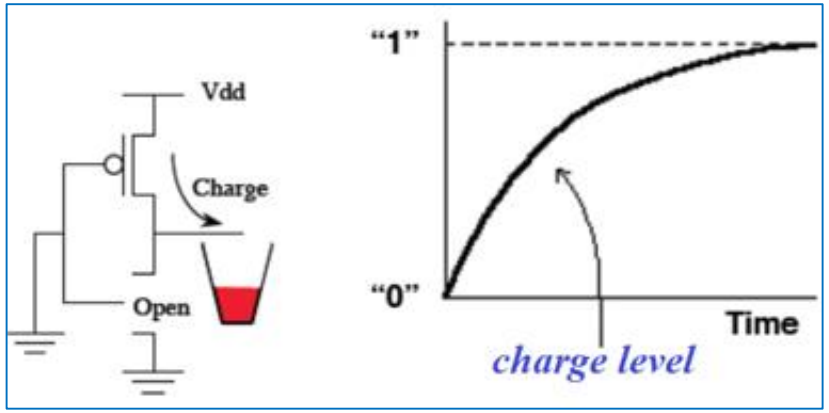


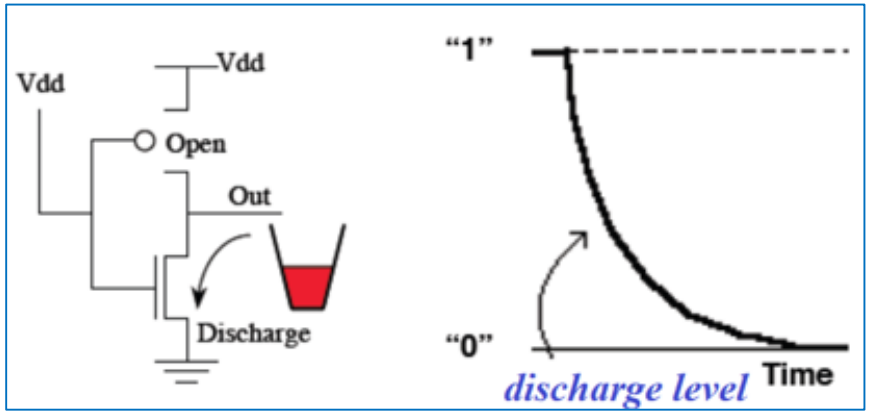


CMOS NOT Gate VTC (Voltage Transfer Curve)









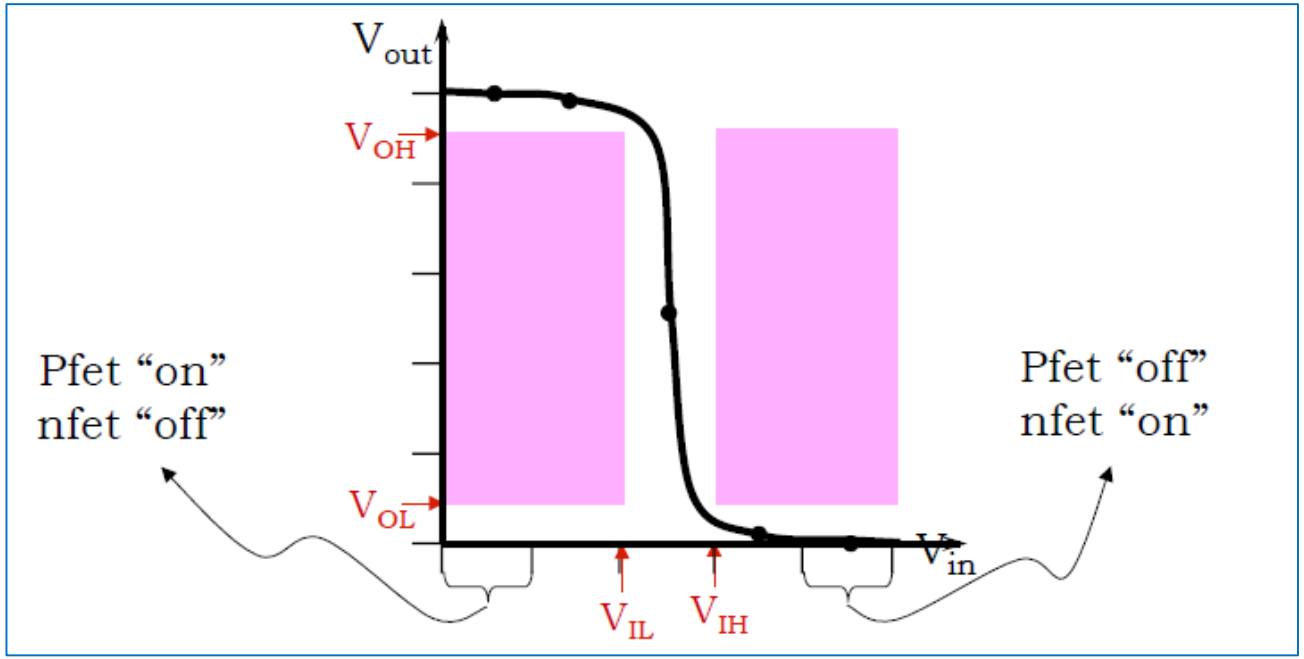
$$C_L = C_{out} + C_{line} + N \cdot C_{in}$$

C_{out} - parasitic capacitance due to transistors configuration between output and GND

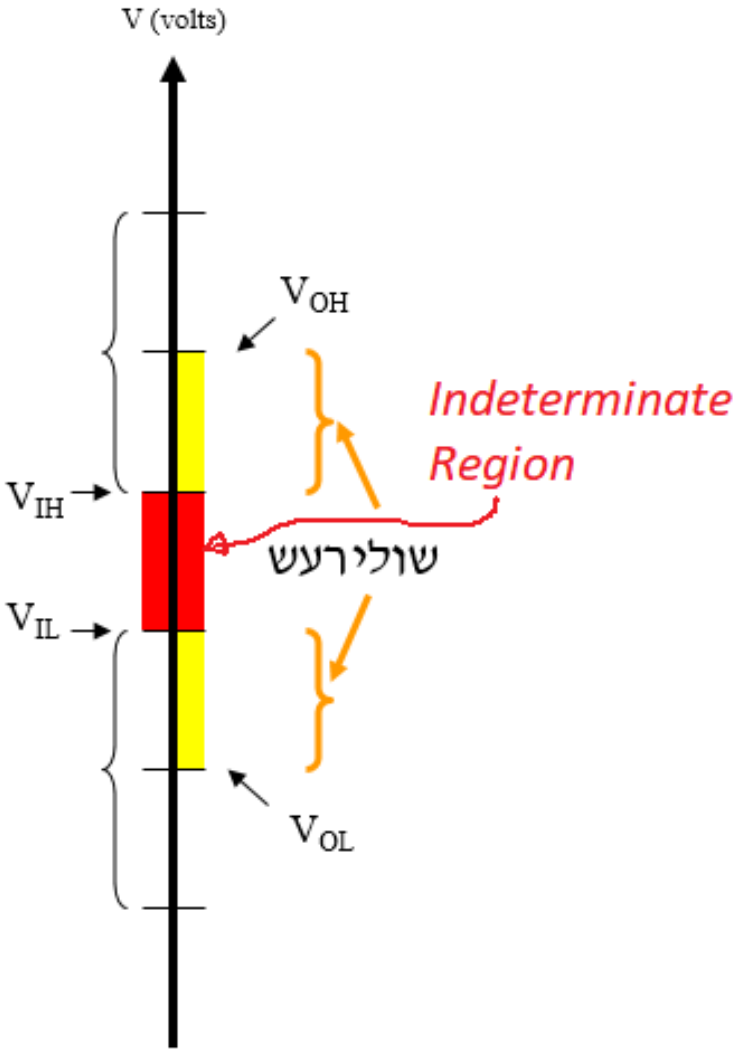
C_{line} - parasitic capacitance due to lines connection

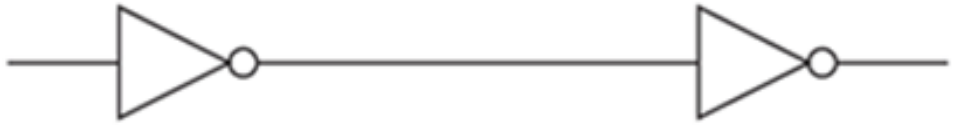
$N \cdot C_{in}$- input capacitance of N gates at the next rank only (CMOS), connected to its output

$$t_{pd} = f(C_L, T[℃], V_{CC})$$



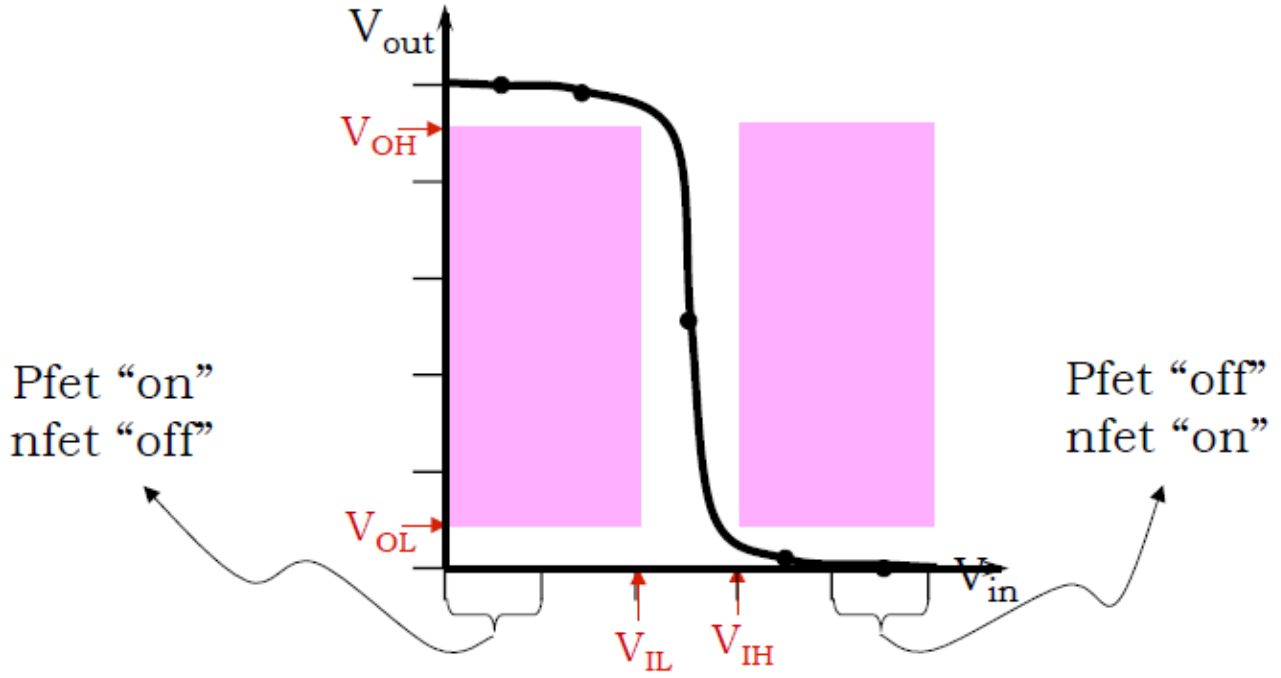
Digital Logic Abstraction





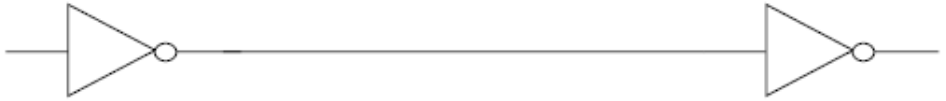
Output Characteristics Input Characteristics

The noise margins overcome the noise that is added to the signal in the transition from one component to another

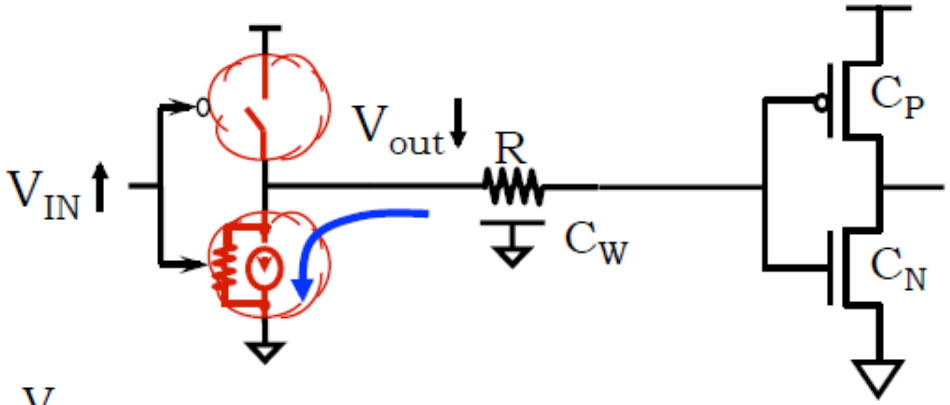


CMOS Timing Specifications

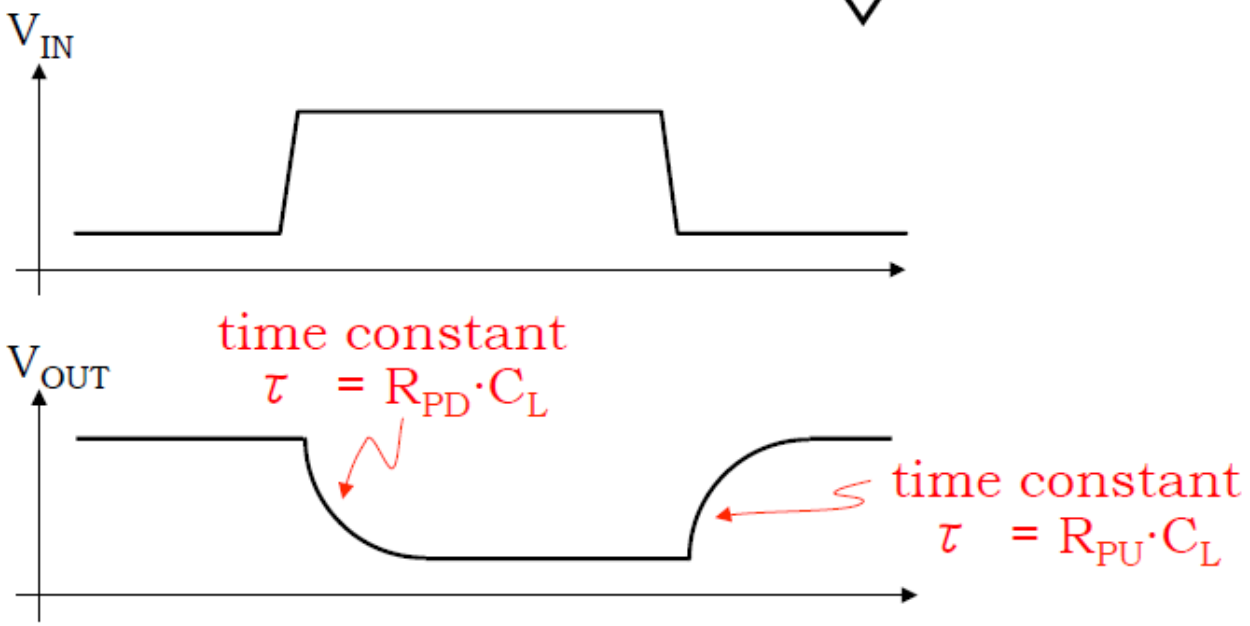
Circuit:



Electrical model:

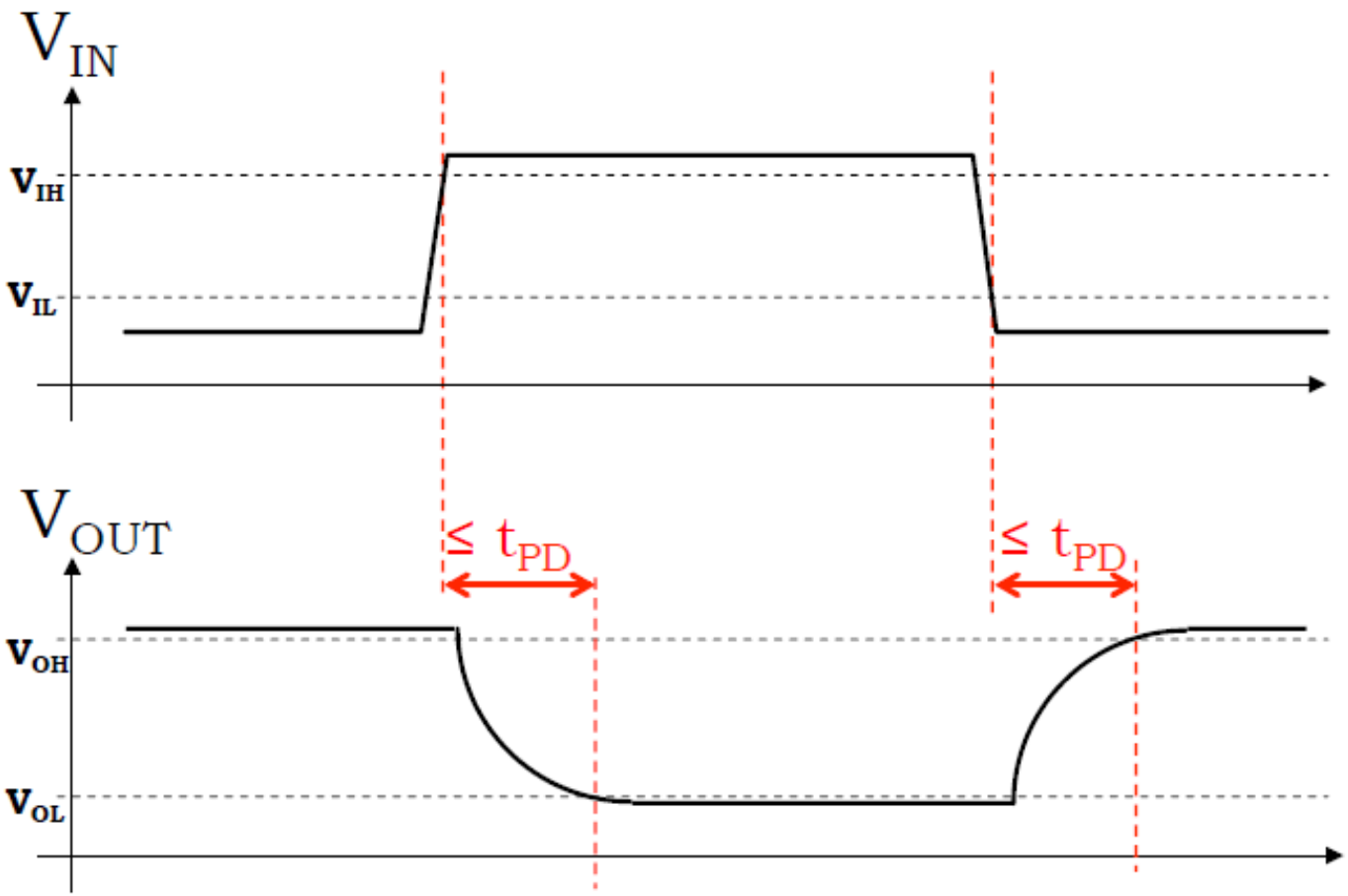


Waveforms:



Propagation delay (t_{PD}):

Propagation delay (t_{PD}): An UPPER BOUND on the delay from valid inputs to valid outputs.

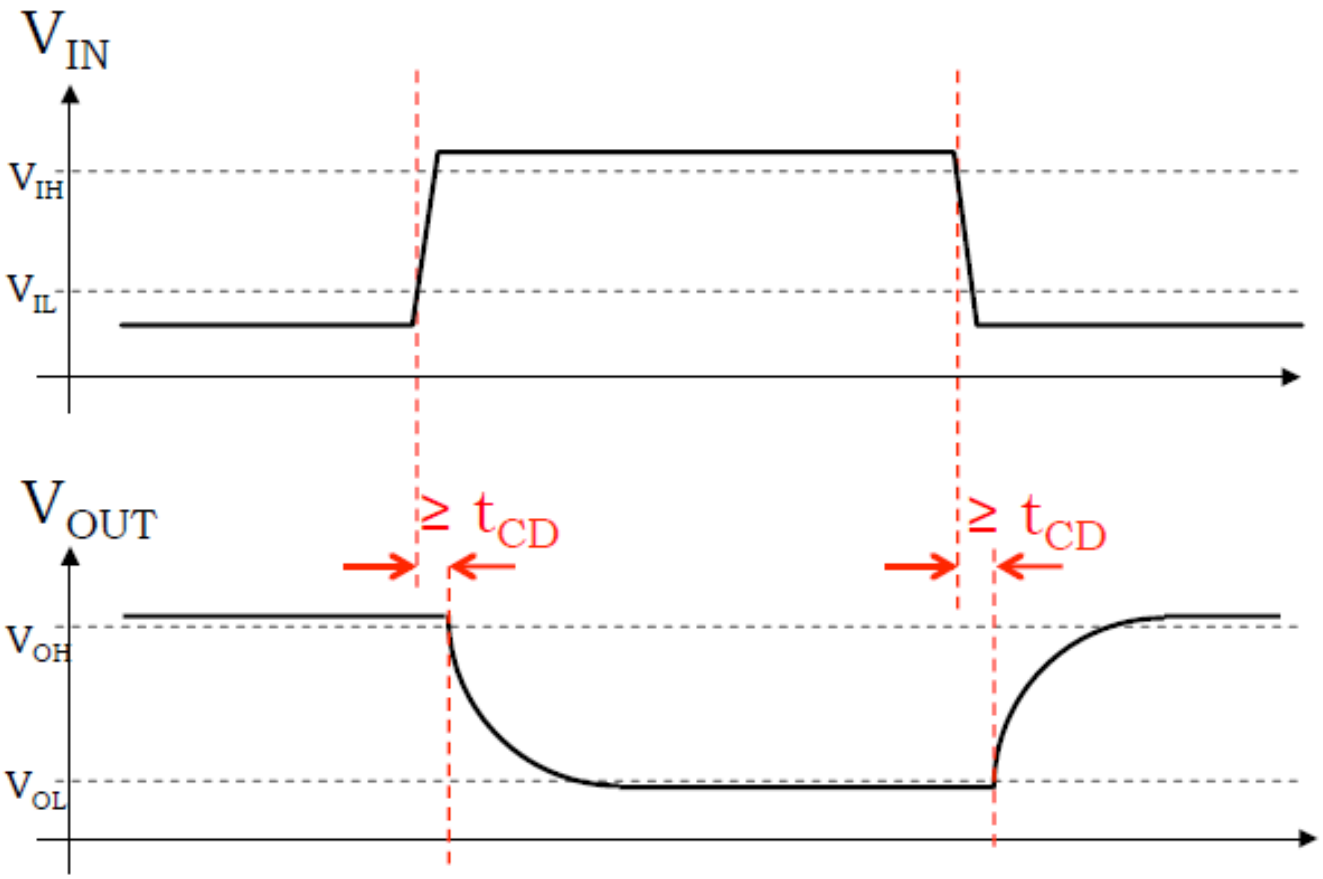


GOAL:
minimize propagation delay!

ISSUE:
keep capacitances low and transistors fast

Contamination Delay

Contamination delay (t_{CD}): A LOWER BOUND on the delay from any invalid input to an invalid output

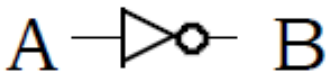


Do we really need t_{CD}?

Usually not… it'll be important when we design circuits with registers (coming soon!)

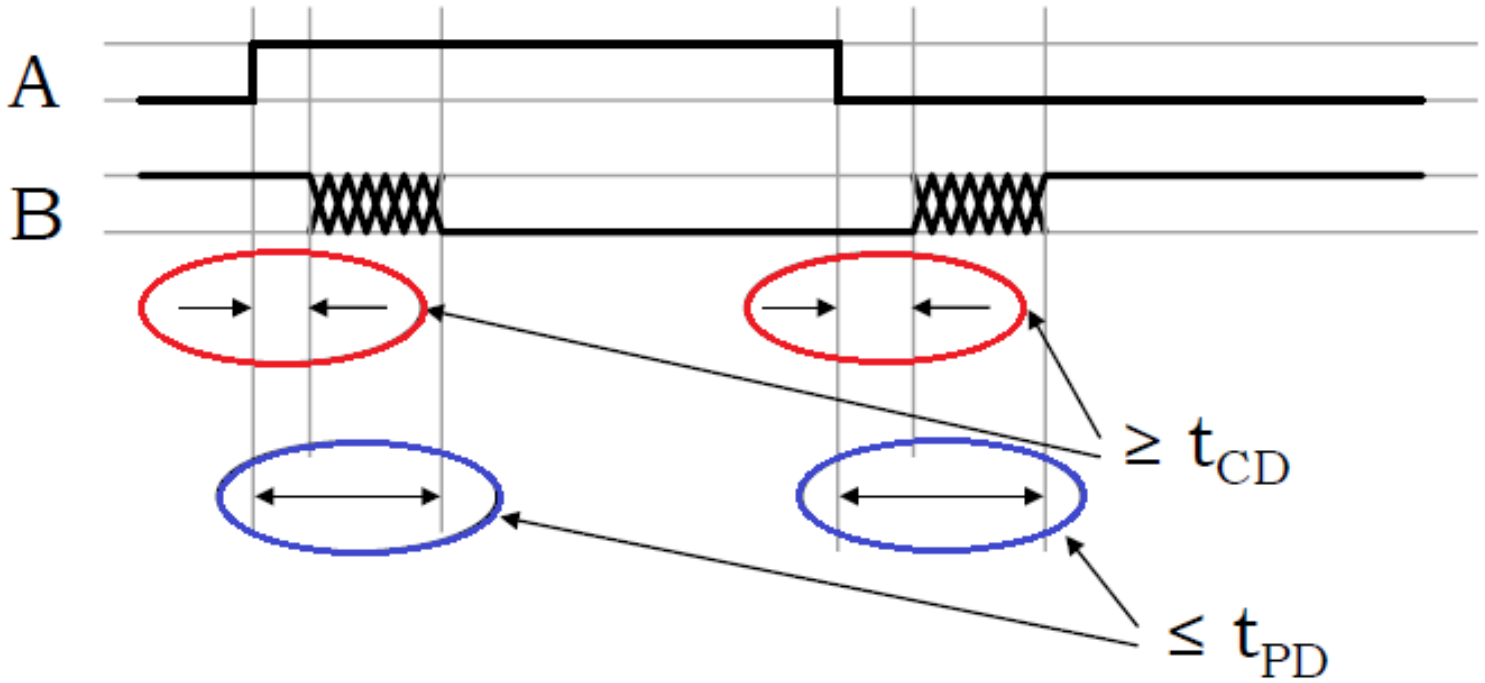
If t_{CD} is not specified, safe to assume it's 0.

Combinational Example



A	B
0	1
1	0

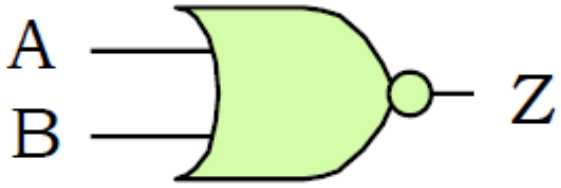
t_{PD} propagation delay
t_{CD} contamination delay



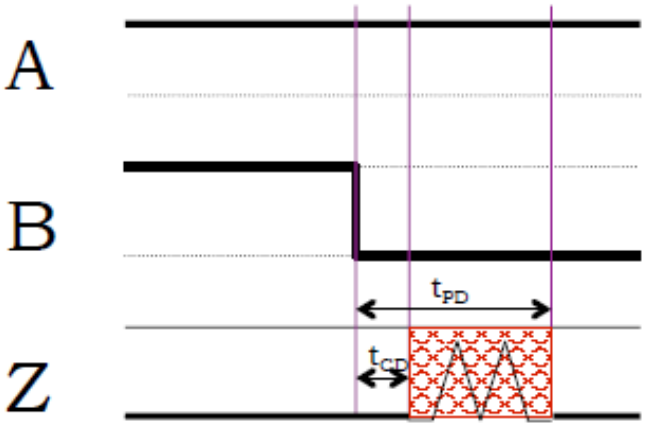
Static Discipline Obedience

- Definition: guarantee on logical elements that ***"if inputs meet valid input thresholds, then the system guarantees outputs will meet valid output thresholds"***, named by Stephen A. Ward and Robert H. Halstead in 1990.
- Implication: Output guaranteed to be valid when *all* inputs have been valid for at least t_{PD}, and, outputs may become invalid no earlier than t_{CD} after an input changes!

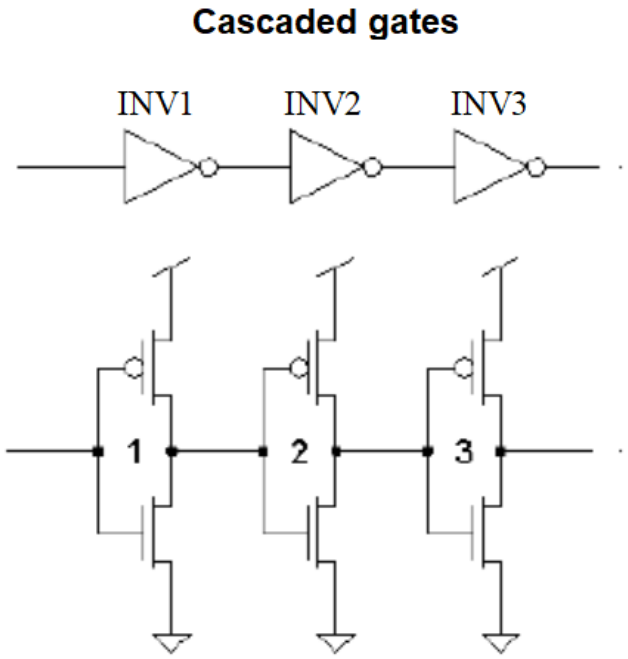
NOR:

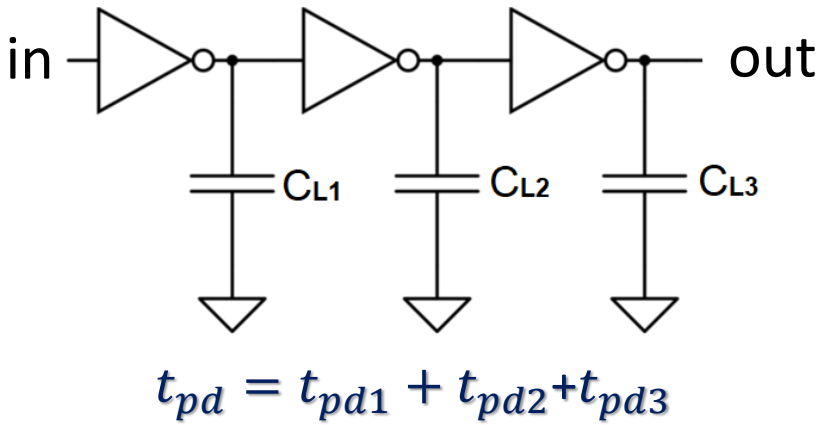


A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

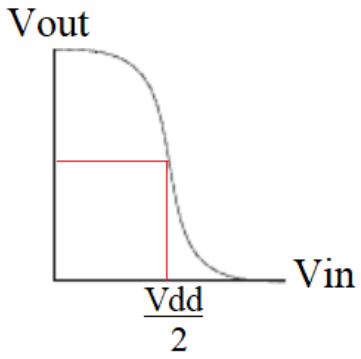


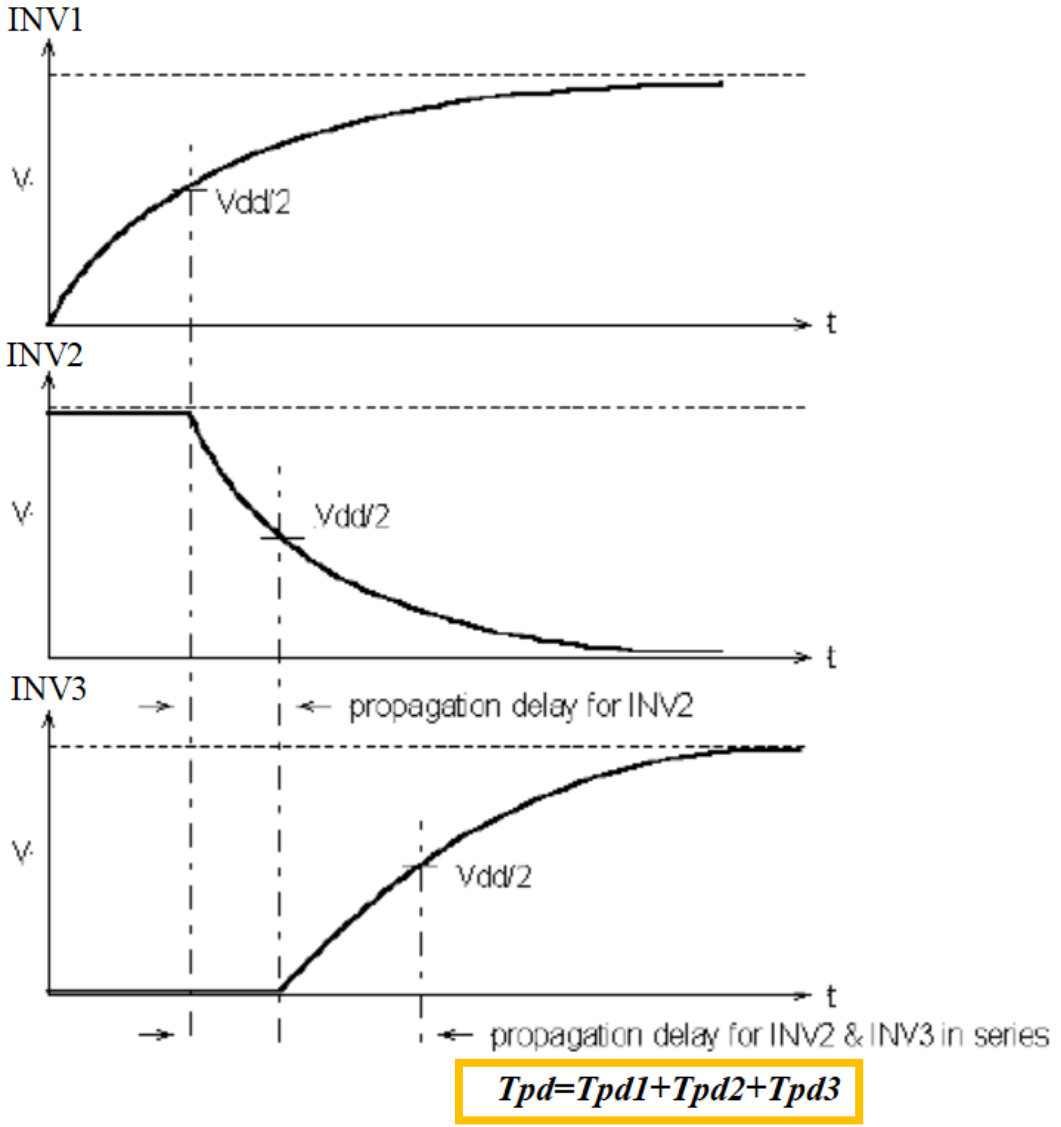
Cascaded gates delay





$$t_{pd} = t_{pd1} + t_{pd2} + t_{pd3}$$





Tpd=Tpd1+Tpd2+Tpd3

Fan-out delay

- The delay of a gate is proportional to its output capacitance. Connecting the output of gate to more than one other gate increases it's output capacitance.
- Driving wires also contributes to fan-out delay.