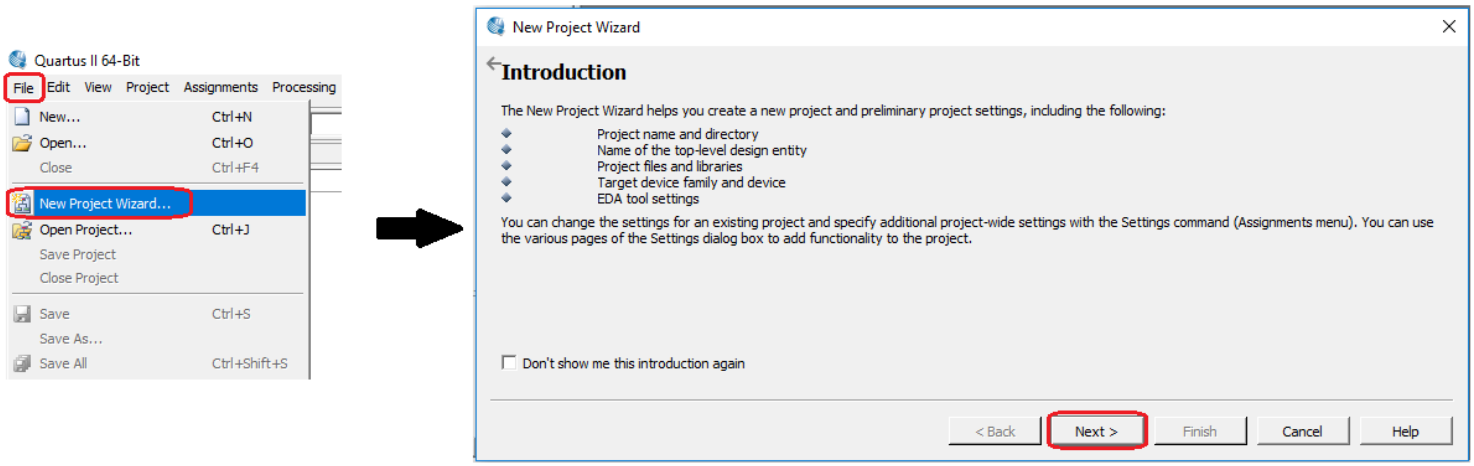
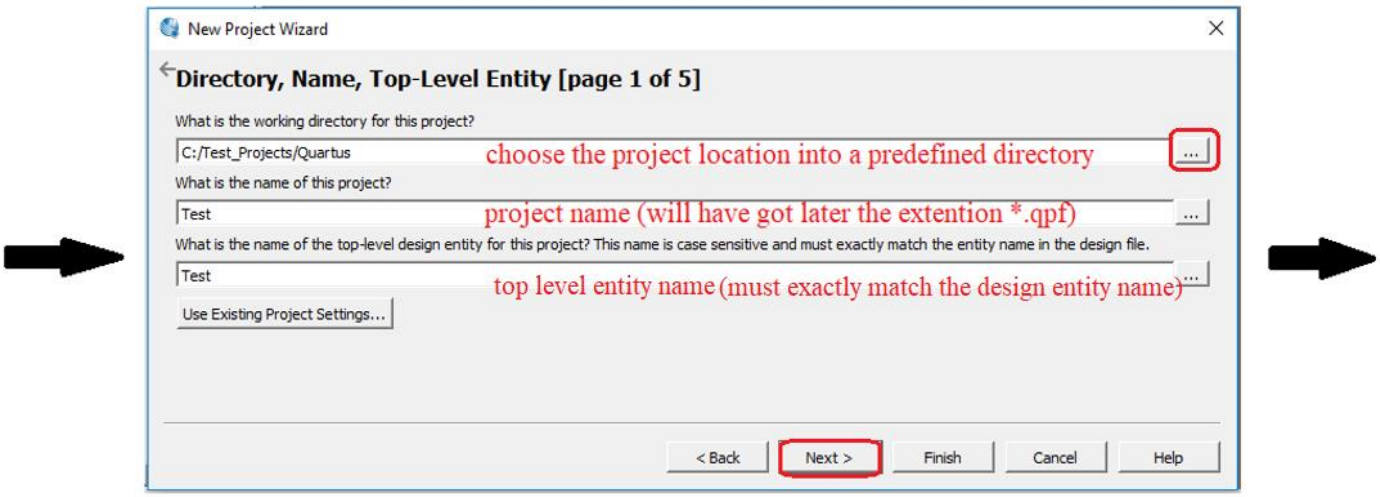
Table of Contents

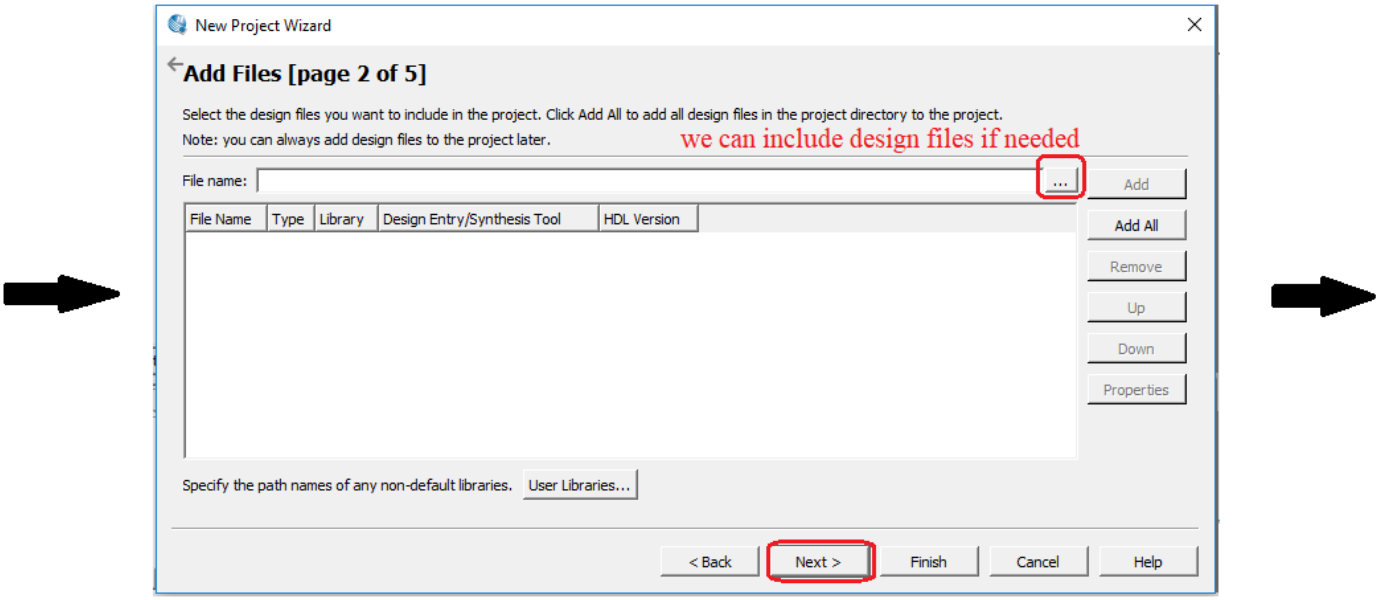
Quartus - Create or Open a Project

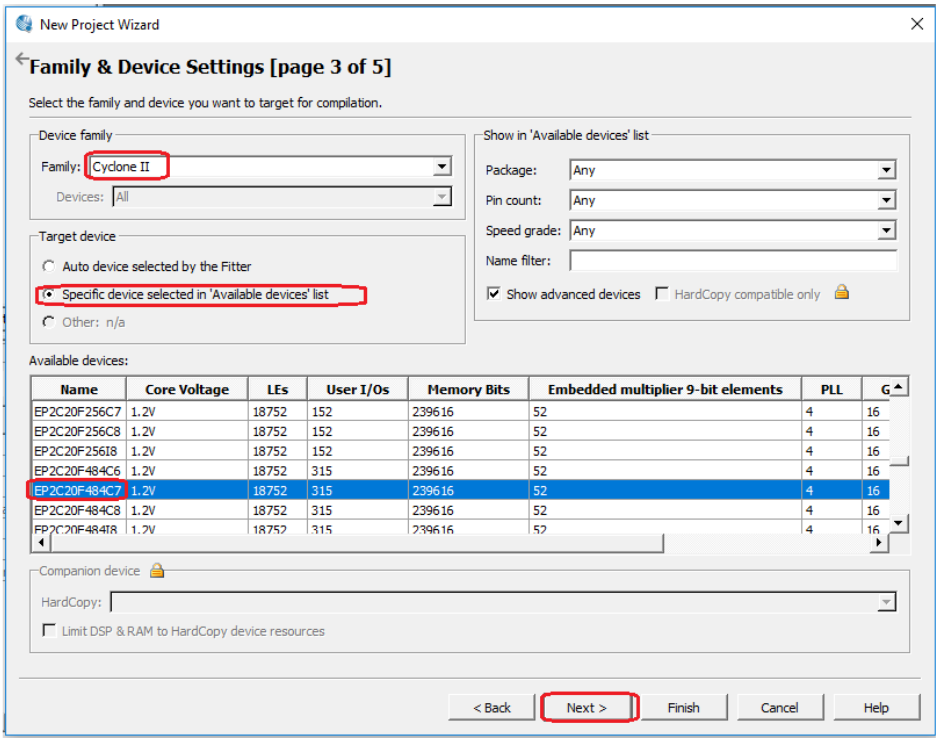
A. Create a New Project:

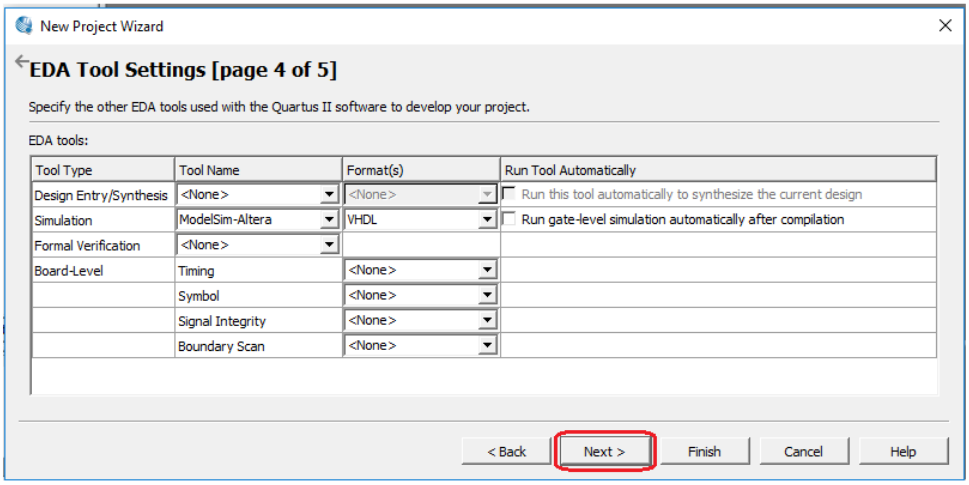
1. Step 1 – create a new project and add VHDL files:

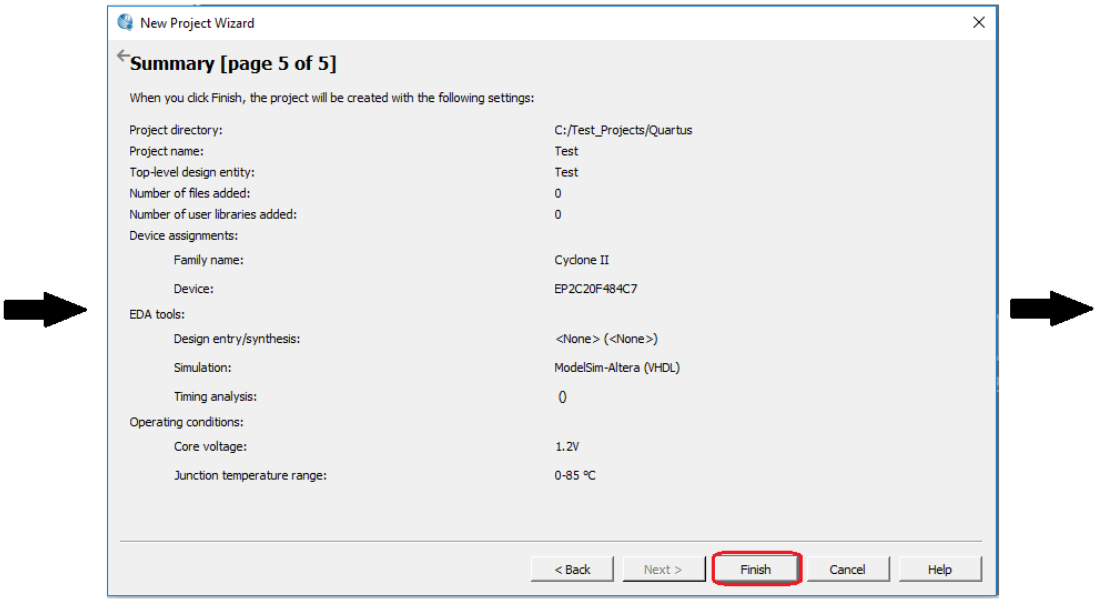




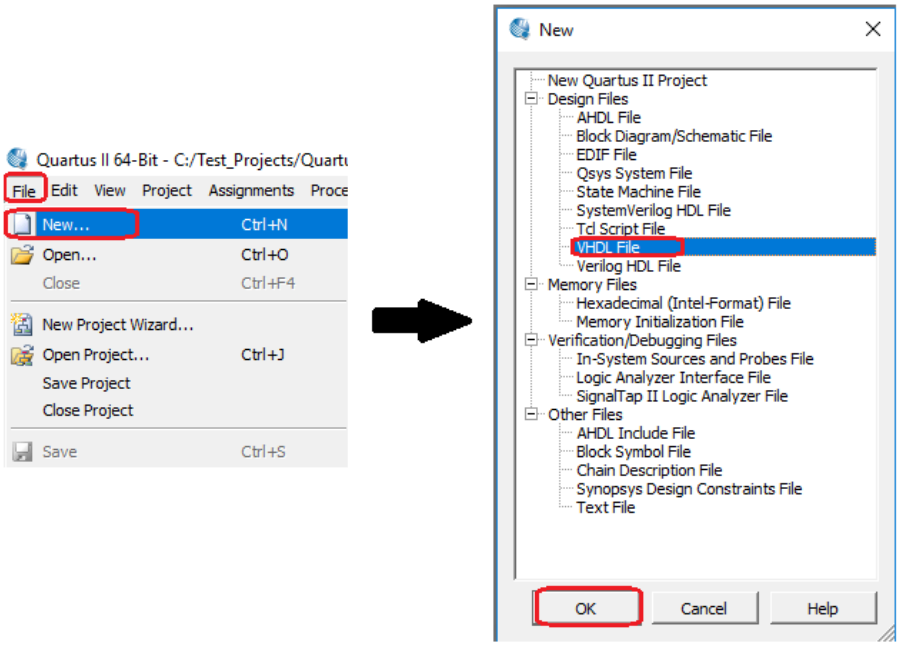



New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
Device family
Family: Cyclone II
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements | PLL | G
EP2C20F256C7 | 1.2V | 18752 | 152 | 239616 | 52 | 4 | 16
EP2C20F256C8 | 1.2V | 18752 | 152 | 239616 | 52 | 4 | 16
EP2C20F256I8 | 1.2V | 18752 | 152 | 239616 | 52 | 4 | 16
EP2C20F484C6 | 1.2V | 18752 | 315 | 239616 | 52 | 4 | 16
EP2C20F484C7 | 1.2V | 18752 | 315 | 239616 | 52 | 4 | 16
EP2C20F484C8 | 1.2V | 18752 | 315 | 239616 | 52 | 4 | 16
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
< Back
Next >
Finish
Cancel
Help

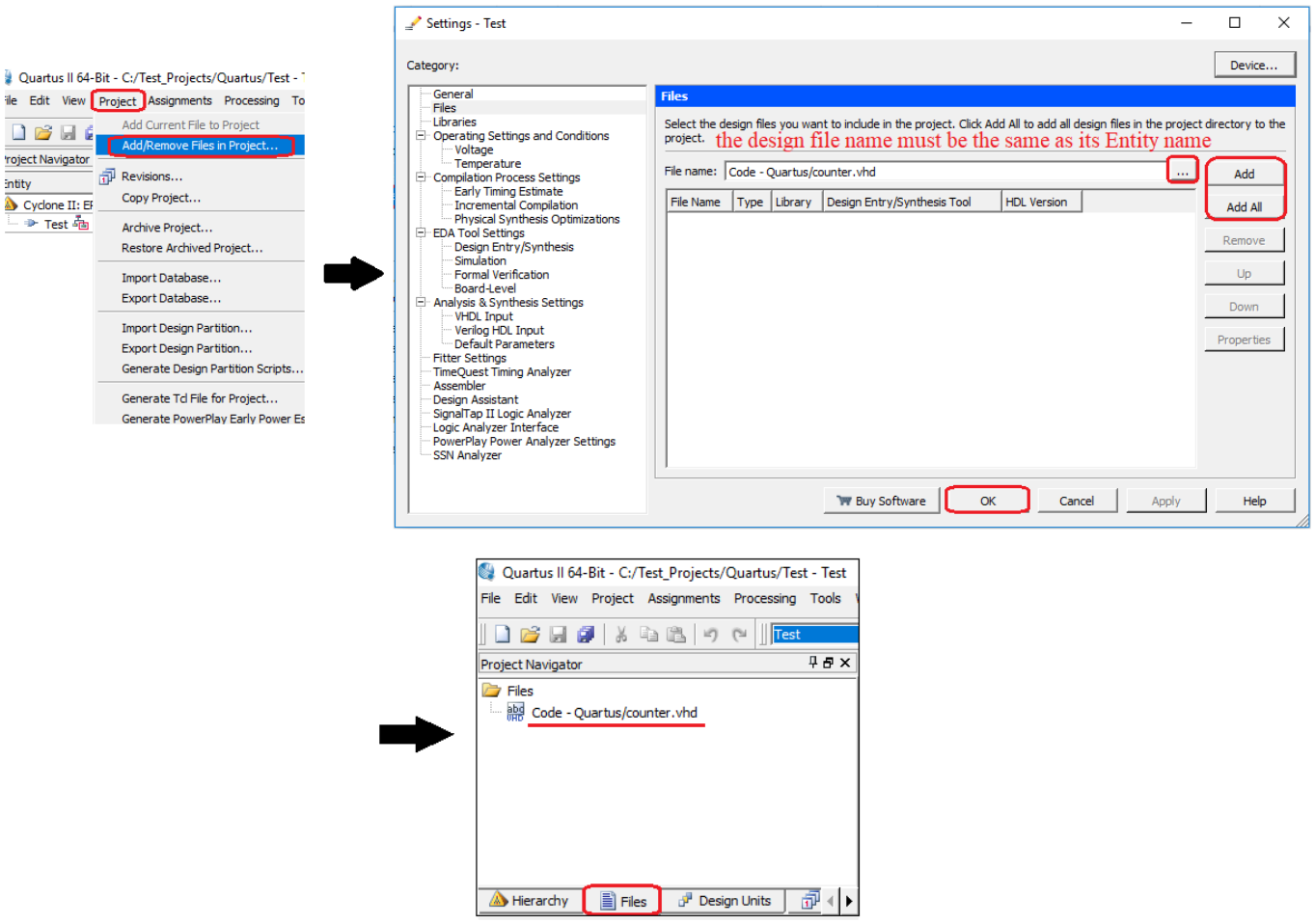

New Project Wizard
EDA Tool Settings [page 4 of 5]
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type | Tool Name | Format(s) | Run Tool Automatically
Design Entry/Synthesis | <None> | <None> | Run this tool automatically to synthesize the current design
Simulation | ModelSim-Altera | VHDL | Run gate-level simulation automatically after compilation
Formal Verification | <None>
Board-Level | Timing | <None>
Symbol | <None>
Signal Integrity | <None>
Boundary Scan | <None>
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Test_Projects/Quartus
Project name: Test
Top-level design entity: Test
Number of files added: 0
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C20F484C7
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim-Altera (VHDL)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help

2. Step 2 – Add project files:
   a. In order to open VHDL blank file use the next step (if you're using VHDL existing files, copy these files into project folder and skip to clause b):

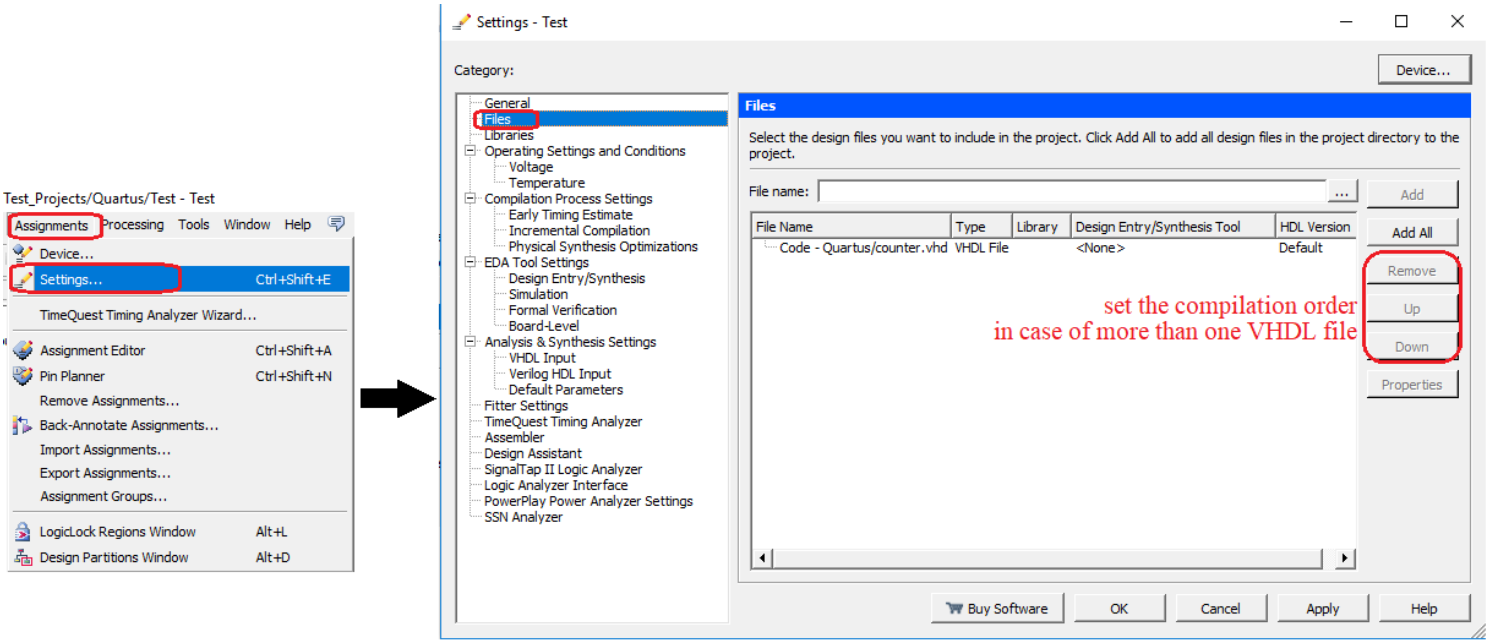


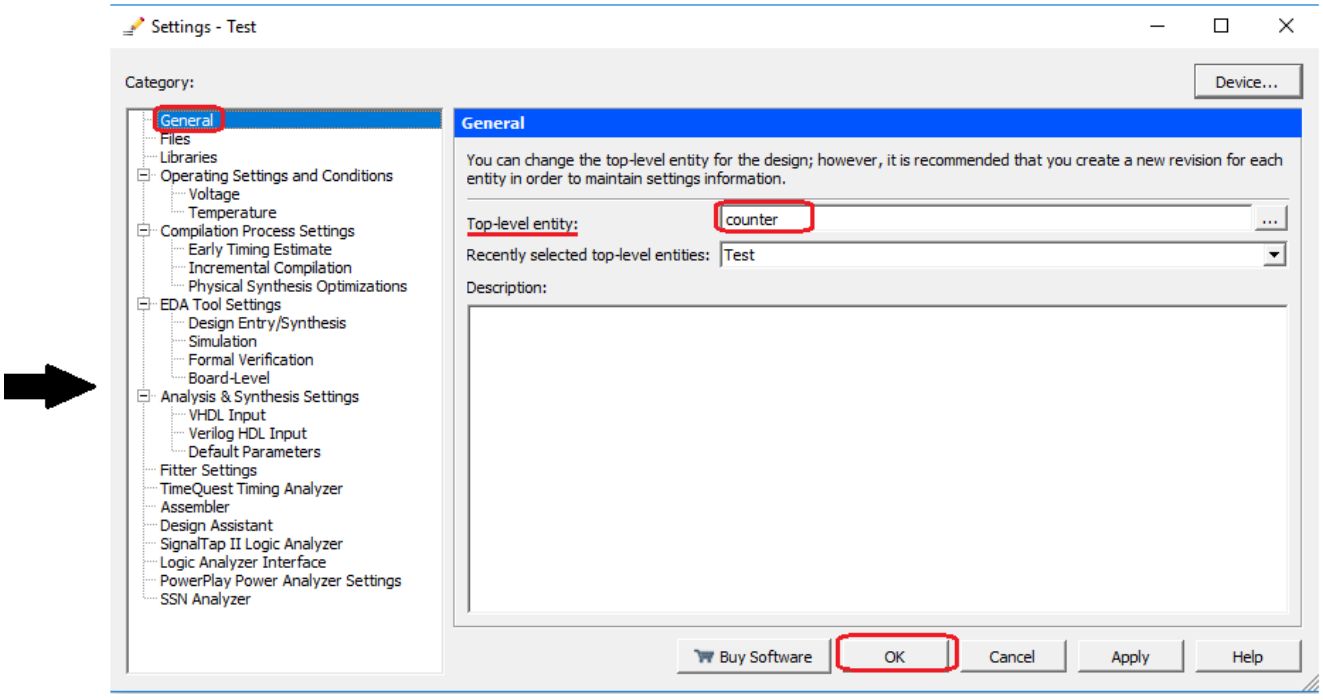
   b. Add the project VHDL existing files:



3. Step 3 – Code compilation:

   a. Set the compilation order and top level entity:





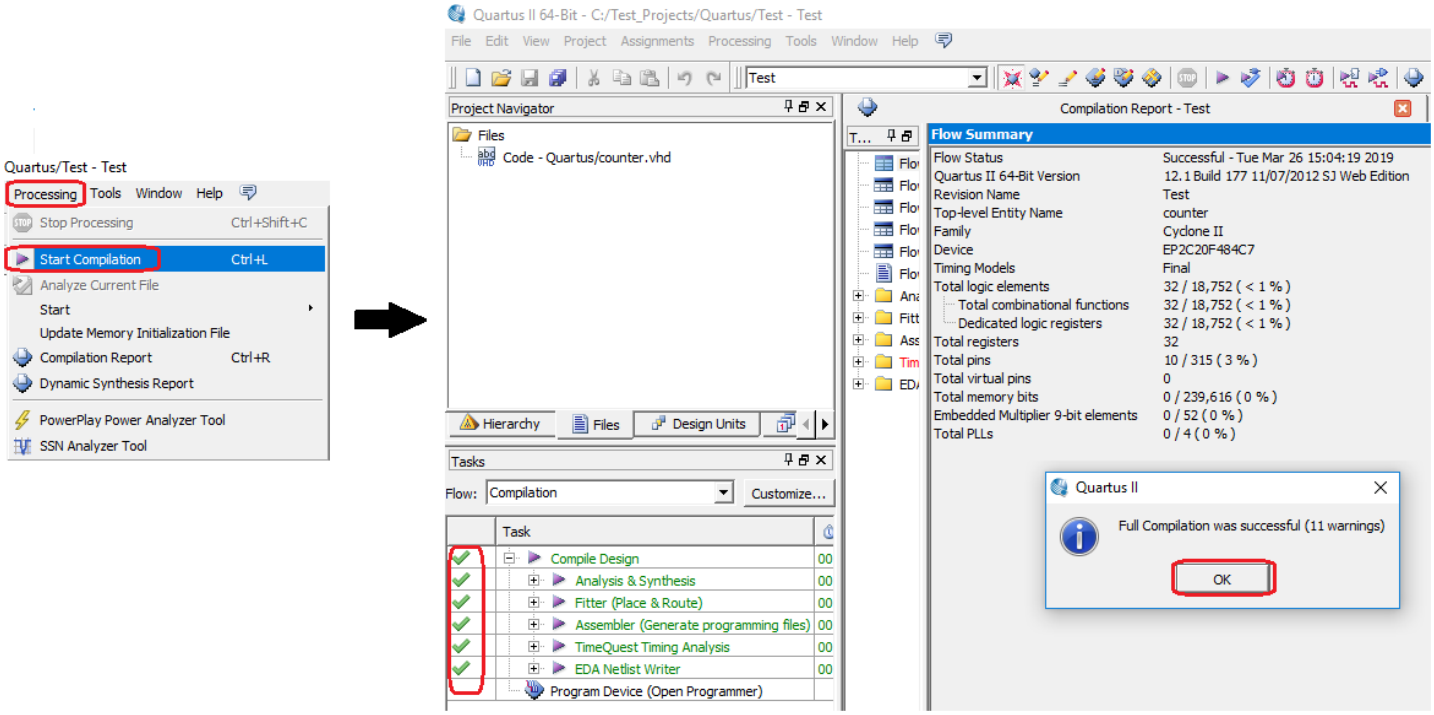
counter.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity counter is port (
    clk,enable : in std_logic;
    q          : out std_logic_vector (7 downto 0));
end counter;

architecture rtl of counter is
    signal q_int : std_logic_vector (31 downto 0):=x"00000000";
begin
    process (clk)
    begin
        if (rising_edge(clk)) then
           if enable = '1' then
                q_int <= q_int + 1;
           end if;
         end if;
    end process;
    q <= q_int(31 downto 24); -- Output only 8MSB
end rtl;
```

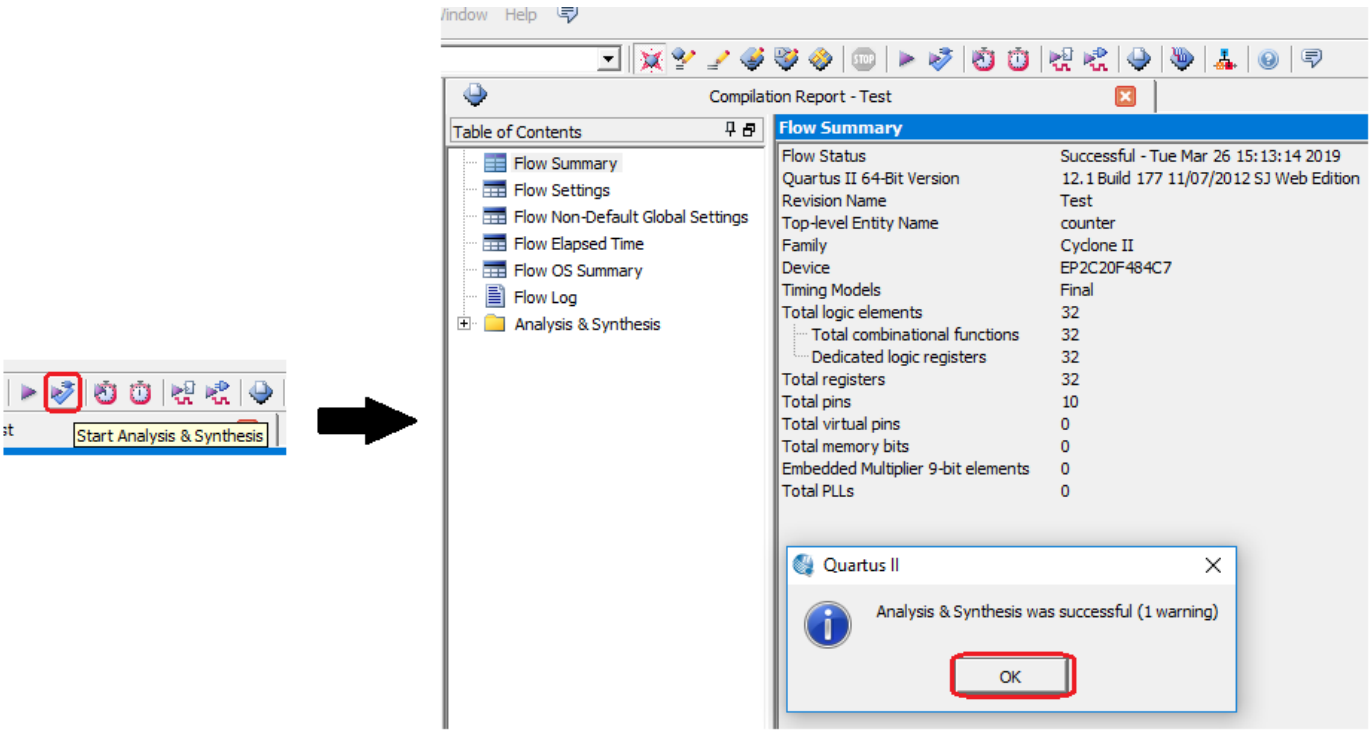
Example application:

- 32bit behavioral counter with enable
- 8 MSB connected to green LEDs
- Enable connected to switch
- Clock to 50MHz onboard oscillator

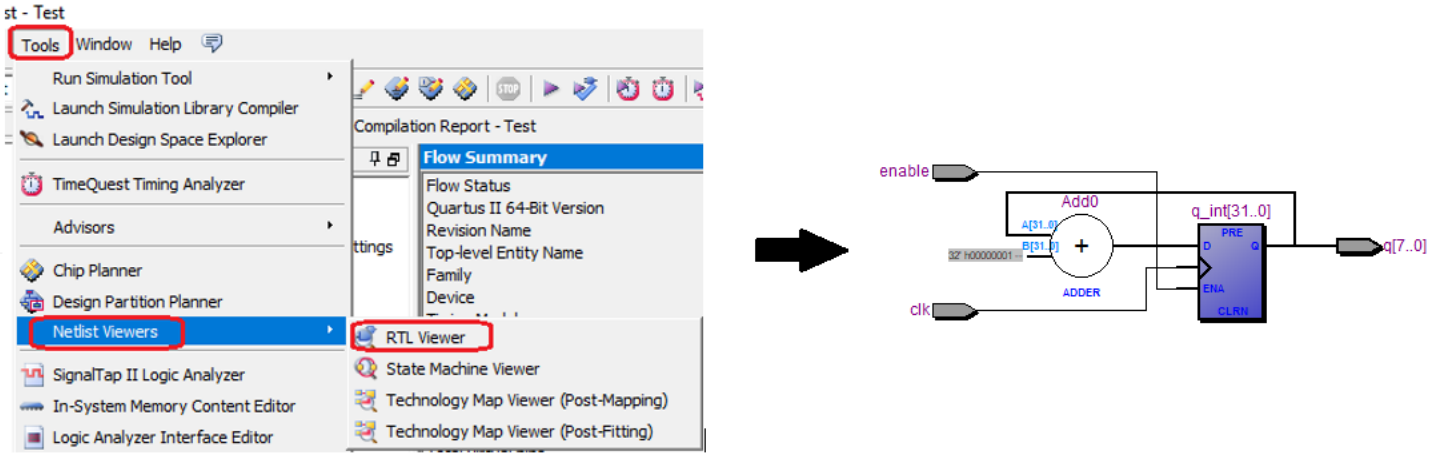
b. Code compilation:



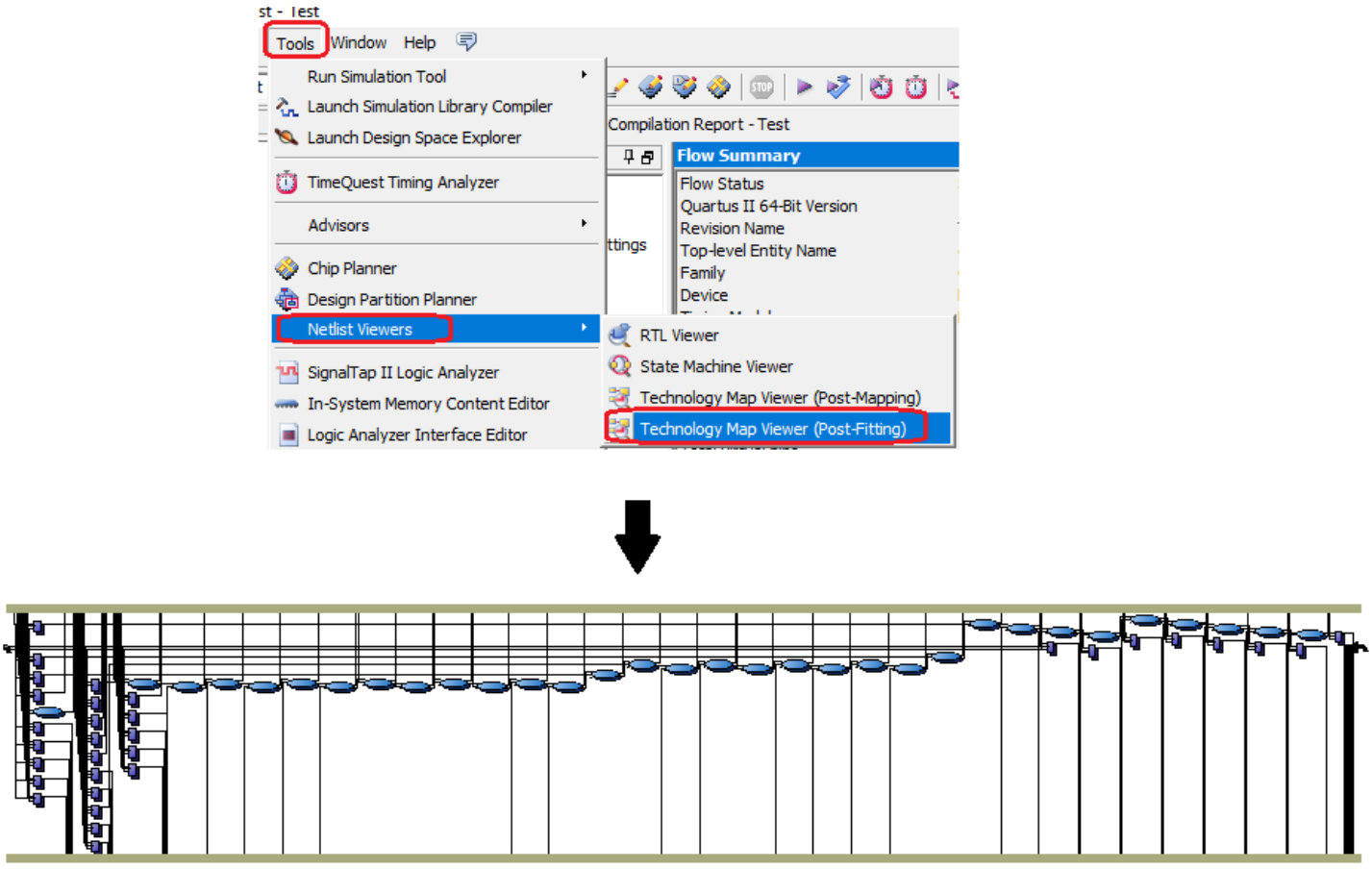
c. Start analysis and synthesis:



4. Step 4 – Synthesis results:
   a. Synthesis **RTL** viewer:

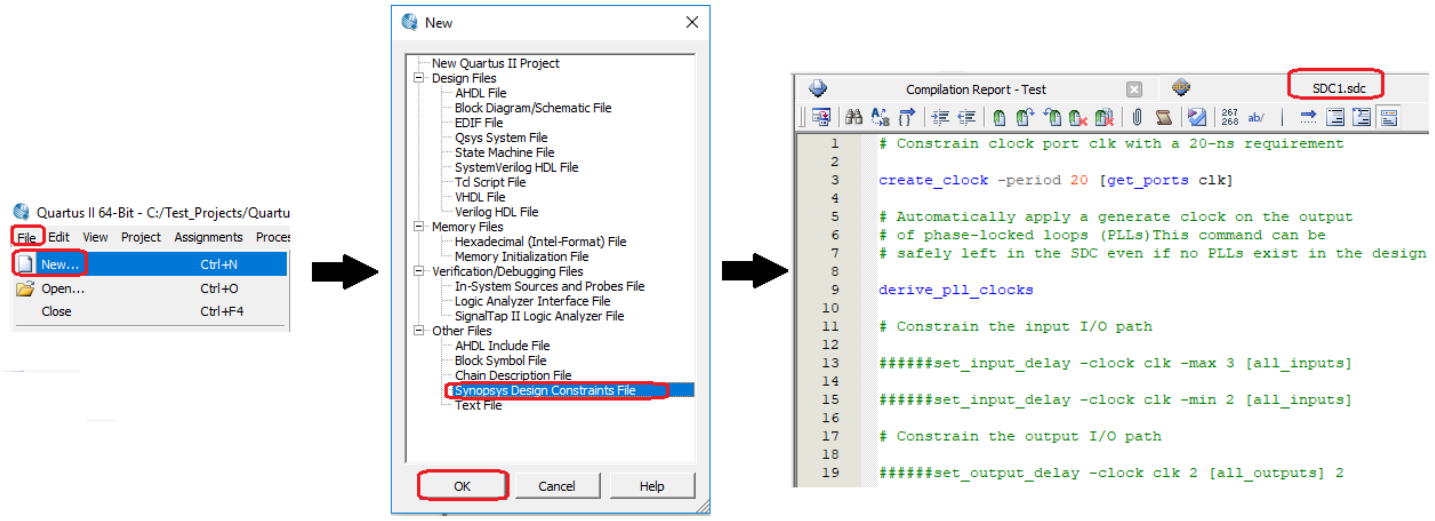


   b. Synthesis **Map** (Post-Fitting) viewer (LEs and FFs combination):

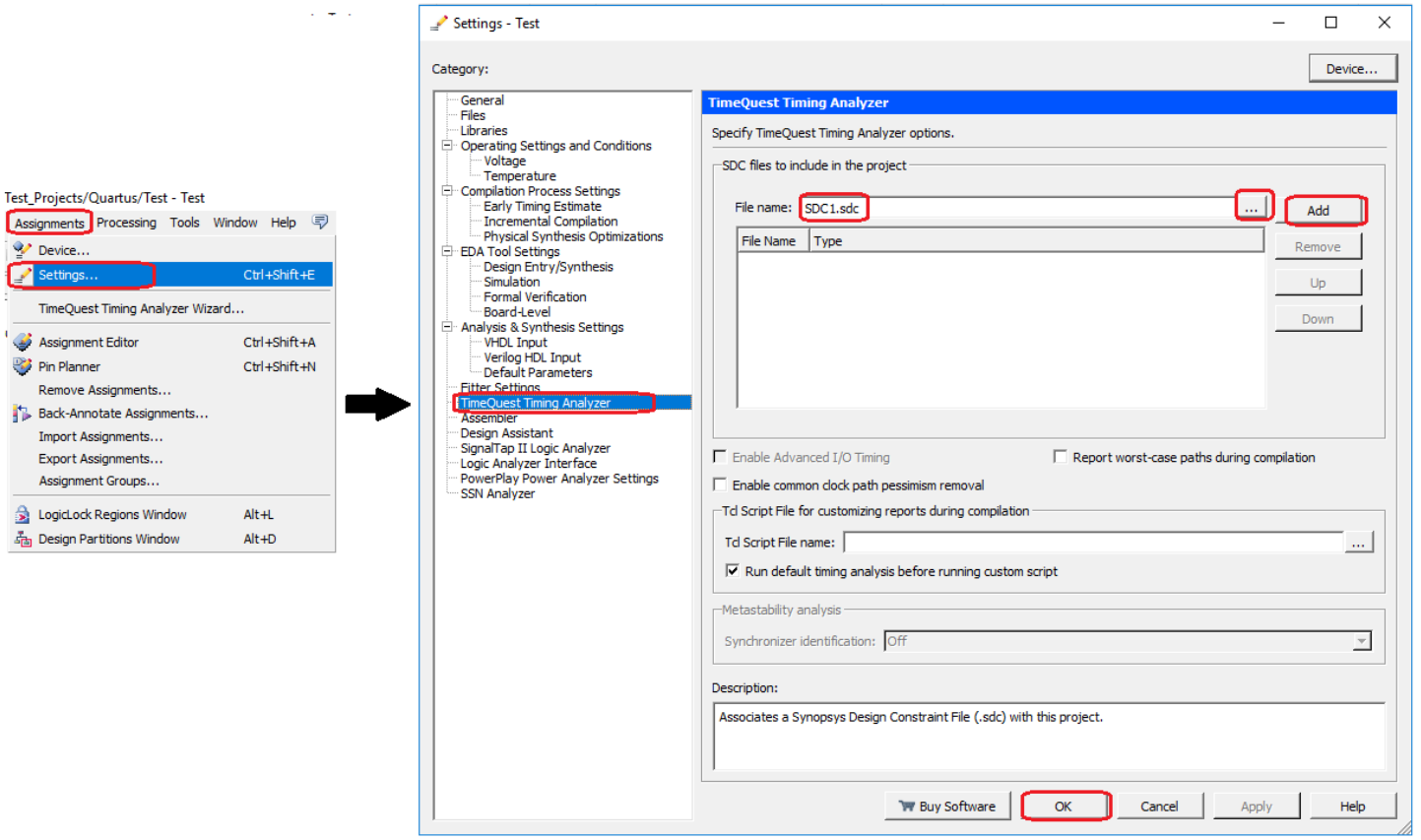


5. Step 5 – Setting system constrains:

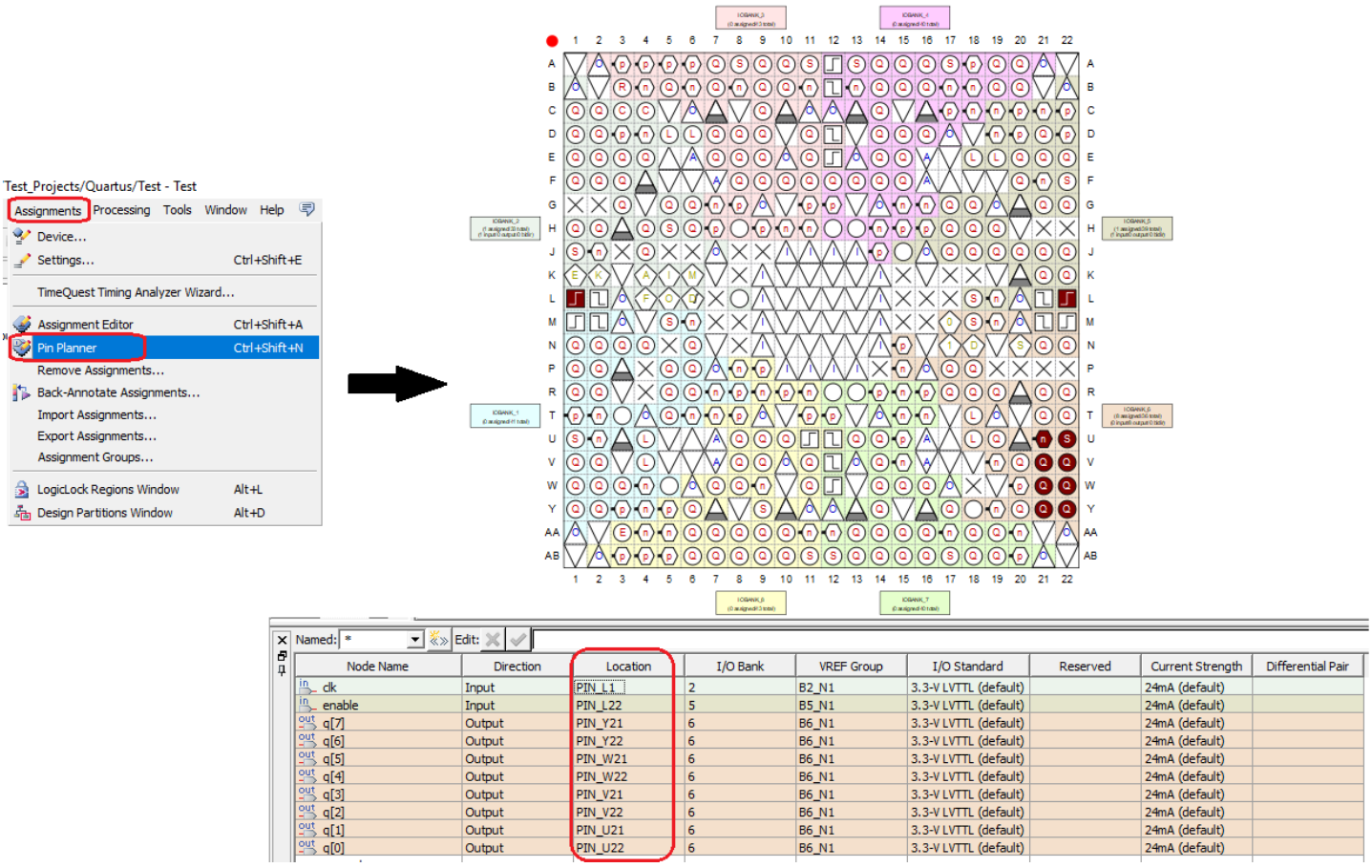
a. Create the system constrains *.sdc file:

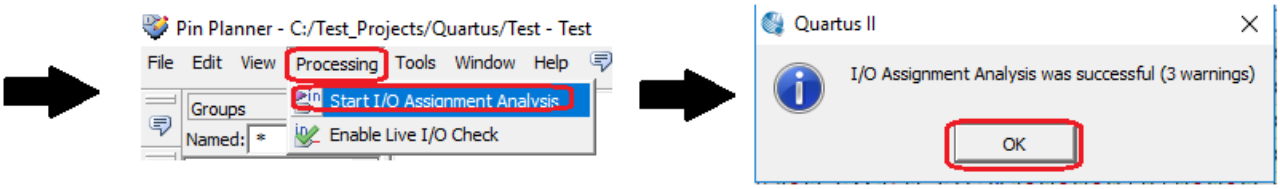


b. Add the *.sdc file to the project:



6. Step 6 – Pin Planner Layout:





Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D12, PIN_E12	27 MHz clock input
CLOCK_50	PIN_L1	50 MHz clock input
CLOCK_24	PIN_A12, PIN_B12	24 MHz clock input from USB Blaster
EXT_CLOCK	PIN_M21	External (SMA) clock input

Table 4.5. Pin assignments for the clock inputs.

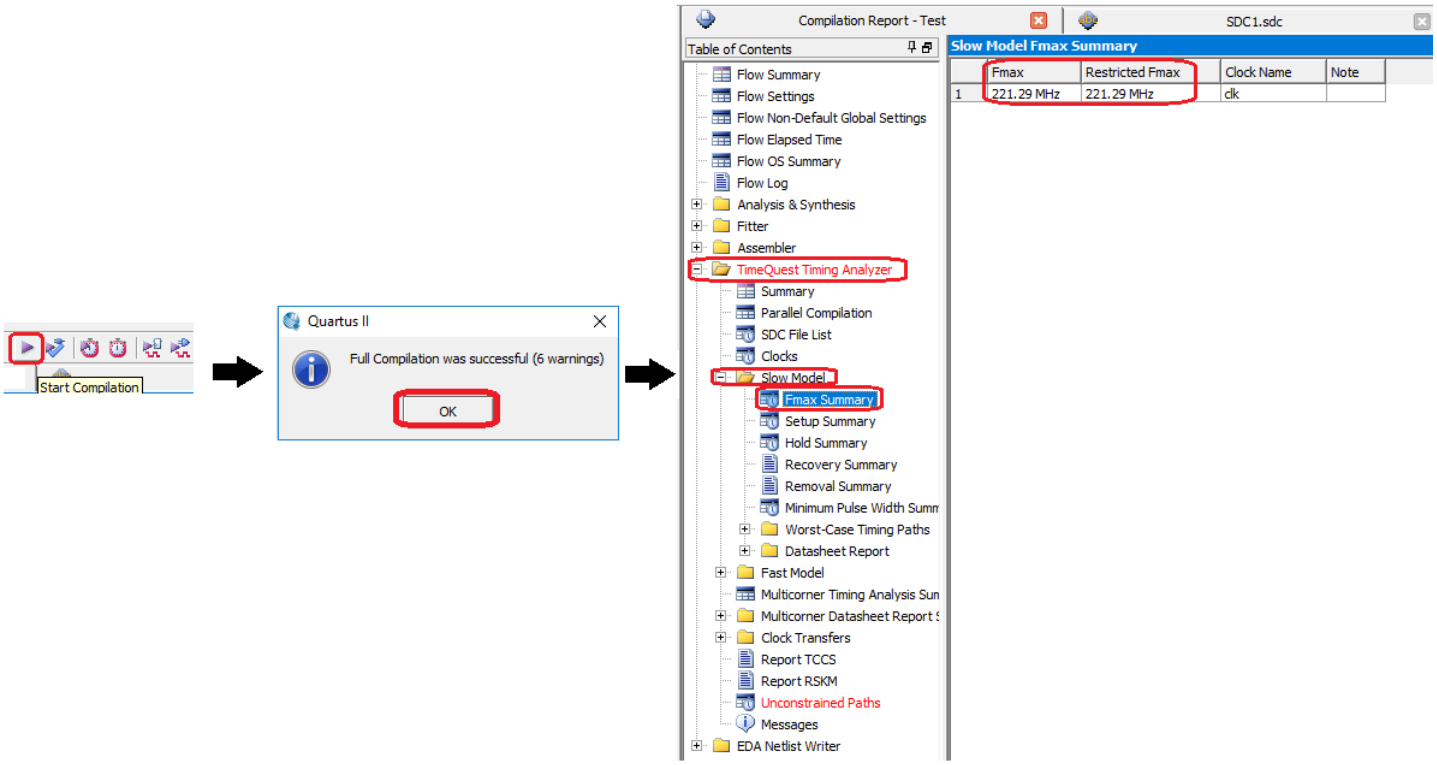
Signal Name	FPGA Pin No.	Description
SW[0]	PIN_L22	Toggle Switch[0]

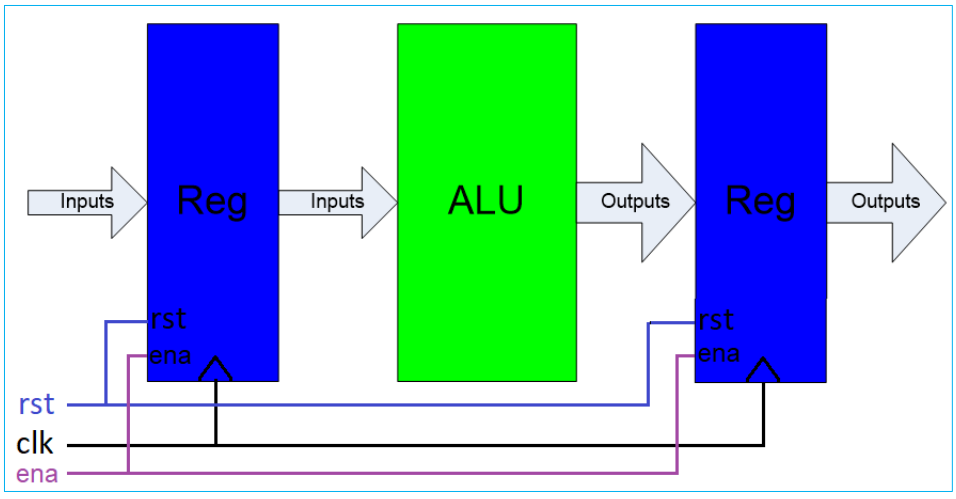
Table 4.1. Pin assignments for the toggle switches.

LEDG[0]	PIN_U22	LED Green[0]
LEDG[1]	PIN_U21	LED Green[1]
LEDG[2]	PIN_V22	LED Green[2]
LEDG[3]	PIN_V21	LED Green[3]
LEDG[4]	PIN_W22	LED Green[4]
LEDG[5]	PIN_W21	LED Green[5]
LEDG[6]	PIN_Y22	LED Green[6]
LEDG[7]	PIN_Y21	LED Green[7]

Table 4.3. Pin assignments for the LEDs.

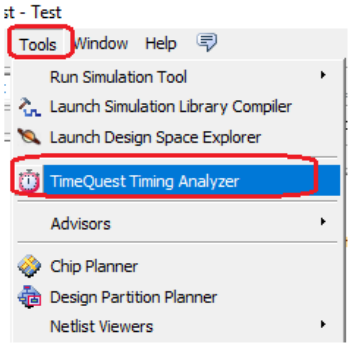
7. Step 7 – Full compilation (finding of f_{max}):

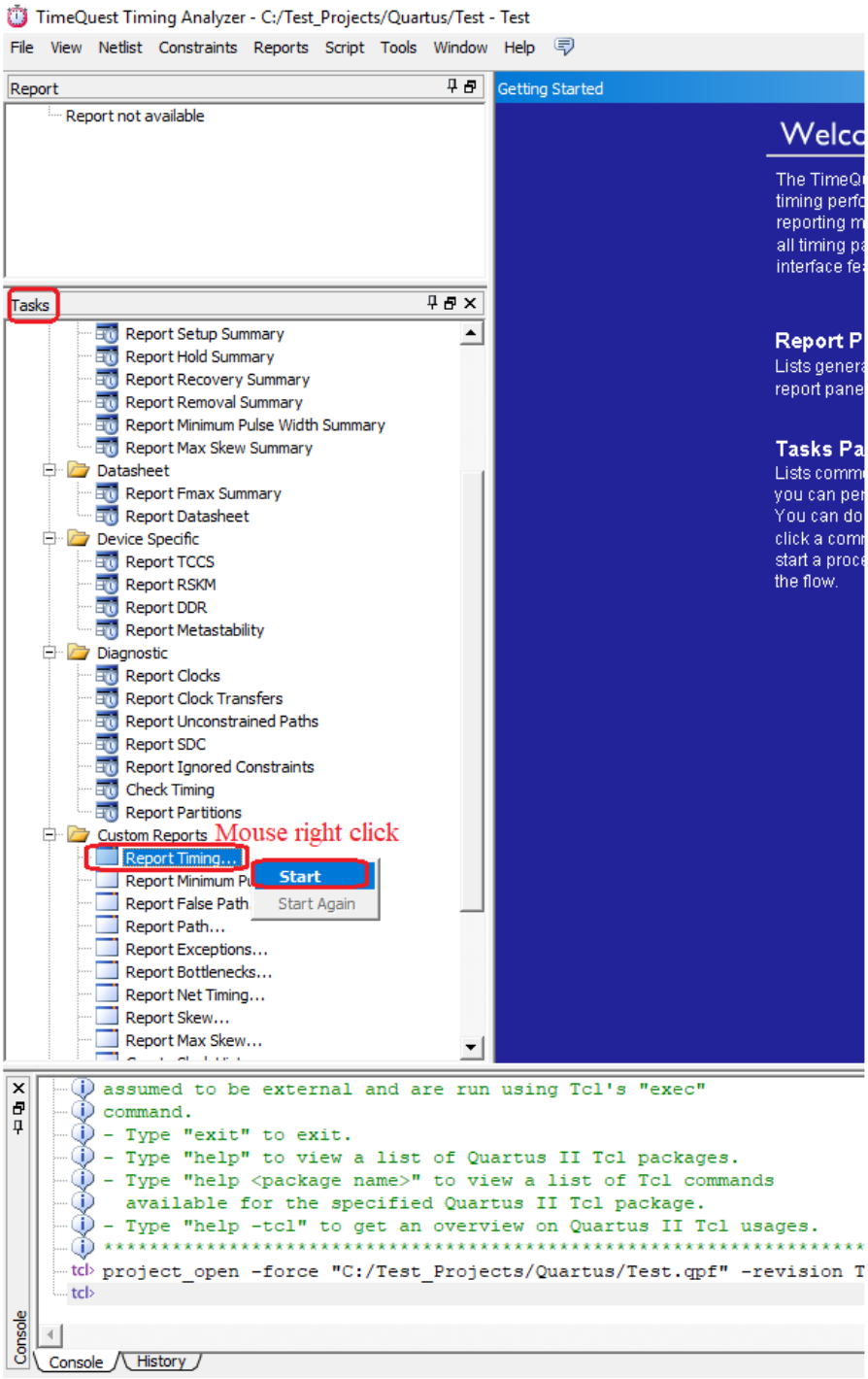


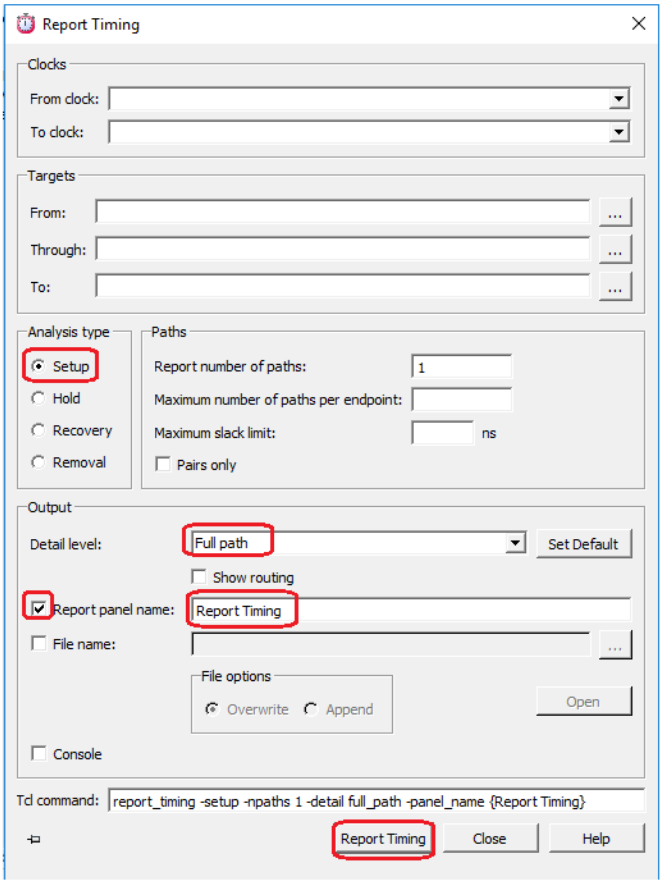


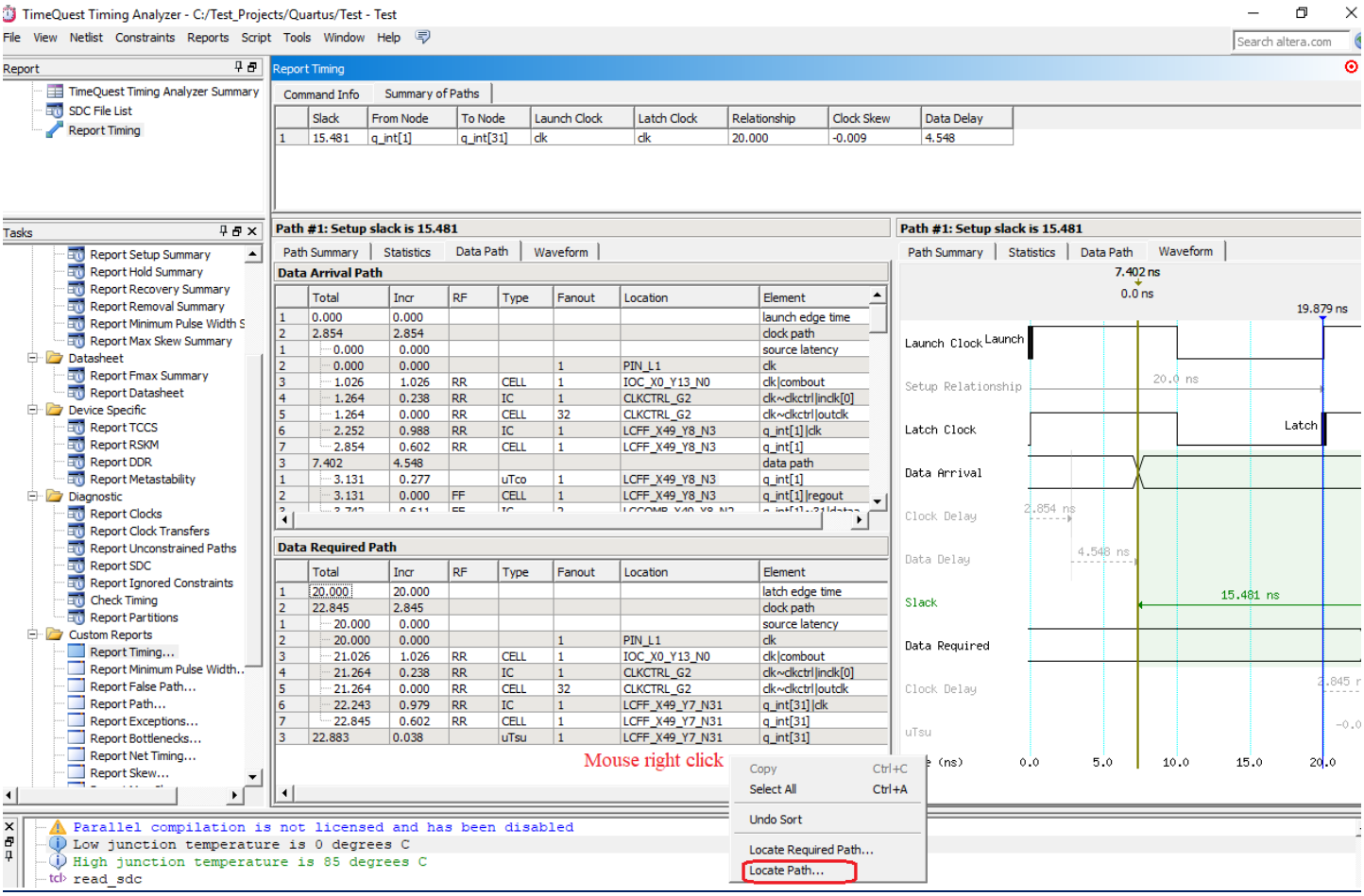
Explanation: In order Quartus IDE can calculate f_{max} the logic design parts must be wrapped by registers

8. Step 8 – Finding The Critical Path Location:

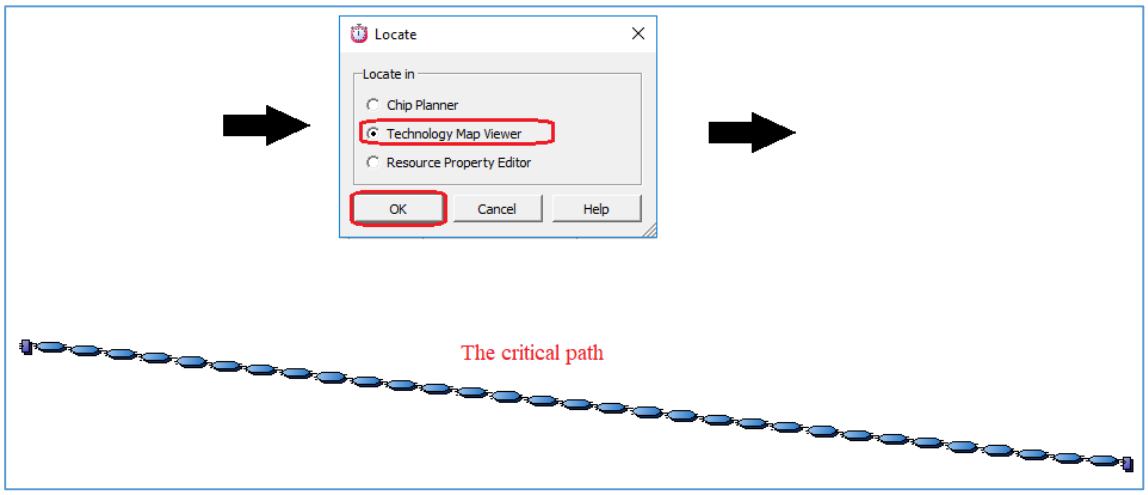




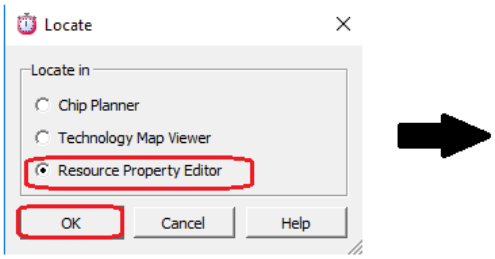

Report Timing
Clocks
From clock:
To clock:
Targets
From:
Through:
To:
Analysis type
Setup
Hold
Recovery
Removal
Paths
Report number of paths: 1
Maximum number of paths per endpoint:
Maximum slack limit: ns
Pairs only
Output
Detail level: Full path
Set Default
Show routing
Report panel name: Report Timing
File name:
File options
Overwrite
Append
Open
Console
Tcl command: report_timing -setup -npaths 1 -detail full_path -panel_name {Report Timing}
Report Timing
Close
Help

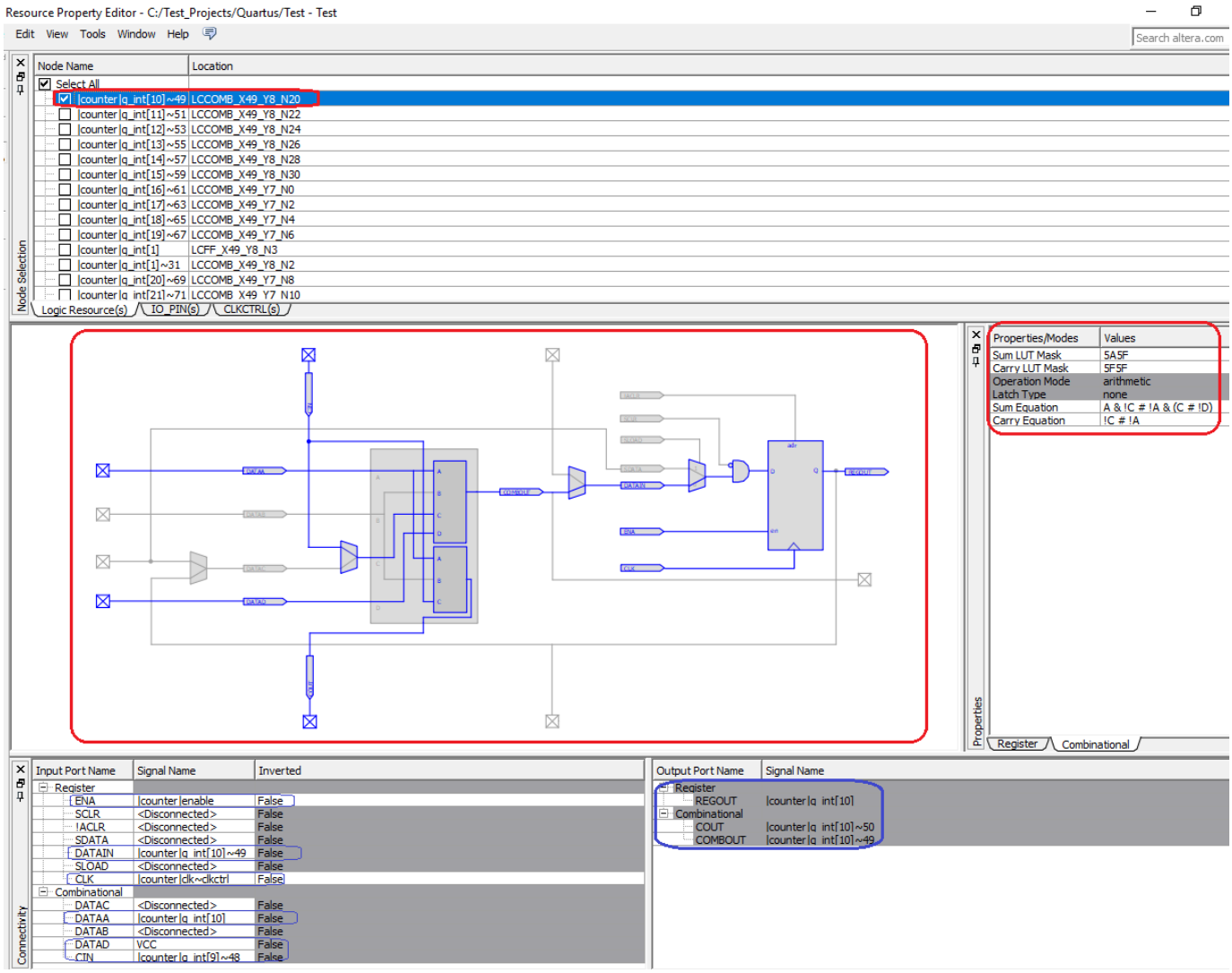

TimeQuest Timing Analyzer - C:/Test_Projects/Quartus/Test - Test
File View Netlist Constraints Reports Script Tools Window Help
Report
TimeQuest Timing Analyzer Summary
SDC File List
Report Timing
Tasks
Report Timing
Command Info
Summary of Paths
Slack From Node To Node Launch Clock Latch Clock Relationship Clock Skew Data Delay
15.481 q_int[1] q_int[31] clk clk 20.000 -0.009 4.548
Path #1: Setup slack is 15.481
Path Summary Statistics Data Path Waveform
Data Arrival Path
Data Required Path
Mouse right click
Copy Ctrl+C
Select All Ctrl+A
Undo Sort
Locate Required Path...
Locate Path...
Parallel compilation is not licensed and has been disabled
Low junction temperature is 0 degrees C
High junction temperature is 85 degrees C
read_sdc

i. Technology Map Viewer:

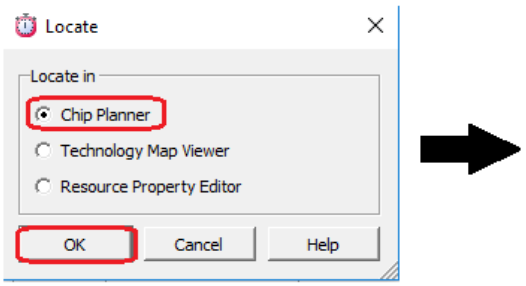


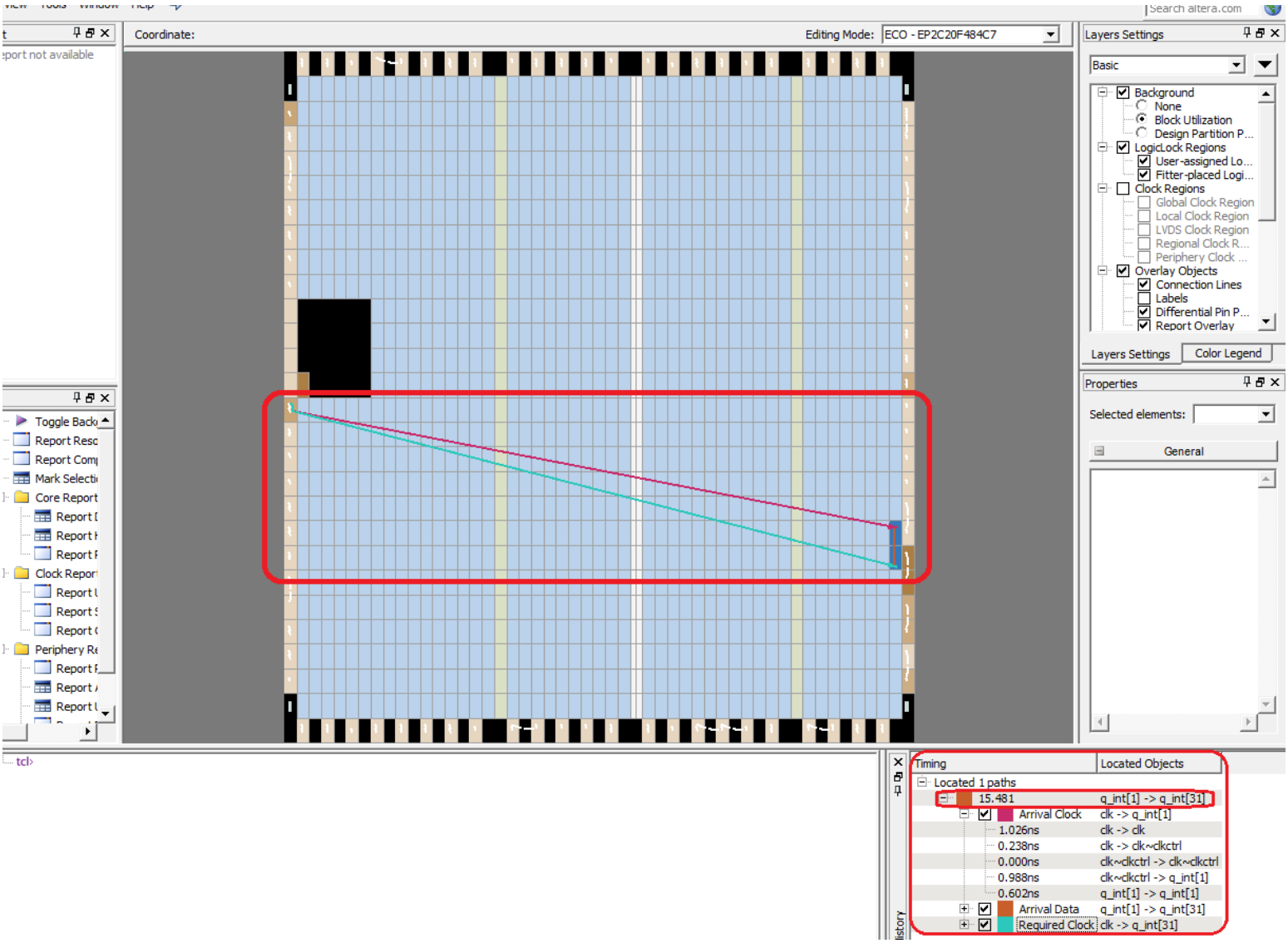
ii. Resource Property Editor:



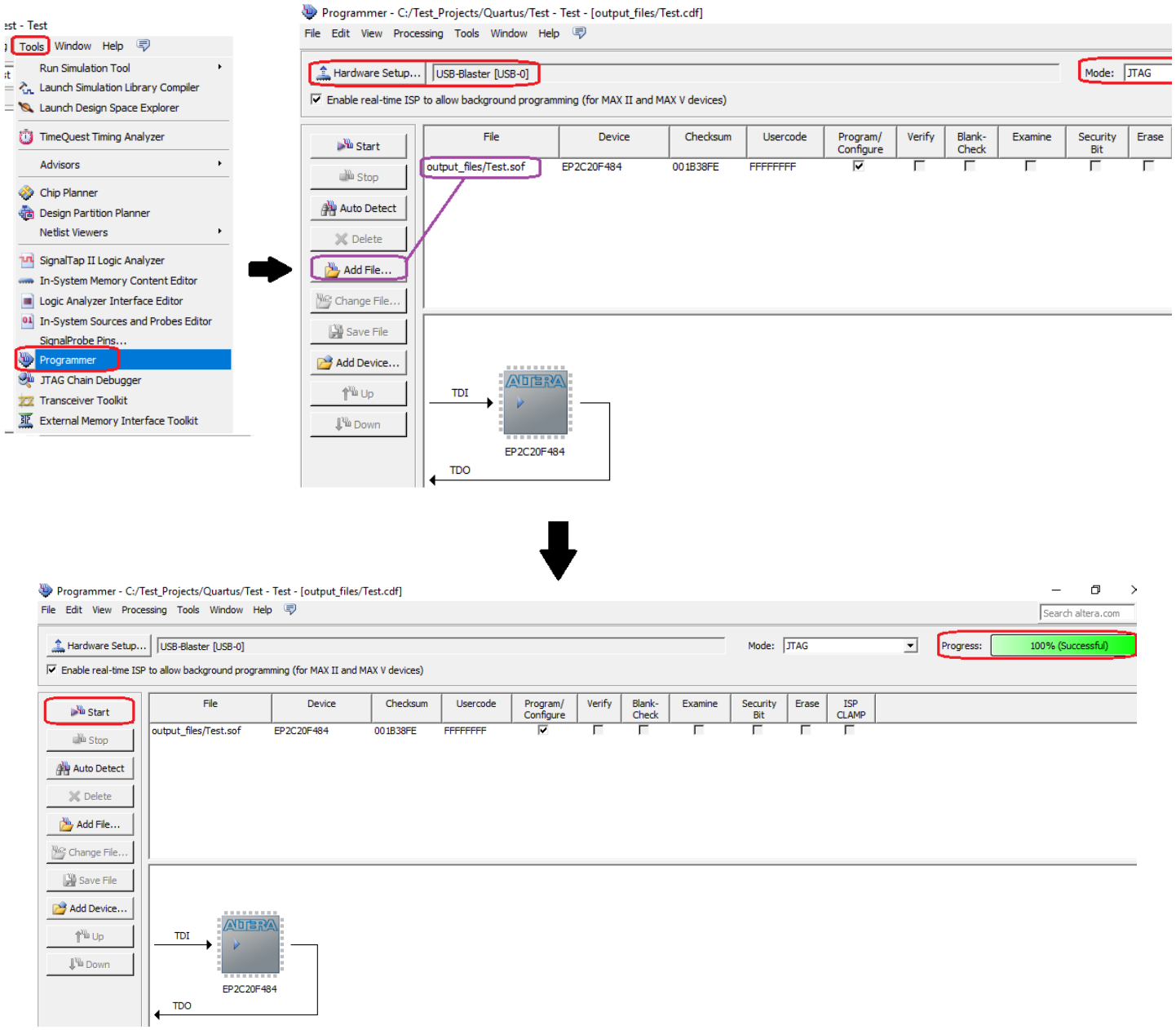


iii. Chip Planner:



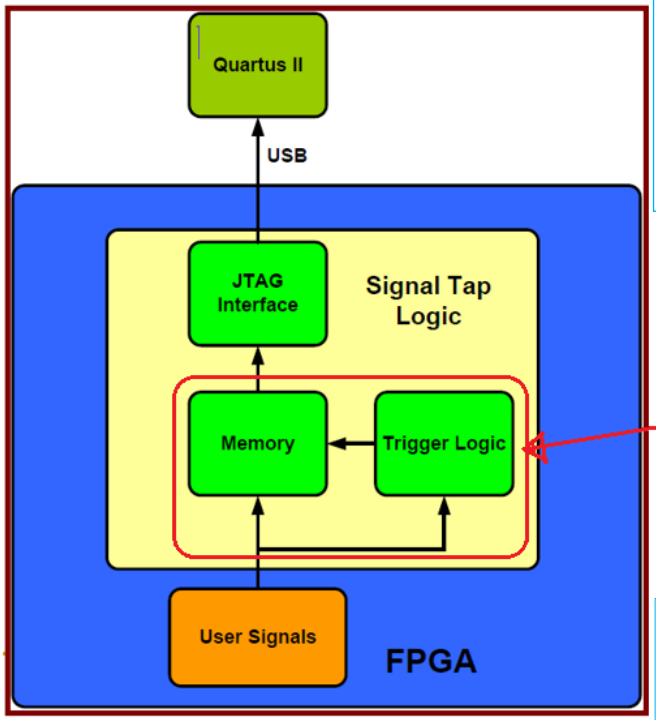


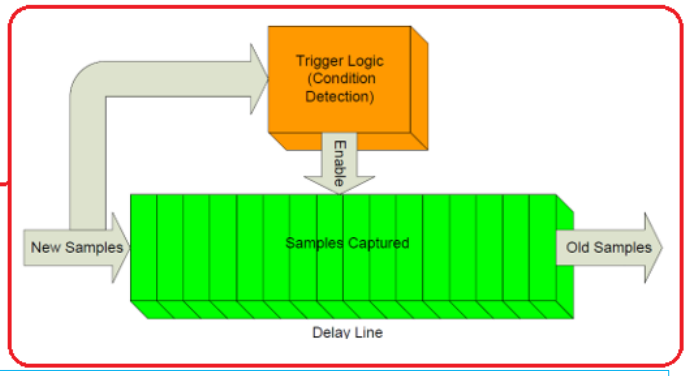
9. Step 9 – Code Programming:



B. Verification – Using Signal TAP:

1. Block Diagram:





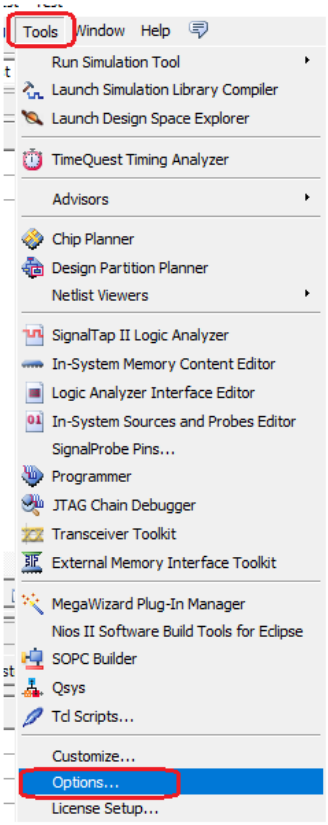
Signal TAP Pros & Cons:

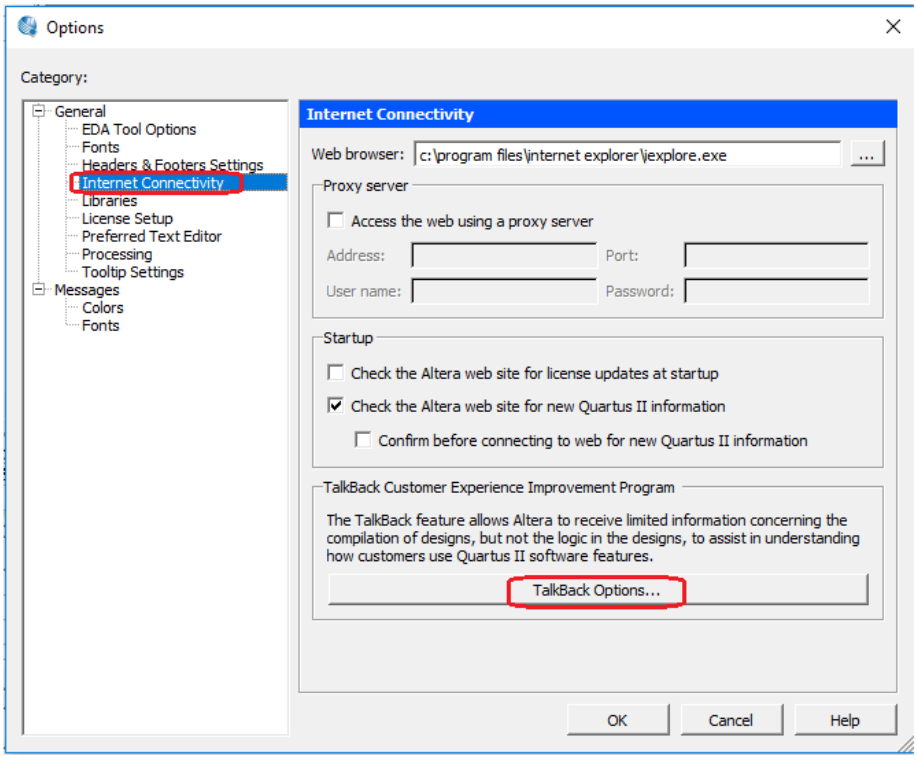
- Captures real time state of FPGA internal signals and pins (up to 200MHz)
- Connects to Quartus II through JTAG
- Do not require huge and expensive equipment
- Uses internal FPGA resources
  - Memory Blocks
  - Logic Elements
- Each time the captured signals list change the design must be recompiled

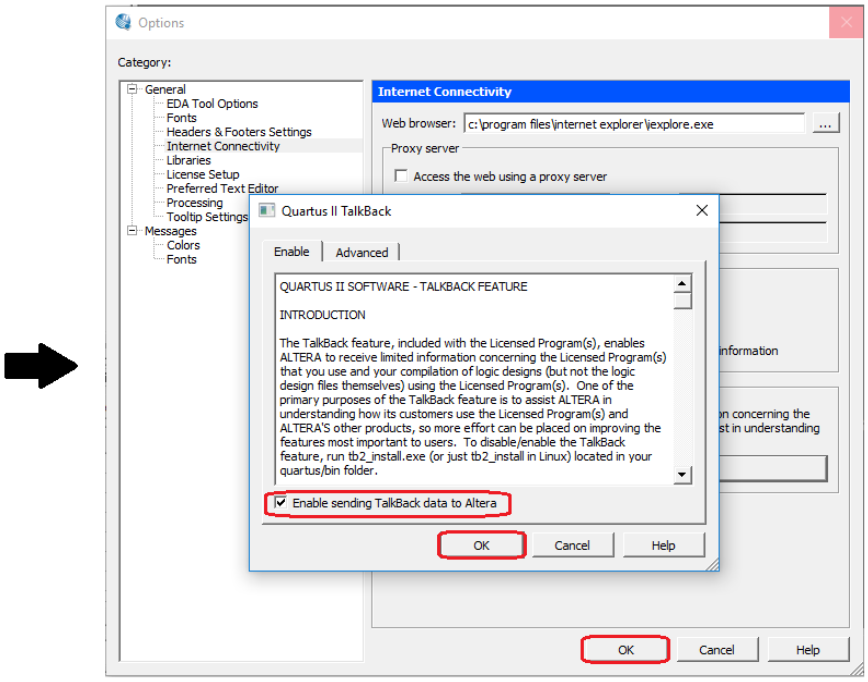
Signal TAP Features:

- Up to 1024 Data Channels
- Multiple Analyzers in One Device
  - Supports Analysis of Multiple Clock Domains
  - Each Analyzer Can Run Simultaneously
- Multiple Analyzers in One Device
- Up to 10 Trigger Levels Per Channel

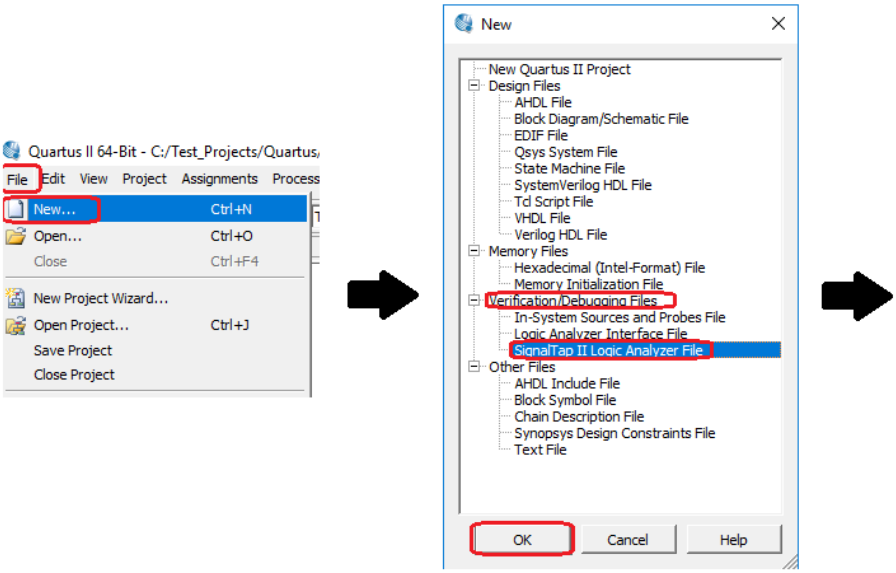
2. Using STP with a student activation license:

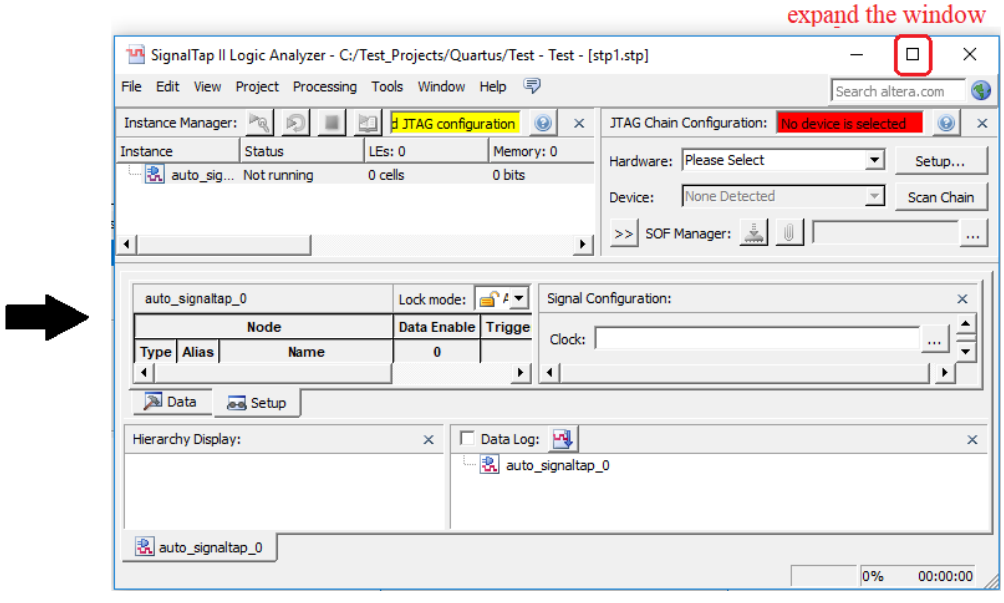




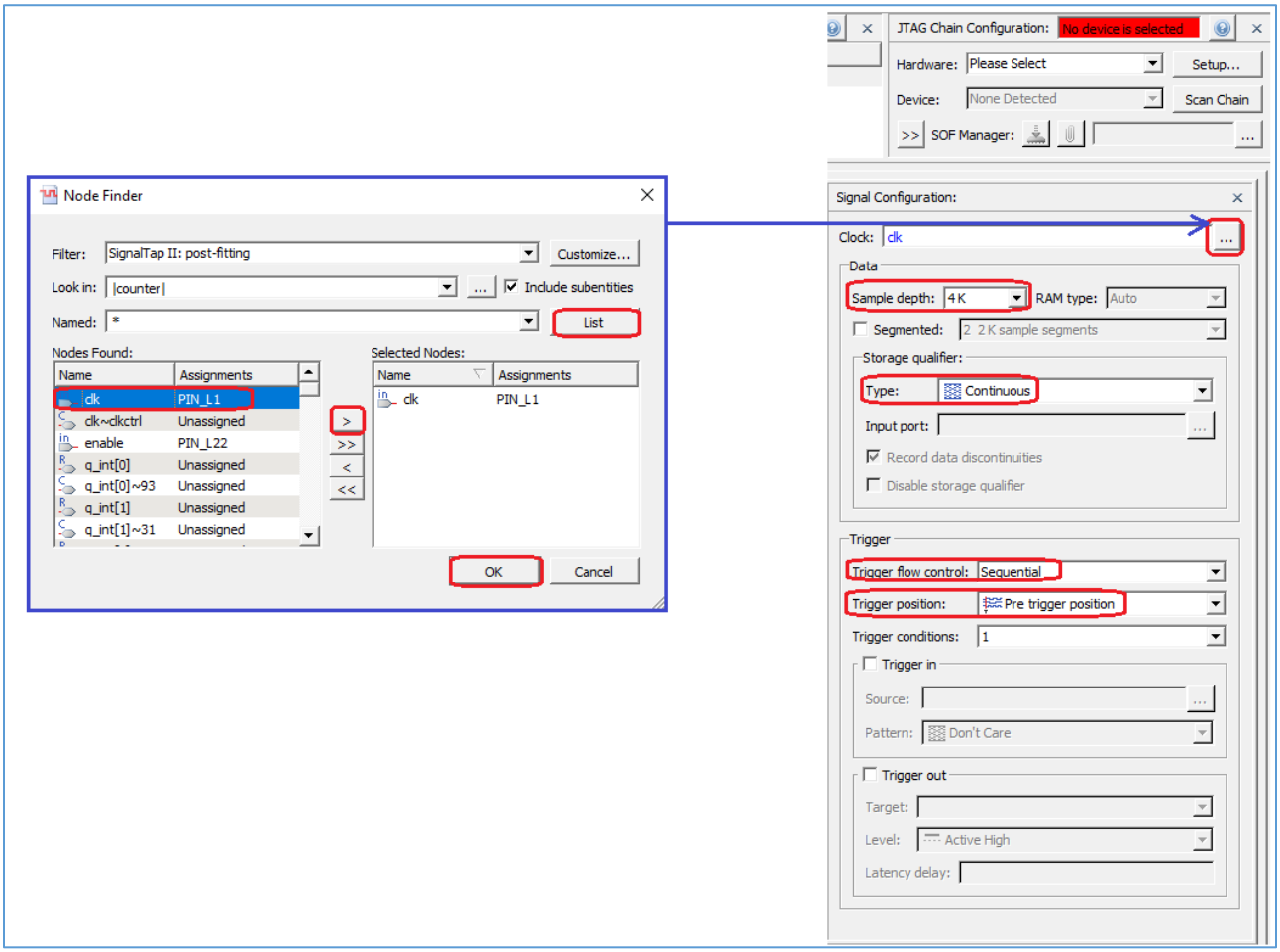


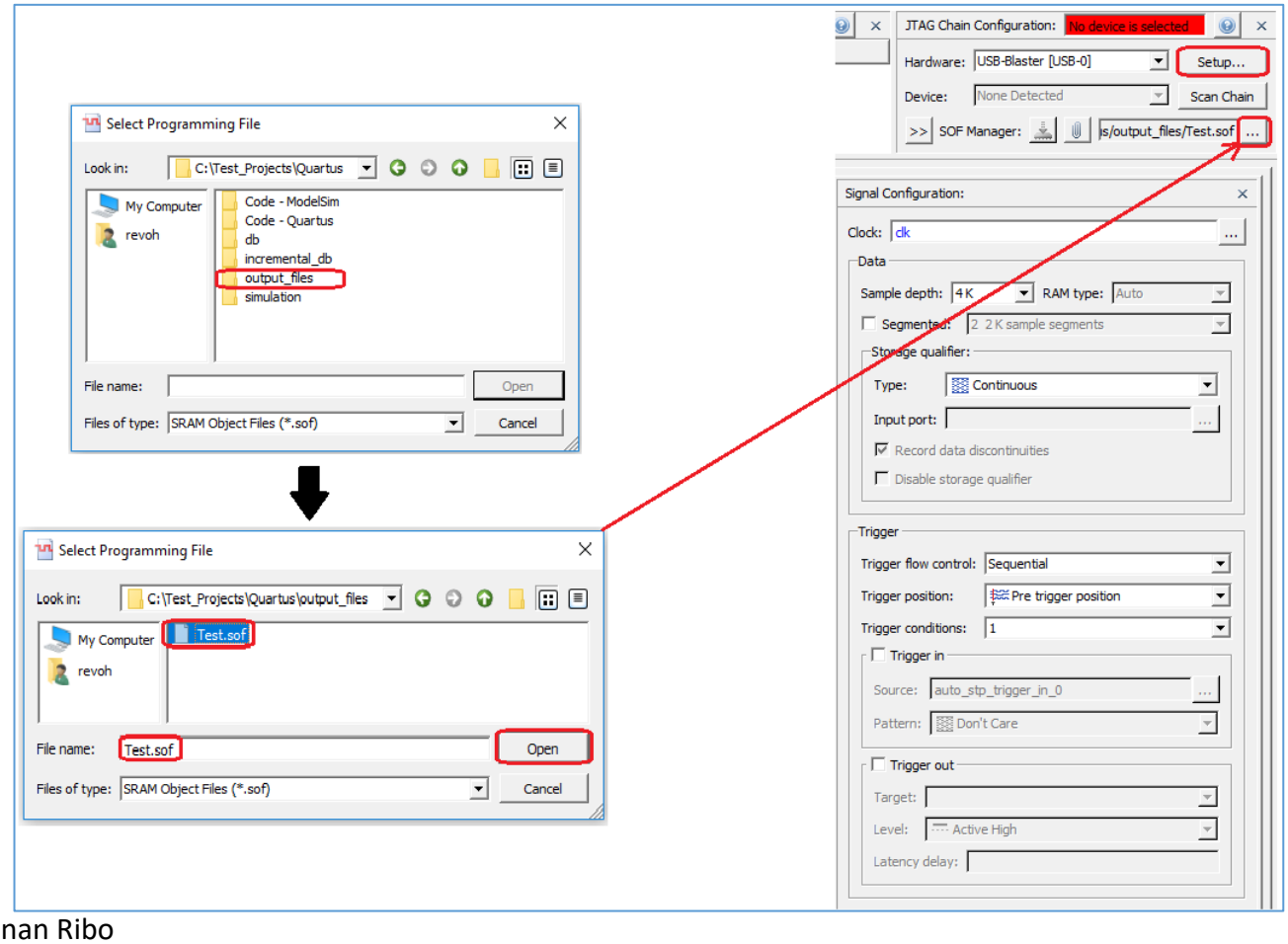
3. Create a new STP file:

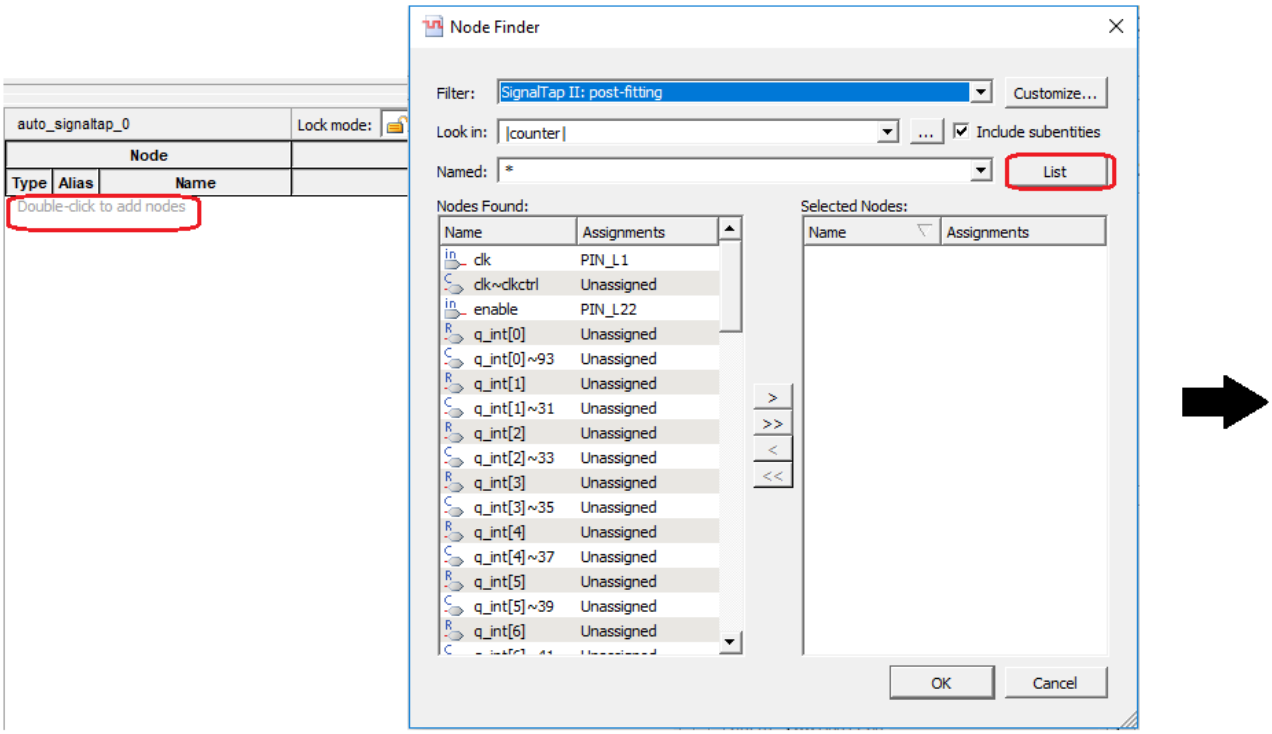




4. Configurations (after expansion of the previous window):






auto_signaltap_0
Lock mode:
Node
Type
Alias
Name
Double-click to add nodes
Node Finder
Filter:
SignalTap II: post-fitting
Customize...
Look in:
|counter|
Include subentities
Named:
*
List
Nodes Found:
Name
Assignments
clk
PIN_L1
clk~clkctrl
Unassigned
enable
PIN_L22
q_int[0]
Unassigned
q_int[0]~93
Unassigned
q_int[1]
Unassigned
q_int[1]~31
Unassigned
q_int[2]
Unassigned
q_int[2]~33
Unassigned
q_int[3]
Unassigned
q_int[3]~35
Unassigned
q_int[4]
Unassigned
q_int[4]~37
Unassigned
q_int[5]
Unassigned
q_int[5]~39
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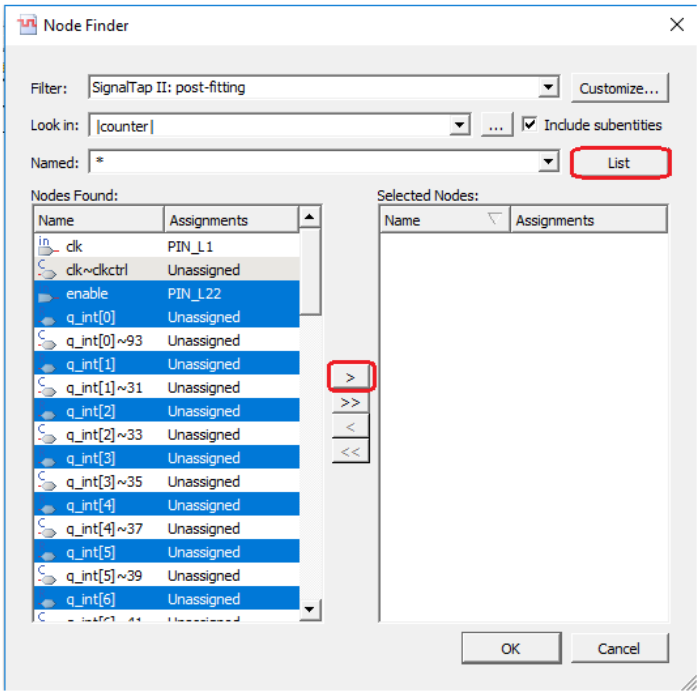
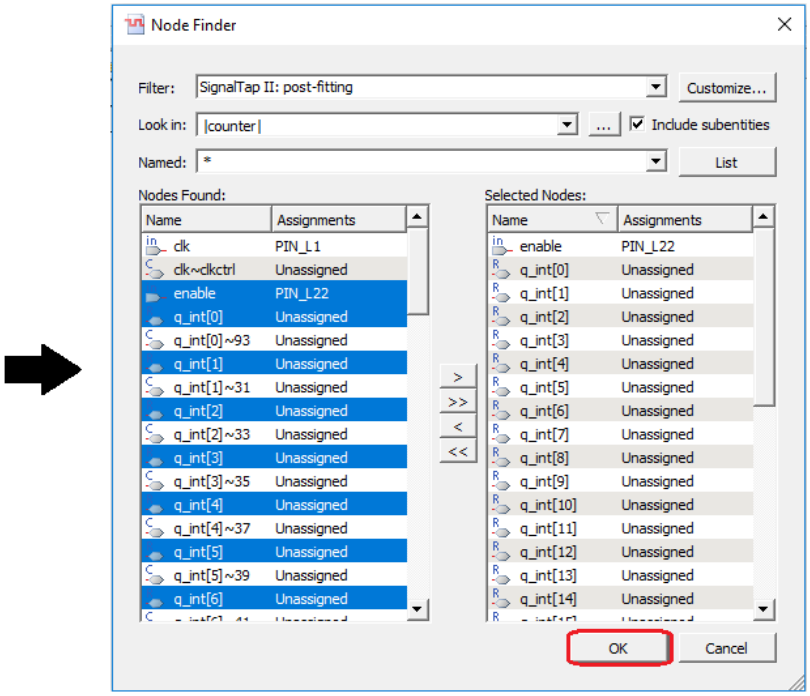
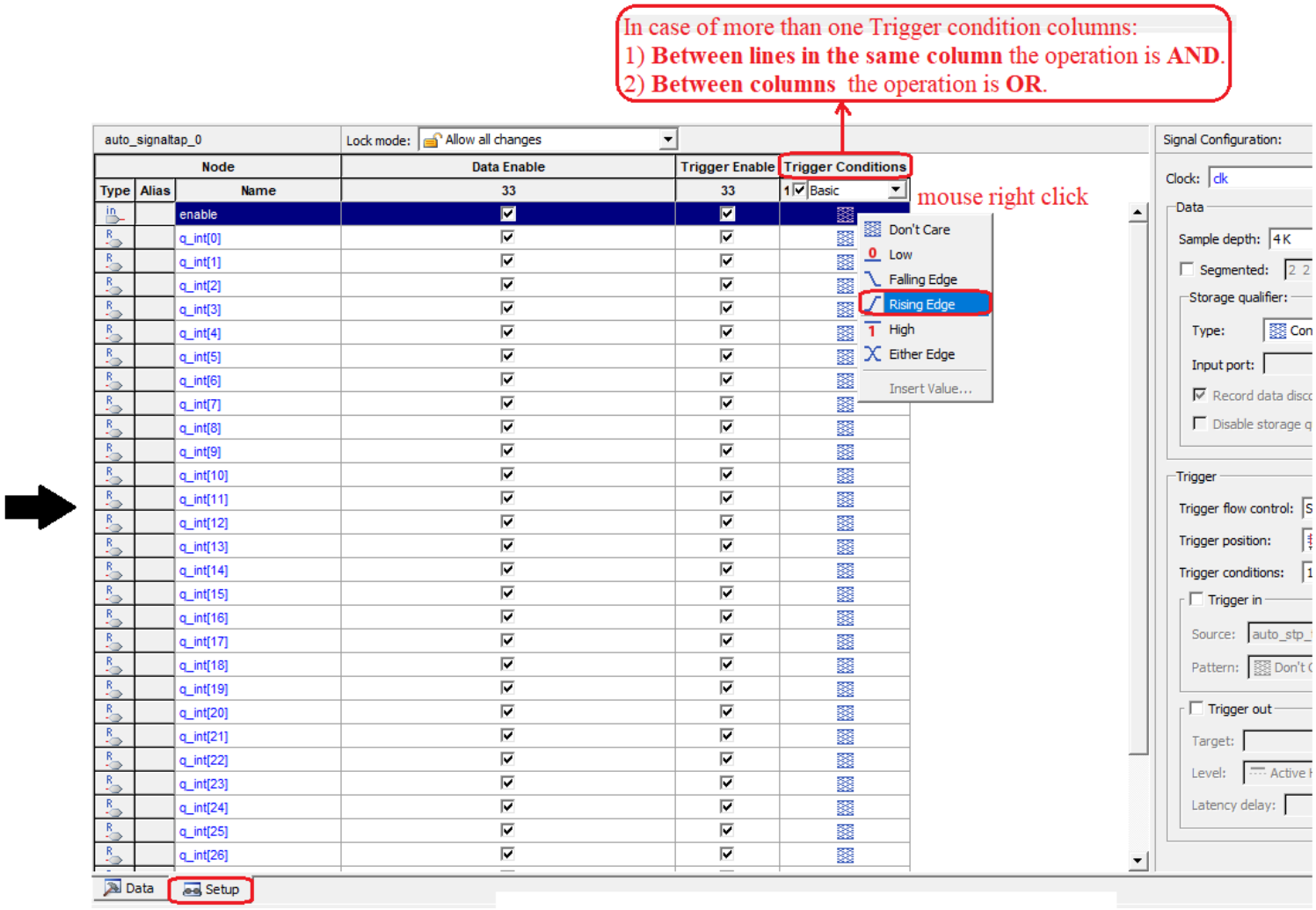
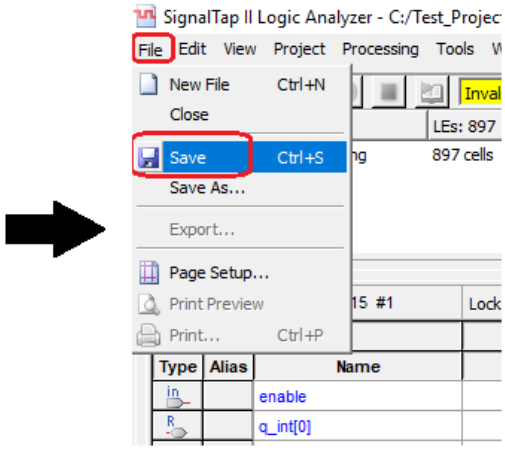
Selected Nodes:
Name
Assignments
>
>>
<
<<
OK
Cancel

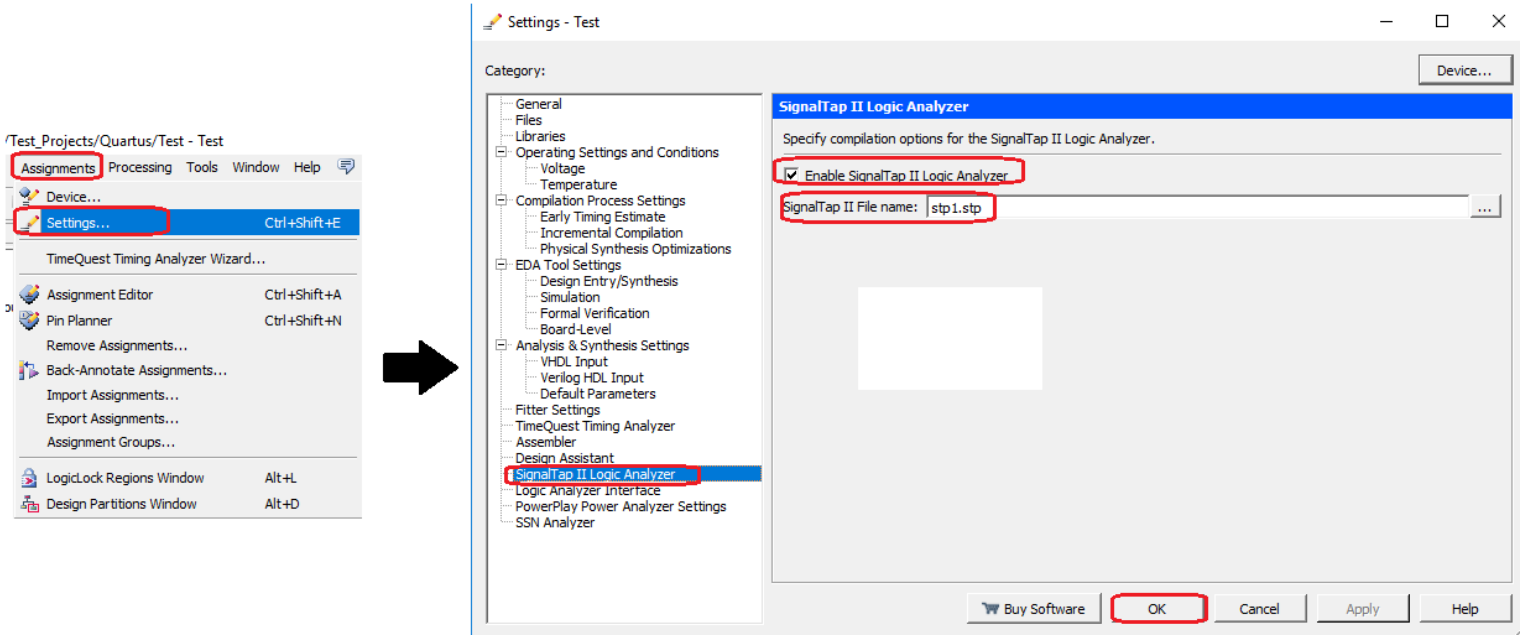

Node Finder
Filter:
SignalTap II: post-fitting
Customize...
Look in:
|counter|
Include subentities
Named:
*
List
Nodes Found:
Name
Assignments
clk
PIN_L1
clk~clkctrl
Unassigned
enable
PIN_L22
q_int[0]
Unassigned
q_int[0]~93
Unassigned
q_int[1]
Unassigned
q_int[1]~31
Unassigned
q_int[2]
Unassigned
q_int[2]~33
Unassigned
q_int[3]
Unassigned
q_int[3]~35
Unassigned
q_int[4]
Unassigned
q_int[4]~37
Unassigned
q_int[5]
Unassigned
q_int[5]~39
Unassigned
q_int[6]
Unassigned
Selected Nodes:
Name
Assignments
>
>>
<
<<
OK
Cancel


Node Finder
Filter:
SignalTap II: post-fitting
Customize...
Look in:
|counter|
Include subentities
Named:
*
List
Nodes Found:
Name
Assignments
clk
PIN_L1
clk~clkctrl
Unassigned
enable
PIN_L22
q_int[0]
Unassigned
q_int[0]~93
Unassigned
q_int[1]
Unassigned
q_int[1]~31
Unassigned
q_int[2]
Unassigned
q_int[2]~33
Unassigned
q_int[3]
Unassigned
q_int[3]~35
Unassigned
q_int[4]
Unassigned
q_int[4]~37
Unassigned
q_int[5]
Unassigned
q_int[5]~39
Unassigned
q_int[6]
Unassigned
Selected Nodes:
Name
Assignments
enable
PIN_L22
q_int[0]
Unassigned
q_int[1]
Unassigned
q_int[2]
Unassigned
q_int[3]
Unassigned
q_int[4]
Unassigned
q_int[5]
Unassigned
q_int[6]
Unassigned
q_int[7]
Unassigned
q_int[8]
Unassigned
q_int[9]
Unassigned
q_int[10]
Unassigned
q_int[11]
Unassigned
q_int[12]
Unassigned
q_int[13]
Unassigned
q_int[14]
Unassigned
>
>>
<
<<
OK
Cancel


In case of more than one Trigger condition columns:
1) Between lines in the same column the operation is AND.
2) Between columns the operation is OR.
auto_signaltap_0
Lock mode:
Allow all changes
Node
Data Enable
Trigger Enable
Trigger Conditions
Type
Alias
Name
33
33
1
Basic
mouse right click
Don't Care
Low
Falling Edge
Rising Edge
High
Either Edge
Insert Value...
Signal Configuration:
Clock:
clk
Data
Sample depth:
4K
Segmented:
Storage qualifier:
Type:
Input port:
Trigger
Trigger flow control:
Trigger position:
Trigger conditions:
Trigger in
Source:
Pattern:
Trigger out
Target:
Level:
Latency delay:
Data
Setup

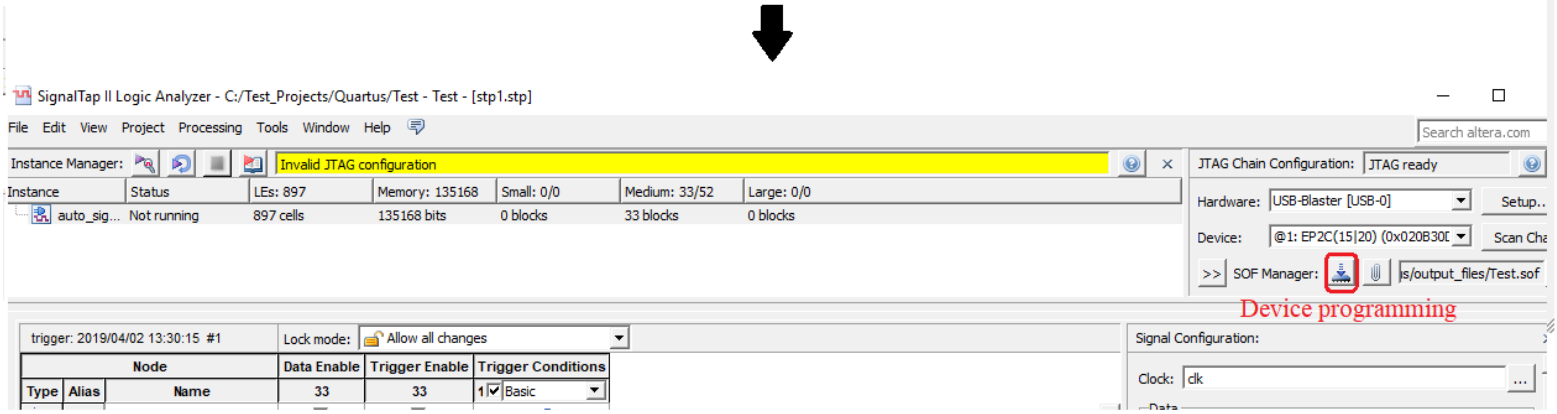

SignalTap II Logic Analyzer - C:/Test_Projec
File
Edit
View
Project
Processing
Tools
New File
Ctrl+N
Close
Save
Ctrl+S
Save As...
Export...
Page Setup...
Print Preview
Print...
Ctrl+P
LEs: 897
897 cells
Type
Alias
Name
enable
q_int[0]

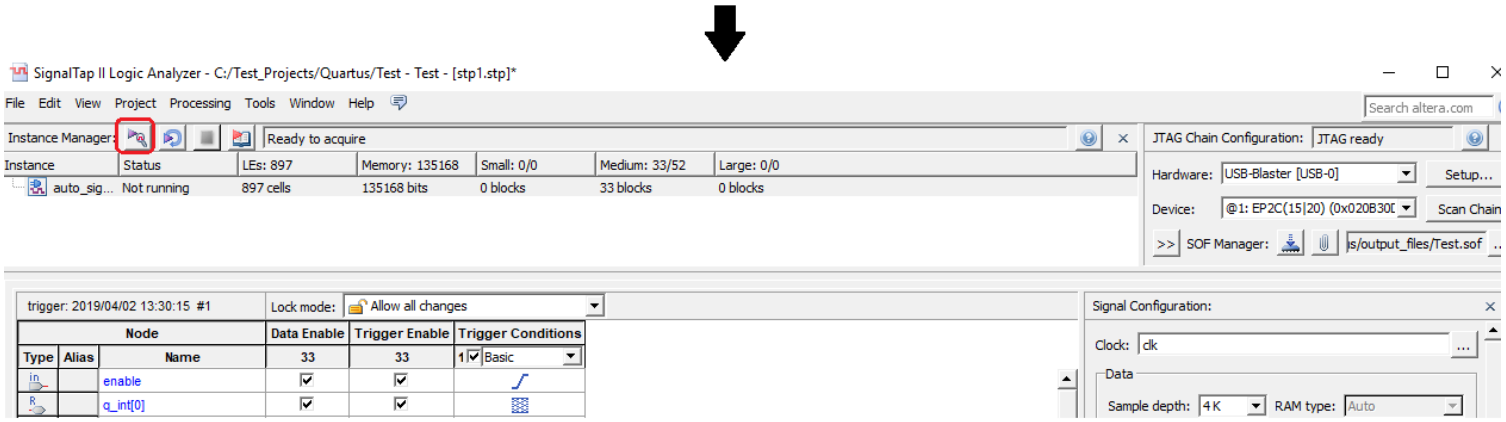
5. Project Compilation and Programming (an eventually the Signals results):

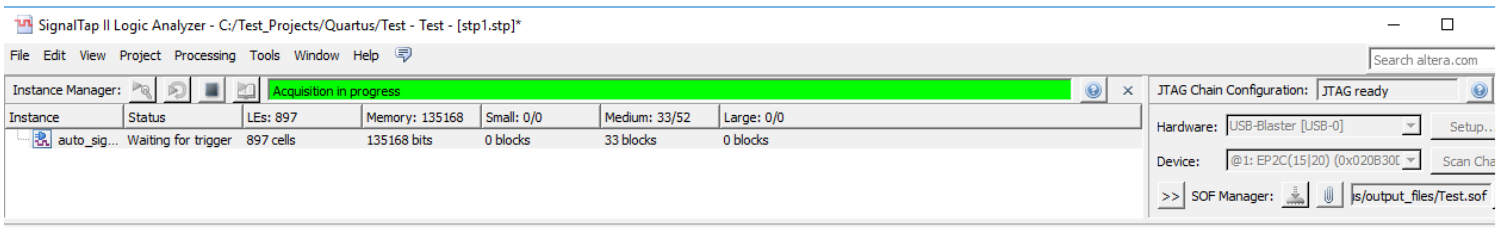


Turn ON the DE1 Board power

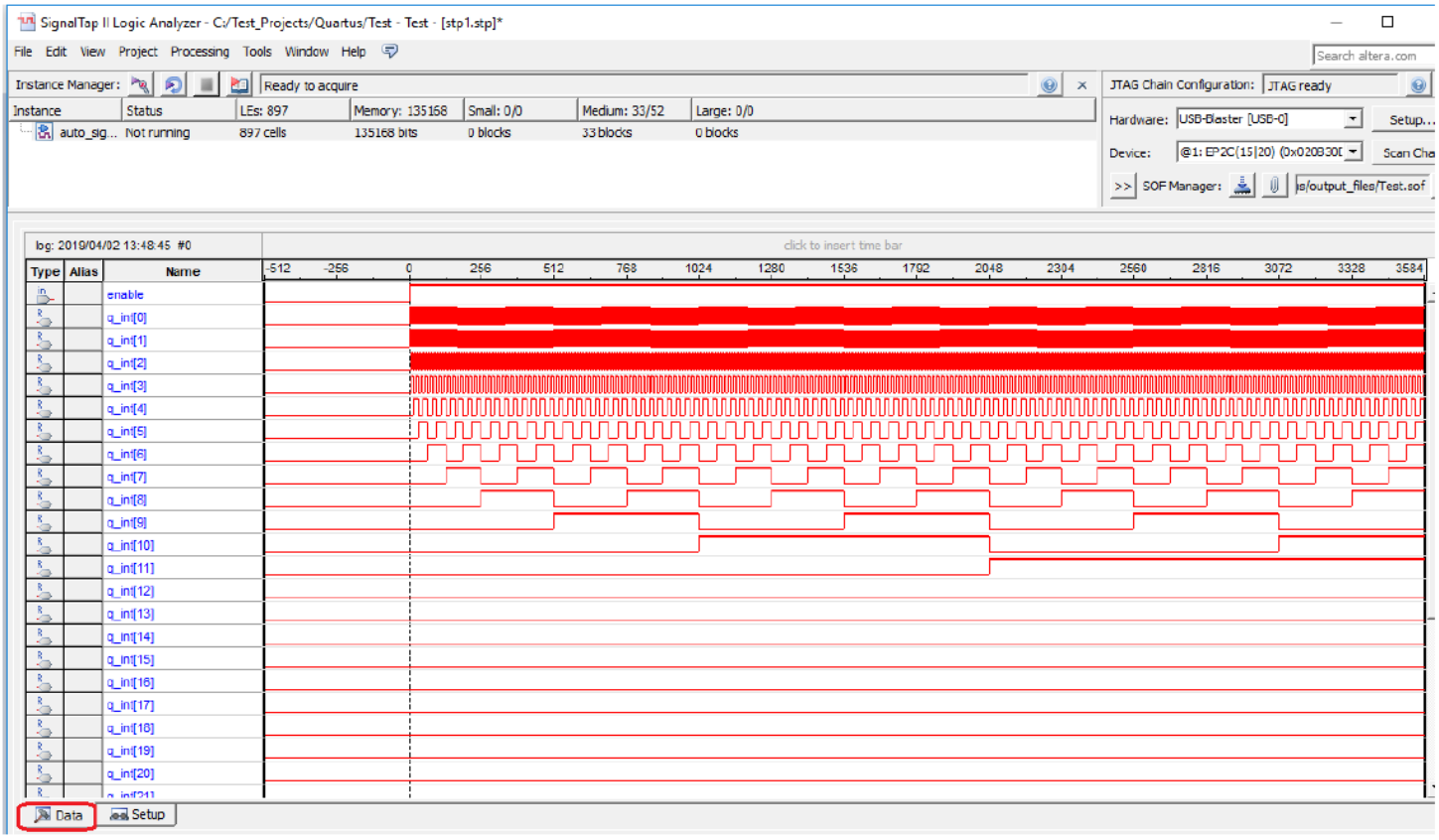
Open the STP file



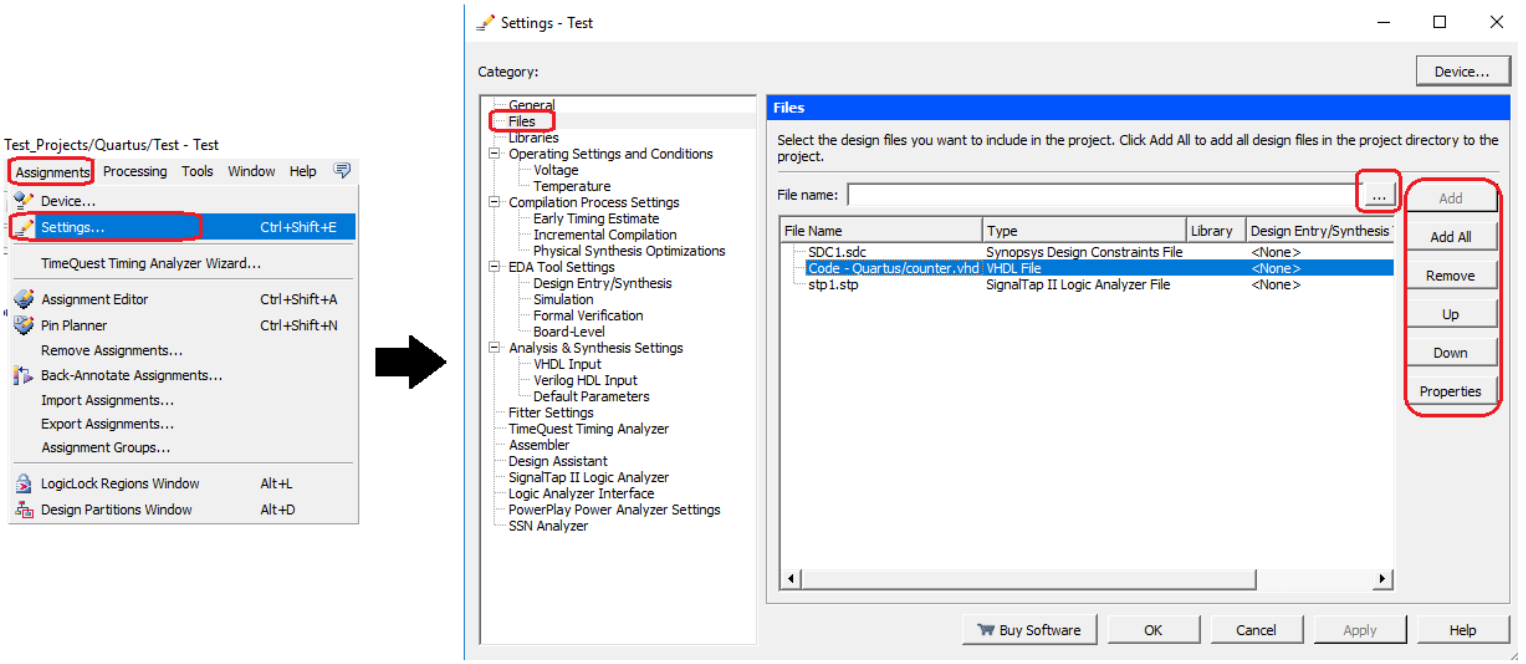




Assert the Trigger



C. Changing the VHDL source files of the project:



D. Open Existing Project: