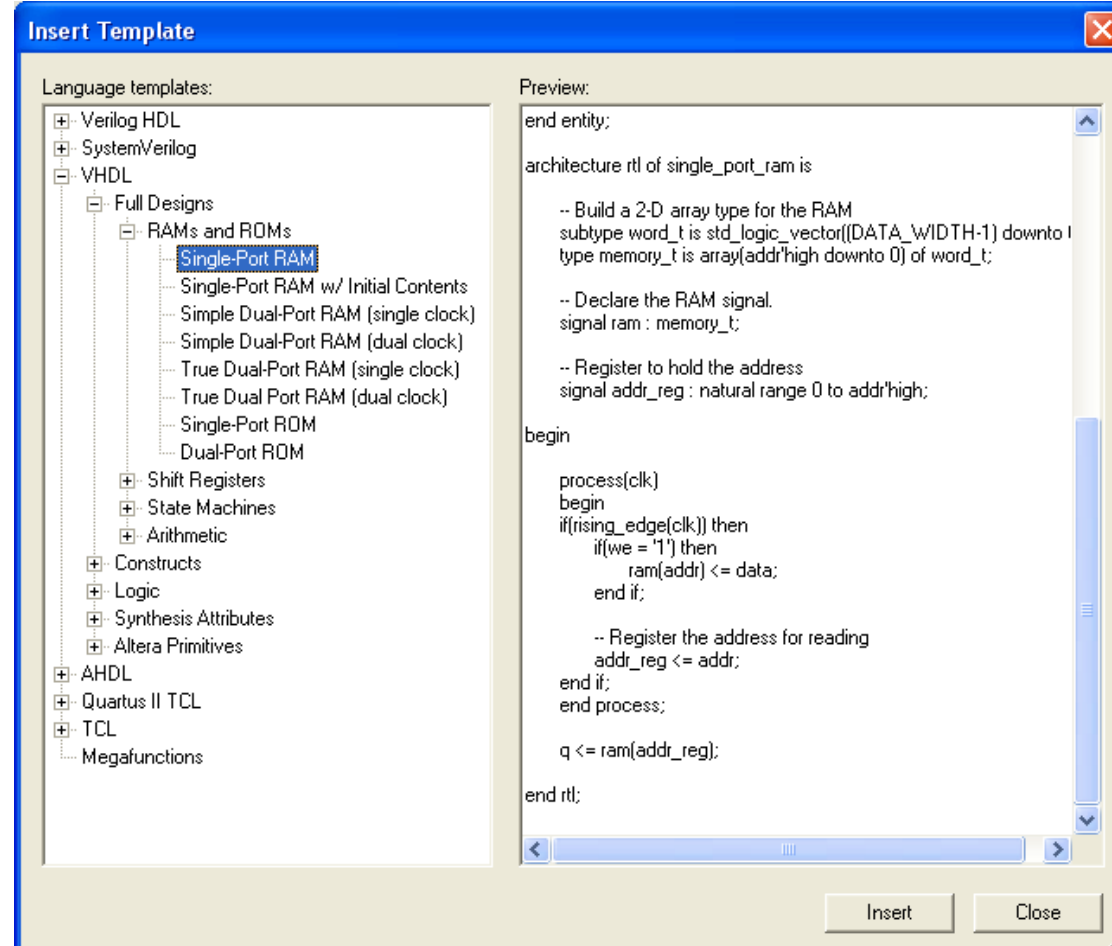


# PLLs and Templates

©Hanan Ribo

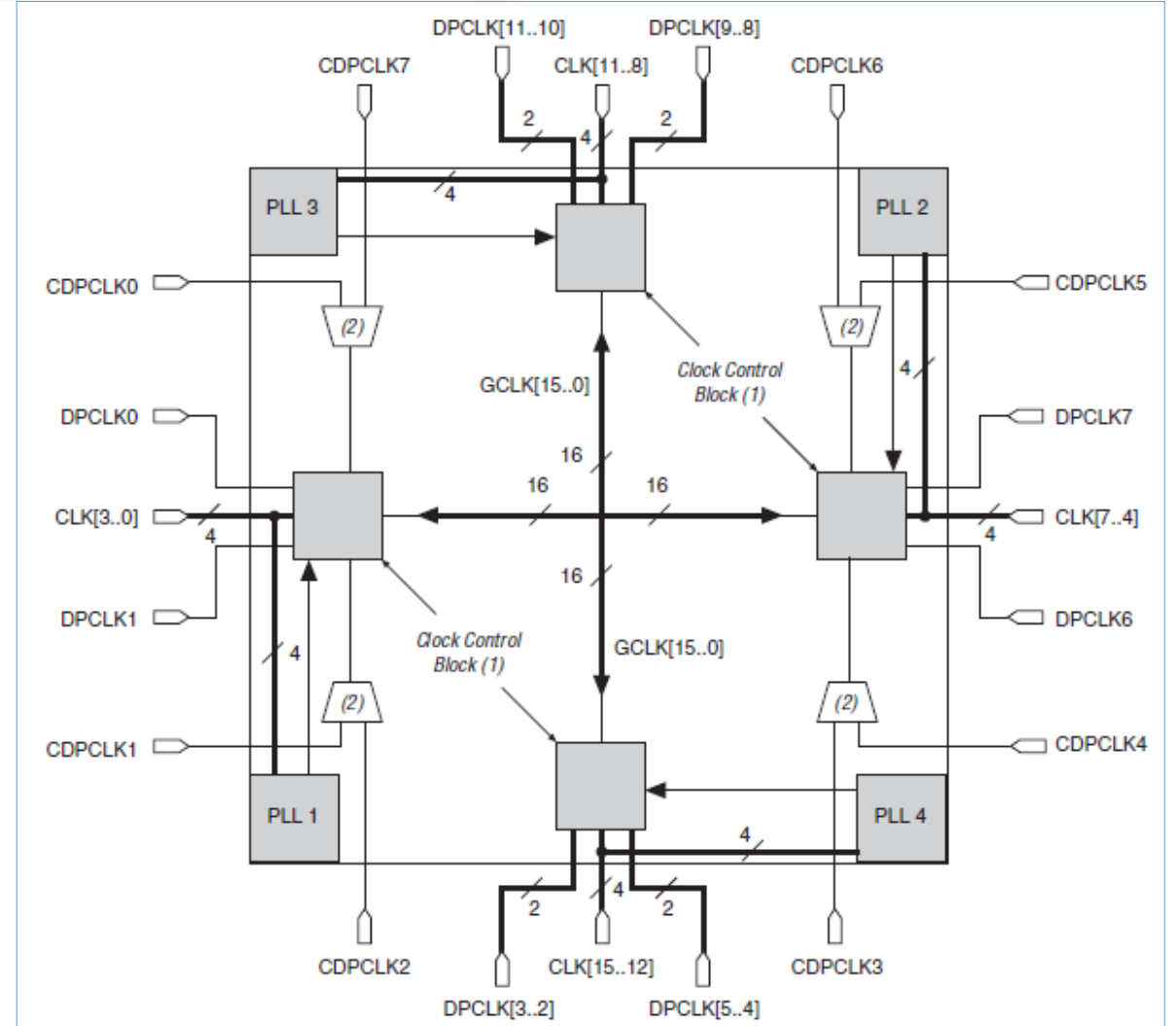
# Hardware Templates

- While in VHDL file push  button on the left
- In a template window select the needed logic template

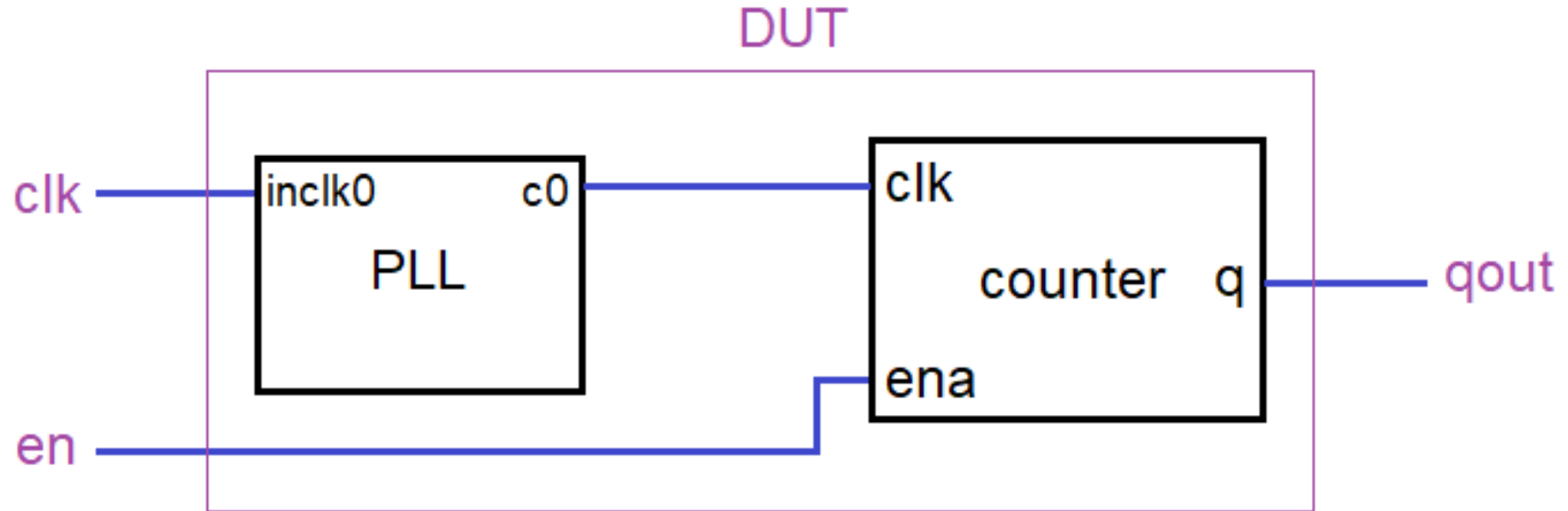


# Cyclone II Clocking

- 16 Global Clocks
- 4 PLLs
- External Oscillator Must be used

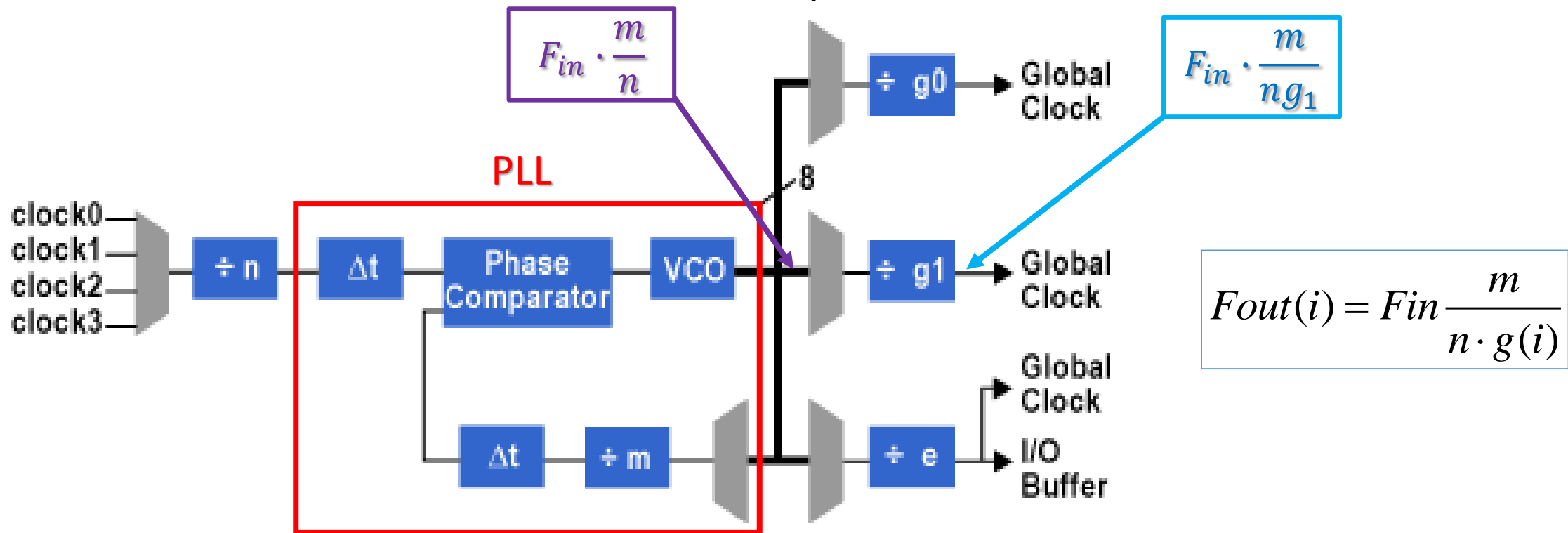


# counter using PLL

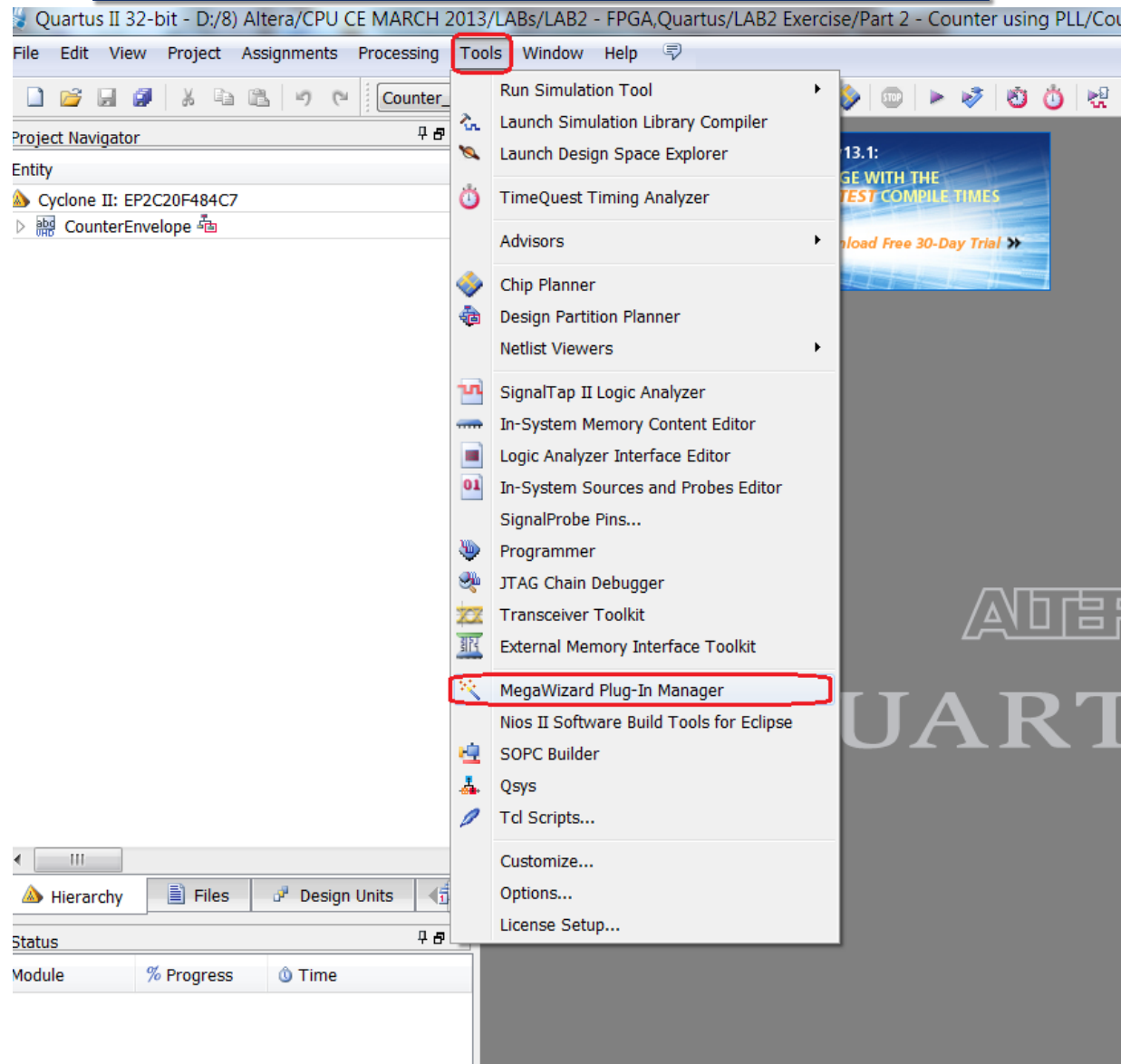


# Cyclone II PLL Structure

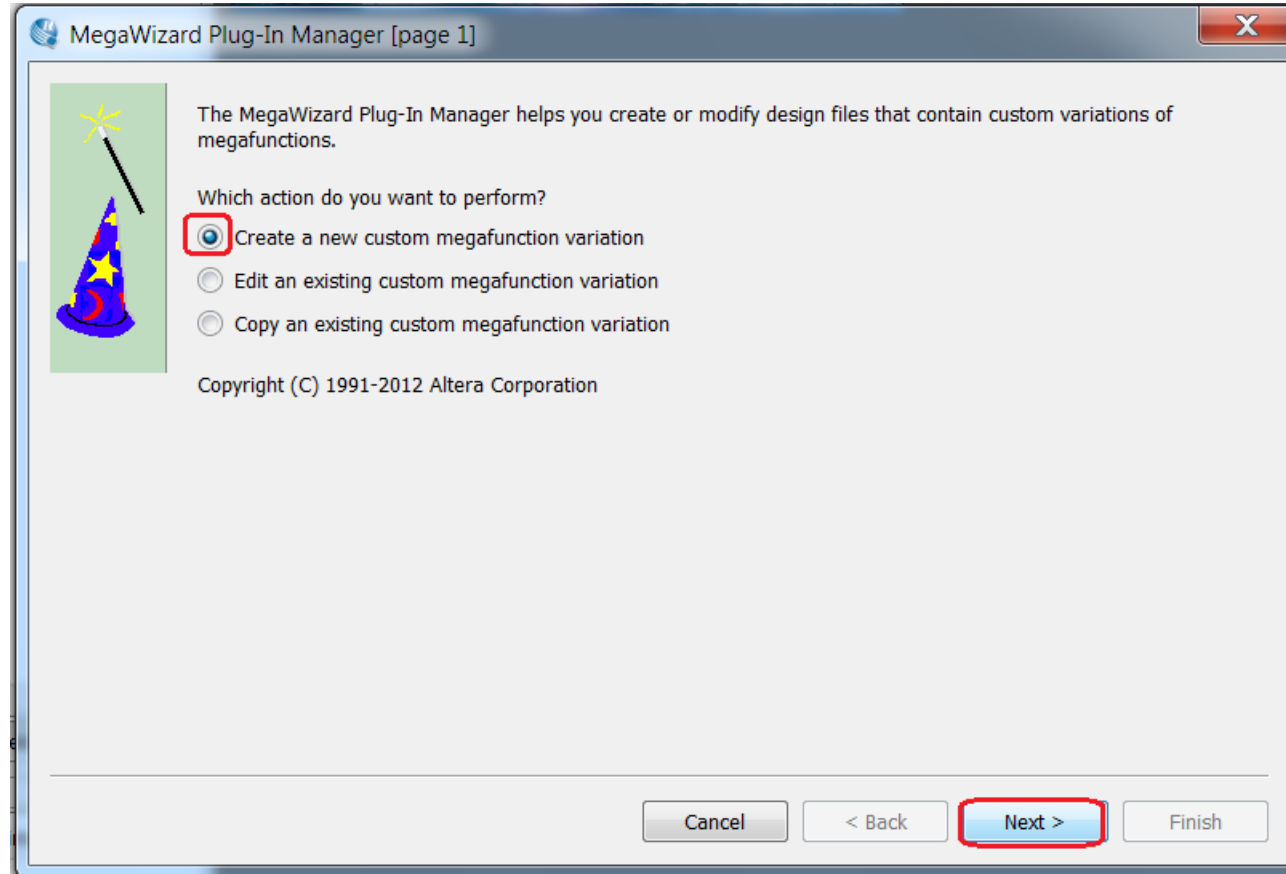
- Enables division and multiplication of clocks
- 3 Outputs with different frequencies
- Input clock can be only from clock pin
- Different Phase shifts between outputs can be achieved



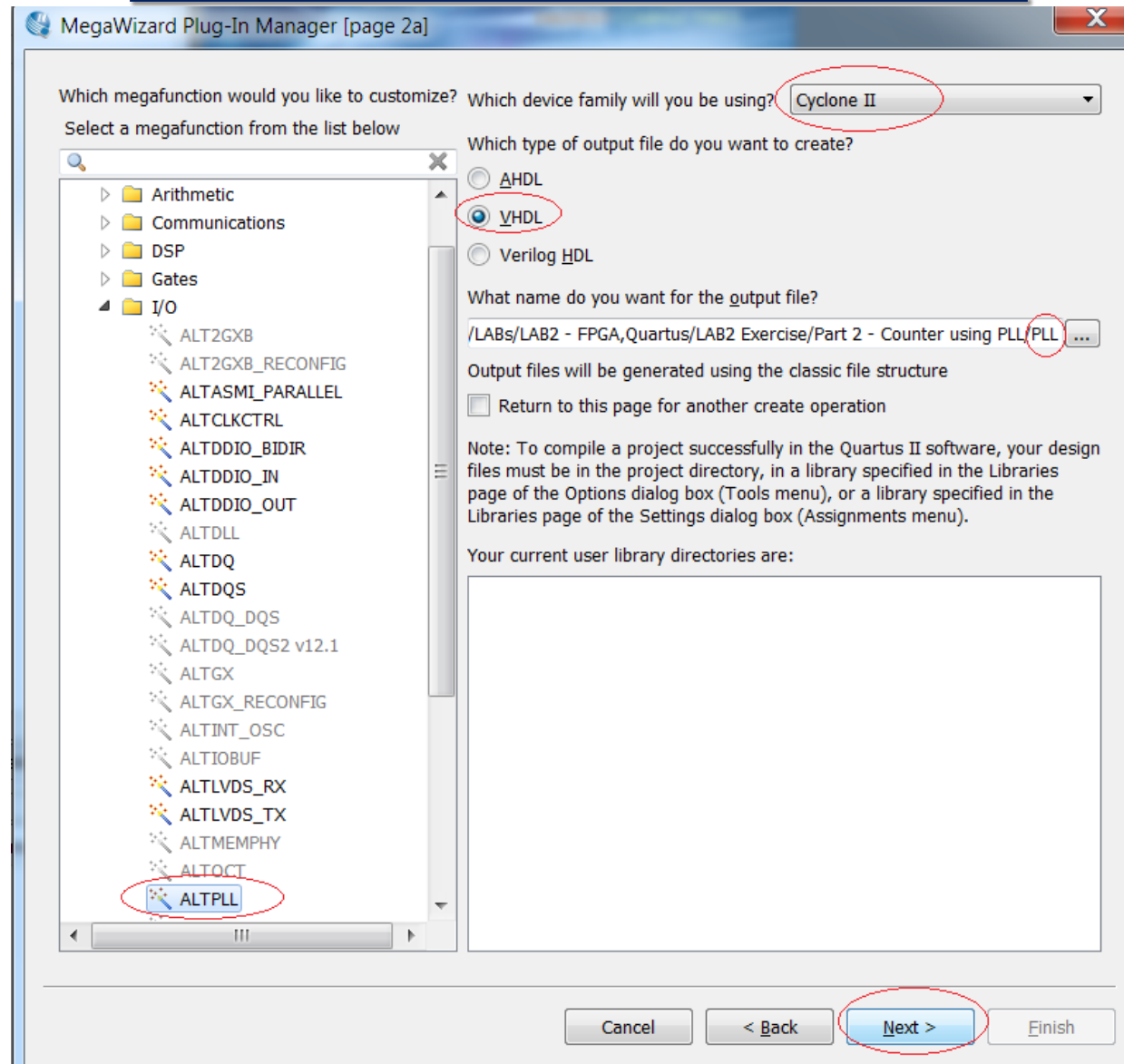
# PLL Wizard – Phase 1



# PLL Wizard – Phase 2



# PLL Wizard – Phase 3





# PLL Wizard – Phase 4

**ALTPLL** [About](#) [Documentation](#)

1 Parameter Settings 2 Output Clocks 3 EDA 4 Summary

General/Modes > Inputs/Lock > Clock switchover >

Currently selected device family: Cyclone II

☒ Match project/default

Able to implement the requested PLL

**General**

Which device speed grade will you be using? 7

☐ Use military temperature range devices only

What is the frequency of the inclk0 input? 50.000 MHz

☐ Set up PLL in LVDS mode Data rate: Not Available Mbps

**PLL Type**

Which PLL type will you be using?

☐ Fast PLL ☐ Enhanced PLL ☒ Select the PLL type automatically

**Operation Mode**

How will the PLL outputs be generated?

☒ Use the feedback path inside the PLL

☒ In normal mode

☐ In source-synchronous compensation Mode

☐ In zero delay buffer mode

☐ Connect the fbmimic port (bidirectional)


☐ With no compensation

☐ Create an 'fbn' input for an external feedback (External Feedback Mode)

Which output clock will be compensated for? c0

Cancel < Back Next > Finish

# PLL Wizard – Phase 5

 **ALTPLL**

AboutDocumentation

1Parameter Settings2Output Clocks3EDA4Summary

General/ModesInputs/LockClock switchover

PLL

inclk0  
areset

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	1/1	0.00	50.00

c0  
locked

Cyclone II

Able to implement the requested PLL

Optional Inputs

- ☐ Create an 'pllana' input to selectively enable the PLL
- ☒ Create an 'areset' input to asynchronously reset the PLL
- ☐ Create an 'pfdena' input to selectively enable the phase/frequency detector

Lock Output

- ☒ Create 'locked' output
- ☐ Enable self-reset on loss lock
- ☐ Hold 'locked' output low for  cycles after the PLL initializes


Advanced Parameters

Using these parameters is recommended for advanced users only

- ☐ Create output file(s) using the 'Advanced' PLL parameters
  - Configurations with output clock(s) that use cascade counters are not supported

Cancel< BackNext >Finish

# PLL Wizard – Phase 6

 **ALTPLL**

AboutDocumentation

1Parameter Settings

2Output Clocks

3EDA

4Summary

General/ModesInputs/LockClock switchover

PLL

inclk0  
areset

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	1/1	0.00	50.00

c0  
locked

Cyclone II

Able to implement the requested PLL

☐ Perform input clock switch when the PLL has lost lock

Clock Switchover

☐ Create an 'inclk1' input for a second input clock  
What is the frequency of the 'inclk1' input?

100.000MHz

☒ Create a 'clkswitch' input to manually select between the input clocks  
(The 'clkswitch' input will behave as an input clock selection control input)

☐ Allow PLL to automatically control the switching between input clocks  
(The 'clkswitch' input will behave as a manual override control input)

Input Clock Switch

☐ Perform input clock switch when the primary clock goes bad

☒ Create a 'clkswitch' input to dynamically control the switching between input clocks

Perform the input clock switchover after

1

input clock cycles

☐ Create an 'activeclock' output to indicate the input clock being used  
(0 inclk0 is being used/ 1 inclk1 is being used)

☐ Create a 'clkloss' output (indicates that input clock switchover is initiated)

☐ Create a 'clkbad' output for each input clock  
(0 input clock is toggling/ 1 input clock is not toggling)

Cancel&lt; BackNext &gt;Finish

# PLL Wizard – Phase 7

MegaWizard Plug-In Manager [page 6 of 10]

**ALTPLL** [About](#) [Documentation](#)

1 Parameter Settings 2 **Output Clocks** 3 EDA 4 Summary

clk c0 > clk c1 > clk c2 >

**PLL**

inclk0  
areset  
c0  
locked

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	3/2	0.00	50.00

Cyclone II

### c0 - Core/External Output Clock

Able to implement the requested PLL

☒ Use this clock

**Clock Tap Settings**

	Requested Settings	Actual Settings
<input type="radio"/> Enter output clock frequency:	100.00000000 MHz	75.000000
<input checked="" type="radio"/> Enter output clock parameters:		
Clock multiplication factor	3	3
Clock division factor	2	2
Clock phase shift	0.00 deg	0.00
Clock duty cycle (%)	50.00	50.00

Note: The displayed internal settings of the PLL is recommended for use by advanced users only


Description	V <sub>t</sub>
Primary clock VCO frequency (MHz)	7..
Modulus for M counter	15

Per Clock Feasibility Indicators

c0 c1 c2

Cancel < Back **Next >** Finish

# PLL Wizard – Phase 8

 **ALTPLL**

AboutDocumentation

1 Parameter Settings2 Output Clocks3 EDA4 Summary

clk c0>clk c1>clk c2>

PLL

inclk0  
areset  
c0  
locked

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	3/2	0.00	50.00

Cyclone II

### c1 - Core/External Output Clock

Able to implement the requested PLL

☐ Use this clock

Clock Tap Settings

	Requested Settings	Actual Settings
<input type="radio"/> Enter output clock frequency:	100.00000000 MHz	Invalid
<input checked="" type="radio"/> Enter output clock parameters:		
Clock multiplication factor	1	Invalid
Clock division factor	1	Invalid
Clock phase shift	0.00 deg	Invalid
Clock duty cycle (%)	50.00	Invalid

Note: The displayed internal settings of the PLL is recommended for use by advanced users only


Description	Value
Primary clock VCO frequency (MHz)	7..
Modulus for M counter	15

Per Clock Feasibility Indicators

c0 c1 c2

Cancel< BackNext >Finish

# PLL Wizard – Phase 9

 **ALTPLL**

[About](#) [Documentation](#)

1 Parameter Settings

2 Output Clocks

3 EDA

4 Summary

clk c0 > clk c1 > **clk c2** >

PLL

inclk0  
areset

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	3/2	0.00	50.00

c0  
locked

Cyclone II

### c2 - Core/External Output Clock

Able to implement the requested PLL

☐ Use this clock

**Clock Tap Settings**

	Requested Settings	Actual Settings
<input type="radio"/> Enter output clock frequency:	100.00000000 MHz	Invalid
<input checked="" type="radio"/> Enter output clock parameters:		
Clock multiplication factor	1	Invalid
Clock division factor	1	Invalid
Clock phase shift	0.00 deg	Invalid
Clock duty cycle (%)	50.00	Invalid

Note: The displayed internal settings of the PLL is recommended for use by advanced users only


Description	V <sub>c</sub>
Primary clock VCO frequency (MHz)	7..
Modulus for M counter	15

Per Clock Feasibility Indicators

**c0** c1 c2

Cancel < Back **Next >** Finish

# PLL Wizard – Phase 10

 **ALTPLL**

AboutDocumentation

1 Parameter Settings2 Output Clocks3 EDA4 Summary

PLL

inclk0  
areset

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	3/2	0.00	50.00

c0  
locked

Cyclone II

Simulation Libraries

To properly simulate the generated design files, the following simulation model file(s) are needed

File	Description
altera_mf	Altera megafunction simulation library

Timing and resource estimation

Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party EDA synthesis tool, using a timing and resource estimation netlist can allow for better design optimization.


Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.

Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.

☐ Generate netlist

Cancel< BackNext >Finish

# PLL Wizard – Phase 11

 **ALTPLL**

AboutDocumentation

1 Parameter Settings2 Output Clocks3 EDA4 Summary

PLL

inclk0  
areset

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	3/2	0.00	50.00

c0  
locked

Cyclone II

Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:  
C:\Users\Han\Desktop\Part 1 - Counter\

File	Description
<input checked="" type="checkbox"/> PLL.vhd	Variation file
<input checked="" type="checkbox"/> PLL.ppf	PinPlanner ports PPF file
<input type="checkbox"/> PLL.inc	AHDL Include file
<input checked="" type="checkbox"/> PLL.cmp	VHDL component declaration file
<input checked="" type="checkbox"/> PLL.bsf	Quartus II symbol file
<input type="checkbox"/> PLL_inst.vhd	Instantiation template file

Cancel< BackNext >Finish