

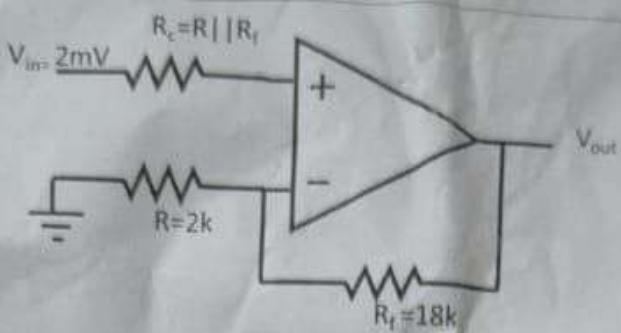
National Institute of Technology Patna
Mid-Semester Examination - March 2025

Course Title: Linear Integrated Circuits
Full Marks: 30

Course Code: EC45113
Time: 2 Hours

Instructions: (i) Attempt all questions. (ii) Consider missing data appropriately.

			CO	Bloom's Taxonomy
Q1	Explain the BJT current mirror circuit and find the expression of output current I_{out} in terms of I_{in} for Q2, which is m times larger than Q1.		CO-1	L1, L2, L3
Q2	(i) Compare the characteristics of an ideal op-amp and a practical op-amp. (ii) Calculate V_o and I_o for the given ideal op-amp.	[5]	CO-1	L1, L2
Q3	Derive the expression for the closed loop gain of a non-inverting op-amp with finite open loop gain A.	[5]	CO-1	L1, L2
Q4	What is the total output voltage of a given circuit if the input offset voltage is 0.1mV, input offset current = 5nA, and input bias current = 50nA?	[5]	CO-1	L2, L3



Q5 Explain the Schmitt trigger circuit using an op-amp. Draw the output waveform and find its duty cycle.

OR

Draw the circuit, drive the transfer function of a first-order low-pass Butterworth filter, and explain its frequency response.

CO-1,
CO-2

L3, L4

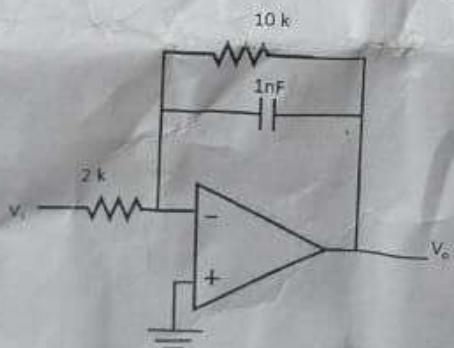
Q6 Draw the circuit diagram and output waveform for the op-amp-based positive-biased clipper circuit.

OR

Find the nature of the filter and cut-off frequency for the configuration shown in Figure.

CO-1,
CO-2

L2, L3, L4



(5)

NATIONAL INSTITUTE OF TECHNOLOGY PATNA
 Department of Electronics and Communication Engineering
MID SEMESTER EXAMINATION, Jan-May 2025

B.Tech: Semester-IV

Course Name: Digital IC Design

Maximum Time: 2 hours

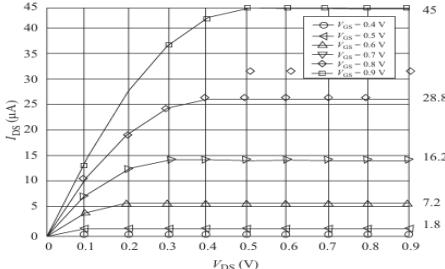
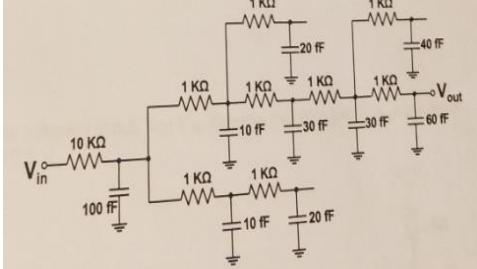
Branch: ECE

Course Code: EC45131

Max. Marks: 30

Instruction:

1. Attempt all questions. Write only what is asked, and keep your answers to the point.
2. The Marks, CO (Course Outcome) and BL (Bloom's Level) related to questions are mentioned on the right-hand side margin.
3. Attempt any two options from each question.

		Marks	CO	BL
Q1. (a)	Write the (i) steps of p-well CMOS fabrication process, (ii) design abstraction levels in digital circuits in brief and (iii) why slope is -1 for defining V_{IL} and V_{IH} in CMOS VTC.	(2+2+1)		R
(b)	The following I-V characteristics of an n-channel MOSFET is shown in Fig. 1(a). (i) What are the values of β_n and V_{t0} ? (ii) If $V_{GS} = 0.65$ V, what is the value of I_{DS} in the saturation region? (iii) What is the minimum value of V_{DS} for operating in the saturation region if $V_{GS} = 0.75$ V?	(3+1+1)	CO1	C
	 (a)  (b)			
	Fig. 1			
(c)	Explain the layout design rule with its need and draw stick diagram of 3 input CMOS NOR gate.	(3+2)		U
(d)	Draw RC equivalent model of NMOS & PMOS transistor. Compute the propagation delay of interconnect network used in VLSI chip from V_{in} to V_{out} using Elmore delay. [See Fig. 1(b)]	(1+4)		P
Q2. (a)	Calculate the critical voltages and noise margin for a CMOS inverter, if $V_{DD} = 3.3$ V, $V_{tn} = 0.3$ V, $V_{tp} = -0.3$ V, $\beta_n = 60 \mu\text{A/V}^2$, and $\beta_p = 20 \mu\text{A/V}^2$. Also calculate the power dissipation for a load of 0.1 pF and frequency of 100 MHz.	(4+1)		R. E
(b)	Explain the transient analysis of a CMOS inverter and calculate propagation delay assuming $V_{DD}=5$ V? Justify use of inverter in digital IC design with explanation of reference inverter.	(2+2+1)	CO2	R, U
(c)	Consider a CMOS inverter with the following parameters: nMOS $V_{Tn} = 0.6$ V pMOS $V_{Tp} = -0.7$ V $\mu_n C_{ox} = 60 \mu\text{A/V}^2$ $\mu_p C_{ox} = 25 \mu\text{A/V}^2$ $(W/L)_n = 8$ $(W/L)_p = 12$ Calculate the noise margins and the switching threshold (V_{th}) of this circuit. The power supply voltage is $V_{DD} = 3.3$ V.	5		R. E
(d)	Design of a CMOS inverter circuit: Use the same device parameters as in Problem Q 2. (c). The power supply voltage is $V_{DD} = 3.3$ V. The channel length of both transistors is $L_n = L_p = 0.8 \mu\text{m}$. (inga) Determine the (W_n/W_p) ratio so that the switching (inversion) threshold voltage of the circuit is $V_{th} = 1.4$ V. (ii) Plot VTC.	5		R. E

Q3. (a)	(i) Determine the transistor sizing ratio for a CMOS 4 to 1 Multiplexer given that pull up network have a width-to-length ratio $(W/L)_{\text{pull-up}} = 15$ and pull-down network have $(W/L)_{\text{pull-down}} = 10$. Assume a 180 nm CMOS baseline process technology from SCL Chandigarh. Also, compute input & output capacitance of same CMOS 4 to 1 Multiplexer assuming diffusion capacitance is C and equal pull up to pull down ratio. (ii) Design an FO4 Inverter to Drive Four Inverters Following the Principles of a Digital IC Designer.	(4+1)	CO ₃	E
(b)	(i) Design half adder using pass transistor logic and CMOS transmission gate (ii) compute propagation, contamination delay, parasitic delay & logical effort of 3-input NAND gate.	(2+3)		U
(c)	Discuss the issue of Dynamic logic and their solutions in detail.	5		R
(d)	Draw the corresponding circuit diagram for the function (i) $Y = \overline{A(D+E)} + BC$ and find an equivalent CMOS inverter circuit, (W/L) for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all PMOS transistors and $(W/L)_n = 10$ for all nMOS transistors. (ii) Implement the logic function using CMOS logic $f(x_1, x_2, x_3, x_4) = \Sigma m(0, 1, 2, 4, 6, 8, 10, 12, 14)$	(3+2)		P

★★★All the Best ★★★

राष्ट्रीय प्रौद्योगिकी संस्थान पटना / NATIONAL INSTITUTE OF TECHNOLOGY PATNA

Mid-Semester Examination-March-2025

Course Title: Electromagnetic Field Theory
Maximum Marks: 30
Semester: IV

Course Code: EC45101
Time: 2 hours
Section: A & B

Instructions: (i) All questions are compulsory (ii) Consider missing data appropriately.

- Starting from Ampere's Circuit Law deduce corresponding Maxwell Equation. Why did Maxwell introduce the concept of displacement current? [6 Marks]
- (i) Express the vector field $\vec{H} = xy^2z\hat{a}_x + x^2yz\hat{a}_y + xyz^2\hat{a}_z$ in cylindrical and spherical coordinates.
(ii) A circular disc of radius 'a' carries charge $\rho \text{ c/m}^2$ lying in xy plane. Find electric field at $(0, 0, h)$. [6 marks]
- Two extensive homogeneous isotropic dielectrics meet on plane $z=0$. For $z \geq 0$, $\epsilon_{r1} = 4$ and for $z \leq 0$, $\epsilon_{r2} = 3$. A uniform electric field $\vec{E}_1 = 5\hat{a}_x - 2\hat{a}_y + 3\hat{a}_z \text{ kV/m}$ exist for $z \geq 0$. Find
(i) \vec{E}_2 for $z \leq 0$.
(ii) The angles E_1 and E_2 make with the interface
(iii) The energy densities in J/m^3 in both dielectrics
(iv) The energy within a cube of side 2m centered at $(3, 4, -5)$ [6 marks]
- Conducting spherical shells with radii $a = 10 \text{ cm}$ and $b = 30 \text{ cm}$ are maintained at a potential difference of 100 V such that $V(r = b) = 0$ and $V(r = a) = 100 \text{ V}$. Determine V and \vec{E} in the region between the shells. If $\epsilon_r = 2.5$ in the region, determine the total charge induced on the shells and the capacitance of the capacitor. [6 marks]
- State and prove the Uniqueness Theorem. [6 marks]

$$C = \frac{4\pi \epsilon_0 \epsilon_r}{\frac{1}{a} - \frac{1}{b}}$$

$$4\pi \cdot 67 \mu C$$

$$Q = \frac{4\pi \epsilon_0 \epsilon_r}{\frac{1}{a} - \frac{1}{b}} \cdot V$$

$$Q = \int \rho dV$$

$$C = \frac{Q}{V}$$

PF 21



NIT Patna, ECE Department

Subject: Wireless Sensor Network (EC45121)

Course: B. Tech (ECE), Semester: 4th, Time: 2.00, Hours, MM: 30

Assume missing data, if any and mention it in the answer copy

	PART-A	Marks	CO
Q1)	1) A sensor network in WSN can be of _____ topology. e) Star f) Multi-hop wireless mesh g) Advanced multi-hop wireless mesh h) All the above	1	1,3
	2) The propagation technique in WSN between hops of network can be _____. b) Routing b) Flooding c) Connecting d) Both a and b	1	3,4
	3) Name the type of Mobility-		
	4) IEEE 802.11 defines basic service set as building block of a wireless _____. b) LAN b) WAN c) MAN d) ALOHA	1 1	1,2,3 1,2,3
	5) Write the full form of following- c) CSMA-CA d) LEACH	1	5

PTO

	PART B: Short Answer, answer any three.		
Q2	<p>a) What do you mean by Localization scheme? Mention the name of its type.</p> <p>b) Define optimization goals of WSN. Discuss the network life time as performance matrix.</p> <p>c) Explain about the count to infinity problem and explain one method to resolve it.</p> <p>d) What do you mean by the service interface? How does it helpful in establishing a WSN?</p> <p>e) What are the antenna requirements for the different types of cluster grids in WSN?</p> <p>f) Write the differences between AODV and AOMDV protocols.</p>	3	3
		3	2
		3	2, 3
		3	1, 2
		3	2, 3
		3	1, 3
	PART C: Attempt any 04 (Four) questions from Q3 to Q8		
Q3	Define Sensor node and explain in brief the component of its block diagram?	4	1,2
Q4	What do you mean by Hidden node and exposed node Problem? Explain one way to resolve it	4	5
Q5	Define the Protocol stack for sensor networks and explain in brief about each layers.	4	1,2,4
Q6	Explain about the WSN Network Architecture. Define the single and multi-hop WSN.	4	1, 4
Q7	What do you mean by the triangulation and trilateration? Explain the different methods for triangulations considering two and three anchor nodes.	4	2, 3
Q8	Consider, there are three anchors on their positions (x_1, y_1) , (x_2, y_2) and (x_3, y_3) with the distances between the anchors and node of the unknown position, r_1, r_2 and r_3 . Find the position of an unknown node.	4	3, 4

NATIONAL INSTITUTE OF TECHNOLOGY PATNA

Department of Computer Science and Engineering

Mid Semester Examination, January-June 2025

Program & Dept.: B.Tech-M.Tech-DD-ECE

Course Name: Object Oriented Programming

Maximum Time: 2 hours

Semester- 4th

Course Code: CS45101

Max. Marks: 30

Instructions:

1. Attempt all questions. Write a concise and precise answer.
2. Assume any suitable data, if necessary.
3. The marks, Course Outcome (CO), and Bloom's Level (BL) related to questions are mentioned at the end of each question.

Questions

1	a) How does Object-Oriented Programming (OOP) improve code re-usability and maintainability compared to Procedural-Oriented Programming? Provide examples. [4 M][CO1][BL1,BL3]
	b) Explain the Java memory structure and describe the roles of the Heap, Stack and Method Area in memory management. [3 M][CO1][BL1,BL2]
	c) JRE (Java Runtime Environment) and JDK (Java Development Kit) both include the JVM. Why is the JDK necessary for Java development if the JRE can run Java applications? [3 M][CO1][BL4,BL5]
2	What will be the output of the following code snippet/program? Provide a step-by-step explanation of how the output is derived. [2 × 5 = 10] [CO2][BL4]
	a) int[][] m = {{1,1,1,1},{1,2,3,4},{2,2,2,2},{2,4,6,8}}; int sum = 0; for (int k = 0; k < m.length; k++) { sum = sum + m[m.length-1-k][1]; } System.out.print(sum);
	d). class Test { static int x = 10; int y; public static void main(String[] args){ Test obj1 = new Test(); Test obj2 = new Test(); obj1.x = 30; obj1.y = 40; System.out.println(obj2.x + " " + obj2.y); }
	b). System.out.println(-10 >> 2);
	c). public class Test { public static void main(String[] args) { Double a = 10.5; Double b = 10.5; System.out.println(a == b); }}
	e). public class Test { public static void main(String[] args) { String s = "Java"; s.concat("Programming"); System.out.println(s); }}
3	a). Write a Java program to manage seat bookings in a movie theater. Each row has a different number of seats. Allow users to book a seat by entering the row and seat number, then display the seating arrangement before and after booking. [4M][CO3][BL2,BL5]
	b). Write a Java program to track the number of objects created for a class and display the total count. [2M][CO2][BL4,BL5]
	c). Write a Java program to check whether a given string is a palindrome. Ignore spaces and case sensitivity while making the comparison. [4M][CO2][BL2,BL4]



National Institute of Technology Patna
Department of Electronics and Communication Engineering
Subject Code: EC45102 (Microprocessor and Microcontrollers)

MID-SEM EXAMINATION

DOE: 11 /03 /2025 (FN)

MM: 30M

Time: 2 H

B.Tech: 4th SEM (ECE-1&2/DD-EC-MV/ME)

[30 Marks]

Note: Answer all questions.

1. (a) Write down the main differences between Von Neumann and Harvard architecture.
[CO-1] [2M]

(b) Define PSW. And, explain PSW in 8086 microprocessors. [CO-1] [3M]

(c) Explain the CWR format of 8255 in I/O and BSR mode. [CO-2, CO-3] [3M]

or

Explain the physical memory organization of 8086 microprocessor with the help of a suitable diagram. [CO-1, CO-2] [3M]

(d) Identify the given instruction as 'true' or 'false'. If 'true,' mention the associated addressing mode, and if 'false,' write down the appropriate justification. [CO-1, CO-2] [2 M]

XCHG [3000H], [5000H]

INC [AX]

ADD [3000H], 5000H

MOV DS, [5000H]

(AX)

2. (a) Explain the function of the following signals of 8086. [CO-1] [3M]

(i) ALE (ii) DT/R (iii) READY (iv) LOCK (v) BHE (vi) S0', S1', S2'

(b) Draw and describe the architecture of 8086 microprocessors and explain the concept of pipelining using a suitable example or diagram. [CO-2] [4M]

(c) Add the content of the memory location 2000H: 0500H to contents of 3000H: 0600H and store the result in 5000H: 0700H. [CO-3] [3M]

3. (a) Draw and explain the timing diagram for a read operation in minimum mode of 8086.
[CO-1, CO-2] [5M]

(b) What is a Maximum Mode system? Draw and design an 8086-based max mode system. Also, select suitable mapping. The system has 32KB EPROM using 16KB chips and 128 KB RAM using 32KB chips. [CO-1, CO-2, CO-4] [5M]

Regd

16

24 x 27 = 16

National Institute of Technology Patna
 Department of Electronics and Communication Engineering
 Mid-Semester Examination – Jan-Jun 2025

Course: B.Tech.
 Code: EC45103

Semester: IV
 Subject: Digital Signal Processing

Time: 02 Hours
 Full Marks: 30

Attempt all questions. Assume the missing data if any.

Q.1 Answer the following questions

[8×1.5]

- Compute 4-point DFT of the sequence $x(n) = \frac{\sin \pi n}{2}$ for $0 \leq n \leq 3$.
- Let $X(k)$ be the DFT of the sequence $x(n) = \{1, 2, 1, 1, 2, -1\}$. Find the sequence $y(n)$ whose DFT is given by $Y(k) = e^{-j\pi k} X(k)$ using relevant properties of DFT.
- The first five points of 8-point DFT of a real valued sequence are $\{28, -4 + j9.565, -4 + j4, -4 + j1.656, -4\}$. Determine the remaining three points.
- Let $x(n) = \{1, 2, 0, 3\}$. Find Circular shifted signal $x_2(n) = x((n+2)_4)$.
- Why a zero-phase filter cannot be realized for real-time applications? Explain.
- Between the Goertzel algorithm and FFT, which algorithm is computationally more efficient? Give justification.
- The transfer function of a system is given by $H(z) = \frac{(1-\frac{z}{2})(z-\frac{1}{4})}{(z-\frac{1}{3})(z-\frac{1}{5})}$. Is it a linear phase system? Is it a minimum-phase system?
- Let input $x(n)$ and output $y(n)$ of a filter is related by the difference equation $y(n) = x(n) - x(n-5)$. Identify the type of the filter. Plot its magnitude response.

13x2

- Q.2** Two finite duration sequences are given by: $h(n) = \{1, 0, 1\}$ and $x(n) = \{-1, 2, -1, 0, 1, 3, -2, 1, -3, -2, -1, 0, -2\}$. Use Overlap-add method to find $y(n) = h(n) * x(n)$. Take the length of each section as 4. ~~+3+5+15~~ [3]

- Q.3** The impulse response of a digital system is given by $h(n) = \frac{1}{2}[\delta(n) - \delta(n-1)]$. Find the frequency and phase response of the system, and draw the pole and zero plot. Identify the filter type. Convert this filter to a comb filter of order 5. [4]

- Q.4** A digital notch/band-stop filter is required to remove an undesirable hum with frequency $f_0 = 60$ Hz associated with a power supply in an ECG recording application. Assume the sampling frequency of ECG signal is $f_s = 500$ sample/sec. Design a second order IIR notch filter to remove the hum. [4]

- Q.5** Compute the 4-point DFT of the following sequence, $x(n) = (-1)^n$ using DIT-FFT algorithm. Draw the butterfly diagram. [4]

- Q.6** The channel transfer function of a communication channel is given by,

$H(z) = \frac{(1+0.2z^{-1})(1-9z^{-2})}{(1+0.81z^{-2})}$. Obtain a stable equalizer that will compensate the distortion introduced by the channel on the transmitted signal. *Clue: Equalizer is the inverse channel.* [3]

$A(z)$

minm

$12 + 1 \times 8 \times 3$
 10×4

$-1 + (-3)$
 $-1 - (-3)$