RFPA5542 WLAN POWER AMPLIFIER

5 GHz WLAN PA (11a/n/ac)

Introduction

This application note explains the operation of the RFPA5542 5GHz WLAN PA. The RFPA5542 is a three-stage power amplifier (PA) designed for Wi-Fi 802.11a/n/ac systems. It provides <1.8% EVM dynamic, EVM at +23 dBm output power using MCS9 VHT80 (11ac) waveform while drawing 285 mA from a +5 V DC supply. This PA is a 50-ohm part and is housed in a 4.0 x 4.0 mm QFN package.

For more detailed information, please refer to the RFPA5542 datasheet.

Product Details

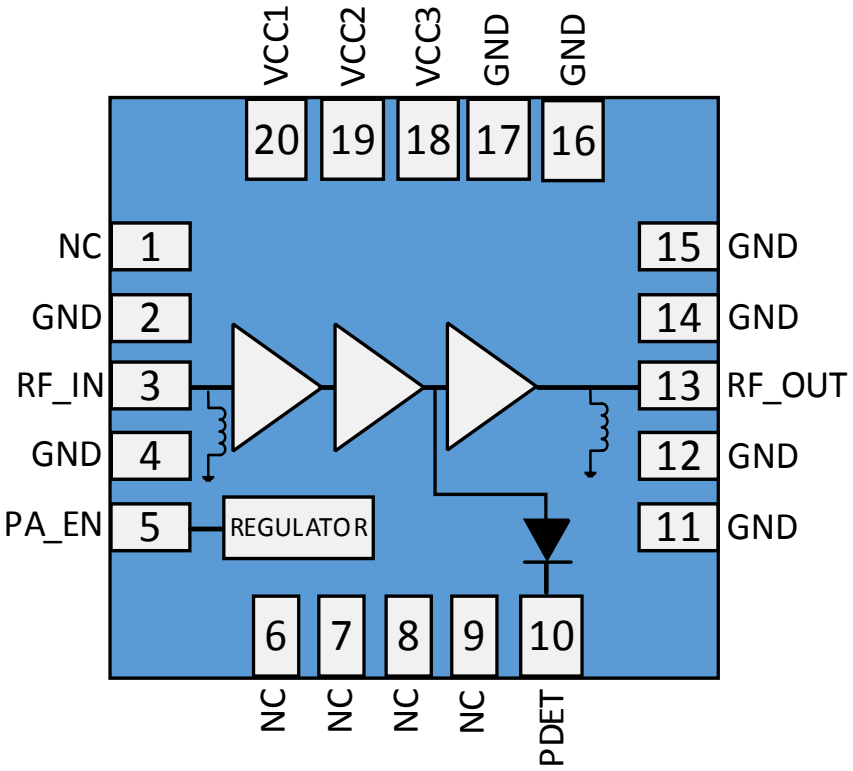


Figure 1. Functional Block Diagram & Pin-out Detail

Table 1. RFPA5542 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1, 6, 7, 8, 9	NC	Not connected internally. It may be left floating or connected to ground.
2, 4,11, 12, 14, 15, 16, 17	GND	Ground connection.
3	RF_IN	RF input, internally matched to 50Ω and DC shorted. External DC blocking capacitor required.
5	PA_EN	Input enable bias voltage — regulated internally.
10	PDET	Power detector. Provides an output voltage proportional to the RF output power level.
13	RF_OUT	RF output, internally matched to 50Ω and DC shorted. External DC blocking capacitor required.
18	VCC3	3rd stage supply voltage.
19	VCC2	2nd stage supply voltage.
20	VCC1	1st stage supply voltage.
GND Paddle	GND	RF/DC Ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB mounting pattern for suggested footprint.

Evaluation Board Information

The Qorvo RFPA5542 Evaluation Board (EVB) is designed to provide performance representative of that obtainable in an actual application. The EVB is designed to operate with 50 Ω load impedances at all RF ports, which are provided with SMA connector interfaces. No tuning is applied between the module RF pins and the EVB SMA connectors.

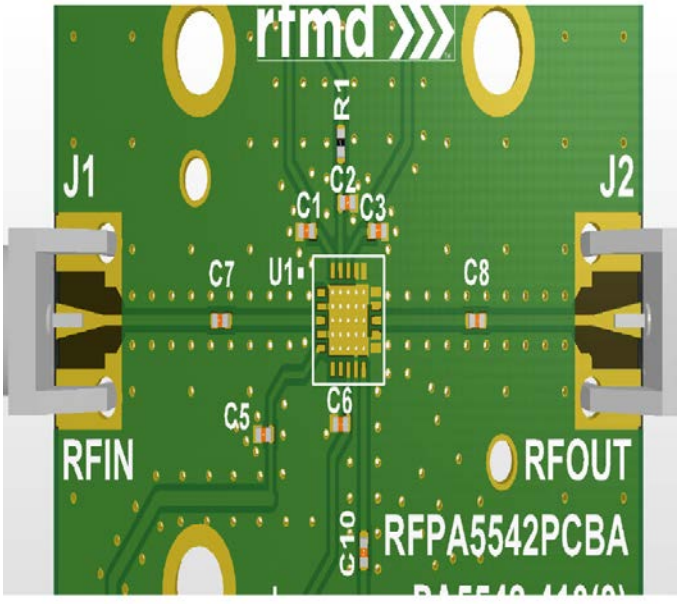


Figure 2a. RFPA5542 Evaluation Board Photo.

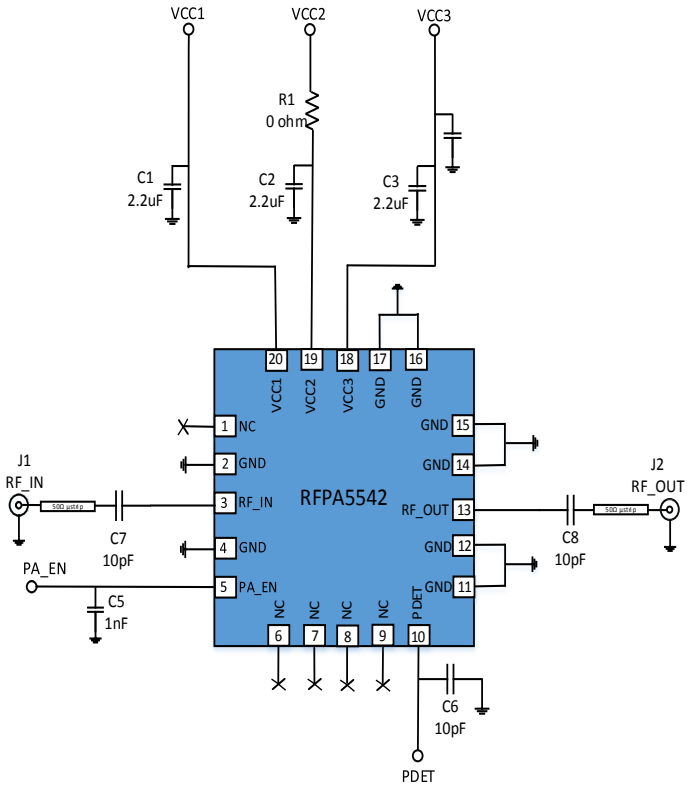


Figure 2b. RFPA5542 -EVB Schematic

Please Note:
All SMDs are 0402 size unless stated otherwise on the schematic.

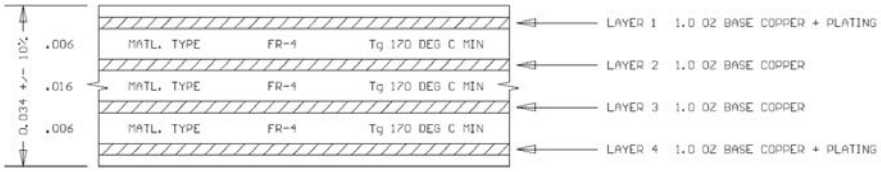


Figure 2c. RFPA5542 -PCB Stack-up

Recommended Biasing Sequence

Table 2 below provides the logic truth table for the RFPA5542.

OPERATING MODE	PA_EN
TX ON	HI
TX OFF	LO

Table 2. RFPA5542 Logic Truth Table.

The correct timing of the RFPA5542 logic control and RF input is required to ensure optimal performance and reliable operation. Below is turn on/off procedure.

Transmit Power-On Procedure:

1) Connect Power Supplies in OFF mode (0 V) to VCC and PA_EN pins.
2) Apply +5.0 V to VCC pins.
3) Apply control voltages. (+3.0 V to PA_EN)
4) Apply RF input signal to J1 (RF_IN pin 3); measure RF output on J2 (RF_OUT pin 13)
5) Power detector output voltage can be monitored on PDET, pin 10

Transmit Power-Off Procedure:

1) Remove RF input signal.
2) Set PA_EN to 0 V.
3) Set the Power Supply Voltages on VCC to 0 V.

Transmit Timing Diagram
Power ON / OFF Sequence

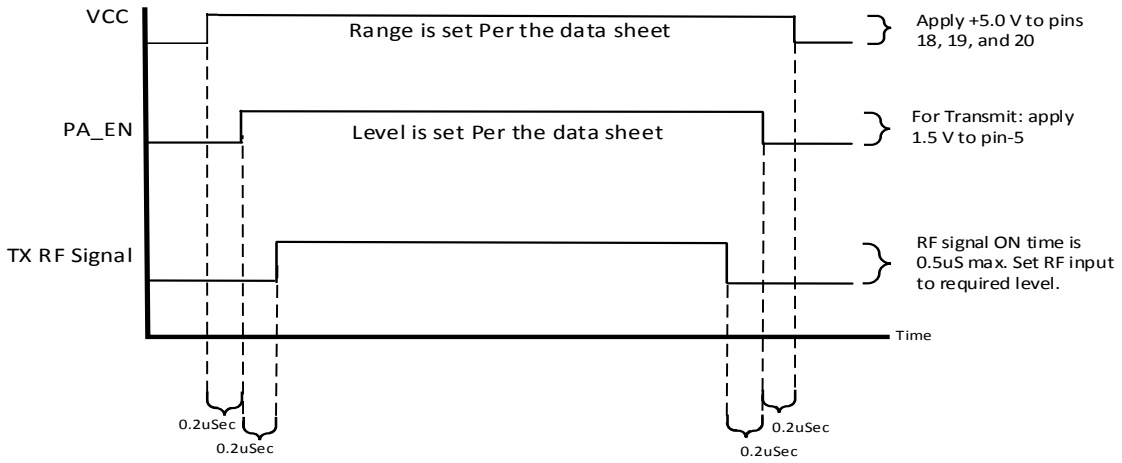


Figure 3. RFPA5542 Timing Diagram.

Notes:

1. RF Signal for each specific mode is applied after the DC bias is applied
2: Total ON/OFF time includes from 10% of control switching to 90% of RF power
3: Listed values on diagram are typical. The maximum is 0.5us for each mode

System Architecture Application Circuit Recommendations

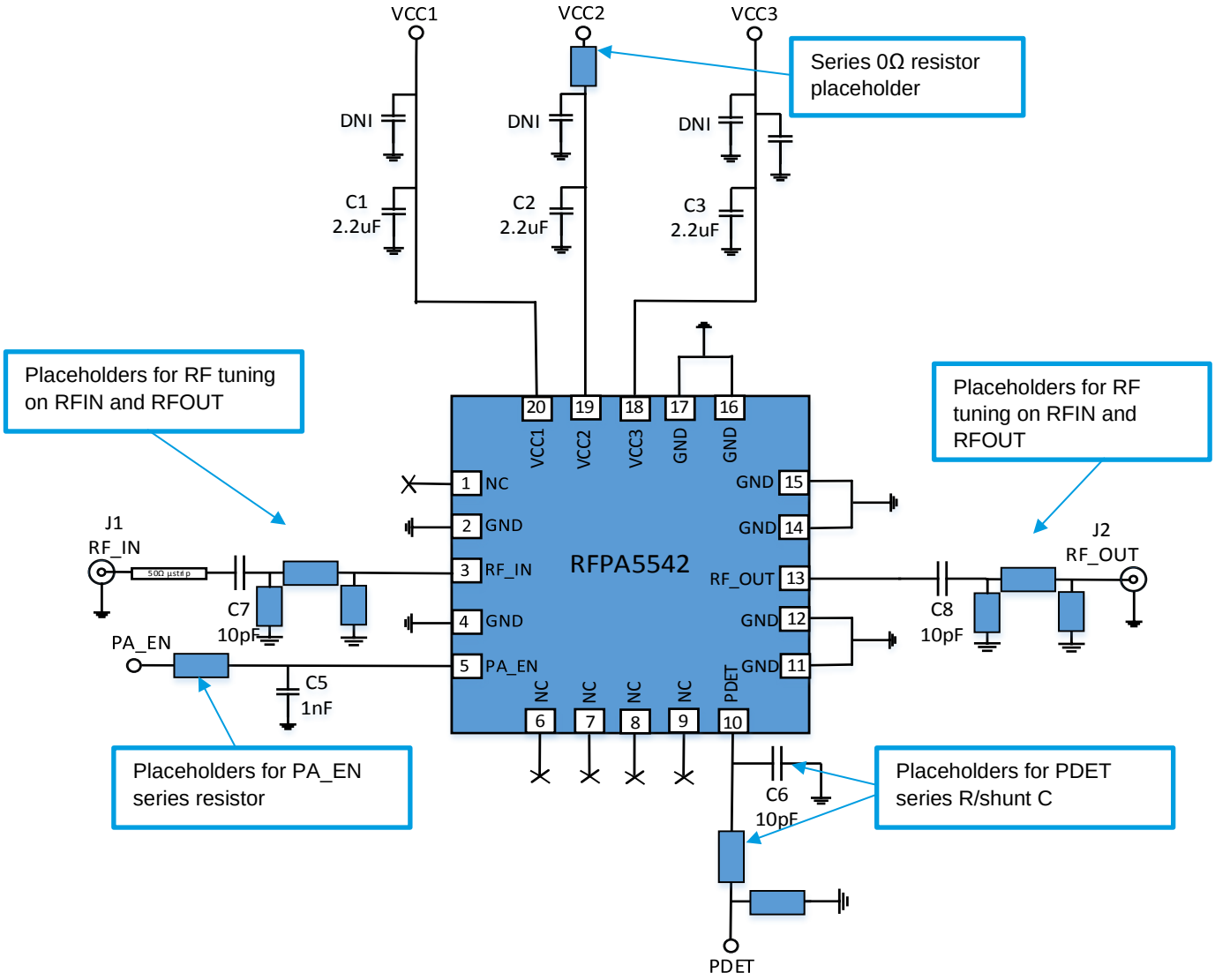


Figure 4. Recommended Application Circuit in a System.

1. The above schematic shows recommended bypassing values based on RFPA5542 -EVB. Customer should ensure that sufficient bypassing is provided based on their PCB layout. In addition, all bypass capacitors should be placed as close as possible to respective FEM pins, with the lowest values placed closest to the part pin. It is also recommended that at least one ground via be placed right next to each bypass capacitor ground pad to minimize ground return inductance between the capacitor and the FEM ground.

2. In case there is DC present on the lines connecting RF paths on the board, we recommend using DC block per the recommended values in the schematic. There is no DC present on RF ports of FEM internally. Low value external DC blocking capacitors, however, can be beneficial for improving ESD immunity and overall ruggedness in the presence of transients. The capacitor values should be chosen to be series resonant at approximately mid band. 100 pF is a good choice, assuming the use of standard 0402 or 0201 SMD capacitors.

3. PDET (pin 10) should not be left floating and should be terminated with 10 pF or 100pF capacitor if this pin is not being used.

4. Suggest having a series element to customer layout at the output of PDET (pin 10) to have the flexibility of a series R/shunt C, if required. R1 can be replaced as 0 Ohm. Since output of detector goes into ADC that acts as high impedance, therefore, external shunt R2 may not be needed for pin 10.

5. Recommend using a "pi" placeholder for tuning flexibility at RFIN and RFOUT ports. In addition, tuning placeholders are recommended close to FEM. TCVR matching components should be placed closer to TCVR with 50 Ohm trace connecting to "pi" placeholder near the FEM Input.

6. NC is no connect and can be left floating or grounded on the board. Grounding this pin can add better mounting integrity. If grounding, we suggest to GND it close to FEM pin.

7. Route control lines on separate layer, other than the signal layer, whenever possible and isolate control line traces from RF and VCC traces.

8. It is recommended to fully populate the ground slug with as many thermal vias as possible and to add ground vias around RF traces. We recommend following Qorvo evaluation board layout guidelines as close as possible. RFPA5542 evaluation board uses 12 mil vias and 22 mil pads. Gerber files are available upon request.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any FEM, including the RFPA5542. In addition to providing connectivity between the FEM and external components, the PCB layout is a part of the overall circuit. The RF and DC parasitic of the traces, along with coupling between traces, must be evaluated. The RFPA5542 Evaluation Board PCB layout guidelines provides a good starting point for designing the layout in the actual application.

RF Traces

All PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on top layer to minimize coupling with other RF, control input, and DC traces. If it is not possible for some reasons to route RF traces on top layer, we suggest to make sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals by adding solid ground planes (with vias) between them to minimize coupling and cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

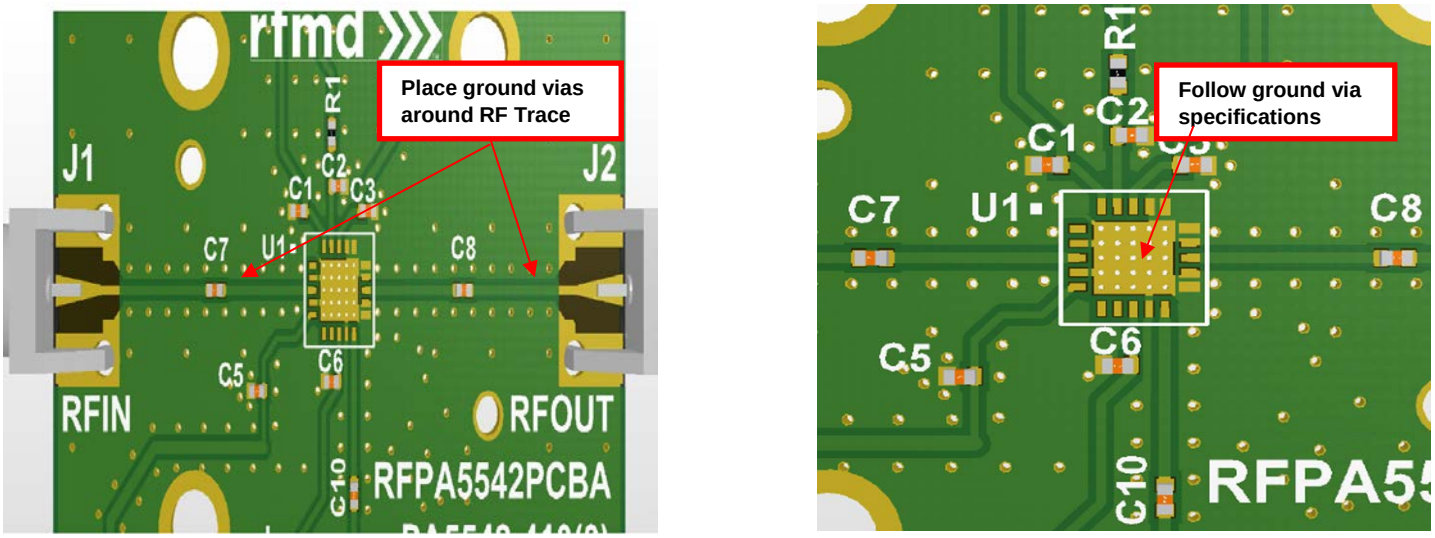


Figure 5a. Example Recommended PCB layout Considerations.

Grounding Considerations

Connect module center ground pad directly to main ground plane layer using as many vias as possible. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Close attention should be paid to the grounding of the PA ground slug, the solid metalized area on the bottom side of the package. This serves as the primary RF and DC ground return for the entire PA, as well as the primary path for heat removal. A larger number of via holes should be distributed over the entire ground area below the PA to provide good RF and DC ground returns, as shown in **Figure 5b** below.

Additionally, the vias will serve as a low resistance thermal path between the PA and the PCB. Vias passing through multiple copper layers provide the best overall RF, DC, and thermal performance. Ensure proper vias on ground slug / paddle for better thermal consideration. RFPA5542 ground slug / paddle has special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo evaluation board should be replicated. The Qorvo layout files in Gerber format can be provided upon request.

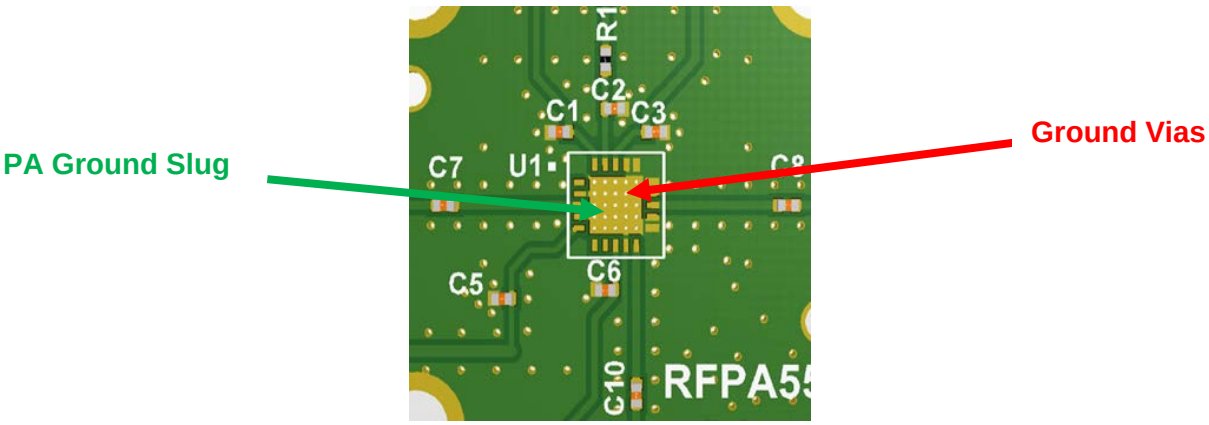


Figure 5b. Example Recommended Ground Via Placement on Module Ground Slug.

DC Layout Considerations

The most important layout consideration for the VCC DC traces is that they provide low impedances back to their main supply rail. Where possible, power planes should be used to route these traces. Where this is not possible due to space constraints, the traces should be made as wide as possible, using multiple copper layers if necessary to achieve an equivalent width of 2 mm or more. There should be at least one ground layer between these traces and any RF traces even though both are running diagonal to each other on different layers to minimize coupling. When connecting all VCC pins on the board together, we recommend connecting VCC pins (pin 18, 19 and 20) before bypass capacitors as shown in figure 5c. In addition, we suggest running a longer trace for better isolation.

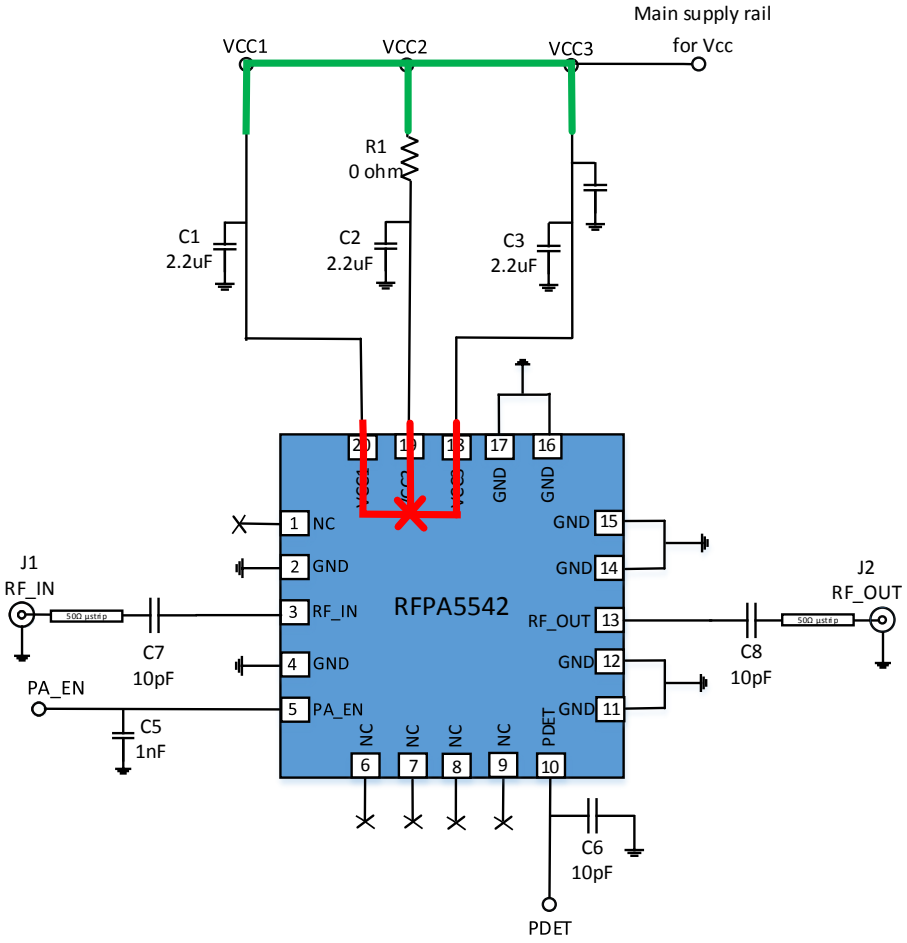


Figure 5c. Recommended Configuration While connecting VDD and VCC pins

PCB Footprint Recommendations

See **Figures 6a and 6b** below for the recommended package outline drawing and solder mask patterns.

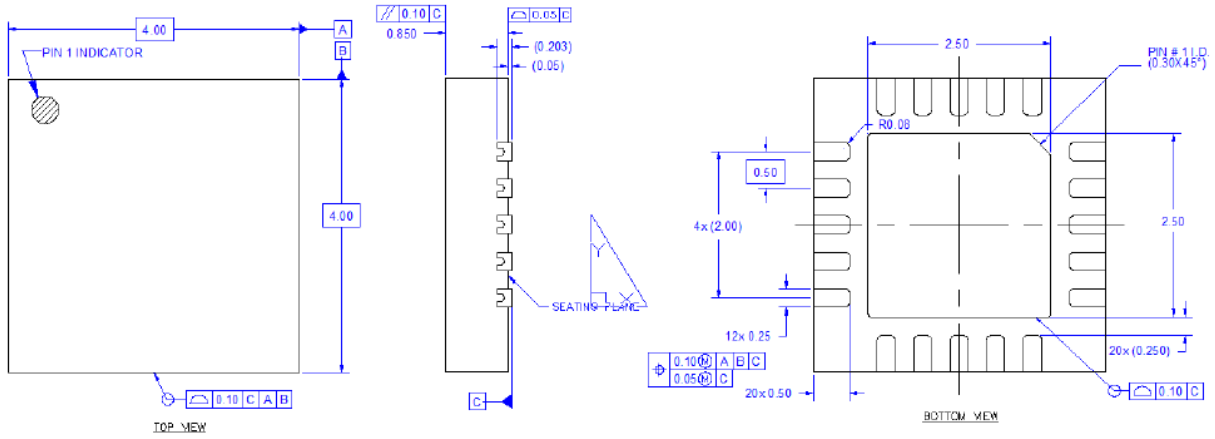


Figure 6a. RFPA5542 Package Outline Drawing.

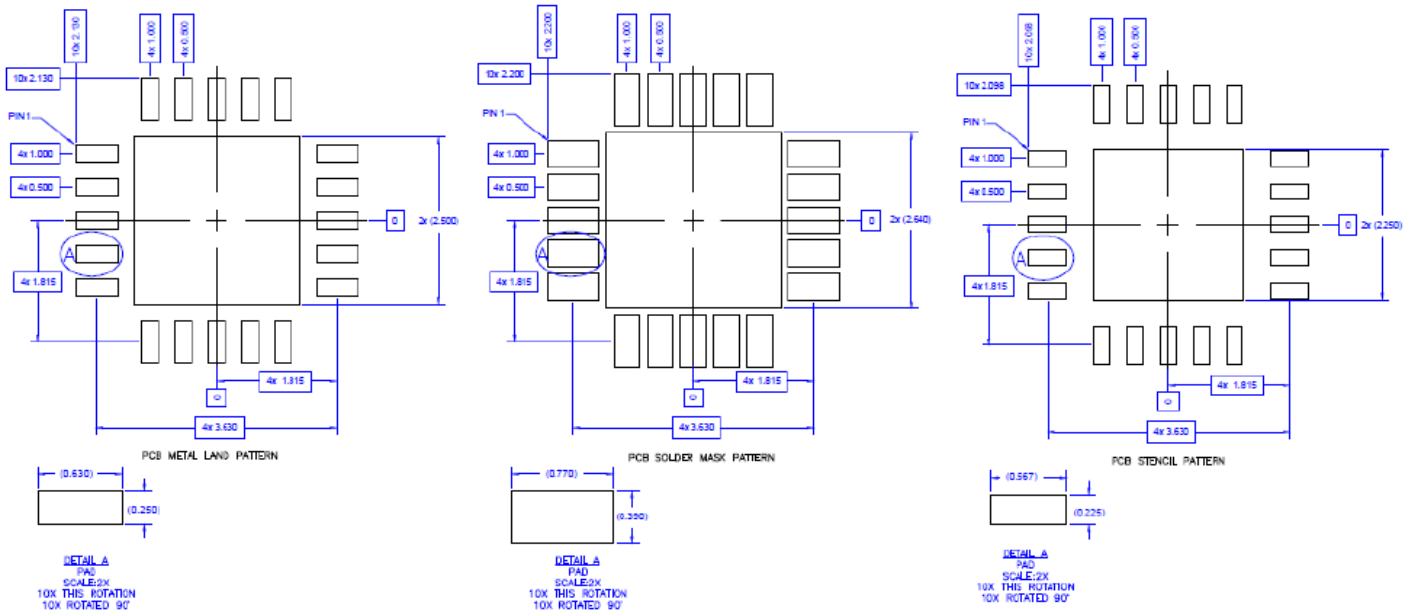
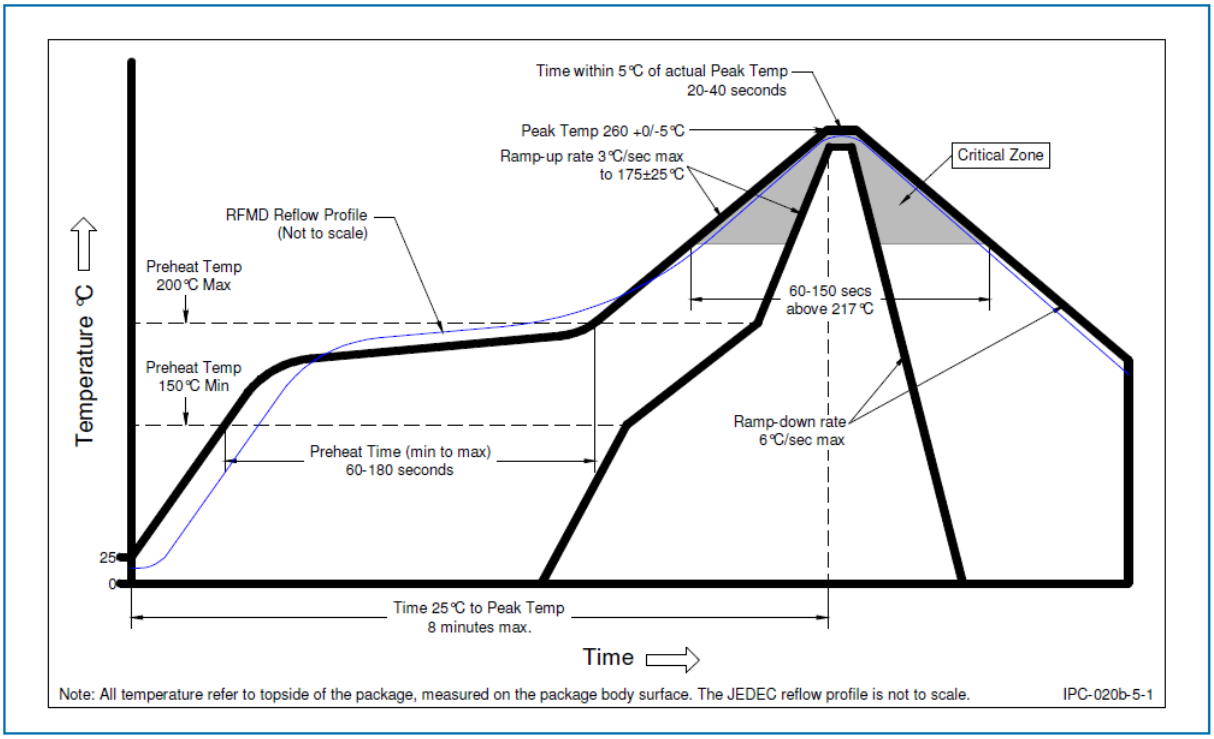


Figure 6b. PCB Footprint Recommended Solder Mask Pattern.

Thermal vias for center slug “B” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the Qorvo evaluation board layout.

REFLOW PROFILE & SOLDER PASTE

Figure 6c illustrates the recommended reflow profile for the RFPA5542.



CONDITIONS	
Ramp-up rate	3 ºC/second max.
Preheat temperature 175 (±25) ºC	180 seconds max.
Temperature maintained above 217 ºC	60 to 150 seconds
Time within 5 ºC of actual peak temperature	20 to 40 seconds
Peak temperature range	260+0/-5 ºC
Ramp-down rate	6 ºC/second max.
Time 25 ºC to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed
Maximum reflow temperature	260 ºC

Figure 6c. Recommended Reflow Profile and Conditions.

Maximum reflow temperature is 260°C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification except for the maximum reflow temperature of 260 °C.

Solder paste used for the Qorvo high temperature reflow qualification.

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

Figure 6d. Solder Paste Specification

Support Data

For any further data on RFPA5542, please request Qorvo point of contact such as marketing, sales or representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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