

ARM WMA Decode Middleware for Linux RTM0AC0000ADWMAMZ1SL32C

Product Manual

RTM0AC0000ADWMAMZ1SL32E-01

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1. Overview

1.1. Overview of This Document

This Document is the Product Manual for ARM WMA Decode Middleware for Linux. For function specification, please read related document [1].

1.2. Related Document

Table 1-1 shows the related documents. Table 1-2 shows the processor-related documents.

Table 1-1 List of Related Document

No	Document Name	Description
[1]	WMA Decode Middleware User's Manual	This document shows function specifications.

Table 1-2 List of Processor-related Document

No	Document Name	Title
[2]	WHITE PAPER(Rev.2.0)	big.LITTLE Processing with the Cortex-A15 and Cortex-A7 Processors
[3]	ARM IHI 0042E	Procedure Call Standard for the ARM Architecture (Nov 30, 2012)

2. Product Specification

2.1. Basic Specification

Table 2-1 shows the basic specification of this Middleware.

Table 2-1 Basic Specification

Item	Description
Target CPU	ARM Cortex-A15/A7
Endian	Little Endian
Supported OS	Linux 3.10
Development Environments	gcc version 4.8.3 20140401 (prerelease) (Linaro GCC 4.8-2014.04)
Dependent Library	This Middleware requires the math library.

2.2. Memory Requirements

Table 2-2 shows memory requirements of this Middleware.

Table 2-2 Memory Size Requirements

Memory Type	Location	Memory area name		Size (in bytes)	
Instruction	ROM	Instruction area		94,052	
Data		Constant table area			
		Other area(Depended on the compiler)			
	Middleware work area		65,536		
	Area breakdown	Static area	Size breakdown	49,152	
		Scratch area		16,384	
	User work area		53,424		
	Area breakdown	Input buffer	Size breakdown	20,480	
		Output buffer		32,768	
		Structure		176	
	Stack area		2,048		
Other area(Depended on the compiler)		1,020			

[Note] Area whose location is shown as ROM in the location column can be included in RAM or ROM.

[Note] Area whose location is shown as RAM in the location column can be included RAM only.

2.3. Performance

Table 2-3 shows processing capability of this Middleware.

Table 2-3 Processing Capability

Item	Description
Average processing load	About 11.8 MHz [Note] Frequency = 44.1kHz/Bit rate = 128 kbps/Number of channels = 2

[Note] The value above varies depending on the frequency, bit rate, and data.

[Note] The value above is measured on R-Car H2 Evaluation Board (ARM Cortex-A15).

[Note] The value above is a reference value which does not indicate a guaranteed level of performance.

2.4. Version information

Table 2-4 shows version information of this Middleware.

Table 2-4 Version Information

Item	Description
Version information	0x00000130 (Version 1.30)

3. List of files

The file list of this Middleware is shown in Table 3-1.

Table 3-1 File list of this Middleware

Directory		Description
RTM0AC0000ADWMAMZ1SL32C		
document	WMASTD_UM_J.pdf	User's Manual(Japanese)
	WMASTD_UM_E.pdf	User's Manual(English)
	RTM0AC0000ADWMAMZ1SL32J-01.pdf	Product Manual(Japanese)
	RTM0AC0000ADWMAMZ1SL32E-01.pdf	Product Manual(English)
lib	libWMASTD_L.so.1.3	Dynamic link library
	wmastd_Lib.h	Header file of library
sample	parser	the sample program of parser
	src	the sample program of application

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		Page	Summary
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