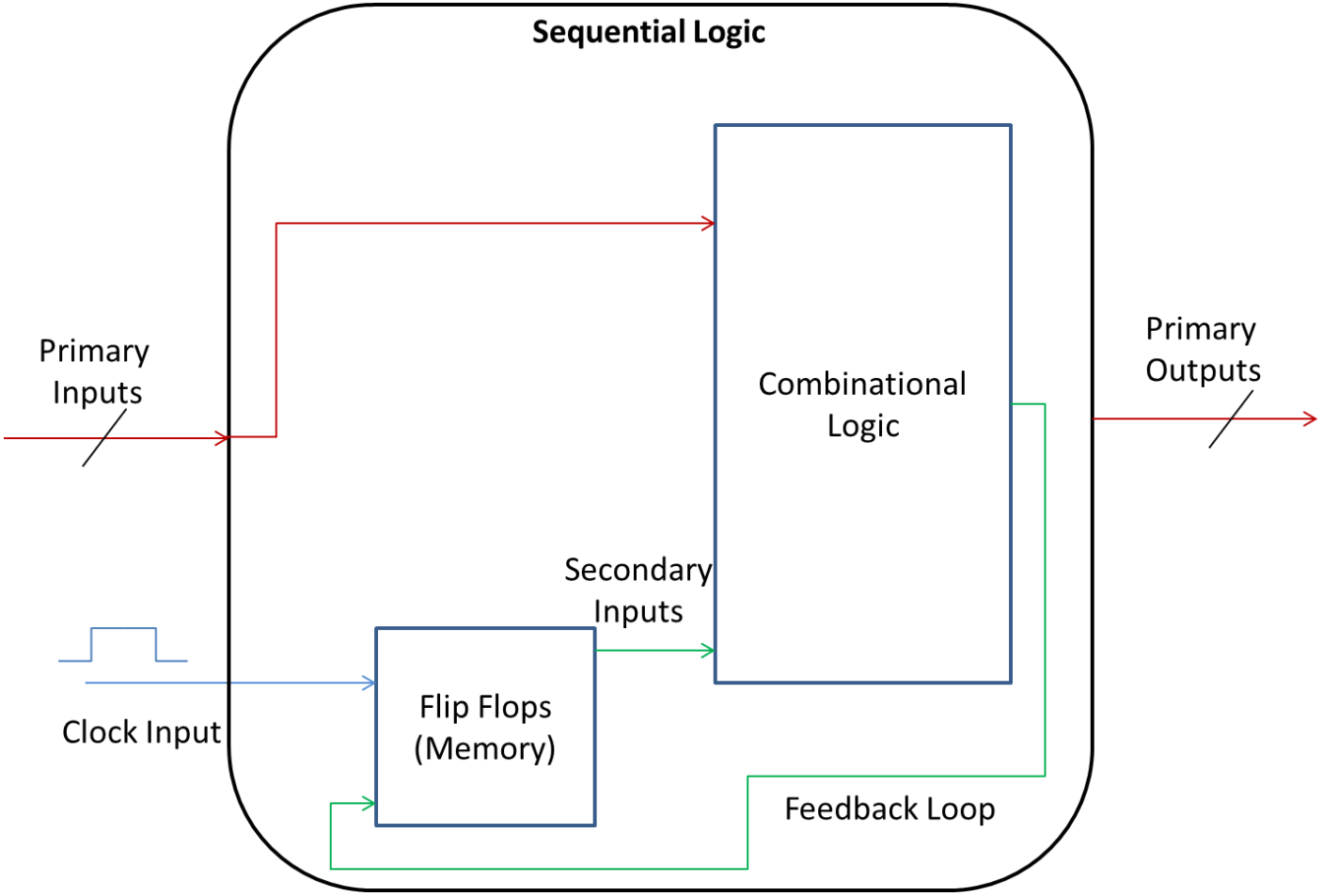
SEQUENTIAL CIRCUITS

Introduction

Sequential circuits is one of the four major topics of digital design:

- Fundamental digital design skills
- Combinational circuits
- Sequential circuits
- Computer organization

Sequential Logic vs Combinational Logic



Sequential Circuits as a Finite State Machine

- Current State

Stored in the memory elements. Finite number of states.

- Next State

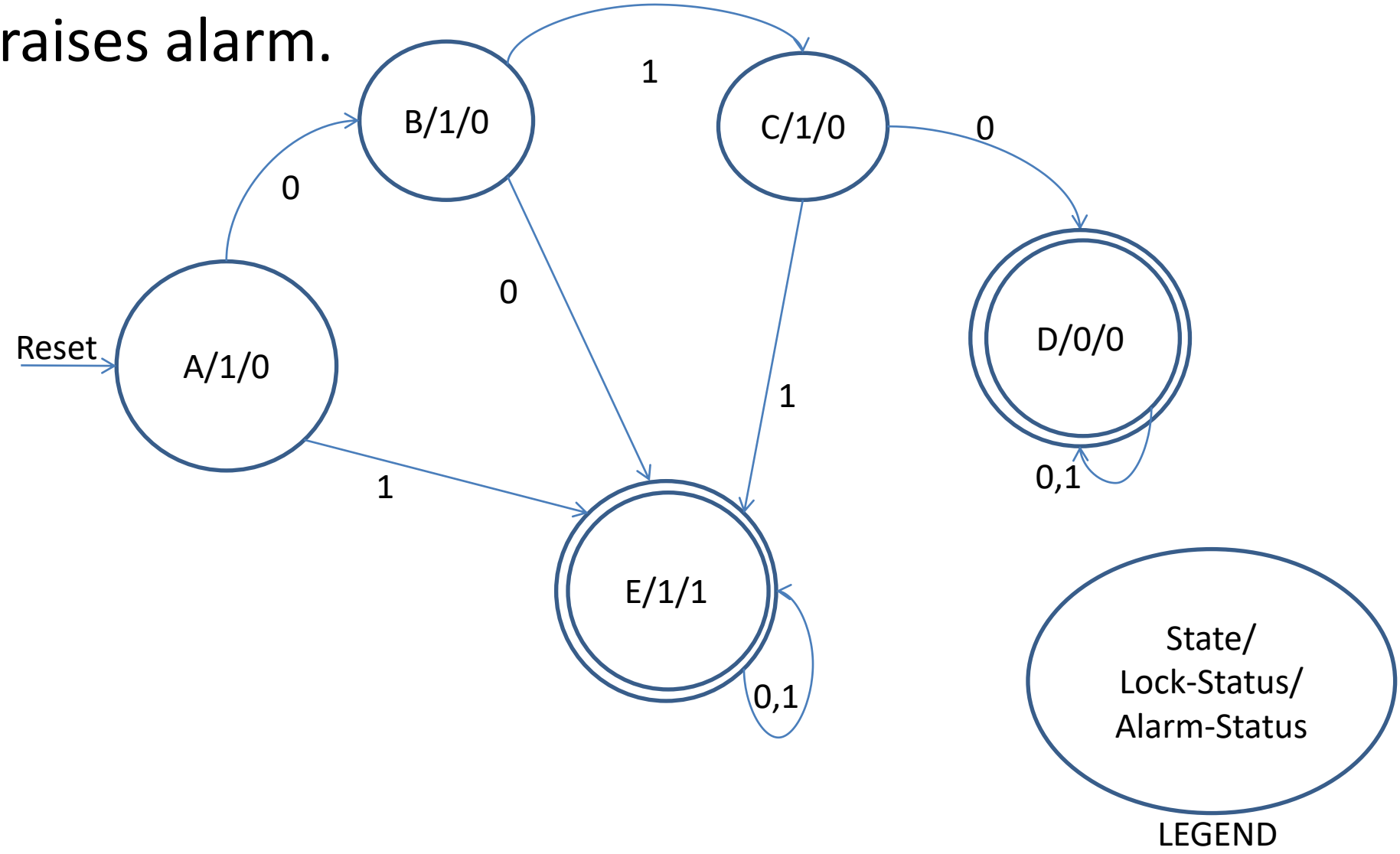
Function of the current state and current inputs.

- Output

Function of the current state and current inputs.

Example- Binary Lock

- Unlocks on 3 bit input being 010, otherwise raises alarm.



Moore and Mealy Machines

- Moore Machine: Output depends only on state transition. Eg: Previous combination lock was a Moore machine.

- Mealy Machine: Output depends not only on state transition but also on the input

Asynchronous vs Synchronous Sequential Circuits

- Clock

Usually a square wave with a fixed frequency.

- Asynchronous Sequential Circuits

The output state changes directly in response to changes in the inputs.

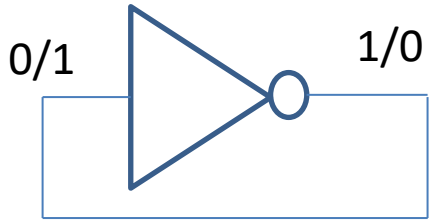
- Synchronous Sequential Circuits

The output state change is constrained to respond to changes in input only at specific time specified by an external clock signal

Basic Memory Elements

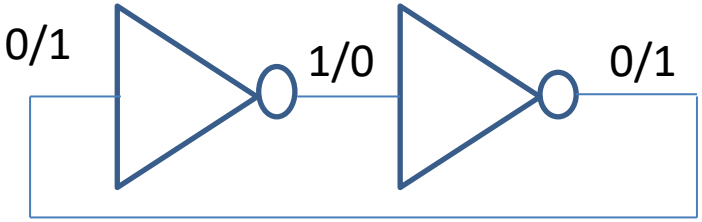
Store 1 bit of information. Bistable Multivibrator.

- Simplest Sequential Circuit



Problem: Oscillating Output

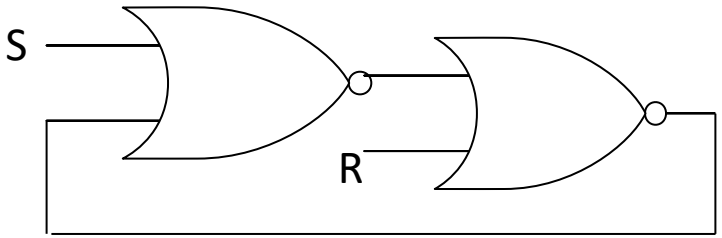
- Add another invertor: Stable Circuit



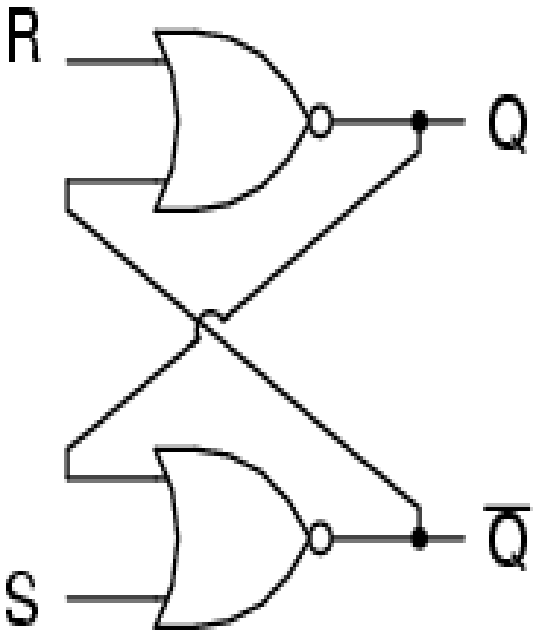
Problem: Unredictable State, no inputs

- Asynchronous Memory Element/LATCH

Add Inputs

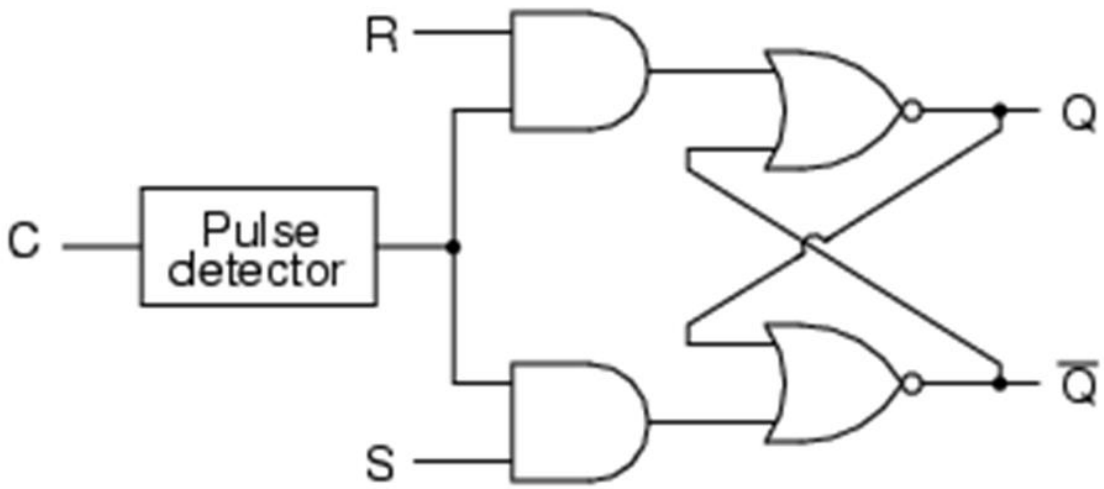


Rearranging: SR Latch or Direct coupled RS Flip flop.



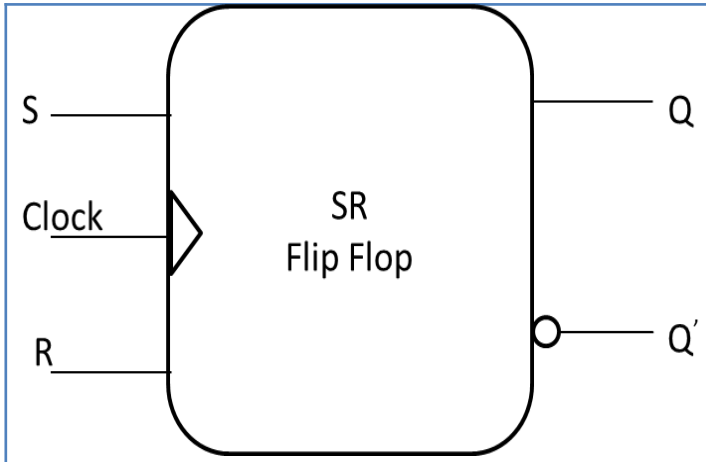
S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

SR Flip Flop



C	S	R	Q	$\overline{Q}$
⎍	0	0	latch	latch
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	?	?
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

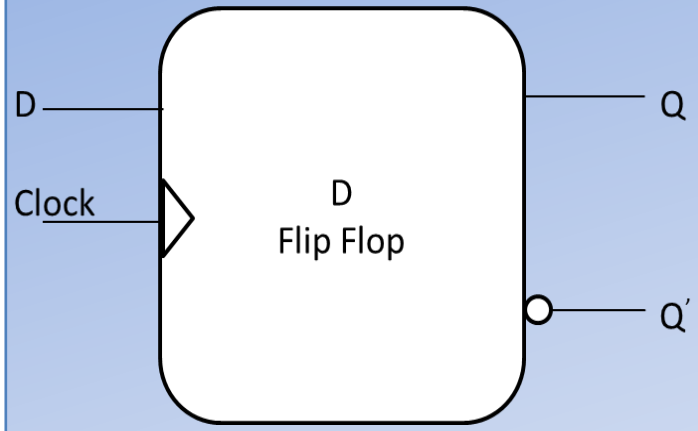
Synchronous Memory Element
Flip Flop (4 Types)



S	R	Q_{t+1}	Q'_{t+1}	Function
0	0	Q_t	Q'_t	No Change
0	1	0	1	Reset to 0
1	0	1	0	Set to 1
1	1	?	?	Indeterminate/Forbidden

State Output Eqn:

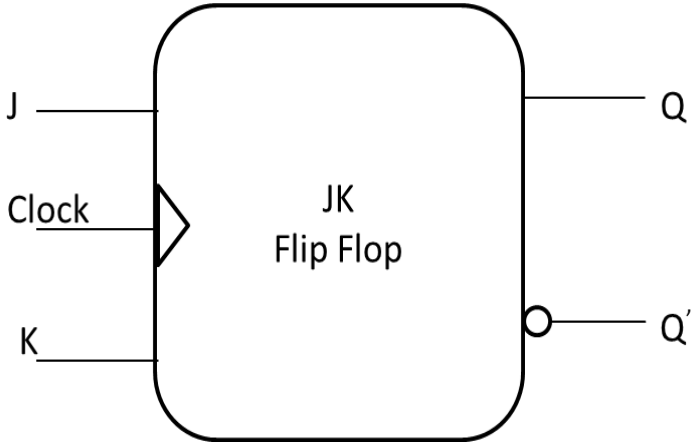
$Q_{t+1}=R'Q_t+S$



D	Q_{t+1}	Q'_{t+1}	Function
0	0	1	Reset to 0
1	1	0	Set to 1

State Output Eqn:

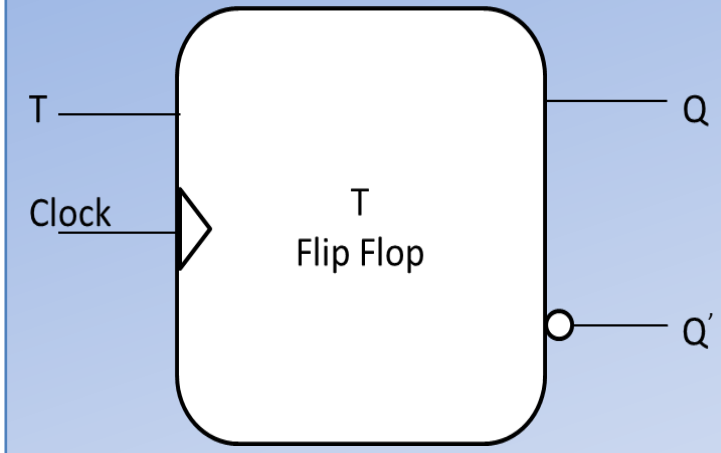
$Q_{t+1}=D$



J	K	Q_{t+1}	Q'_{t+1}	Function
0	0	Q_t	Q'_t	No Change
0	1	0	1	Reset to 0
1	0	1	0	Set to 1
1	1	Q'_t	Q_t	Toggle

State Output Eqn:

$$Q_{t+1}=Q_t'J + Q_tK'$$



T	Q_{t+1}	Q'_{t+1}	Function
0	Q_t	Q'_t	No Change
1	Q'_t	Q_t	Toggle

State Output Eqn:

$$Q_{t+1}=Q_tT + Q_t'T'$$

Which Flip Flop to Choose

- The choice of flip-flop type can affect the complexity of the combinational logic in the resulting sequential circuit.
- The most versatile is the JK, since it can be easily converted into the other two.
- Any one can be converted into one of the other types, but some of these conversions take more logic than others.
- The JK and T flip-flops are most suitable for counters, since they have complementing capability needed in counters. Hence they result in less logic than the other types.
- D flip-flops are the ones found in almost all PLDs. If your design is targeted for a PLD, you are usually stuck with D flip-flops.

Timing Considerations

- Propagation Delay: Although ideally a gate should respond instantaneously to the input, in real situations all devices have some delay associated with signal propagation from input to output called the propagation delay.

- Setup time: Is the minimum duration that the data must be stable at the input before the clock edge

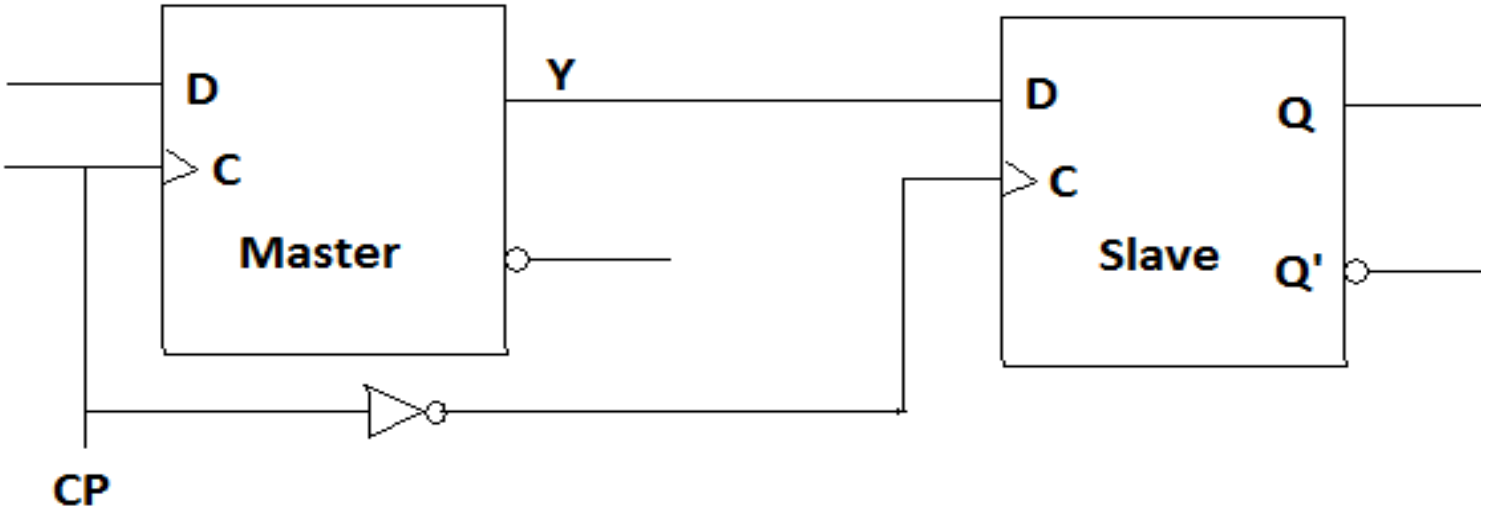
- Hold time: Is the minimum duration that the data must remain stable on the input after the clock edge

Race Around Condition & Solutions

- Short clock pulse: *Let the output react just once.*

  Pulse frequency < Propagation delay

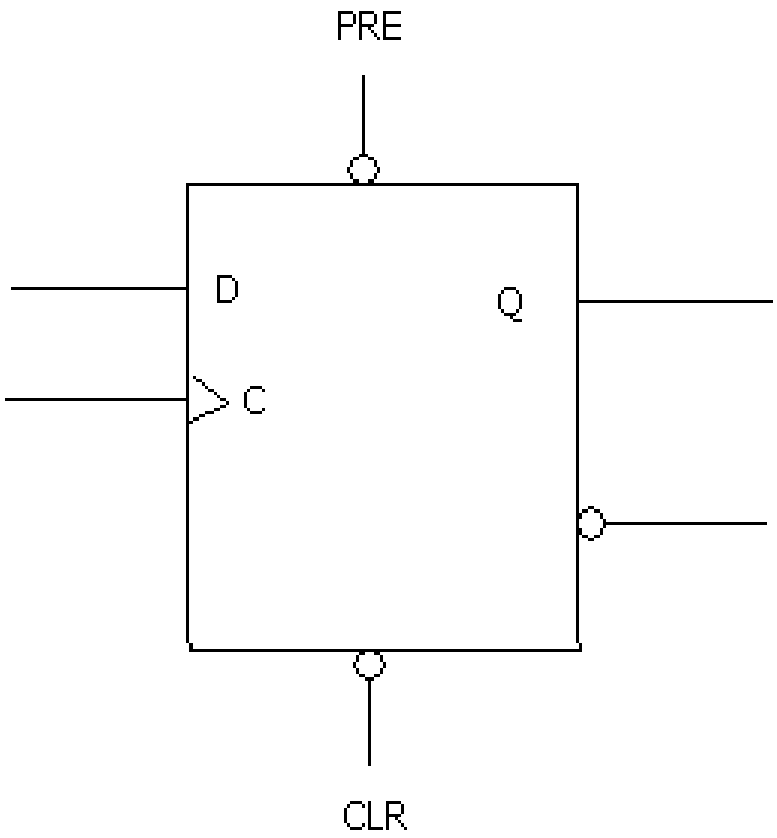
- Master-Slave flip-flop



- Edge-triggered Flip Flops

Much more complicated in circuitry. But devoid of the problems of previous two approaches

Direct Inputs/
Asynchronous Inputs



Excitation Inputs

SR Flip Flop

Current State Q_t	Next State Q_{t+1}	Excitation Inputs		Explanation
		S	R	
0	0	0	X	Either no change SR=00 or reset, SR=01
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	0	Either set-SR=10 or no change- SR=00

D Flip Flop

D	**Q_{t+1}**	**Q'_{t+1}**	**Function**
0	0	1	Reset to 0
1	1	0	Set to 1

- JK Flip Flop

Current State Q_t	Next State Q_{t+1}	Excitation Inputs		Explanation
		J	K	
0	0	0	X	Either no change JK=00 or reset, JK=01
0	1	1	X	Either Toggle- JK=11 or Set- JK=10
1	0	X	1	Either Toggle- JK=11 or Reset– JK=01
1	1	X	0	Either set-JK=10 or no change- JK=00

- T Flip Flop

Current State Q_t	Next State Q_{t+1}	Excitation Input T	Explanation
0	0	0	If there is change, T=1, if no change, T=0
0	1	1	
1	0	1	
1	1	0	

Circuit Analysis

Sequential circuit analysis is useful when

- You need to determine the functionality of an existing sequential circuit

- You want to make changes to an existing sequential circuit, and need to verify the new behaviour

Steps in Analysis

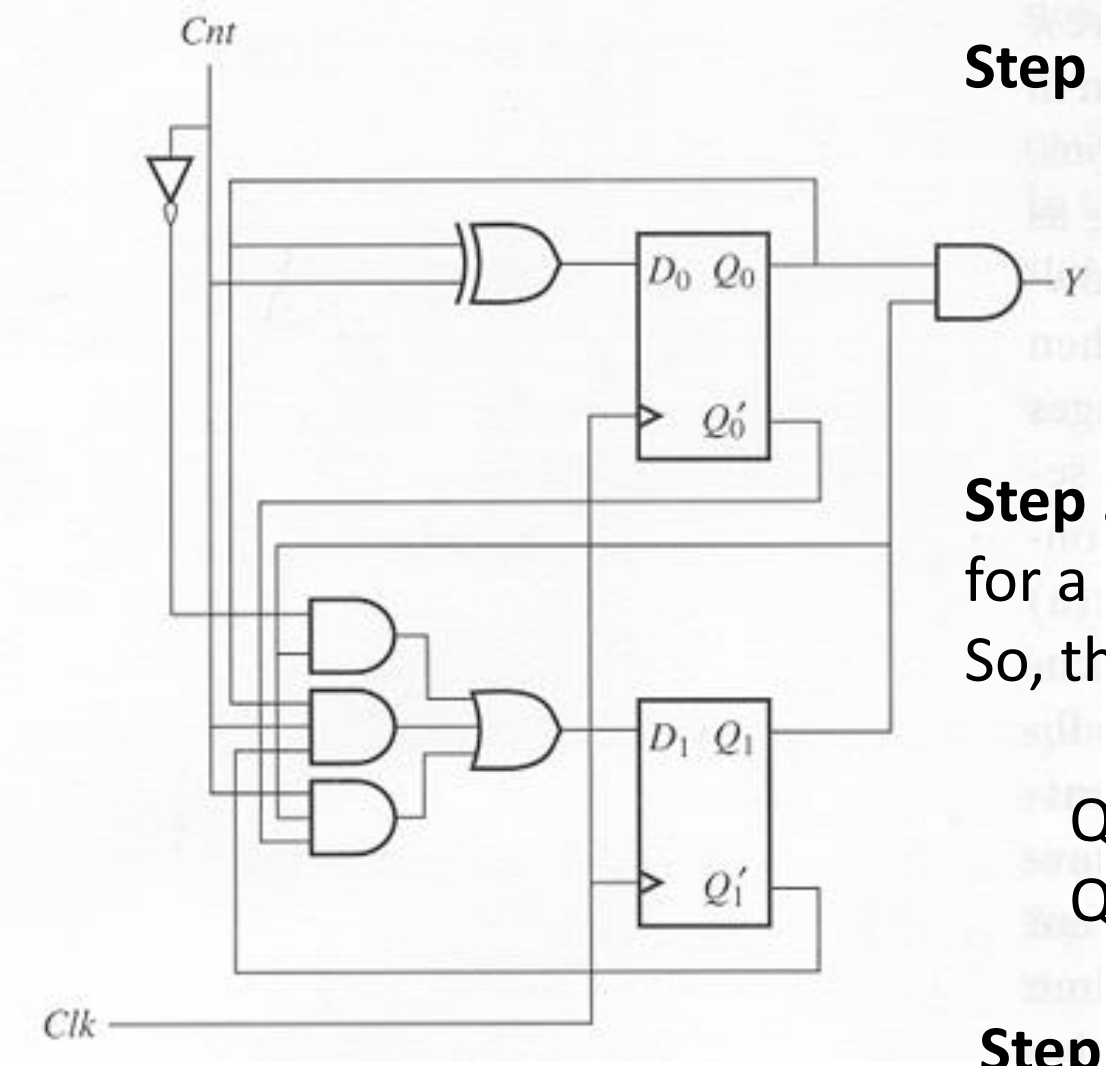
- Excitation equations: Boolean equations that describe the input to the flip-flops.
- Next state equations: Use the excitation equations and the flip-flop characteristic equations to compute the next state of each flip-flop.
- Output equations
- State table
- State diagram

Excitation Inputs

S	R	Q_{t+1}	Q'_{t+1}	Function
0	0	Q_t	Q'_t	No Change
0	1	0	1	Reset to 0
1	0	1	0	Set to 1
1	1	?	?	Indeterminate/Forbidden

Current State Q_t	Next State Q_{t+1}	Excitation Inputs		Explanation
		S	R	
0	0	0	X	Either no change SR=00 or reset, SR=01
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	0	Either set-SR=10 or no change- SR=00

Analysis Example



Step 1: Develop excitation eqns

$D_0 = Q_0 \text{ XOR } C$

$D_1 = C'Q_1 + Q_0CQ_1' + CQ_1Q_0'$

Step 2: The characteristic equation for a D flip-flop is: $Q_{next} = D$

So, the next state equations are:

$Q_{0next} = Q_0 \text{ XOR } C$

$Q_{1next} = C'Q_1 + Q_0CQ_1' + CQ_1Q_0'$

Step 3: Output Equation

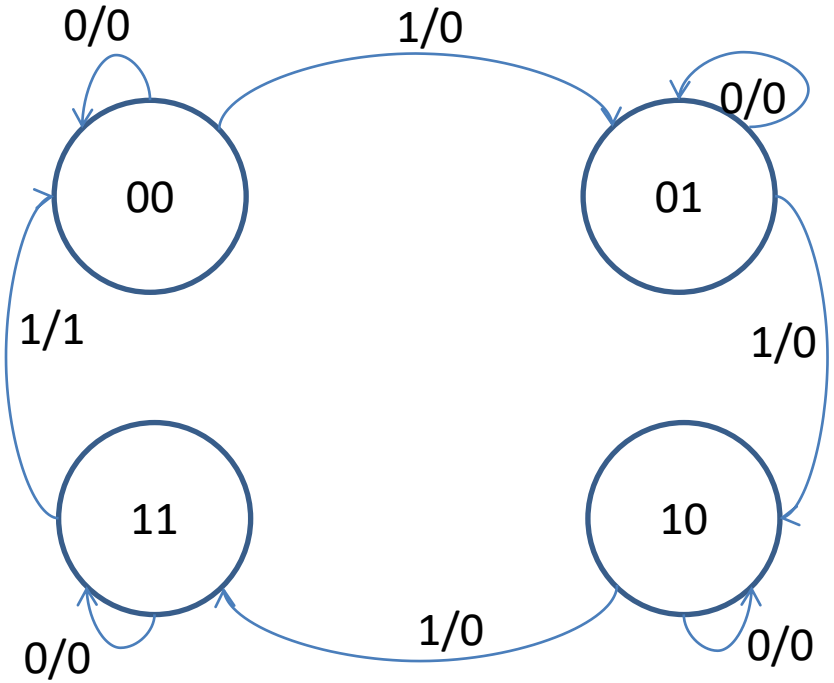
$Y = Q_0Q_1$

Analysis Example Ctd…

Step 3: State Table

Present State	Next State ($Q_{1next}Q_{0next}$)		Outputs
Q_1 Q_0	**C=0**	**C=1**	**Y**
0 0	0 0	0 1	0
0 1	0 1	1 0	0
1 0	1 0	1 1	0
1 1	1 1	0 0	1

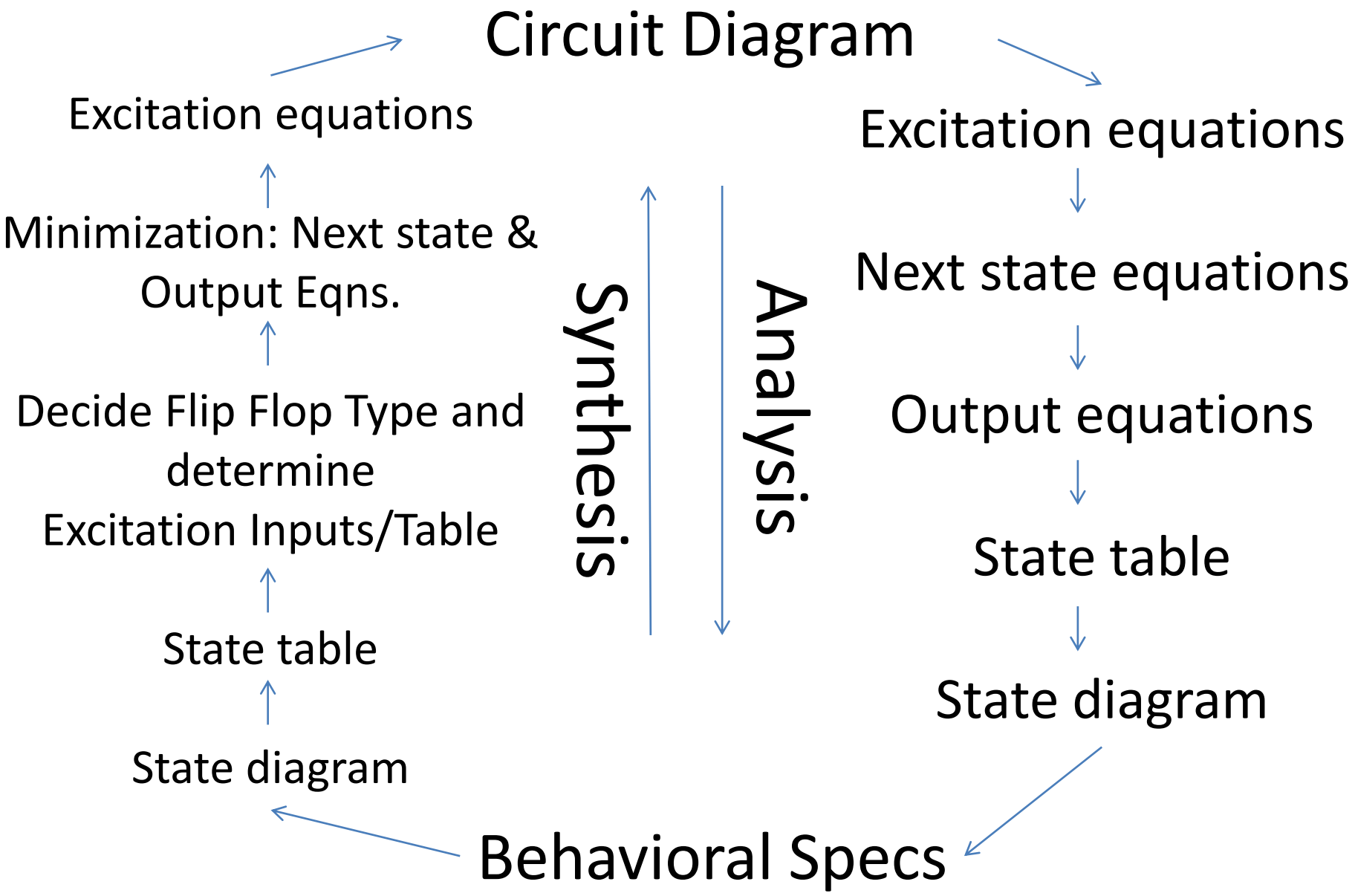
- Step5: State Diagram



Conclusion:

- This circuit is a forward counter, with no state change when input C=0, and proceeding to next count on input c=1.
- The output Y is the carry output, which can be used to cascade with another unit
- Note: We can see that this is an example of a Mealy Machine

CIRCUIT SYNTHESIS



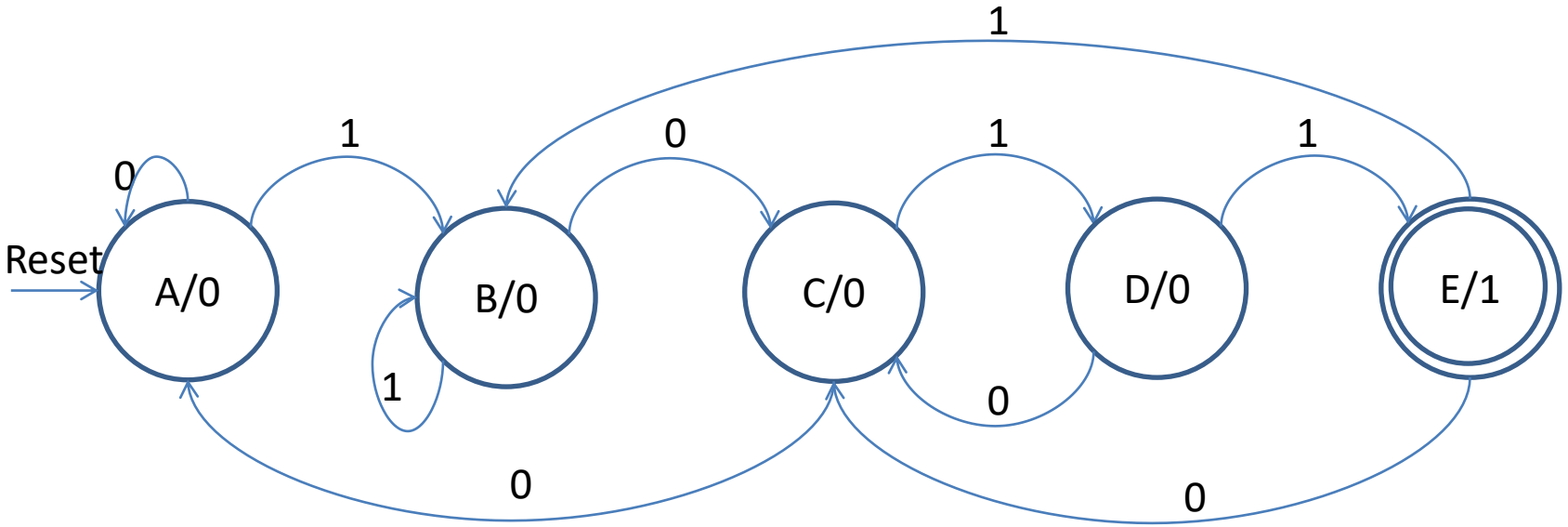
Examples of Sequential Circuits

- Sequence generator. Eg: Up down counter
- Pattern Recognizer/ Sequence detector
    1. Even Parity Checker
    2. Sequence Detector for 1011
    3. Mod 3 detector
- Sequence Transformer
- Other Complex Examples:
  - Vending machine
    - Machine accepts tokens of Rs 5. Coffee is for Rs 10.
    - May add more complexity by accepting different coin combinations, multiple output options, return of change etc.
  - Robotic Ant in a maze FSM
  - Traffic Lights Controller

Circuit Design/Synthesis Example

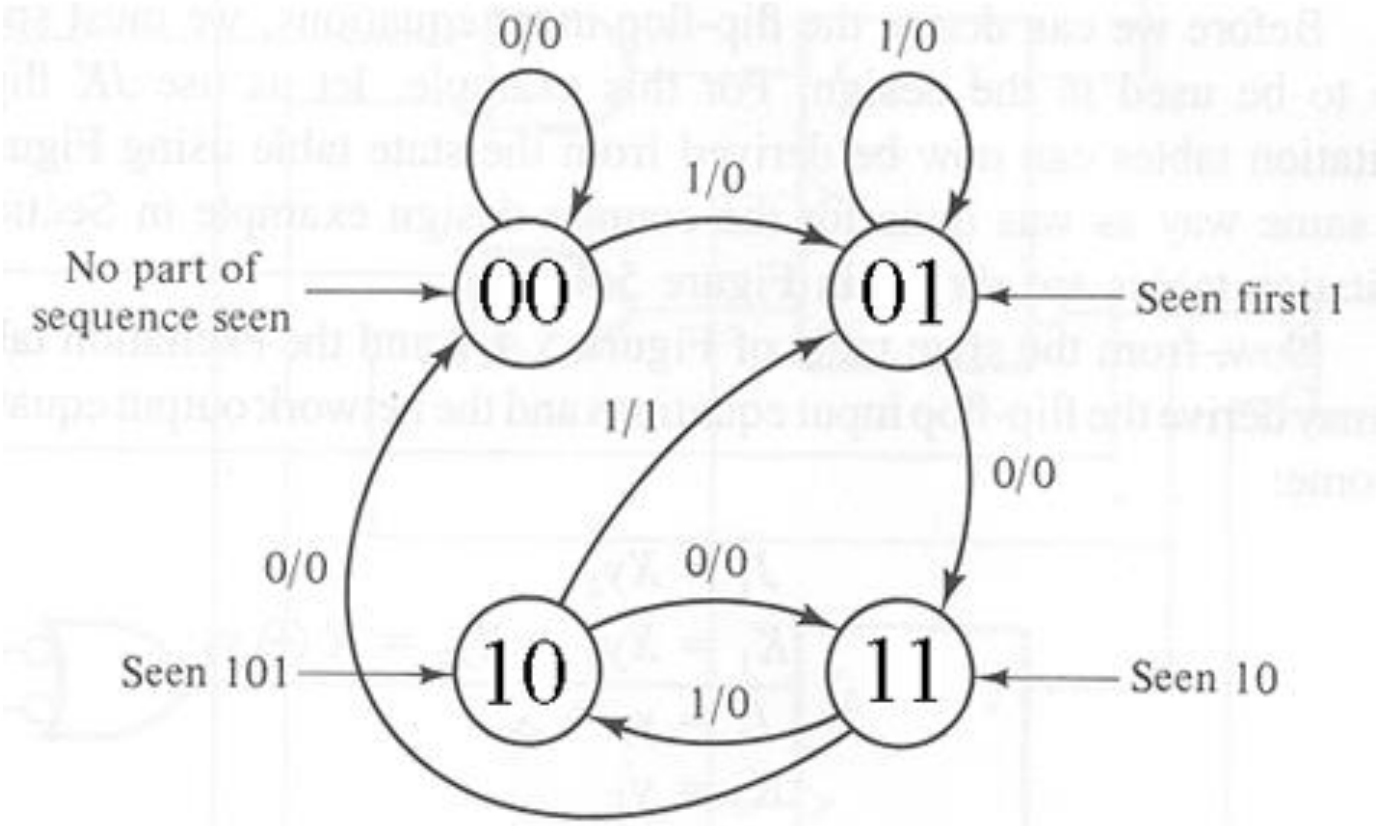
Problem Statement: 1011 Sequence Detector

Step 1: State Diagram: Moore Model



A: Start Afresh B: First 1 Seen C: 10 Seen D: 101 Seen E: 1011 Seen, Sequence Detected

Using Mealy Model



Continuing with Moore Model…

Step 2: State Diagram

Present State				External Input	Next State				Output Signal
	X_t	Y_t	Z_t	I		X_{t+1}	Y_{t+1}	Z_{t+1}	S
A	0	0	0	0	**A**	0	0	0	0
B	0	0	1	0	**C**	0	1	0	0
C	0	1	0	0	**A**	0	0	0	0
D	0	1	1	0	**C**	0	1	0	0
E	1	0	0	0	**C**	0	1	0	0
A	0	0	0	1	**B**	0	0	1	0
B	0	0	1	1	**B**	0	0	1	0
C	0	1	0	1	**D**	0	1	1	0
D	0	1	1	1	**E**	1	0	0	0
E	1	0	0	1	**B**	0	0	1	1

Step 3: Excitation Table

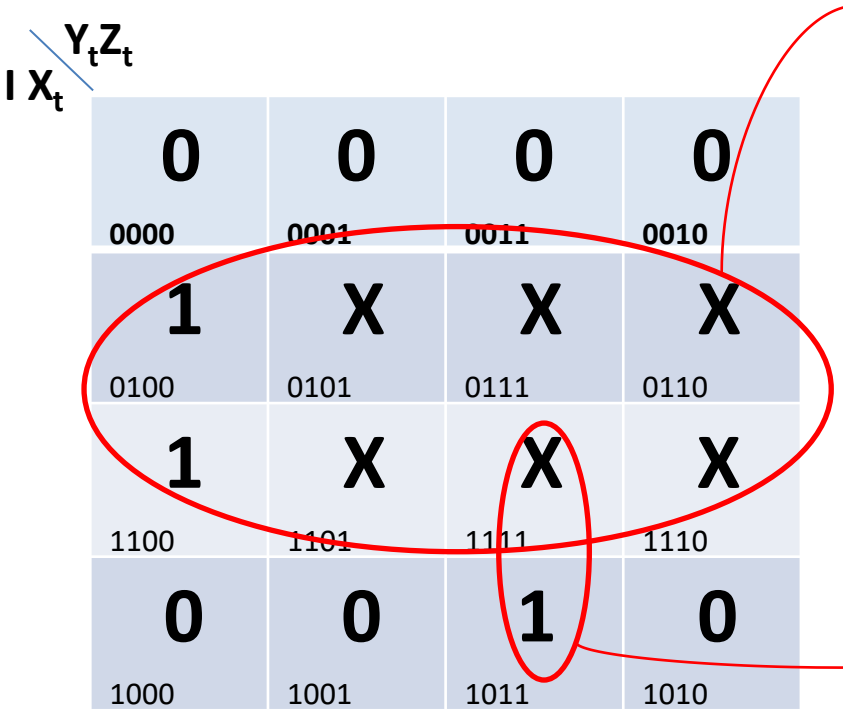
I	Present State			Next State			Output Signal	Excitation Inputs		
	X_t	Y_t	Z_t	X_{t+1}	Y_{t+1}	Z_{t+1}	S	T_x	T_y	T_z
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	1	1	0	1	0	0	0	1	1
0	1	0	0	0	1	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0	1
1	0	0	1	0	0	1	0	0	0	0
1	0	1	0	0	1	1	0	0	1	1
1	0	1	1	1	0	0	0	1	0	1
1	1	0	0	0	0	1	1	1	0	1

Minimization and Input and Output Eqns.

Flip Flop Input and Circuit Output as a function of current state and External Input

- Output Equation: $S = X_t \cdot Y_t' \cdot Z_t'$ (Directly From Table)

- Input Equations: Using Simplification by K-map



$T_x = X_t + I\,Y_tZ_t$

Similarly,

$T_y = I'Y_t + Y_tZ_t' + IX_t$

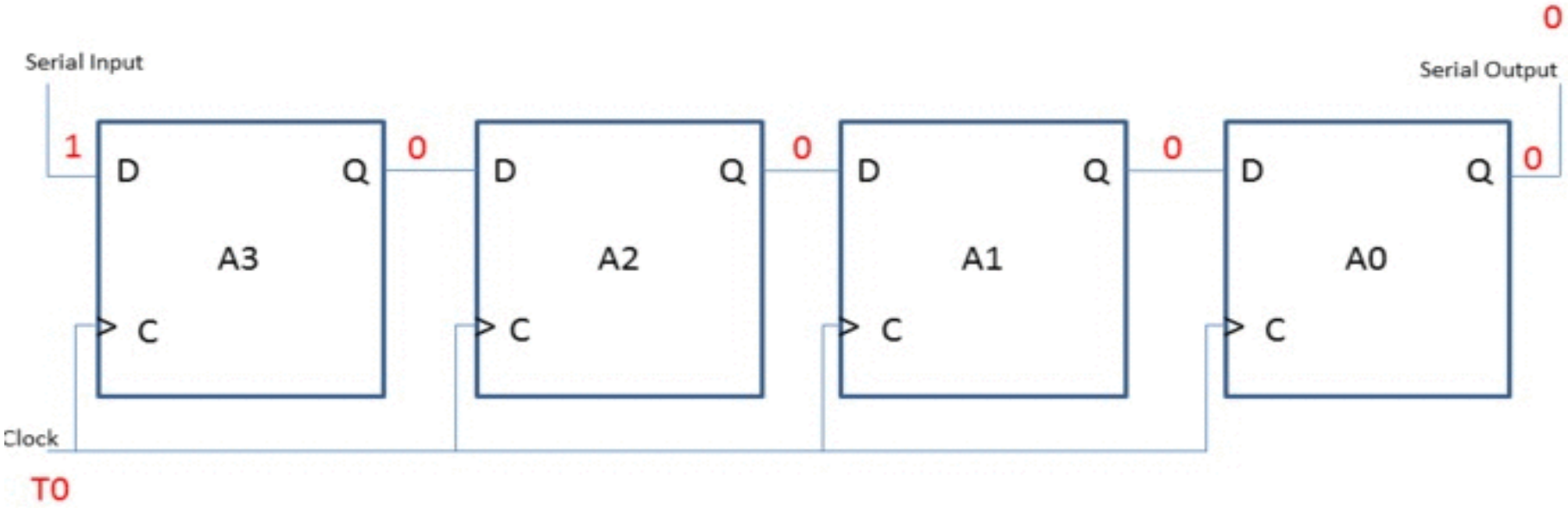
$T_z = IZ_t' + Y_tZ_t + I'Z_t$

Circuit Diagram

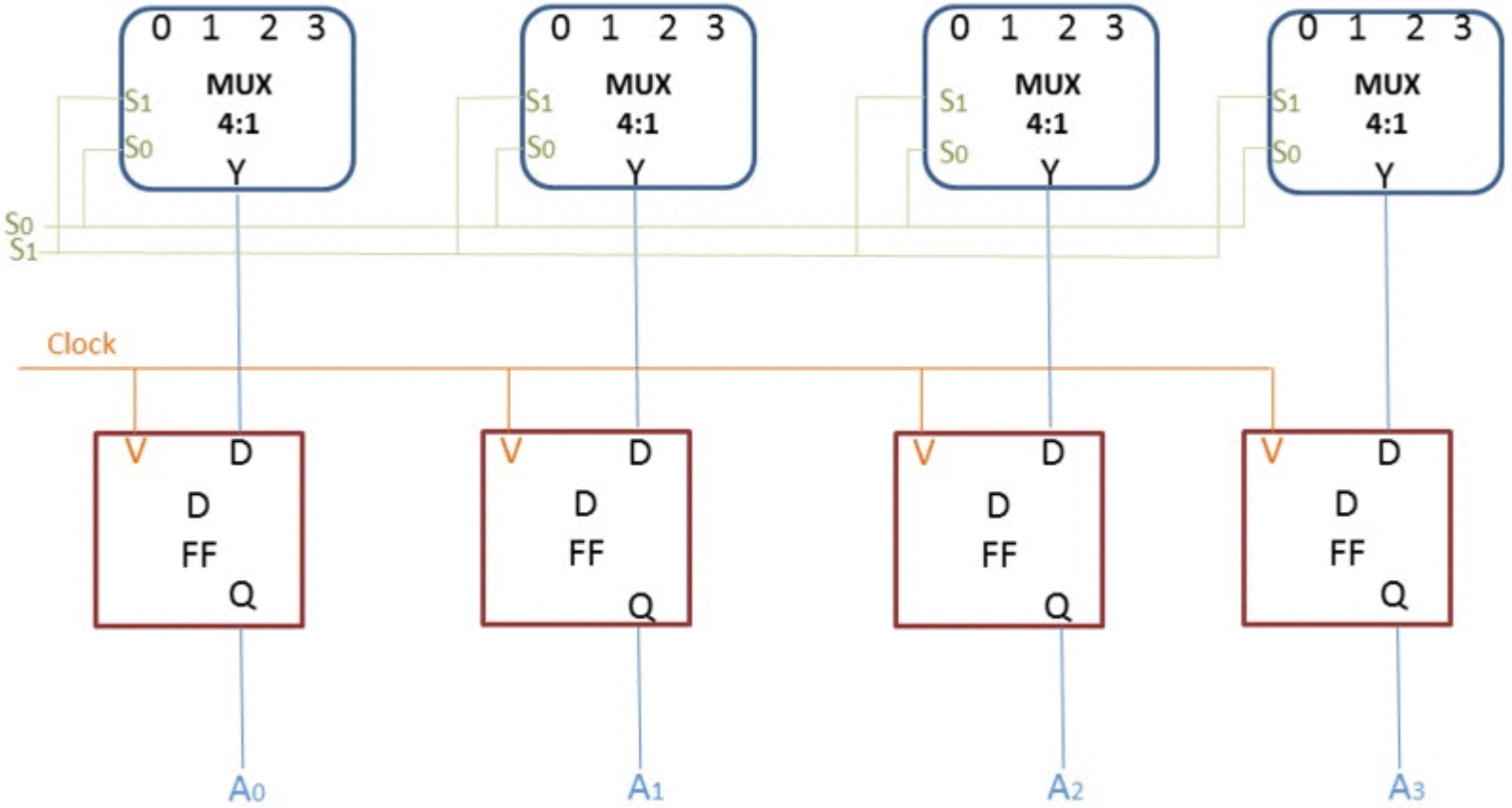
Two Basic Categories of sequential circuits- Registers and Counters

- Registers
  - Parallel In Parallel Out
  - Serial In Serial Out
  - Serial In Parallel Out
  - Parallel In Serial Out

Shift Right Register

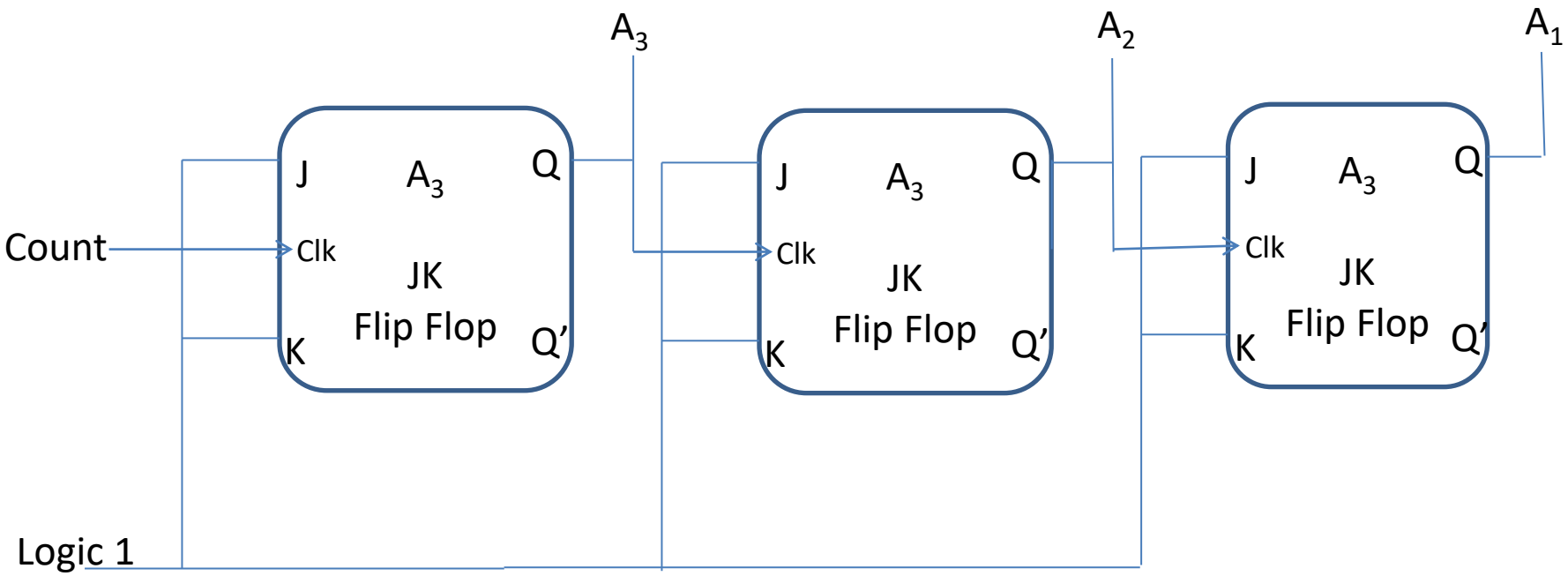


All in one- Bidirectional Shift Register with parallel load

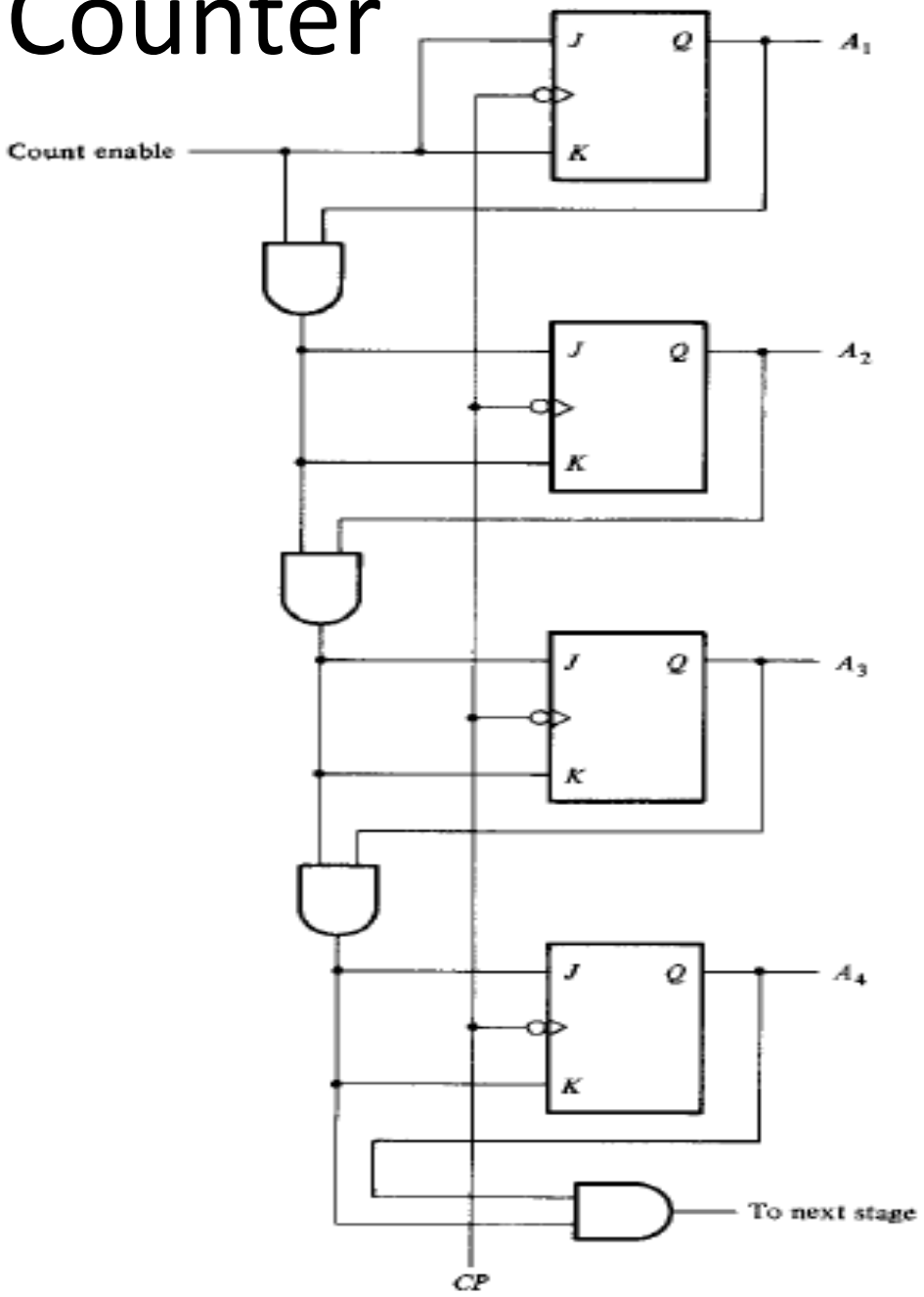


Counters- Asynchronous/ Ripple Counter

Clock applied only to first stage, successive flip flops are clocked using outputs of previous stages

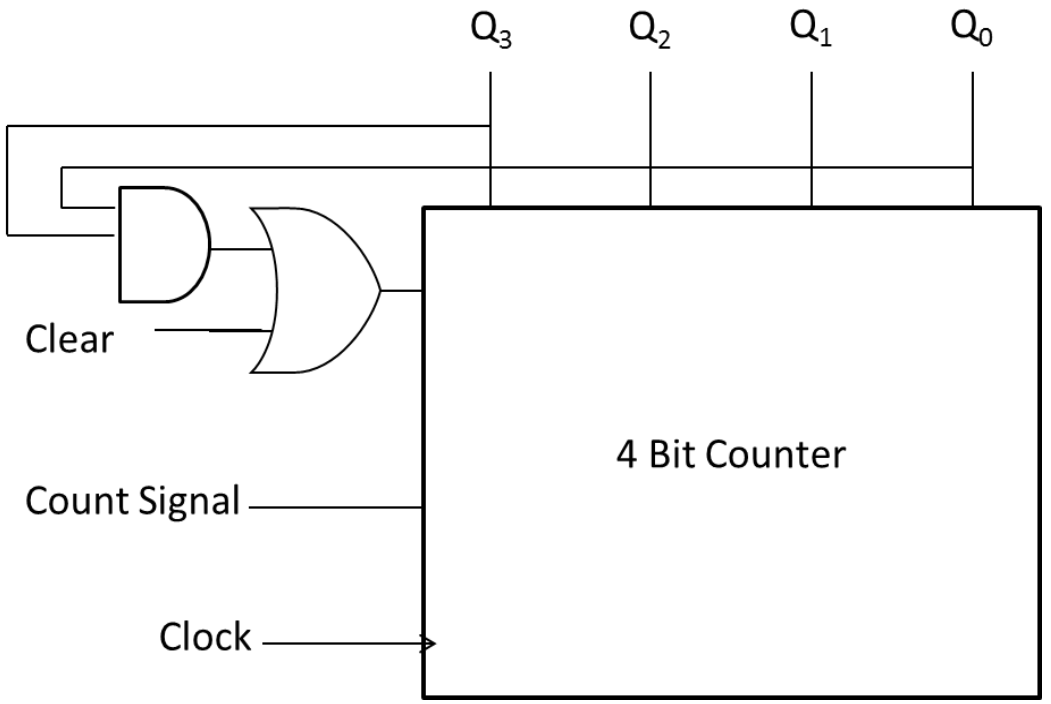


Synchronous Counter

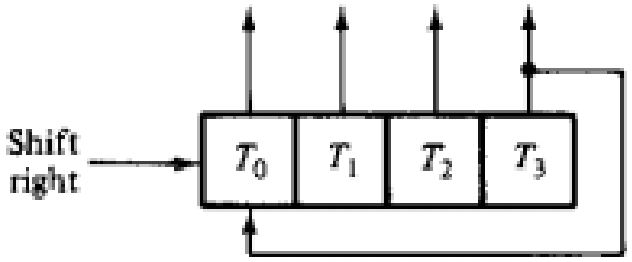


Mod Counter

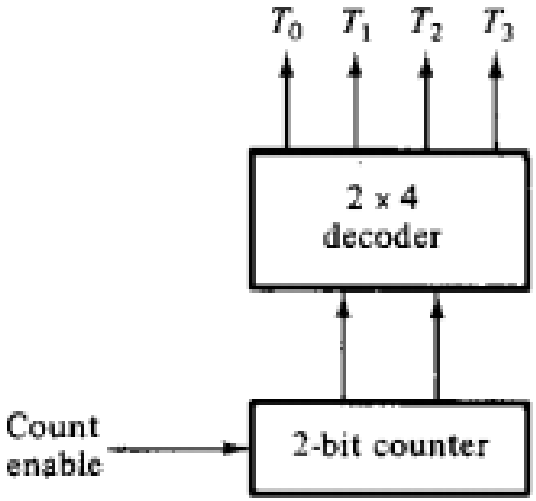
- BCD Counter from 4 bit synchronous counter



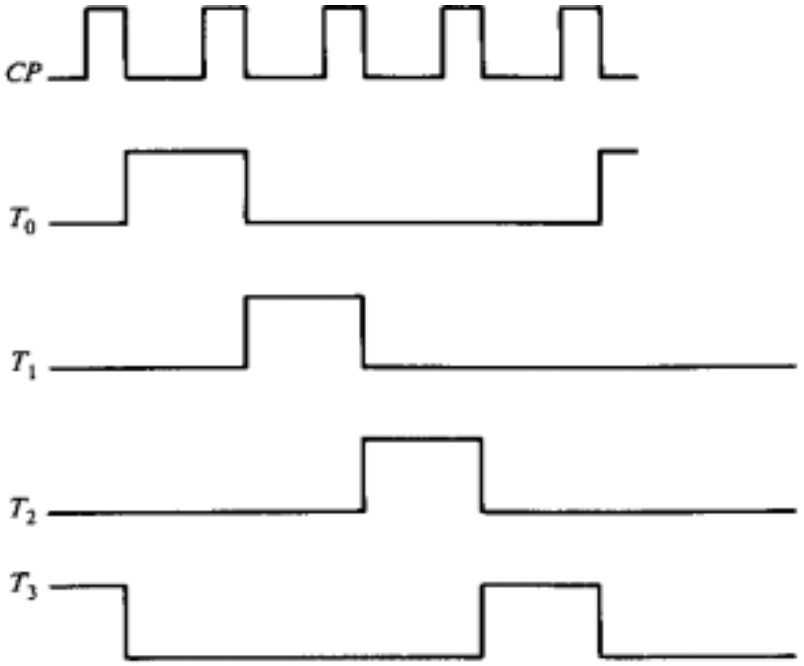
Ring Counter



(a) Ringcounter (initial value = 1000)



(b) Counter and decoder



(c) Sequence of four timing signals

Ring Counters

- A straight ring counter or Overbeck counter:

  -Counts N time signals using N Flip Flops.

  - Circulates single bit around ring of SISO flip flops.

- Switch Tail Counter/ Twisted ring counter/ Johnson counter/ Möbius Counter (or Moebius):

  - Counts 2N states using N flip flops.

  - Connects the complement of the output of the last shift register to the input of the first register and hence circulates a stream of ones followed by zeroes around the ring.

Teaching Tools

Circuit Level

- Hardware within an Electronics Laboratory
- WinLogiLab

Higher Level

- Lc3 Simulator
- CPUSim