

Calibrating Control-Bounded ADCs

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Abstract—The paper considers the calibration of control-bounded analog-to-digital converters. It is demonstrated that variations of the analog frontend can be addressed by calibrating the digital estimation filter. In simulations (both behavioral and transistor level) of a leapfrog analog frontend, the proposed calibration method restores essentially the nominal performance. Moreover, with digital-filter calibration in mind, the paper reformulates the design problem of control-bounded converters and thereby clarifies the role of sampling, desired filter shape, and nominal conversion error.

Index Terms—Control-Bounded Analog-to-Digital Conversion, Calibration, Component Variations, RLS

I. INTRODUCTION

Stabilizing an analog system using a digital control amounts to implicit analog-to-digital conversion. This is the core idea behind the control-bounded analog-to-digital converter (CBADC) concept, first proposed in [1] and further developed in [2] and [3]. The CBADC perspective allows more general analog frontends, i.e., analog system and digital control combinations, at the expense of a post-processing digital estimation step. Specifically, it falls on the digital estimator to consolidate the joint effort of the digital control into an estimate of the input signal fed into the analog system. A CBADC analog frontend partially resembles continuous-time sigma-delta modulators (CT- $\Sigma\Delta$ Ms) [4]. However, in contrast to CT- $\Sigma\Delta$ Ms, the analog frontend of a CBADC may contain high-order filters while having a guaranteed stable nominal operation. Moreover, the high-level design of a CBADC is a continuous-time filter design task, whereas CT- $\Sigma\Delta$ Ms are typically considered a discrete-time design concept converted into the continuous-time domain [5].

Crucially, the digital estimator's ability to estimate relies on its knowledge of the actual analog frontend. As reported in [6], this makes CBADCs particularly sensitive to component variations if not accounted for. In this paper, we address this issue by demonstrating that the digital estimation filter can be calibrated to compensate for such variations.

II. THE LEAPFROG FRONTEND

A single CBADC analog frontend is considered for calibration; the CBADC LF analog frontend, introduced in [2] and further investigated in [6]. A single-ended opamp- RC based implementation of the N th order LF structure is shown in Figure 1. Its basic functionality can be thought of as amplifying an input signal $u(\cdot)$ through a chain-of-integrators, each parametrized by a time constant $R_{\beta_\ell}C_\ell$, while stabilizing the analog states $x_1(\cdot), \dots, x_N(\cdot)$ by local digital control (DC)

signals $s_1(\cdot), \dots, s_N(\cdot)$. The analog frontend gets its name from the R_{α_ℓ} feedback paths which also introduce complex poles in the transfer function from $u(\cdot)$ to the final state $x_N(\cdot)$ (assuming $(s_1(\cdot) = 0, \dots, s_N(\cdot) = 0)$). This transfer function is of fundamental importance for the performance of a CBADC and will be referred to by its impulse response $g_u(\cdot)$. The digital control is implemented as a clocked comparator, generating the binary discrete-time control signals $s_\ell[\cdot]$ which are fed back to the system through a digital-to-analog converter (DAC) with an impulse response $\theta(\cdot)$ as

$$s_\ell(t) \triangleq \sum_k s_\ell[k] \theta_\ell(t - kT). \quad (1)$$

The final state can be written as

$$x_N(t) = (g_u * u)(t) + \sum_{\ell=0}^N (g_\ell * s_\ell)(t) \quad (2)$$

where $g_\ell(\cdot)$ denotes the impulse response of the transfer function from $s_\ell(\cdot)$ to $x_N(\cdot)$.

Finally, $s_0[k] \in \{\pm 1\}$ is a known binary discrete-time reference signal which will be used to calibrate the CBADC frontend. This signal is randomly generated to produce a wideband spectrum, and the ratio $R_{\kappa_0}/R_{\kappa_1}$ is a tradeoff parameter between the time needed for calibration and a reduced maximum input signal swing.

III. THE DIGITAL ESTIMATOR

The output of the converter is an estimate $\hat{u}[k]$, of a filtered and sampled version of $u(\cdot)$, obtained by $N + 1$ linear filters as

$$\hat{u}[k] \triangleq \sum_{\ell=0}^N (h_\ell * s_\ell)[k] + \hat{u}_0 \quad (3)$$

where the reference filter h_0 is a design choice and h_1, \dots, h_N , and the scalar offset \hat{u}_0 , will be subject to calibration.

As shown in Appendix A, $\hat{u}[\cdot]$ can be decomposed into

$$\hat{u}[k] = (h_u * u)(kT) + (\tilde{g}_u * x_N)(kT) + e_c[k] \quad (4)$$

where $h_u(\cdot)$ is the impulse response of the desired signal transfer function (STF). The second term in (4) is recognized as the nominal conversion error, where $\tilde{g}_u(\cdot)$ is the impulse response of the noise transfer function (NTF) [2]. Using the NTF filter, the STF filter can be written as

$$h_u(t) = -(\tilde{g}_u * g_u)(t) \quad (5)$$

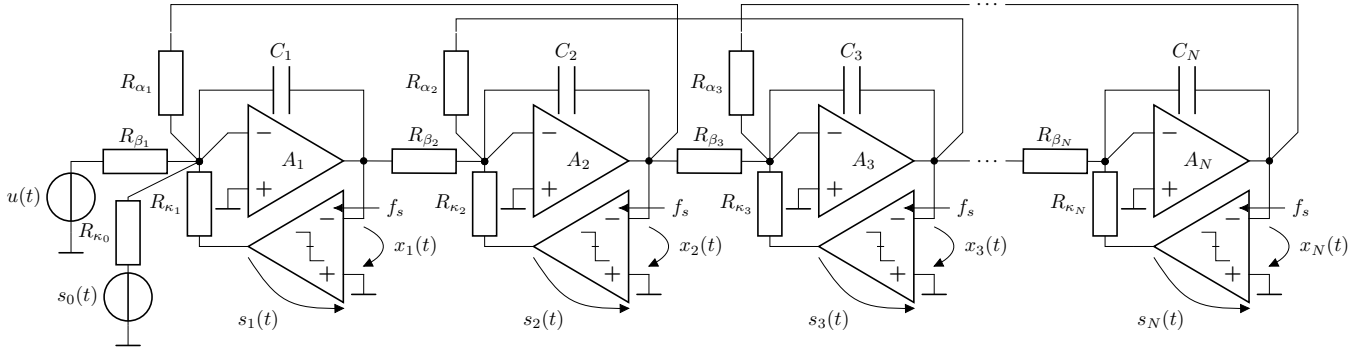


Fig. 1. A single-ended circuit implementation of the N th order homogeneous leapfrog (LF) analog frontend with two input signals: $u(\cdot)$, the unknown signal to be converted, and $s_0(\cdot)$, a known binary reference signal. All signals $u(\cdot)$, $s_0(\cdot)$, \dots , $s_N(\cdot)$, $x_1(\cdot)$, \dots , $x_N(\cdot)$ are represented as voltages.

with $g_u(t)$ as in (2). The last term in (4) is the calibration error

$$e_c[k] \triangleq \sum_{\ell=1}^N \left((h_\ell - \check{h}_\ell) * s_\ell \right) [k], \quad (6)$$

where

$$\check{h}_\ell[k] \triangleq (\tilde{g}_u * g_\ell * \theta_\ell)(kT), \quad (7)$$

are the minimizing filter coefficients to the cost function (9) as will be further described in Section III-A.

The fundamental step in going from (3) to (4) is connecting the desired continuous-time STF filter and the discrete-time reference filter as

$$h_0[k] \triangleq \check{h}_0[k] \propto -(h_u * \theta_0)(kT) \quad (8)$$

where the proportionality relation is due to the fact that $g_u(t) \propto g_0(t)$. The STF filter is a digital design choice that is not subject to calibration. Moreover, the role of sampling, in connection to the STF filter, is emphasized in (4) which opposes the conventional view that sampling is the work of the comparators in Figure 1. Despite the continuous-time nature of the STF filter, it will be enforced by the digital estimator in the discrete-time domain, see (8). Therefore, only samples from its impulse response $h_u(\cdot)$ will be required for estimation and calibration. Furthermore, as the NTF filter is implicitly defined by the circuit implementation, i.e., $g_u(\cdot)$ together with the choice of STF filter, see (5), it is also not subject to calibration.

In summary, (3) and (4) reveals the fundamental idea of the control-bounded ADC concept in two equations: a filtered and sampled version of the input signal, $(h_u * u)(kT)$, can be computed by a discrete-time convolution of the control signals, (3), where the fundamental performance of such an estimate is dictated by the analog frontends ability to both amplify $u(\cdot)$ and bound the magnitude of the last state $x_N(\cdot)$. The calibration error $e_c[\cdot]$ can be made arbitrarily small by conventional calibration techniques as will be shown next.

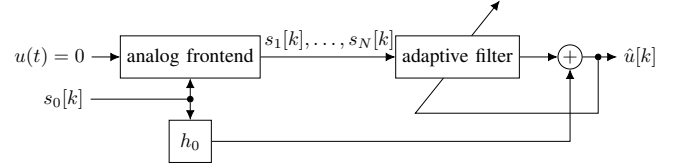


Fig. 2. Adaptive filtering setup for estimating h_1, \dots, h_N using a known reference signal $s_0[\cdot]$ and a fixed reference filter h_0 .

A. Calibration

In the case of no input, i.e., $u(\cdot) = 0$, the impulse responses $\check{h}_\ell[\cdot]$, from (7), are recognized, see Appendix B, as the minimizing filter coefficients $h_1[\cdot], \dots, h_N[\cdot]$ with respect to the cost function

$$\mathbb{E} \left[\left| (h_0 * s_0)[\cdot] + \sum_{\ell=1}^N (h_\ell * s_\ell)[\cdot] + \hat{u}_0 \right|^2 \right]_{u(\cdot)=0} \quad (9)$$

where $s_0[\cdot], \dots, s_N[\cdot]$ are assumed to be zero-mean weakly stationary processes, jointly independent of the assumed zero-mean stationary process $(\tilde{g}_u * x_N)(kT)$, and $\mathbb{E}[\cdot]$ denotes expectation. This implies that the decomposition in (4) can be enforced, and the calibration error term made to vanish, by estimating h_1, \dots, h_N from the discrete-time sequences $s_0[\cdot], \dots, s_N[\cdot]$ alone. In particular, prior knowledge of any of the analog quantities $g_u(\cdot), g_1(\cdot), \dots, g_N(\cdot)$, and $\tilde{g}_u(\cdot)$ are immaterial for such calibration.

From here on, all filters $h_\ell[\cdot]$ are chosen as FIR filter with equal filter length $K = 512$. Additionally, the reference filter $h_0[\cdot]$ is determined by standard FIR filter design methods (-3 dB gain at bandwidth edge) and its coefficient scaled by $-R_{\kappa_0}/R_{\beta_1}$ while all other $h_\ell[\cdot]$ are initialized with all zero coefficients. These choices of filter length and filter shape are mainly motivated by simplicity and consistency of notation. Clearly, for a given application, better reference filter design choices could yield superior filtering performance at reduced complexity.

1) *Adaptive Filtering:* One way of estimating h_1, \dots, h_N from (9) is an adaptive filtering scheme as shown in Figure 2.

In this work, only frontend calibration, i.e., $u(\cdot) = 0$ during calibration, is considered. However, we conjecture that, a modified version of Figure 2 could transform the general content of this paper into a background calibration setting. Unfortunately, this falls outside the scope of this paper.

For the adaptive filter in Figure 2, variations of the least mean squares (LMS) or recursive least squares (RLS) algorithms [7] can directly be applied. An advantage of LMS algorithm is its low complexity as it only uses the gradient of (9), i.e., $2E[s_\ell[\cdot]\hat{u}[\cdot]]$, in its update rule where

$$s_\ell[k] \triangleq (s_\ell[k - K/2], \dots, s_\ell[k + K/2])^T \in \{\pm 1\}^K. \quad (10)$$

To decrease the number of calibration iterations, at the expense of additional computational and memory complexity, the RLS algorithm [7], [8] is a viable alternative. For simplicity, only the RLS algorithm was considered in this work. The RLS algorithm minimizes the cost function

$$\underset{\mathbf{h}}{\operatorname{argmin}} \sum_{k=0}^{K_i} \lambda^{K_i-k} |\hat{u}[k]|^2 + \lambda_i^K \delta \|\mathbf{h}^0\|_2^2, \quad (11)$$

for $0 < \lambda \leq 1$, and $\delta \geq 0$, which converge to (9) for $\lambda < 1$ and the number of calibration iterations $K_i \rightarrow \infty$. The algorithm proceeds recursively as

$$\boldsymbol{\alpha}_k = \mathbf{V}^{k-1} \mathbf{s}[k] \quad (12)$$

$$\mathbf{g}_k = \boldsymbol{\alpha}_k (\lambda + \mathbf{s}[k]^T \boldsymbol{\alpha}_k)^{-1} \quad (13)$$

$$\mathbf{V}^k = \frac{1}{\lambda} (\mathbf{V}^{k-1} - \mathbf{g}_k \boldsymbol{\alpha}_k^T) \quad (14)$$

$$\mathbf{h}^k = \mathbf{h}^{k-1} - \hat{u}[k] \mathbf{g}_k \quad (15)$$

where

$$\mathbf{s}[\cdot] \triangleq (\mathbf{s}_1[\cdot]^T, \dots, \mathbf{s}_N[\cdot]^T, 1)^T \in \{\pm 1\}^{K_\Sigma}, \quad (16)$$

$$\mathbf{h}[\cdot] \triangleq (h_1[\cdot]^T, \dots, h_N[\cdot]^T, \hat{u}_0)^T \in \mathbb{R}^{K_\Sigma}, \quad (17)$$

$K_\Sigma = NK + 1$, $\boldsymbol{\alpha}_k \in \mathbb{R}^{K_\Sigma}$, $\mathbf{g}_k \in \mathbb{R}^{K_\Sigma}$, and $\mathbf{V}^k \in \mathbb{R}^{K_\Sigma \times K_\Sigma}$ is a symmetric matrix. The regularization in (11) is enforced by initializing the matrix $\mathbf{V}^0 = \delta^{-1} \mathbf{I}_{K_\Sigma}$ where \mathbf{I}_{K_Σ} is the K_Σ -by- K_Σ identity matrix. Throughout this paper, $\lambda = 1.0 - 10^{-12}$ and $\delta = 0.01$ for all simulations.

IV. SIMULATION RESULTS

The circuit from Figure 1 is parameterized, in accordance with [6], for a nominal performance of 76.5 dB signal-to-noise ratio (SNR) at 10 MHz signal bandwidth and a system order of $N = 6$. Specifically, the time constants are chosen as follows: $R_{\alpha_\ell} C_\ell = 98.63$ ns, $R_{\beta_\ell} C_\ell = 10.30$ ns, $R_{\kappa_\ell} C_\ell = 4R_{\beta_\ell} C_\ell$, for every ℓ with the exceptions of $R_{\beta_1} C_1 = 2R_{\beta_{\ell \neq 1}} C_{\ell \neq 1}$. This results in a maximum input signal swing that is twice that of the maximum state swing and half that of the maximum control signal swing. The comparators in Figure 1 are clocked at $f_s = 194.7$ MHz resulting in an oversampling ratio (OSR) of approximately 10.

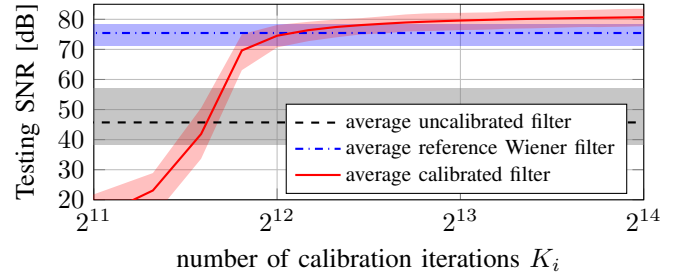


Fig. 3. The testing error performance for the uncalibrated and reference case as well as the RLS algorithm convergence behaviour as a function of the number of calibration iterations. The colored areas, associated with each case, represent the range of testing performance over all 128 sample circuits.

A. Behavioral Simulation

A component variation scenario is considered where all time constants $(R_{\kappa_0} C_1)$, $(R_{\alpha_\ell} C_\ell)$, $(R_{\beta_\ell} C_\ell)$, and $(R_{\kappa_\ell} C_\ell)$ are subject to variations from their nominal values. Ideal amplifiers, comparators, and passive components were modeled in Verilog-A, and using the Spectre simulator, 128 Monte Carlo simulations were conducted where each of the mentioned time constants are drawn independently and uniformly at random within $\pm 10\%$ of their nominal values. Every sample circuit is simulated with (testing) and without (training) a test sinusoidal input signal and the calibration is then conducted on the latter, and validated on the former, dataset. The test signal has a frequency of $f_s/2^8 \approx 760$ kHz and an amplitude of -1 dBFS to avoid potential instability due to the component variations. We use $R_{\kappa_1}/R_{\kappa_0} = 0.1$ and the Wiener filter from [3] (with η^2 chosen as (22) in [3]), with the true time constants, as a reference for the calibration results. Figure 3 shows the average testing performance for the uncalibrated Wiener filter (with nominal filter coefficients), the reference Wiener filter (using true filter coefficients), and the RLS algorithm's testing performance as a function of the number of calibration iterations. As stated in [6], without calibration, the digital estimator suffers significant performance degradation due to mismatch between the digital estimator and the, assumed nominal, analog frontend parametrization. Clearly, the mismatch can be managed as the RLS algorithm reaches the reference filter performance after $\approx 2^{12}$ iterations. The leapfrog structure is known for its resilience towards component variations, which is confirmed by the (average, maximum, minimum) SNR performance of (80.70, 83.51, 77.68) and (75.45, 78.38, 71.34) dB for the calibrated filter and reference Wiener filter respectively. Figure 4 shows the power spectral density (PSD), of (3), from a representative sample of the testing dataset. The discrepancy around the bandwidth frequencies, between the Wiener reference and the calibrated filter, is due to the $h_0[\cdot]$ being designed as standard FIR filter and not the Wiener filter from [3]. As the SNR is determined directly from the PSD, this also explains why the calibrated filter outperforms the reference filter in Figure 3.

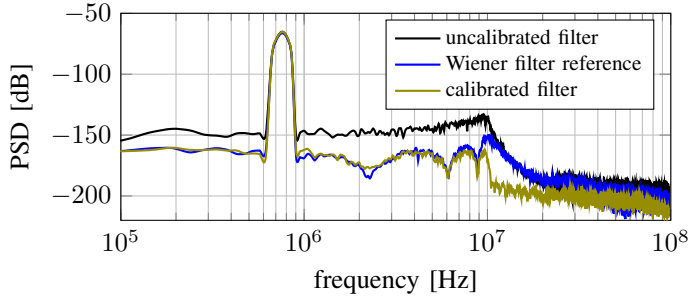


Fig. 4. A representative PSD of (3) from one of the realizations in Section IV-A.

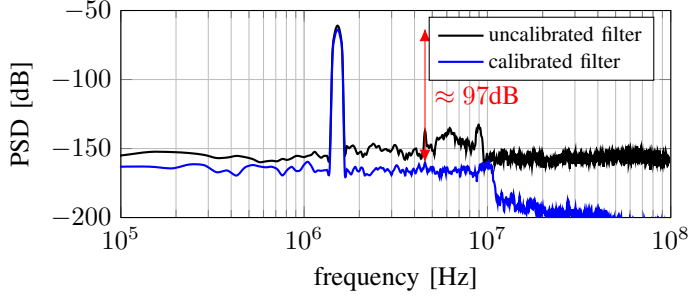


Fig. 5. Uncalibrated (61.7 dB SNDR) and calibrated (80.9 dB SNDR) PSDs of (3) from the transistor level simulation in Section IV-B. From the figure we also recognize a small non-linearity resulting in a SFDR of ≈ 91 dB.

B. Transistor Level Simulation

A transistor level implementation of Figure 1 was designed and simulated with Spectre in 65-nm CMOS technology. The specifics are as follows: 1.2 V power supply, $C_1 = 11.7$ pF, $C_2 = C_3 = 2.925$ pF, and $C_4 = C_5 = C_6 = 975$ fF, an input signal amplitude range of 600 mVpp and $R_{\kappa_1}/R_{\kappa_0} = 0.03$. The comparators have an input referred noise of $130 \mu\text{Vrms}$ which was achieved by extending the decision time to a quarter of the control period. Stability issues, due to the long decision time, were addressed by ternary comparators with decision thresholds at ± 50 mV. The ternary comparators result in a reduced maximum state swing, by approximately 30%, which translates into ≈ 3 dB SNR gain, see (4). The amplifiers are class AB two-stage RC-compensated amplifiers as in [9] with an simulated input-referred noise of $67.03 \mu\text{Vrms}$. They are non-uniformly downsized to somewhat match the diminishing thermal noise and linearity requirements. The approximate scaling can be seen from the resulting simulated power consumption as $P_{A_1} = 8.5$ mW, $P_{A_2} = P_{A_3} = 2.3$ mW, and $P_{A_4} = \dots = P_{A_6} = 0.9$ mW. In Figure 5, both the calibrated and uncalibrated PSDs of the estimate from (3) are shown for a FS input signal at $f_s/2^7 \approx 1.5$ MHz. A signal-to-noise-and-distortion ratio (SNDR) of 80.9 (calibrated) and 61.7 (uncalibrated) dB and a SFDR of ≈ 97 dB is estimated directly from the PSD. The implementation has a simulated total power consumption of 18.43 mW resulting in a predicted Schreier FoM of 168.24 dB and a Walden FoM of 101.6 fJ/conv.

V. CONCLUSIONS

Both theoretical and practical aspects of calibrating CBADCs were addressed. The proposed calibration algorithm was validated using both behavioral and transistor level simulations, confirming recovery of essentially nominal performance. The introduction of calibration to the CBADC concept splits the CBADC design task into two disjoint parts: an analog front-end where the fundamental performance follows from analog design parameters and a digital calibration step that is agnostic to the analog implementation.

APPENDIX

A. The Signal Estimate Decomposition

The discrete-time convolution can be written as

$$\begin{aligned} (\check{h}_\ell * s_\ell)[k] &\triangleq \sum_{k_1} s_\ell[k_1] \check{h}_\ell[k - k_1] \end{aligned} \quad (18)$$

$$= \sum_{k_1} s_\ell[k_1] (\tilde{g}_u * g_\ell * \theta_\ell)((k - k_1)T) \quad (19)$$

$$= \int (\tilde{g}_u * g_\ell)(\tau) \sum_{k_1} s_\ell[k_1] \theta_\ell(kT - \tau - k_1T) d\tau \quad (20)$$

$$= \int (\tilde{g}_u * g_\ell)(\tau) s_\ell(kT - \tau) d\tau \quad (21)$$

$$= (\tilde{g}_u * g_\ell * s_\ell)(kT) \quad (22)$$

where the steps to (19) and (21) follows from the definitions in (7) and (1) respectively. Additionally,

$$\begin{aligned} (\tilde{g}_u * g_0 * s_0)(kT) &= (\tilde{g}_u * (x_N - (g_u * u)))(kT) - \sum_{\ell=1}^N (\check{h}_\ell * s_\ell)[k] \end{aligned} \quad (23)$$

where (23) follows from (2) and reversing the steps in (18)-(22) for $(\tilde{g}_u * g_\ell * s_\ell)(kT)$. Replacing $(h_0 * s_0)[k]$ with (23) in (3) and rearranging results in (4).

B. The Wiener Filter

Assuming $\hat{s}[\cdot] \triangleq (h_0 * s_0)[\cdot]$, $\mathbf{s}[\cdot]$, and $w[k] \triangleq -(\tilde{g}_u * x_N)(kT)$ to be zero-mean weakly stationary processes and $w[\cdot]$ to be jointly independent of $\mathbf{s}[\cdot]$, the minimizing solution to the cost function in (9), i.e., minimizing $\mathbb{E}[\|\hat{s}[\cdot] + (\mathbf{h}^T * \mathbf{s})[\cdot]\|^2]$, with respect to $\mathbf{h}[\cdot]$, see (16) and (17), follows by the orthogonality principle as

$$(\mathbf{h}^T * \mathbf{R}_s)[\cdot] = \mathbf{R}_{\hat{s}s}[\cdot], \quad (24)$$

where $\mathbf{R}_s[\cdot] \triangleq \mathbb{E}[(\mathbf{s} * \mathbf{s}^T)[\cdot]]$ and $\mathbf{s}_c[\cdot] \triangleq \mathbf{s}[-\cdot]$. Convolving both the left hand and right hand side of (2) with $\tilde{g}_u(t)$, enforcing $u(t) = 0$, reversing the steps from (18)-(22), and finally rearranging, gives $\hat{s}[\cdot] = (\mathbf{g}^T * \mathbf{s})[\cdot] + w[\cdot]$ where $\mathbf{g}[k] \triangleq ((\tilde{g}_u * g_1 * \theta_1)(kT), \dots, (\tilde{g}_u * g_N * \theta_N)(kT))^T$. Subsequently,

$$\mathbf{R}_{\hat{s}s}[\cdot] \triangleq \mathbb{E}[(\hat{s} * \mathbf{s}^T)[\cdot]] = (\mathbf{g}^T * \mathbf{R}_s)[\cdot] \quad (25)$$

and plugging (25) into (24), and assuming a full rank \mathbf{R}_s , results in $h_\ell[\cdot]$ as given by $\check{h}_\ell[\cdot]$ in (8).

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