SURNAME, NAME:	**GROUP:**

Question 1 (2.5 points; 20 minutes)

a) Obtain the representation of $A=265_{10}$ in the following digital systems:

Binary	100001001_2
Octal	411_8
Hexadecimal	109_{16}

0'75p

b) Given the number $B = 100000110_{CA2}$ represented in *2's-complement,* obtain the decimal representation.

$B = 100000110_{CA2}$

$= -1 \cdot 2^8 + 1 \cdot 2^2 + 1 \cdot 2^1 = -250$

0'75p

c) Perform the following operations using 2's complement representations: B-A. Explain if there is overflow in the operation.

$B = -250$

$A = +265 \rightarrow -A = 10111110111_{CA2}$

$B - A = -250 - (+265) = -515$

1p

CA2 (10 bits) $\begin{cases} -512 \\ +511 \end{cases}$

10 bits.

overflow

$$\begin{array}{r} 1100000110 \\ +\ 1011110111 \\ \hline 0111111101 \end{array}$$

positive

SURNAME, NAME:	**GROUP:**

Question 2 (2.5 points; 20 minutes)

Generate a circuit, with 4 inputs and 1 output, to detect the 5 least significant numbers of your DNI, without repetitions[1]. This circuit should also take into account the letter of the Document, if between A and L it should also detect the numbers 11 (0xB) and 13 (0xD) and if from M to Z the numbers to be included will be 12 (0xC) and 14 (0xE).

As an example, if your DNI were 40985665R, then the numbers to be detected are: 5, 6, 8, 9, 0, C and E.

a) Generate the truth table

a	b	c	d	Z

[1] If your DNI does not include 5 different numbers then use the ones it has.

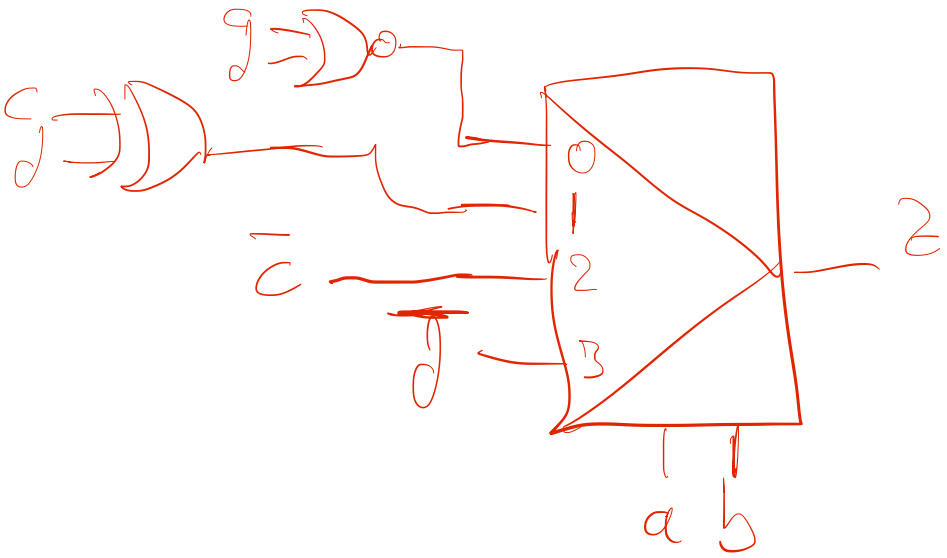
b) Write down the output Z in terms of MinTerms and MaxTerms

$\Sigma(0,5,6,8,9,12,14)$

$\Pi(1,2,3,4,7,10,11,13,15)$

0'75 p

c) Implement the circuit with 1 Mux of 2 control inputs plus the logic gates you consider



1 p

SURNAME, NAME:	**GROUP:**

Question 3 (3 points; 30 minutes)

Given the following VHDL code:

```
ARCHITECTURE first_partial OF exam IS
-- Signal declaration
signal s: std_logic_vector (1 downto 0);
signal e: std_logic;
signal f: std_logic_vector (3 downto 0);
BEGIN

s<=a&b;

PROCESS( s,c,d,a    )
BEGIN
CASE s IS
           WHEN "00" =>     e <= '0';
           WHEN "01" =>     e <= '1';
           WHEN "10" =>     e <= c xor d;
           WHEN OTHERS => e <= d AND a;
           END CASE;
END PROCESS;

PROCESS( a,b,e,s    )
BEGIN
f(0)<=a OR b;
f(1)<=e;
f(3 downto 2)<=s;
END PROCESS;


y <=  "11" WHEN f(3) = '1' ELSE
      "10" WHEN f(2) = '1' ELSE
      "01" WHEN f(1) = '1' ELSE
      "00";
      eo <= '1' WHEN f = "0000" ELSE '0';

END first_partial;
```

MUX

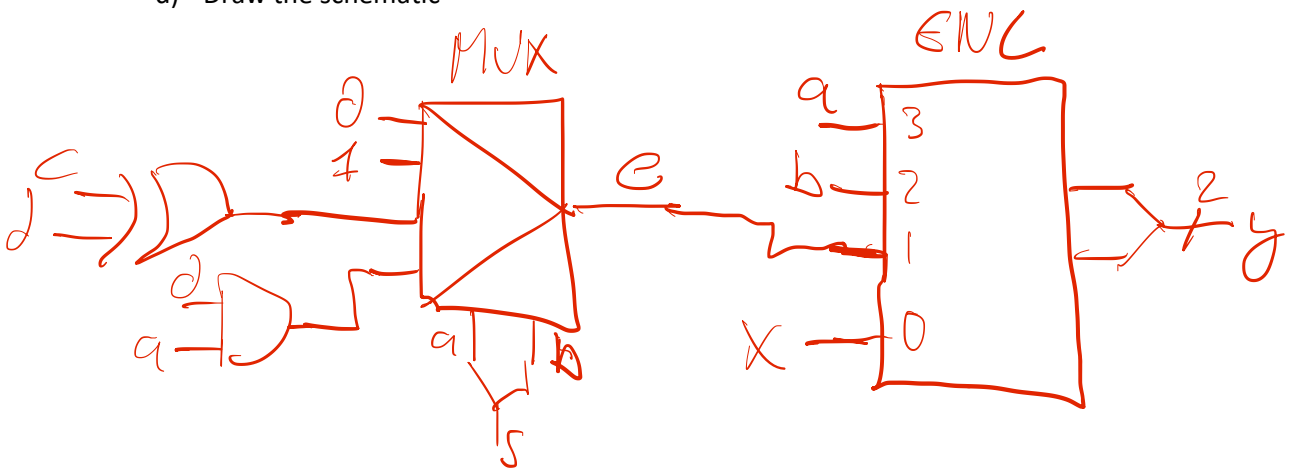
ENC

a) Describe the entity of this circuit

```
entity exam is
port(a,b,c,d: IN std_logic;
     eo: OUT std_logic;
     y: OUT std_logic_vector(1 downto 0));
end exam;
```

0'5p

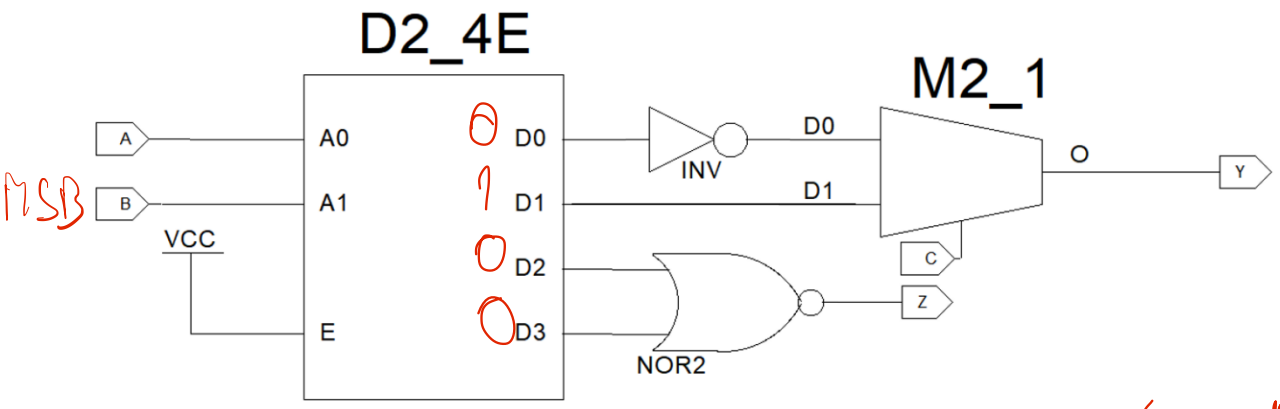
b) Declare the necessary signals (in the code) 0'75
c) Fill the sensitivity lists (in the code) 0'75
d) Draw the schematic



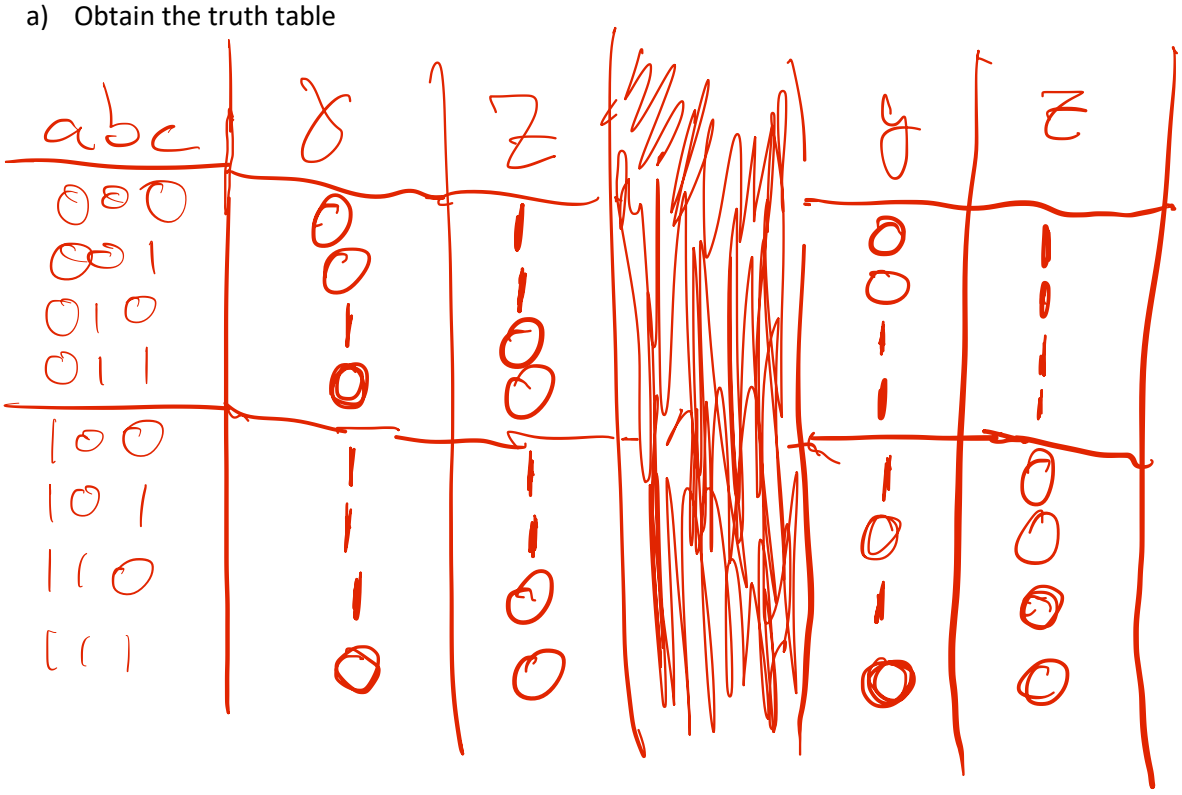
1p

Question 4 (2 points; 20 minutes)

Given the following circuit:



a) Obtain the truth table



b) Describe the architecture for this circuit in VHDL.

```
architecture f of q4 is

begin
  z <= Not b;

process (a,b,c)
  begin
    if a='0' then
      y <= b and Not c;

    else
      y <= b nand c;
    end if
end process;
```

1p