SURNAMES, NAME: **GROUP:**

Problem 1 (20 minutes – 2 points)

a) (50%) Complete the next table with the representation of the numbers considering the different systems/codes using 8 bits:

	A	**B**
Decimal		
Natural binary		
Hexadecimal		
BCD		
OCTAL	**+73**	
2s-Complement		**10001101**

b) (50%) Using **A** and **B** of (a), perform the followings operations in 2s-complement (8bits). Indicate whether there is overflow or not and why. In case there is overflow, indicate what would be the correct result:

A+B

A-B

-A+B

SURNAMES, NAME: **GROUP:**

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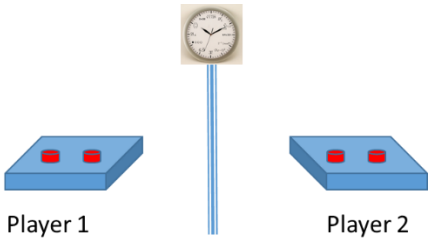
Problem 2 (30 minutes – 4 points)

Implement an electronic version of the game where 2 players can push 0, 1 or 2 buttons at a given and synchronised moment. If the sum of these is even[1], then player 1 wins (Output=0), if odd winner is player 2 (Output=1). **(4 points)**



a) Fill in the truth table **(1.2 points)**

Player1_1	Player1_2	Player2_1	Player2_2	Z
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

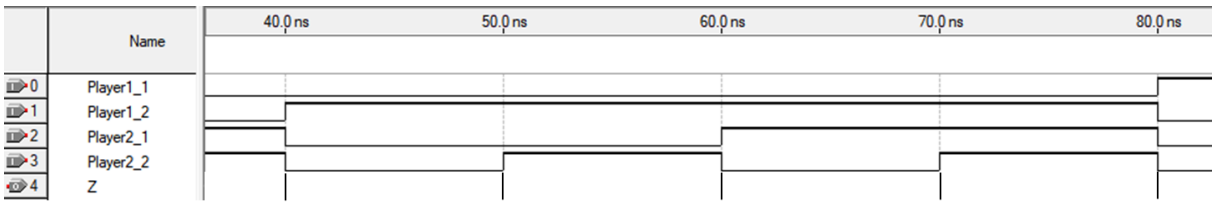
b) Write down the output Z using the first canonical form. Specifically, the complete numerical form and the first 3 terms. **(0.3 points)**

[1] Consider 0 as Even

SURNAMES, NAME: **GROUP:**

c) Implement a valid VHDL architecture for this circuit. **(1.5 points)**

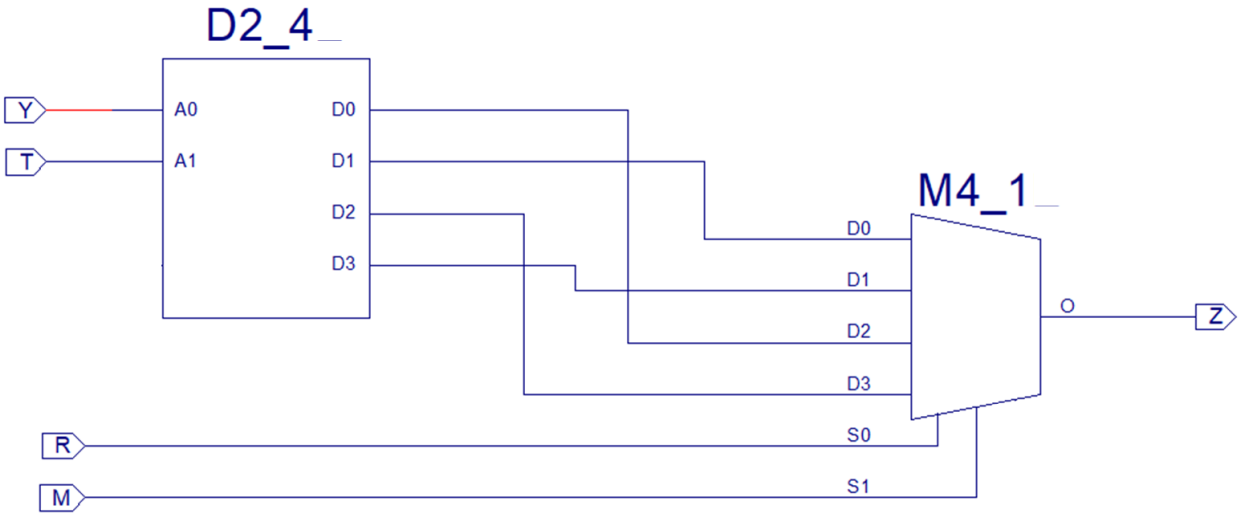
d) Complete the simulation report shown below, adding the expected values of the output signal for the time interval between 40 and 80 ns **(1 point)**



SURNAMES, NAME: **GROUP:**

Problem 3 (30 minutes – 4 points)

Given the following circuit, where the D2_4 is a 2 to 4 decoder and the M4_1 is a 4 to 1 multiplexer **(4 points)**



a) Fill in the truth table, adding names of inputs in the way you consider as more appropriate **(1.5 points)**

				Z
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

SURNAMES, NAME: **GROUP:**

b) Write down the output Z using the second canonical form. Specifically, the complete numerical form and the first 3 terms. **(0.5 points)**

c) Define the entity of this circuit **(0.7 points)**

d) Write down a valid VHDL implementation for this circuit using processes. If you use intermediate signals to define this architecture add them also in the schematic you have **(1.3 points)**