IMPORTANT:

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Time: 3h

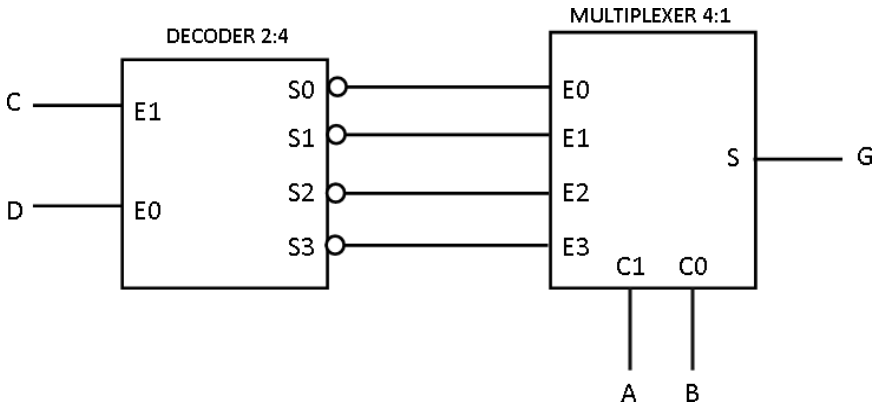
<u>Problem 1</u> (2.5 pts)

Given the function F,

$$F(a,b,c,d) = \sum_{4}(0,3,4,5,6,8,11,12,14)$$

a) Obtain the simplified logical expression F in terms of product of sums (POS).
b) Realize the function F only using a 4:1 MUX and the least number of possible logic gates.

Given the circuit in the figure,



c) Obtain the truth table for output function G and inputs A, B, C, D. Consider A is the most significant variable and D is the least significant variable.
d) Obtain the simplified logical expression of output G in terms of sum of products (SOP).
e) Implement the function G using the least number of possible logic gates.

Problem 2 (2.5 pts)

We want to design the control system for filling a storage tank which gets water supply from an underground stream through a submersible pump.
The system has two inputs:
• **M**, a signal coming from a sensor installed in the tank, which is activated when the water level in the tank is above its maximum level and is disabled otherwise.
• **m**, a signal coming from a 2nd sensor installed in the tank, which is activated when the water level in the tank is above the minimum level and turns off otherwise.

The system has two outputs:
- **B**, a signal that handles switching on/off engine of the water-pump.
- **A**, a fault-signal which is activated when the information provided by the level sensors is inconsistent, i.e. the maximum level sensor is active and the minimum level sensor inactive.

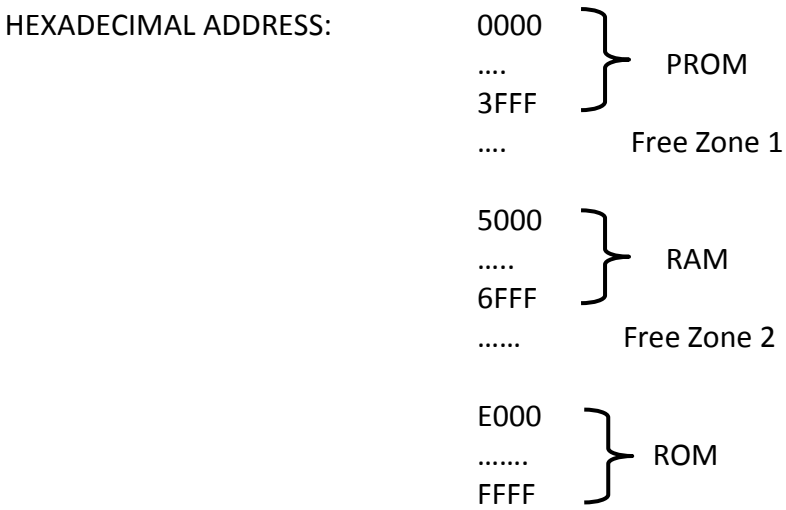
The water-pump ensures that the water-tank level is always between the maximum and minimum levels: it has to start-up when the water level goes below the minimum level and it has to stop when the water level rises above the maximum level. In case of any fault, the pump must remain stopped.

It is asked:
Design a Moore FSM that implements this system. Use rising-edge triggered synchronous D flip-flops. Answer the following questions with justification:

a) Obtain the state-transition diagram.
b) Determine the number of flip-flops and coding assigned to the states.
c) Get the transition table of the states and the outputs.
d) Obtain the simplified algebraic expressions of the state functions and the outputs.
e) Get the complete scheme of the automated circuit. Also, add an initialization asynchronous signal **I**. A value of "0" in this signal will drive the circuit into a state in which the two outputs remain deactivated.

Problem 3 (3.0 pts)

Using memory circuits, PROM of 16kx4, RAM of 4kx8 and ROM of 8kx8, we want to configure the following memory map (8-bit data).



Obtain:

a) Number of positions of the memory zones
b) Number of positions of the free zones.
c) Necessary memories (the available ones) to implement the memory zones.
d) Equations of activation of each memory chip, considering that control inputs of the memories are active low.
e) Implement using a decoder with three inputs, outputs (active low) and necessary logic gates.

NAME: **GROUP:**

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Problem 4 (2.0 pts)

Answer to the following questions, circling the correct answer. If you make a mistake, correct it so that the answer is clear and not ambiguous, or it will be considered as 'incorrect'.

The score in this question will be proportional to:

Number of correct answers – (Number of wrong answers)/3

(Unanswered questions will not be taken into account)

1. Data-path is:
   a) A set of combinational functional units that process data.
   b) A set of functional units processing sequential data.
   c) A set of functional units, both combinational and sequential data processing.
   d) None of the above.

2. What component does not belong to a data-path structure?
   a) ALU (arithmetic logic unit).
   b) Buses.
   c) Registers.
   d) instruction decoder.

3. The control unit:
   a) Co-ordinates the behaviour of external peripherals ensuring the correct sequence of operations.
   b) Co-ordinates the behaviour of internal peripherals ensuring the correct sequence of operations.
   c) Co-ordinates the behaviour of the data path providing timing and control signals to ensure the correct sequence of operations.
   d) None of the above.

4. Which element does not belong to a control unit?
   a) FSMs (finite state machines).
   b) Registers.
   c) ALU.
   d) None of the above.

5. The control unit:
   a) Is a part of a microprocessor.
   b) Is not a part of a microprocessor.
   c) Has an inner and outer part to the microprocessor.
   d) None of the above.

6. An ASIC (application specific integrated circuit):
   a) Is an integrated circuit designed and developed to meet a specific application, such as a control circuit in a mobile phone.
   b) Is an integrated circuit based on programmable logic.
   c) Both of the above are true.
   d) The first two are not true.

7. A CPLD (complex programmable logic device):
   a) is an integrated circuit that can be configured to implement only combinational digital devices.
   b) is an integrated circuit that can be configured to implement only sequential digital devices.
   c) is an integrated circuit that can be configured to implement combinational and sequential digital devices.
   d) None of the above.

8. What element forms part of a microprocessor:
   a) Instruction Decoder.
   b) Program Counter (PC).
   c) Instruction register (IR).
   d) All of the above.

9. An instruction cycle of a microprocessor:
   a) can be processed at a stage: instruction decoding, properly configuring data path.
   b) can be processed in two stages: instruction loading in the IR and instruction decoding, properly configuring data path.
   c) can be processed in three stages: instruction loading in the IR, the instruction decoding, and initialization of the program counter (PC).
   d) None of the above.

10. A jump and bifurcation instruction:
    a) Modifies the PC (program counter).
    b) Modifies the PC and the lowest memory address.
    c) Modifies the IR and highest memory address.
    d) None of the above.

11. A data-transfer instruction:
    a) can transfer data between registers.
    b) only transfers data between two partitions of a hard disk.
    c) is used to encrypt data to be transferred.
    d) None of the above.

12. An arithmetic-logic instruction:
    a) Performs operations with the ALU.
    b) Performs only AND, OR and NOT operations.
    c) Performs only 'summation' operation in 2's complement.
    d) None of the above.

13. The operands of an instruction:
    a) Indicate data which applies an operation code (opcode).
    b) Indicate data that applies only arithmetic operations.
    c) Indicate data that applies only logical operations.
    d) None of the above.

14. The assembly language of a microprocessor:
    a) Allows high-level programming on known microprocessor architecture.
    b) Allows low-level programming on known microprocessor architecture.
    c) Allows low-level programming without knowing the architecture of a microprocessor.
    d) Allows programming of a microprocessor without knowing its architecture.