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Problem 1 (2,5 puntos)

A 4-bit data package **(D)** is transmitted on a telecommunication channel. We want to design a combinational circuit that implements the following functionality:

- Output **Parity (1 bit)**. Compute the odd-parity bit of the transmitted data.
- Output **Difference (multiple bits)**. Compute using 2s-complement the difference between the number of 0's and 1's (0's -1's) of the 4-bit transmitted.

a) Describe using VHDL the entity of the circuit. Explain the election of the data type and how this election will affect the architecture.

```
ENTITY Problem_1 IS
PORT(
D: IN STD_LOGIC_VECTOR (3 downto 0);          --4 bit input (must be converted to signed/unsigned to use arithmetic operations
Parity: OUT STD_LOGIC;                        -- 1-bit the result of the XOR/XNOR of the different bits of D
Difference: OUT STD_LOGIC_VECTOR (3 downto 0) -- 4 bit output necessary to represent numbers from +4 to -4
);
END Problem 1;
```

b) Truth Table of the system.

D3	D2	D1	D0	Parity	Difference3	Difference2	Difference1	Difference0	DEC
0	0	0	0	1	0	1	0	0	+4
0	0	0	1	0	0	0	1	0	+2
0	0	1	0	0	0	0	1	0	+2
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	0	0	1	0	+2
0	1	0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	1	0	-2
1	0	0	0	0	0	0	1	0	+2
1	0	0	1	1	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	1	1	1	0	-2
1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	1	1	0	-2
1	1	1	0	0	1	1	1	0	-2
1	1	1	1	1	1	1	0	0	-4

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Problem 2 (4 puntos)

a) Obtain the equivalent schematic for the following VHDL code.

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3
4  ENTITY exam IS
5      PORT
6      (
7          A :  IN  STD_LOGIC_VECTOR (1 downto 0);
8          B :  IN  STD_LOGIC_VECTOR (1 downto 0);
9          Y :  OUT  STD_LOGIC;
10         Z :  OUT  STD_LOGIC
11     );
12 END exam;
13
14 ARCHITECTURE bdf_type OF exam IS
15
16 SIGNAL AUX1,AUX3: STD_LOGIC;
17 SIGNAL S,AUX2:STD_LOGIC_VECTOR (1 downto 0);
18
19 BEGIN
20
21 S<=A(1)& B(1);
22 AUX1<=A(0) AND B(0);
23
24 PROCESS (S,AUX1,AUX2)
25 BEGIN
26 CASE S IS
27 WHEN "00" => z <= AUX1;
28 WHEN "01" => z <= AUX2(0);
29 WHEN "10" => z <= AUX2(1);
30 WHEN OTHERS => z <= S(0);
31 END CASE;
32 END PROCESS;
33
34
35
36 AUX2 <= "11" WHEN B(1) = '1' ELSE
37 "10" WHEN B(0) = '1' ELSE
38 "01" WHEN A(1) = '1' ELSE
39 "00";
40 AUX3 <= '1' WHEN A = "00" AND B = "00"  ELSE
41 '0';
42
43 Y<=AUX3;
44
45 END bdf_type;
```

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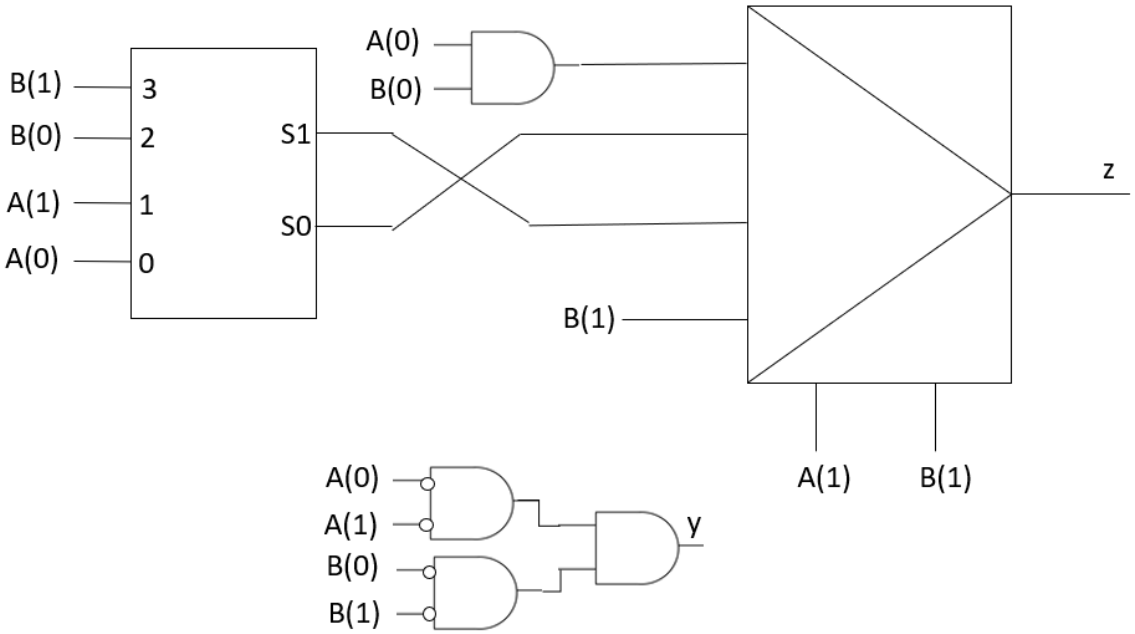
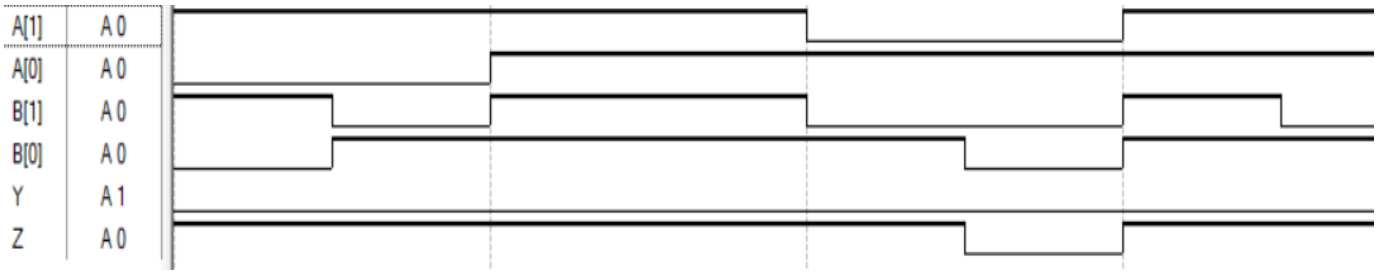
b) Draw the values of Z and Y in the following chronogram.





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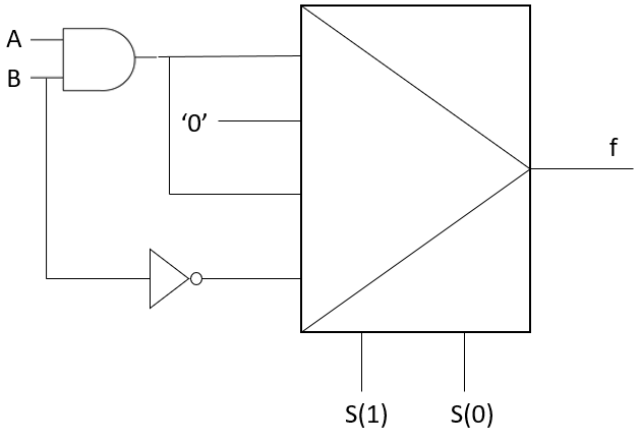
Problema 3(2 puntos)

Write a VHDL process that implements the functionality of the following schematic:




```
PROCESS (S,A,B)
BEGIN
CASE S IS
WHEN "00" => f <= A AND B;
WHEN "01" => f <= '0';
WHEN "10" => f <= A AND B;
WHEN OTHERS => f <= NOT B;
END CASE;
END PROCESS;
```

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Problema 4(1,5 puntos)

1) The binary representation of the decimal number 37,3125
   a) 100101,0101
   b) 101001,0101
   c) 100101,0110
   d) 101001,0110
2) Given the following numbers represented in CA2, A= 11000011 y B=01101100 determine their decimal value.
   A= - 61 B= +108

   Perform the following operations. There is overflow for the following operations? Why?

   A+B =00101111 (+47) Overflow - YES - NO

   A-B = 01010111 (Wrong) Overflow - YES - NO

   Why? Using 8 bits, In two's complement we can represent number from:

   -2^7 <->+ 2^7 -1 → -128 - +127

3) Fill the sensitivity list for the following process:

```
PROCESS ( A,B,C )
        BEGIN
        X<= A OR B;
        IF X='1' then
            Y<='0';
        ELSE
            Y<='1';
        END IF;
        Z<= Y NAND C;
END PROCESS;
```