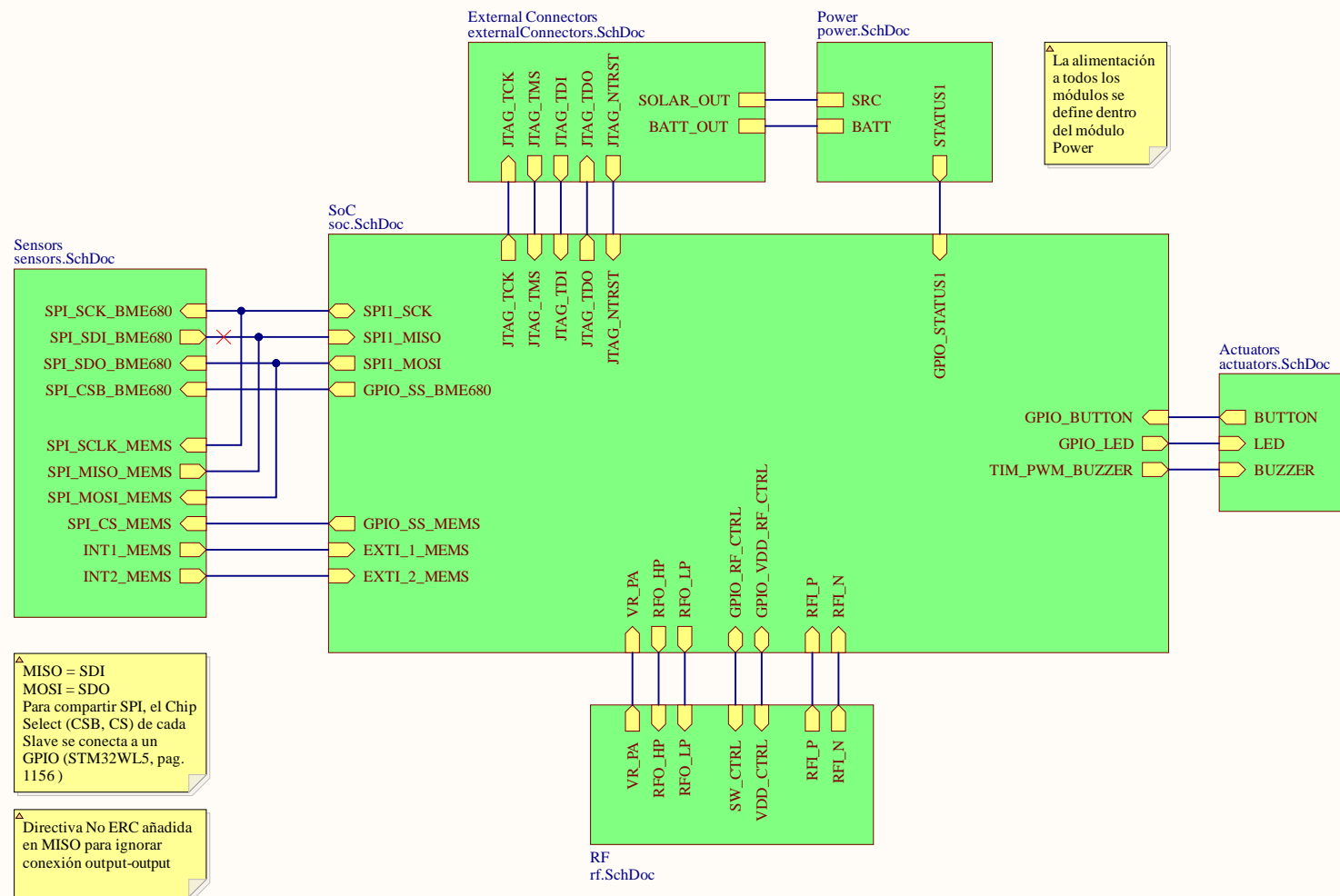


Hefesto

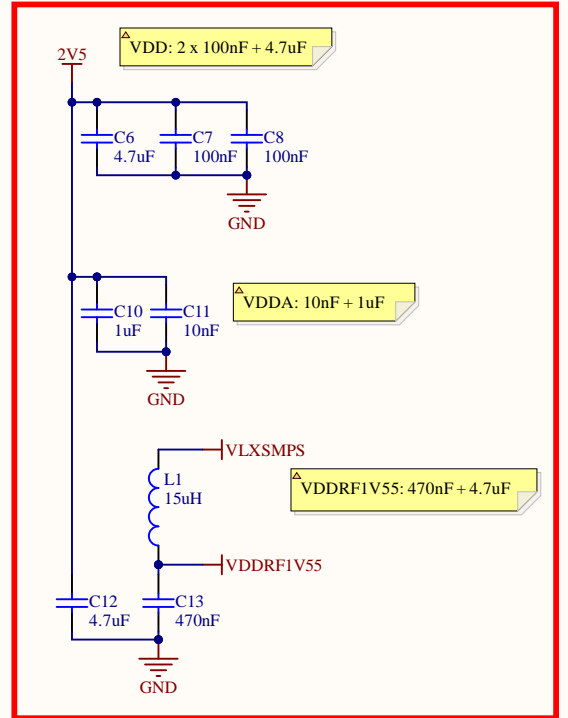
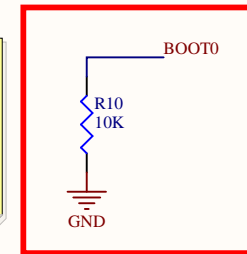
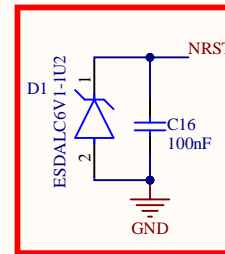
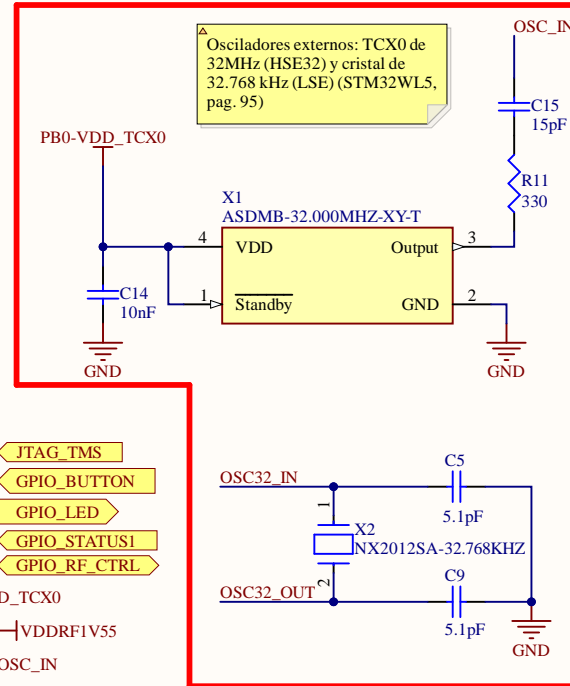
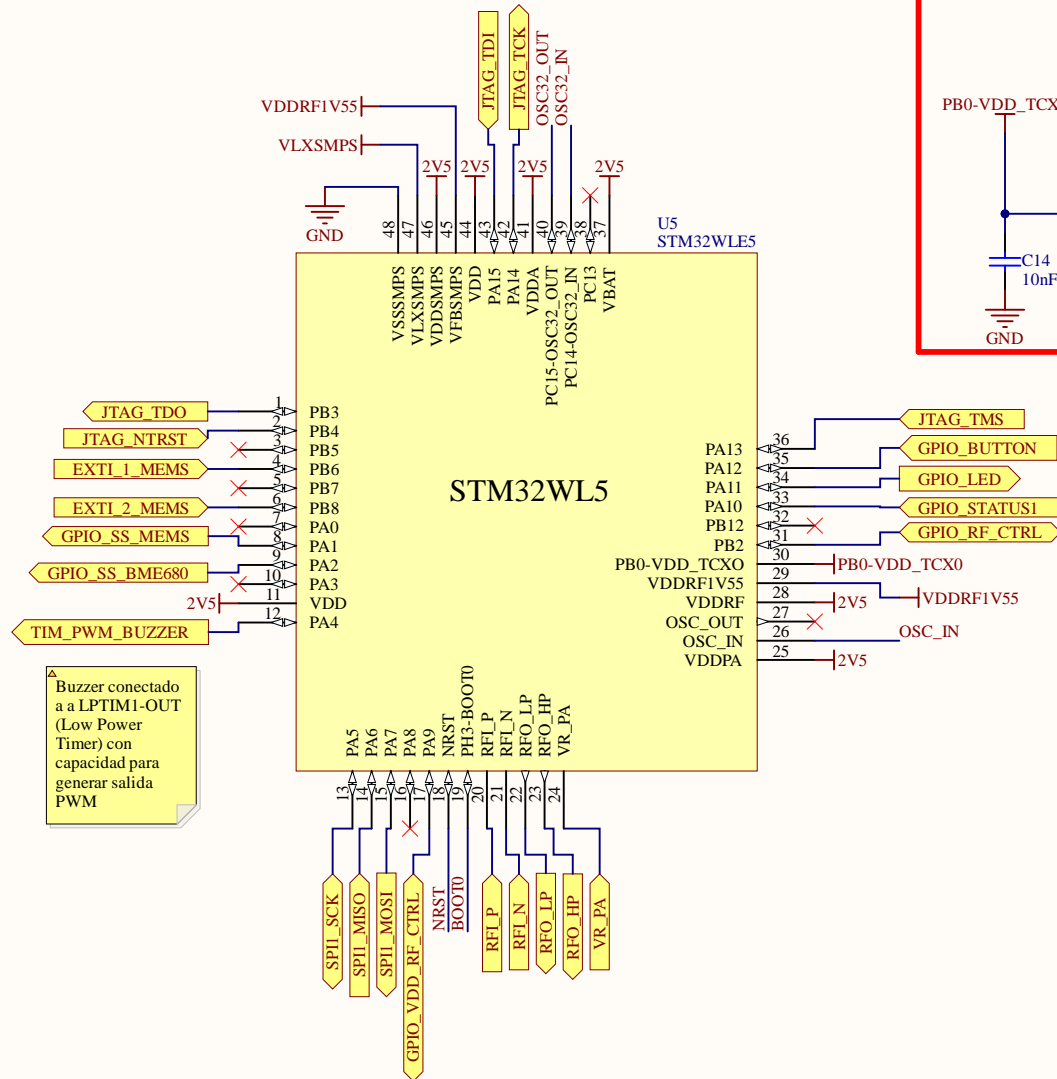




MISO = SDI
MOSI = SDO
Para compartir SPI, el Chip Select (CSB, CS) de cada Slave se conecta a un GPIO (STM32WL5, pag. 1156)

Directiva No ERC añadida en MISO para ignorar conexión output-output

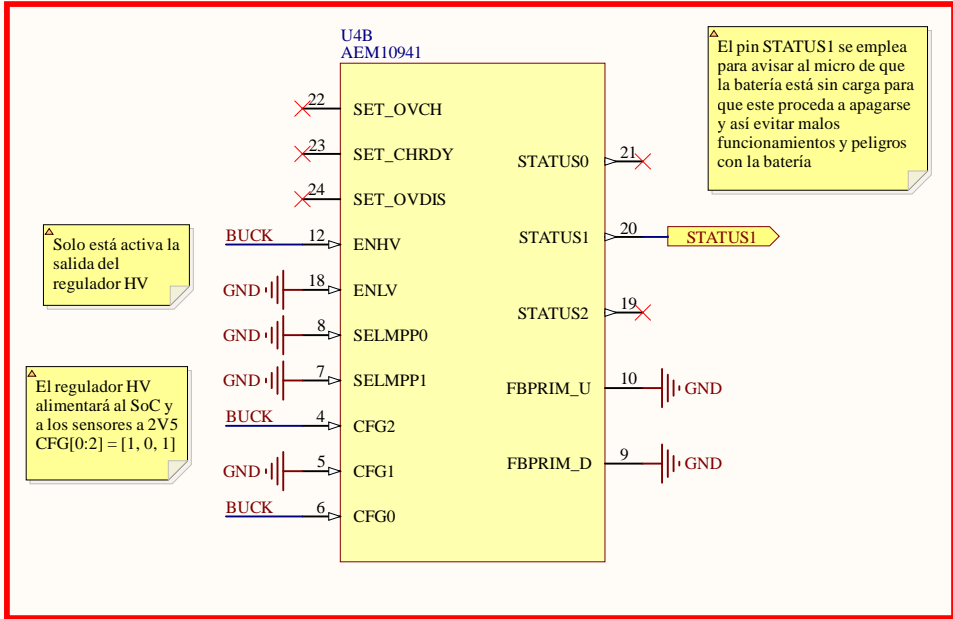
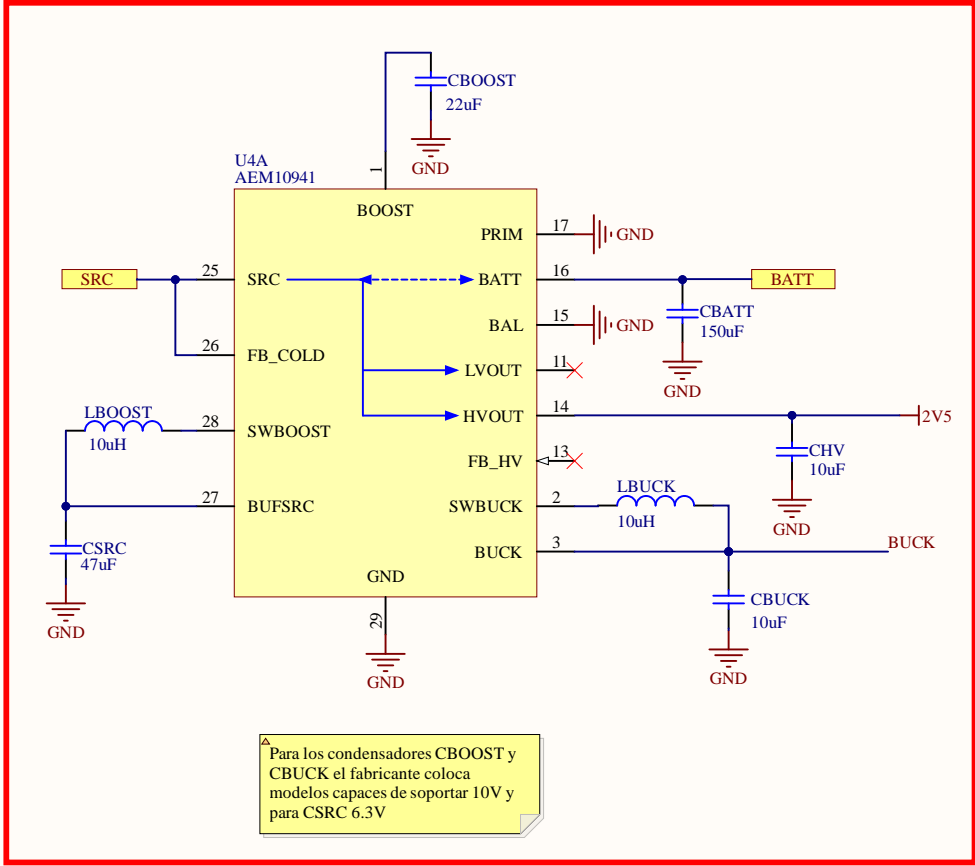
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Size: A4	Number: 1	Revision: v1.0		
Date: 26/03/2023	Time: 17:19:47	Sheet 1 of 7		
License:				
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File: C:\Users\Public\Documents\Altium\projecto_DEOP\main.SchDoc				


SoC



Title: Hefesto				ETSIT	 
Page Contents: soc.SchDoc					
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Date: 26/03/2023	Time: 17:19:47	Sheet 2 of 7			
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Power



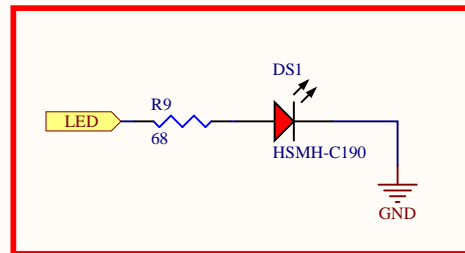
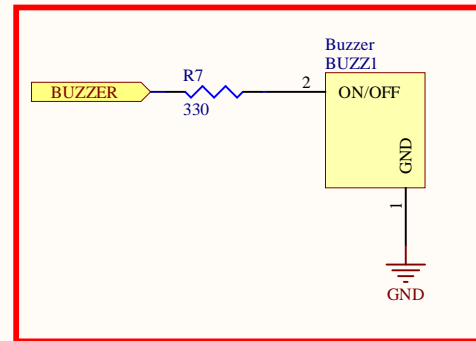
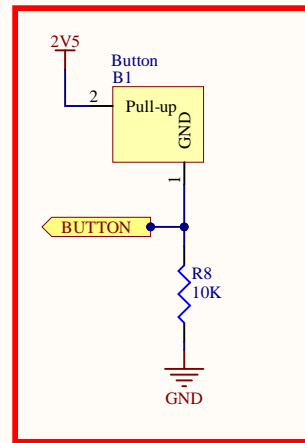
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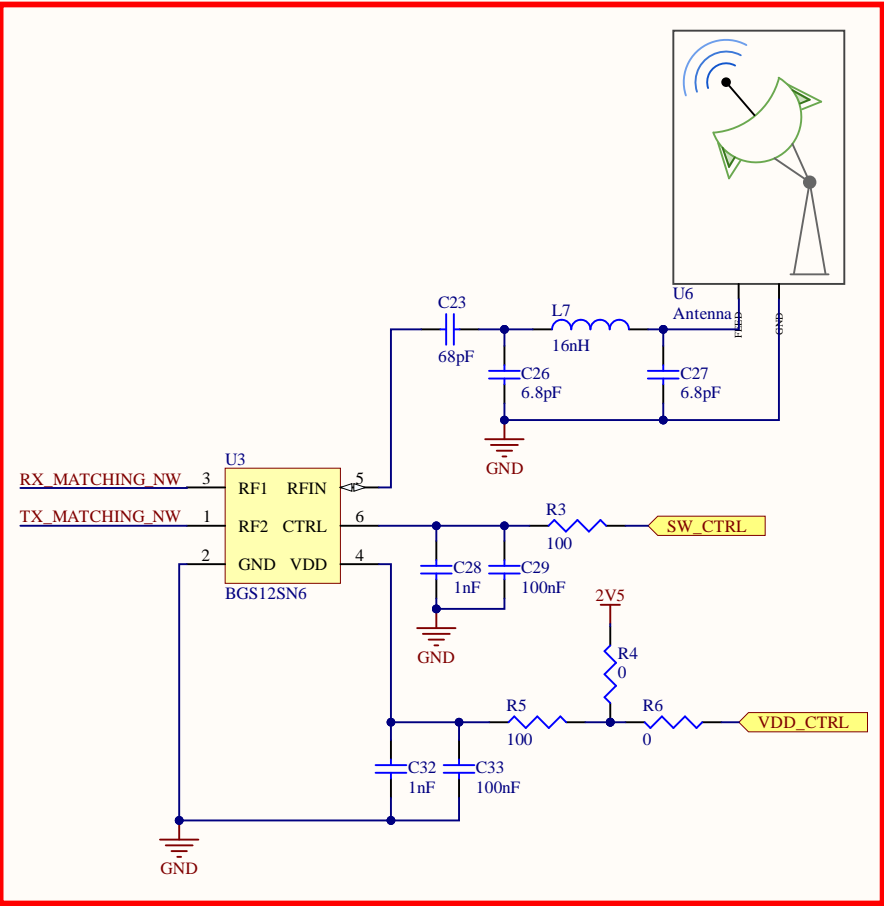
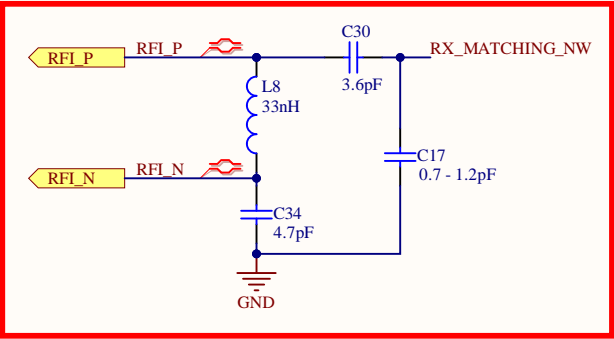
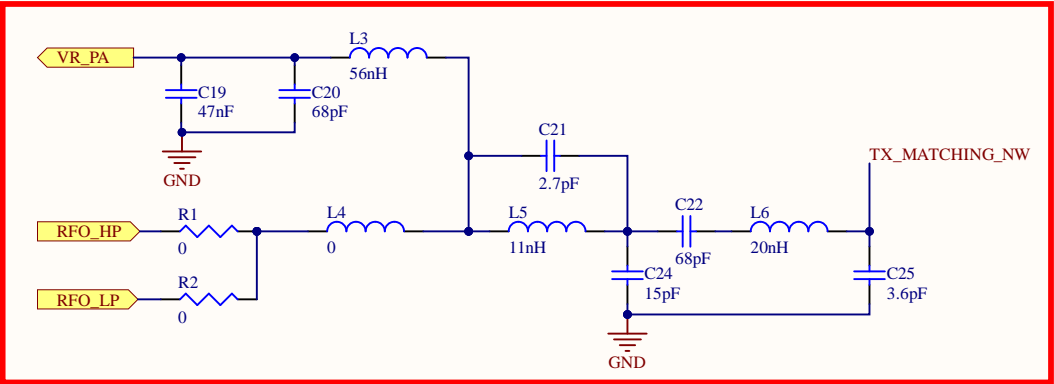
Actuators



Title: Hefesto				 
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Drawn By: David, Andrea		Checked By: None		
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RF



Title: **Hefesto**

Page Contents: **rf.SchDoc**

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Size: **A4**

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Revision: **v1.0**

Date: **26/03/2023**

Time: **17:19:48**

Sheet **6** of **7**

License:

Email: **#NAME?**

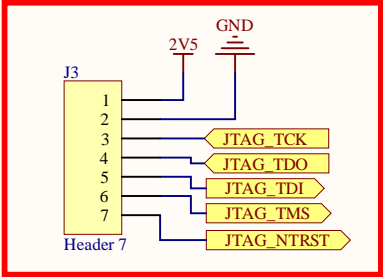
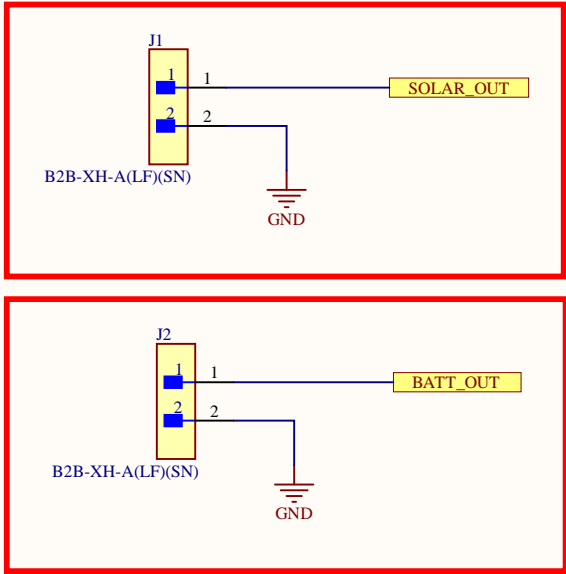
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POLITÉCNICA

External Connectors



Title: Hefesto				
Page Contents: externalConnectors.SchDoc			<i>ETSIT</i>	
Drawn By: David, Andrea		Checked By: None		
Size: A4	Number: 7	Revision: v1.0		
Date: 26/03/2023	Time: 17:19:48	Sheet 7 of 7		
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