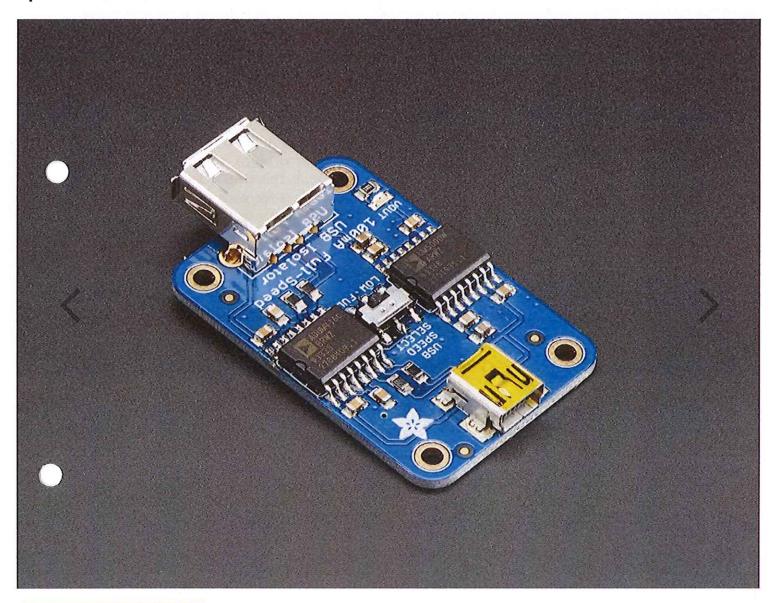
BREAKOUT BOARDS / OTHER

Adafruit USB Isolator - 100mA Isolated Low/Full Speed USB

PRODUCT ID: 2107

\$34.95



1

ADD TO CART

QTY DISCOUNT
1-9 \$34.95
10-99 \$31.46
100+ \$27.96

99 IN STOCK

ADD TO WISHLIST

DESCRIPTION

Have some USB logic analyzer, multimeter or oscilloscope and bumping up against the frustation of a shared earth ground? The Offspring (known for being electrical engineers) wisely sang "Ya gotta keep'em isolated!" Power and signal isolation improves common-mode voltage, enhances noise rejection, and permits two circuits to operate at different voltage levels.

This handy little low-cost USB isolator is exactly what you need to provide protection against harmful noise, ground loops, surges, and spikes. Works with any 1.5Mbps (low speed) or 12Mbps (full speed) USB device. Not for high speed USB devices, often used for video cameras (check your product to make sure its low/full compatible) Based on Analog Device's USB isolators

It is particularly useful when paired with USB testing instruments, you need to separate or isolate your eath ground (thru the USB connector to the computer to the power plug) from your circuit for high voltage, accident-protection, or floating ground needs. Best of all, this USB isolator even has its own isolated 5V power supply that can supply 100mA, making it perfect for your BitScope Micro USB! Protect your computer or laptop, use one of these in between your ports.

New Products 4/1/2015			

TECHNICAL DETAILS

+

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Full/Low Speed 5 kV USB Digital Isolator

Data Sheet

ADuM4160

FEATURES

USB 2.0 compatible Low and full speed data rate: 1.5 Mbps and 12 Mbps Bidirectional communication $4.5 \text{ V to } 5.5 \text{ V V}_{\text{BUS}}$ operation

7 mA maximum upstream supply current @ 1.5 Mbps
8 mA maximum upstream supply current @ 12 Mbps

2.3 mA maximum upstream idle current

Upstream short-circuit protection

Class 3A contact ESD performance per ANSI/ESD STM5.1-2007

High temperature operation: 105°C

High common-mode transient immunity: >25 kV/µs

16-lead SOIC wide-body package version

16-lead SOIC wide body enhanced creepage version

RoHS compliant

Safety and regulatory approvals (RI-16 package)

UL recognition: 5000 V rms for 1 minute per

UL 1577

CSA Component Acceptance Notice #5A

IEC 60601-1: 250 V rms (reinforced)

IEC 60950-1: 400 V rms (reinforced)

VDE Certificate of Conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

V_{IORM} = 846 V peak

APPLICATIONS

USB peripheral isolation Isolated USB hub Medical applications

GENERAL DESCRIPTION

The ADuM4160¹ is a USB port isolator, based on Analog Devices, Inc., iCoupler* technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics and are easily integrated with low and full speed USB-compatible peripheral devices.

FUNCTIONAL BLOCK DIAGRAM V_{BUS1} 1 REG REG (16) VBUS2 GND₁ (2) (15) GND₂ 14) V_{DD2} VDD1 PDEN (13) SPD SPU (S PIN (1) DD-UD+ (10) DD+ 9 GND₂ GND₁

Figure 1.

Many microcontrollers implement USB so that it presents only the D+ and D- lines to external pins. This is desirable in many cases because it minimizes external components and simplifies the design; however, this presents particular challenges when isolation is required. USB lines must automatically switch between actively driving D+/D-, receiving data, and allowing external resistors to set the idle state of the bus. The ADuM4160 provides mechanisms for detecting the direction of data flow and control over the state of the output buffers. Data direction is determined on a packet-by-packet basis.

The ADuM4160 uses the edge detection based *i*Coupler technology in conjunction with internal logic to implement a transparent, easily configured, upstream facing port isolator. Isolating an upstream facing port provides several advantages in simplicity, power management, and robust operation.

The isolator has propagation delay comparable to that of a standard hub and cable. It operates with the bus voltage on either side ranging from 4.5 V to 5.5 V, allowing connection directly to V_{BUS} by internally regulating the voltage to the signaling level. The ADuM4160 provides isolated control of the pull-up resistor to allow the peripheral to control connection timing. The device has a low idle current; so a suspend mode is not required. A 2.5 kV version, the ADuM3160, is also available.

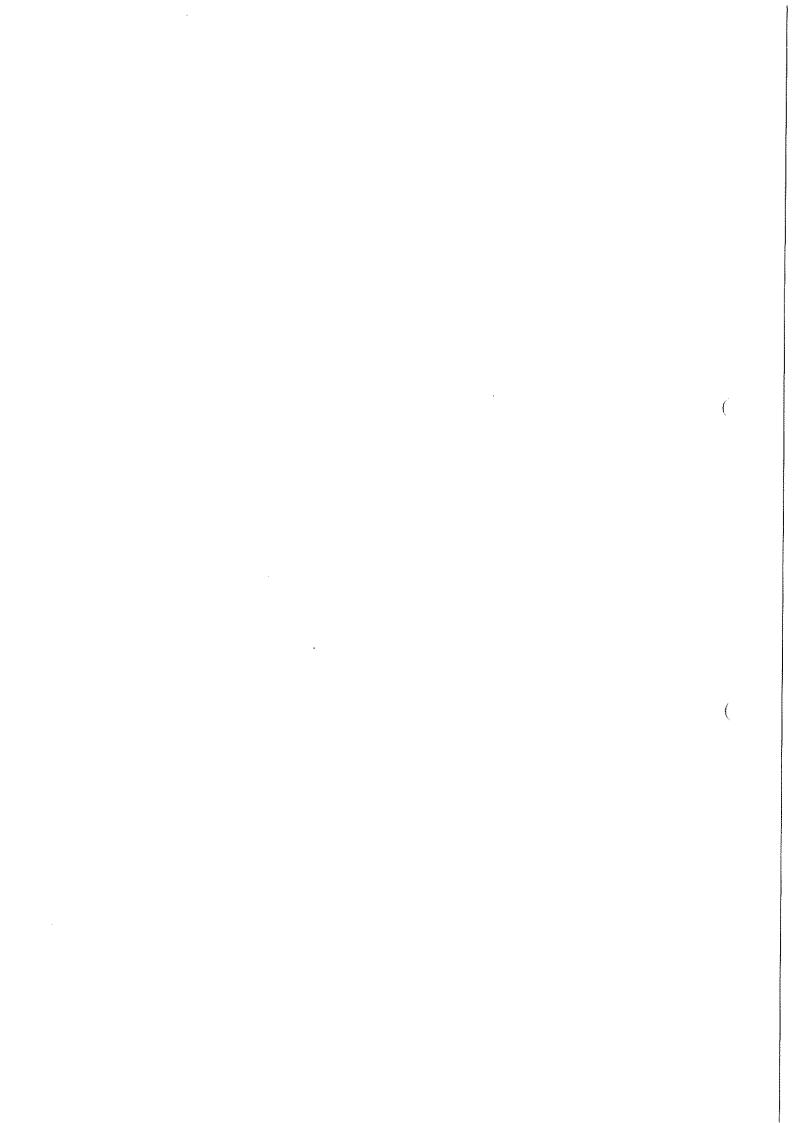


¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329.

Rev. D

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APPLICATIONS INFORMATION FUNCTIONAL DESCRIPTION

USB isolation in the D+/D- lines is challenging for several reasons. First, access to the output enable signals is normally required to control a transceiver. Some level of intelligence must be built into the isolator to interpret the data stream and determine when to enable and disable its upstream and downstream output buffers. Second, the signal must be faithfully reconstructed on the output side of the coupler while retaining precise timing and not passing transient states such as invalid SEO and SE1 states. In addition, the part must meet the low power requirements of the suspend mode.

The *i*Coupler technology is based on edge detection, and, therefore, lends itself well to the USB application. The flow of data through the device is accomplished by monitoring the inputs for activity and setting the direction for data transfer based on a transition from the idle (J) state. When data direction is established, data is transferred until either an end-of-packet (EOP) or a sufficiently long idle state is encountered. At this point, the coupler disables its output buffers and monitors its inputs for the next activity

During the data transfers, the input side of the coupler holds its output buffers disabled. The output side enables its output buffers and disables edge detection from the input buffers. This allows the data to flow in one direction without wrapping back through the coupler making the *i*Coupler latch. Logic is included to eliminate any artifacts due to different input thresholds of the differential and single-ended buffers. The input state is transferred across the isolation barrier as one of three valid states, J, K, or SEO. The signal is reconstructed at the output side with a fixed time delay from the input side differential input.

The *i*Coupler does not have a special suspend mode, nor does it need one because its power supply current is below the suspend current limit of 2.5 mA when the USB bus is idle.

The ADuM4160 is designed to interface with an upstream facing low/full speed USB port by isolating the D+/D- lines. An upstream facing port supports only one speed of operation, thus, the speed related parameters, J/K logic levels, and D+/D- slew rate are set to match the speed of the upstream facing peripheral port (see Table 10).

A control line on the downstream side of the ADuM4160 activates a pull-up resistor integrated into the upstream side. This allows the downstream port to control when the upstream port attaches to the USB bus. The pin can be tied to the peripheral pull-up, a control line, or the $V_{\rm DD2}$ pin, depending on when the initial bus connect is to be performed.

PRODUCT USAGE

The ADuM4160 is designed to be integrated into a USB peripheral with an upstream facing USB port as shown in Figure 4. The key design points are:

- The USB host provides power for the upstream side of the ADuM4160 through the cable.
- The peripheral supply provides power to the downstream side of the ADuM4160.
- The DD+/DD- lines of the isolator interface with the peripheral controller, and the UD+/UD- lines of the isolator connect to the cable or host.
- 4. Peripheral devices have a fixed data rate that is set at design time. The ADuM4160 has configuration pins, SPU and SPD, that determine the buffer speed and logic convention for each side. These must be set identically and match the desired peripheral speed.
- USB enumeration begins when either the UD+ or UDline is pulled high at the peripheral end of the USB cable, which is the upstream side of the ADuM4160. Control of the timing of this event is provided by the PIN input on the downstream side of the coupler.
- Pull-up and pull-down resistors are implemented inside the coupler. Only external series resistors and bypass capacitors are required for operation.

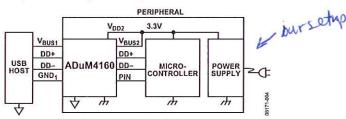


Figure 4. Typical Application

Other than the delayed application of pull-up resistors, the ADuM4160 is transparent to USB traffic, and no modifications to the peripheral design are required to provide isolation. The isolator adds propagation delay to the signals comparable to a hub and cable. Isolated peripherals must be treated as if there were a built-in hub when determining the maximum number of hubs in a data chain.

Hubs can be isolated like any other peripheral. Isolated hubs can be created by placing an ADuM4160 on the upstream port of a hub chip. This configuration can be made compliant if counted as two hub delays. The hub chip allows the ADuM4160 to operate at full speed yet maintains compatibility with low speed devices.

Data Sheet

ADuM4160

Table 10. Truth Table, Control Signals, and Power (Positive Logic)1

V _{SPU} Input	V _{BUS1} , V _{DD1} State	V _{UD+} , V _{UD-} State	V _{SPD} Input	VBUS2, VDD2	V _{DD+} , V _{DD-} State	V _{PIN} Input	Notes
Н	Powered	Active	Н	Powered	Active	Н	Input and output logic set for full speed logic convention and timing.
L.	Powered	Active	L	Powered	Active	H	input and output logic set for low speed logic convention and timing.
L	Powered	Active	Н	Powered	Active	H	Not allowed: Vspu and Vspo must be set to the same value. USB host detects communications error.
Н	Powered	Active	L	Powered	Active	Н	Not allowed: Vspu and Vspp must be set to the same value. USB host detects communications error.
X	Powered	Z	X	Powered	Z	L	Upstream Side 1 presents a disconnected state to the USB cable.
X	Unpowered	X	X	Powered	Z	x	When power is not present on V _{DD1} , the downstream data output drivers revert to high-Z within 32 bit times. The downstream side initializes in high-Z state.
X	Powered	Z	×	Unpowered	X	X	When power is not present on V _{DD2} , the upstream side disconnects the pull-up and disables the upstream drivers within 32 bit times.

¹ H represents logic high input or output, L represents logic low input or output, X represents the don't care logic input or output, and Z represents the high impedance output state.

COMPATIBILITY OF UPSTREAM APPLICATIONS

The ADuM4160 is designed specifically for isolating a USB peripheral. However, the chip does have two USB interfaces that meet the electrical requirements for driving USB cables. This opens the possibility of implementing isolation in downstream USB ports such as isolated cables, which have generic connections to both upstream and downstream devices, as well as isolating host ports.

In a fully compliant application, a downstream facing port must be able to detect whether a peripheral is low speed or full speed based on the application of the upstream pull-up. The buffers and logic conventions must adjust to match the requested speed. Because the ADuM4160 sets its speed by hard wiring pins, the part cannot adjust to different peripherals on the fly.

The practical result of using the ADuM4160 in a host port is that the port works at a single speed. This behavior is acceptable in embedded host applications; however, this type of interface is not fully compliant as a general-purpose USB port.

Isolated cable applications have a similar issue. The cable operates at the preset speed only; therefore, treat cable assemblies as custom applications, not general-purpose isolated cables.

POWER SUPPLY OPTIONS

In most USB transceivers, 3.3 V is derived from the 5 V USB bus through an LDO regulator. The ADuM4160 includes internal LDO regulators on both the upstream and downstream sides. The output of the LDO is available on the $V_{\rm DD1}$ and $V_{\rm DD2}$ pins. In some cases, especially on the peripheral side of the isolation, there may not be a 5 V power supply available. The ADuM4160 has the ability to bypass the regulator and run on a 3.3 V supply directly.

Two power pins are present on each side, V_{BUSx} and V_{DDx} . If 5 V is supplied to V_{BUSx} , an internal regulator creates 3.3 V to power the xD+ and xD- drivers. V_{DDx} provides external access to the 3.3 V supply to allow external bypass as well as bias for external pull-ups. If only 3.3 V is available, it can be supplied to both V_{BUSx} and V_{DDx} . This disables the regulator and powers the coupler directly from the 3.3 V supply.

Figure 5 shows how to configure a typical application when the upstream side of the coupler receives power directly from the USB bus and the downstream side is receiving 3.3 V from the peripheral power supply. The downstream side can run from a 5 V V_{BUS2} power supply as well. It can be connected in the same manner as V_{BUS1} as shown in Figure 5, if needed.

We will use Adafruit us Bisolata mobile. our option, with current PCB;

Supply 5V from Wall wart; directly connect to input voltage of de jach. However, this could be dayerous.

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So, if we connect 9V battery, boom_ we fig the MM 4160.

Prob better + safer if we use 3.3V option above.

This means we need to modify the adaptust module shorting formecting pins 14+16 VBus+ Vop2.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM4160 digital isolator requires no external interface circuitry for the logic interfaces. For full speed operation, the D+ and D- line on each side of the device requires a 24 Ω \pm 1% series termination resistor. These resistors are not required for low speed applications. Power supply bypassing is required at the input and output supply pins (see Figure 5). Install bypass capacitors between V_{BUSS} and V_{DDS} on each side of the chip. The capacitor value should have a value of 0.1 μF and be of a low ESR type. The total lead length between both ends of the capacitor and the power supply pin should not exceed 10 mm. Bypassing between Pin 2 and Pin 8 and between Pin 9 and Pin 15 should also be considered, unless the ground pair on each package side is connected close to the package.

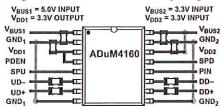


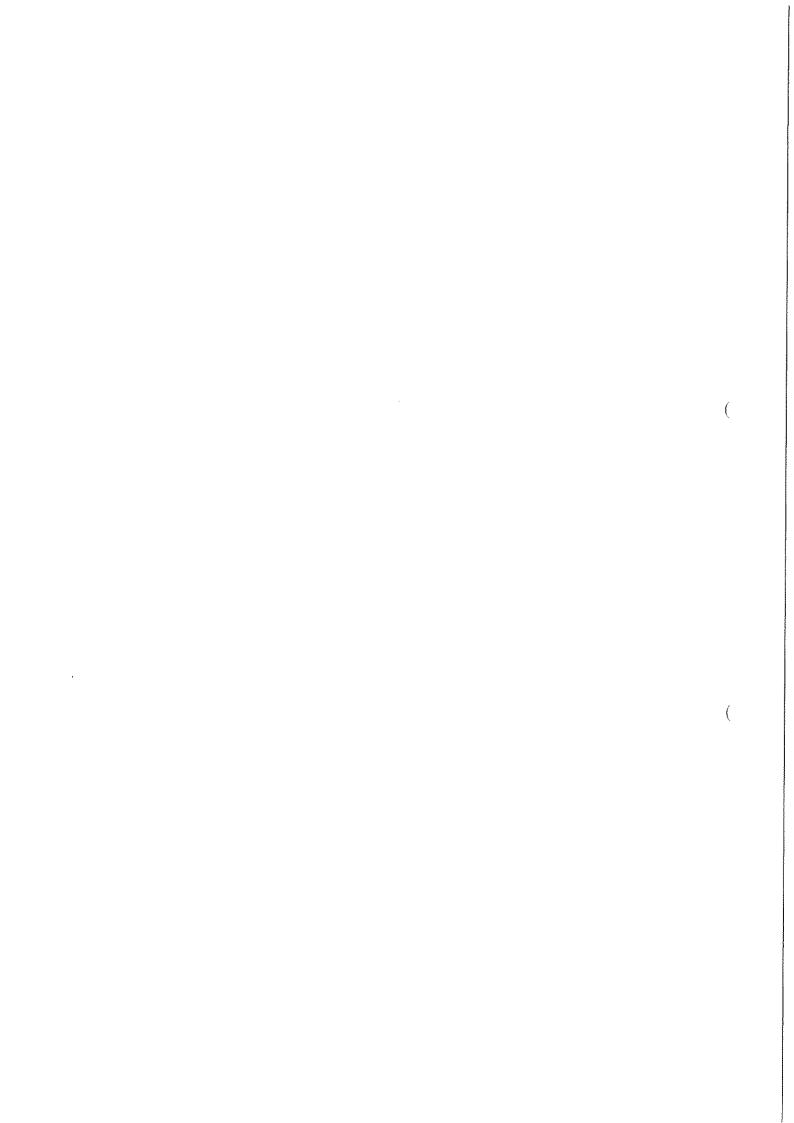
Figure 5. Recommended Printed Circuit Board Layout

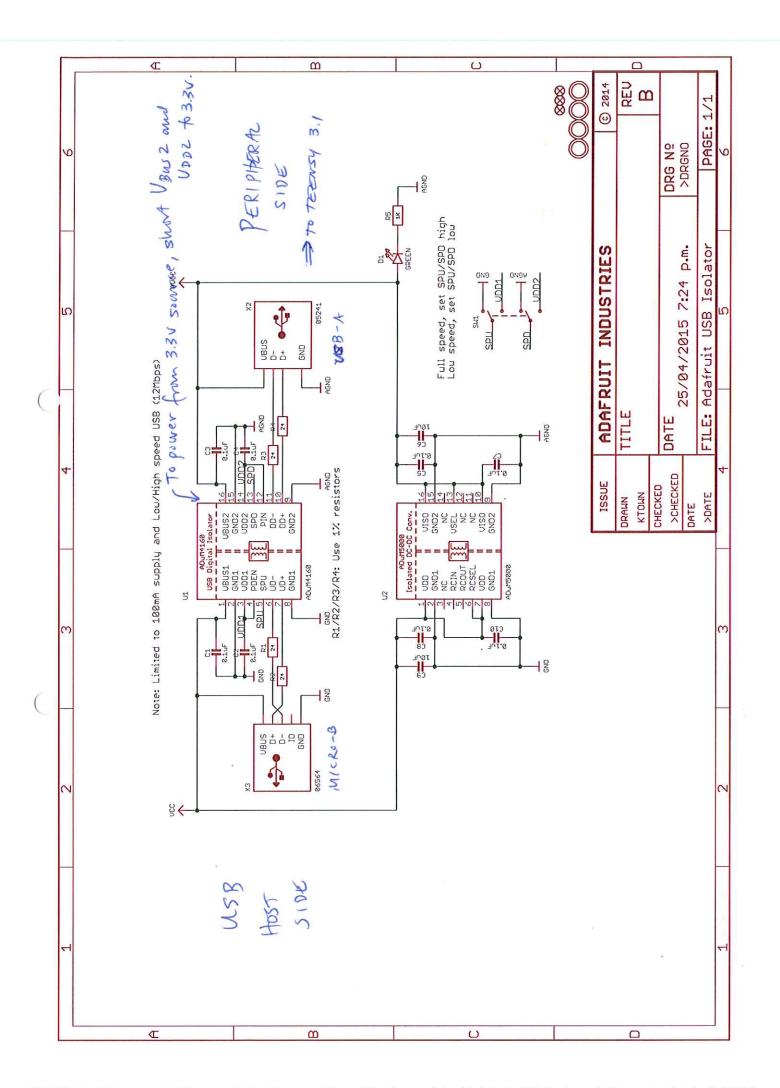
to Vapz

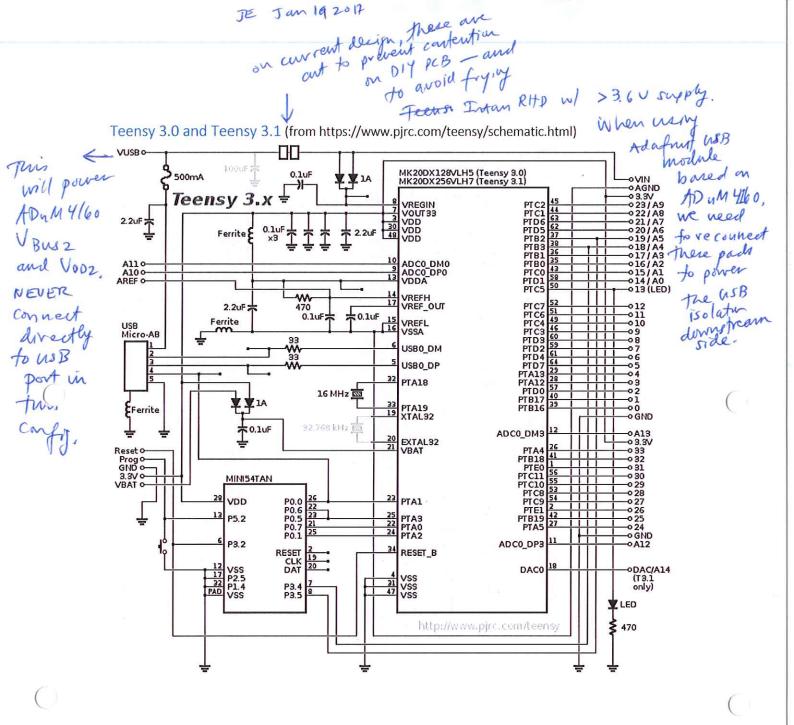
In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than about 12 USB bit times, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 36 USB bit times, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.







Teensy 3.2 Schematic

