1. **The functionality of PORTG and DDRG**

PORTG: this is the port G data register. Bits 7and 6 are reserved and can only access as Read mode, the rest 5 bits can be accessed via read and write modes and the operation details as follows: f PORTGn is written logic one when the PORTG pin n is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTGn has to be written logic zero or the pin has to be configured as an output pin. If PORTGn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If  
PORTGn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

DDRG: Port G data direction register. Again first 2 bits are reserved, this register indicate depending on the value the mode of the corresponding bit in the PORTG data register whether its read or write

Obtaining the assembly code command:

: & “C:\Users\Osama Ramadan\.platformio\packages\toolchain-atmelavr\avr\bin\objdump.exe”/objdump -h -S “D:\TUHH\Study\Semester2\Software for Embedded\Lab\Programming\team-a2\task\_1-2\.pio\build\ses\_avr\firmware.elf”

**Task 1.7: Take a look at Atmel’s ATmega128RFA1**

* size of programmable flash : 128KB P1
* size of internal EEPROM : 4KB P1
* size of internal SRAM : 16KB P1
* available ports : B - D – E – F – G(0-5) P5,6
* available counters/timers : Real Time Counter (RTC), 6 flexible Timer/Counters with compare modes  
  and PWM P4
* peripherals (e.g., UART, ADC) : 10 bit analog to digital converter (ADC) with an optional differential input stage with programmable gain / a SPI serial port /