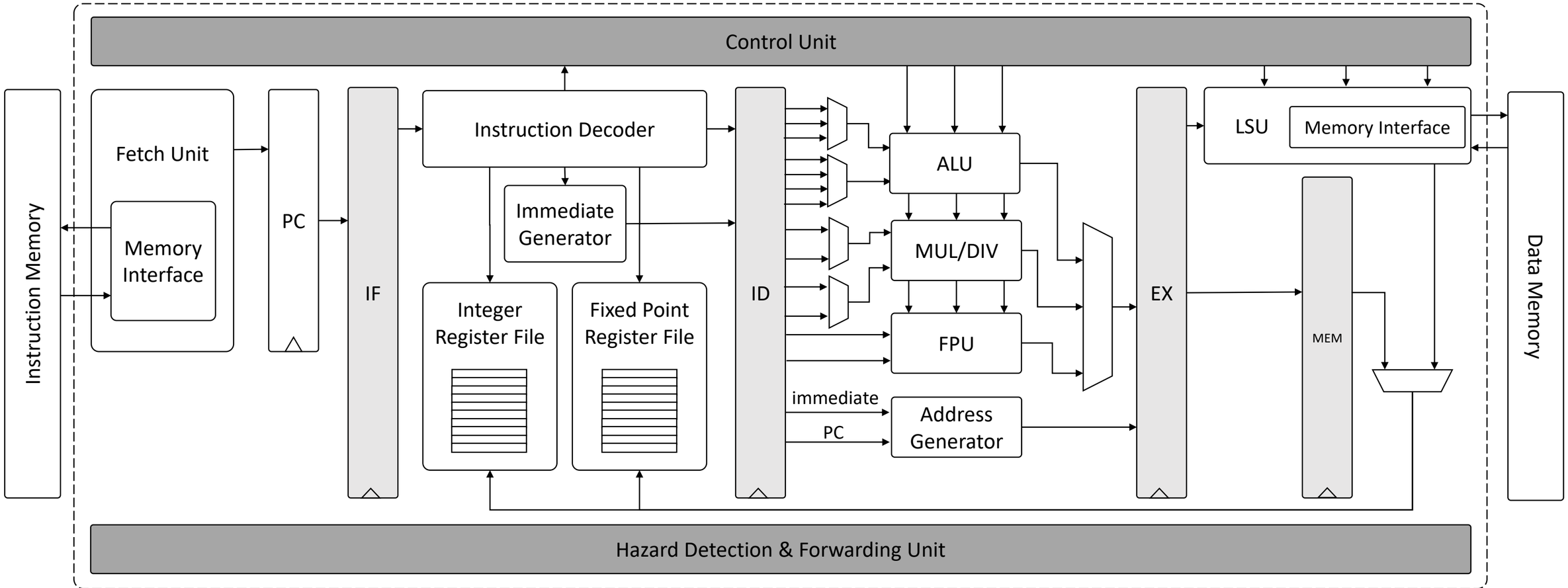
32-bit RISC-V CPU Design

Review and discussion session – August 13th 2023

32-bit RISC-V Core specifications:

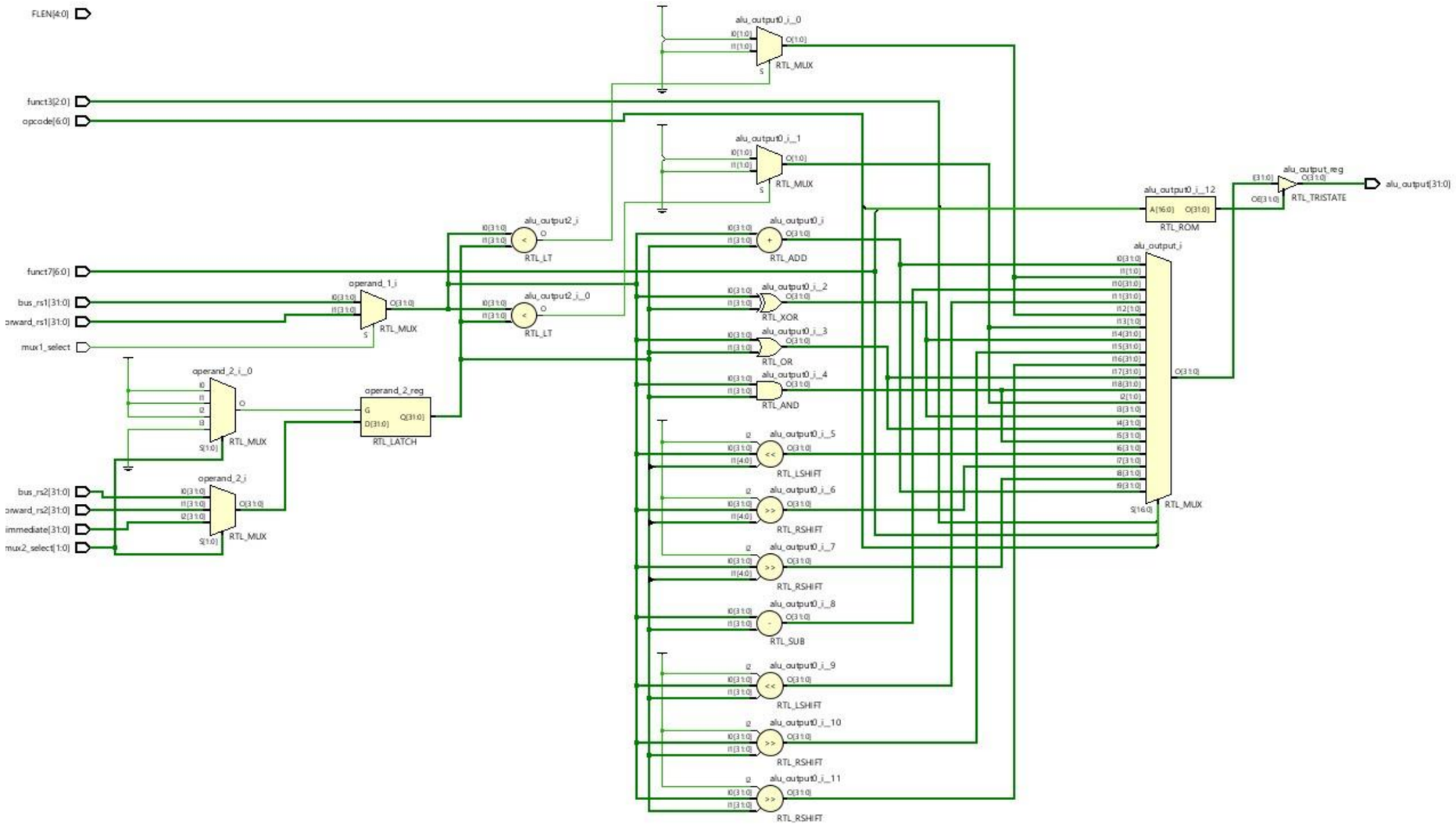
- 5 stage pipelined processor
- I-M-F Extensions from RISC-V standard ISA
- “F” Extension can be considered both “Fixed-Point” and “Floating-Point”
- Approximate Multiplication Unit
  - Controlled by a Special Purpose Register (CSR)
  - 7-Error control bits (128 different accuracies)

CPU Block Diagram:



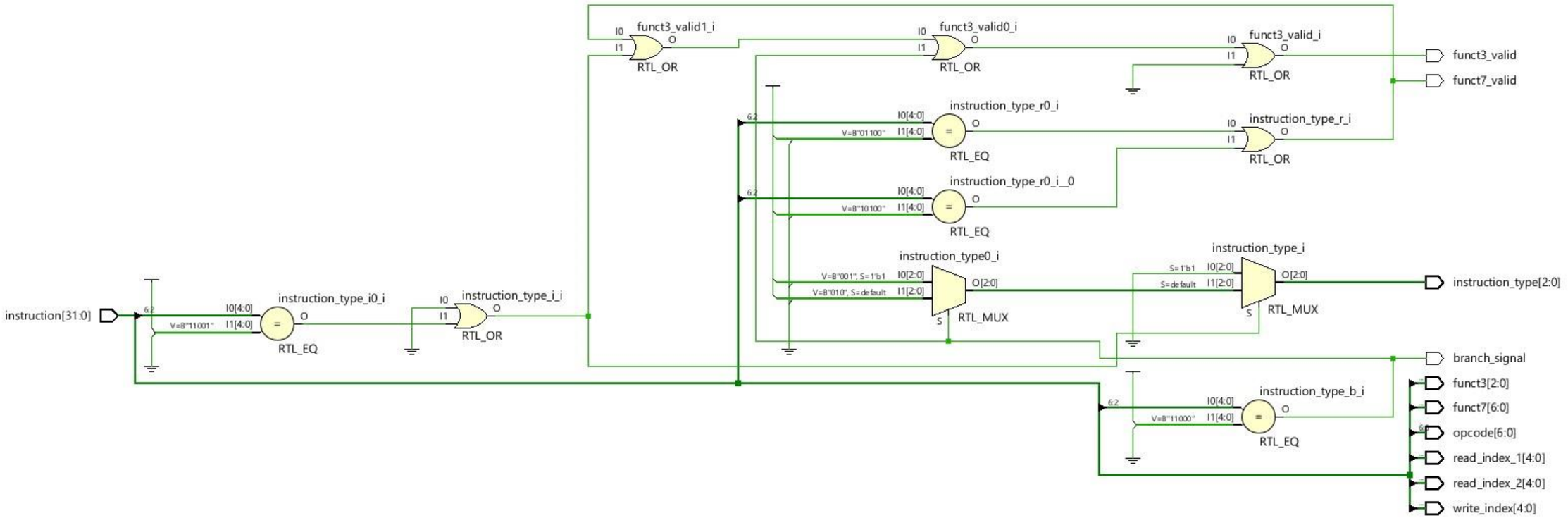
Arithmetic Logic Unit:

Note: Images are taken from RTL Elaborated Design in Xilinx Vivado after synthesis process



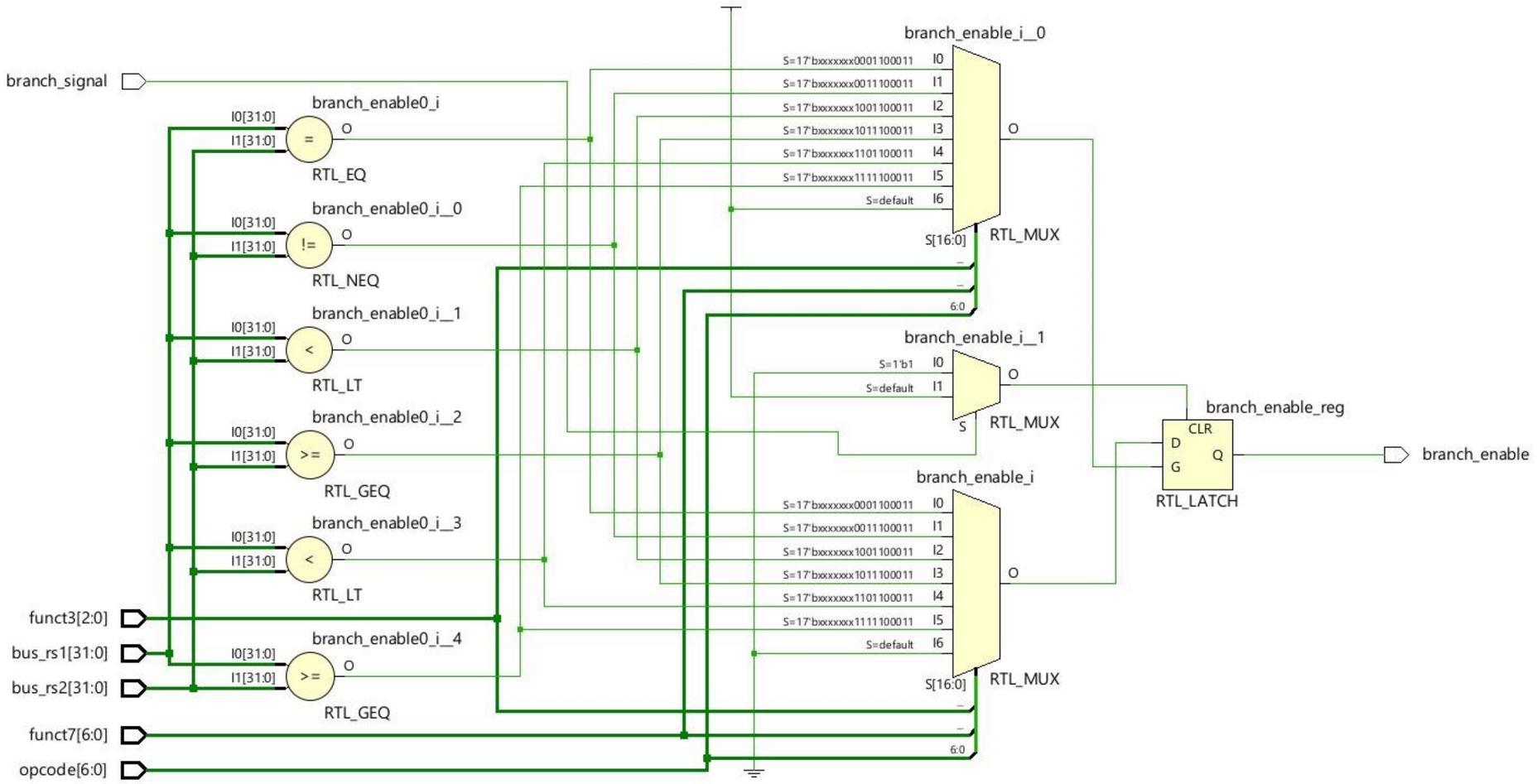
Instruction Decoder:

Note: Images are taken from RTL Elaborated Design in Xilinx Vivado after synthesis process



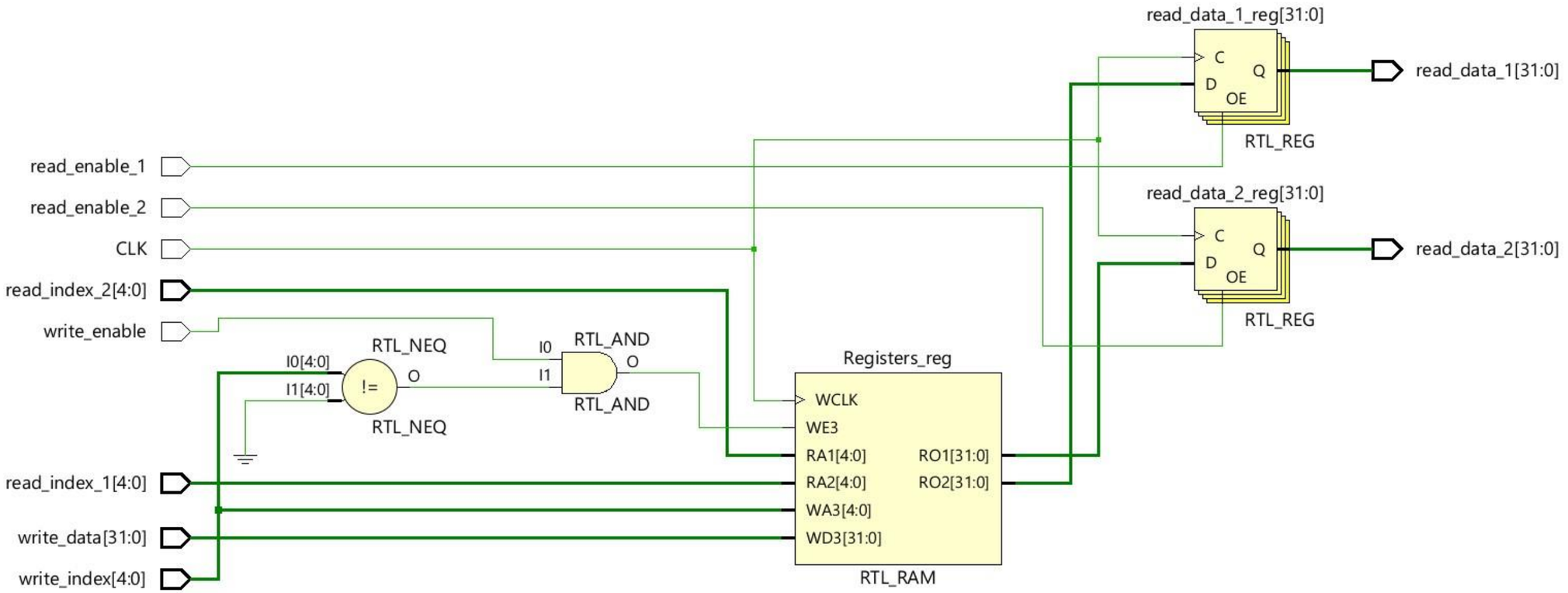
Branch Unit:

Note: Images are taken from RTL Elaborated Design in Xilinx Vivado after synthesis process



Register File:

Note: Images are taken from RTL Elaborated Design in Xilinx Vivado after synthesis process



To do list:

Phase 1:

- Design Control, Hazard and Forwarding Unit.
- Create the pipelined Datapath with the designed modules.
- Complete RV32I extension and test with GCC compiler toolchain in Linux.

➢ *By the end of phase 1, we have a processor which supports GCC and RV32I instructions.*

Phase 2:

- Pipeline Multiplier Unit and add M-Extension Instructions.
- Add DIV instruction support to the core.
- Add FPU to the execution unit.
  - Note: Design must be modular and hierarchical so that FPU could be changed between “Fixed-Point” and “Floating-Point” formats.