(Q 1) Choose the Correct Answer (Only one answer):-

(1) In …… all processors receive the same instruction from the control unit but operate on different items of data.
(a) SISD (b) SIMD (c) MISD (d) MIMD

(2) In ……. Multiple processors perform operations on different pieces of data, either independently or as part of shared memory space.
(a) SISD (b) SIMD (c) MISD (d) MIMD

(3) In ….. Pipelining can be implemented, but only one instruction will be executed at a time.
(a) SISD (b) SIMD (c) MISD (d) MIMD

(4) Modern GPUs, containing Vector processors and array processors, are commonly …… systems.
(a) SISD (b) SIMD (c) MISD (d) MIMD

(5) In …. where multiple processors work on the same data set, performing the same instructions at the same time.
(a) SISD (b) SIMD (c) MISD (d) MIMD

(6) the time for an instruction to complete.
(a) Latency (b) Throughput (c) Clock cycle (d) CPI

(7) the number of instructions completed per second
(a) Latency (b) Throughput (c) Clock cycle (d) CPI

(8) The following instruction R0 = (R1 * R3) + R0. Is considered
(a) SISC (b) RISK (c) CISC (d) RISC

(9) ….. occur when the pipeline changes the order of read/write accesses to operands so that the order differs from the order seen by sequentially executing instructions on an unpipelined processor.
(a) structural hazard (b) data hazard (c) control hazard (d)None

(10) In MIPS the PC is incremented by
(a) 1 byte (b) 2 byte (c) 3 byte (d) 4 byte

(Q2) Consider Processor using a Pipeline with only *four segments* with a *clock cycle time equal to 10* ns to execute the program with *200 instructions*. Assume that the time it takes to process a task is the same in the pipeline and nonpipelined processors, we will have $t_n = kt_p$ where t_p refer to the clock cycle time for a k-segment pipeline processor.

(11) Total time to complete n tasks using a k-segment pipeline calculated by the formula
(a) $[k t_p + (n - 1) t_p]$ (b) $[k t_p + (n - t_p)]$ (c) $[k t_p + n t_p)]$ (d) None

(12) Total time to complete 200 instructions using a 4-segment pipeline =
(a) 203 (b) 2030 (c) 230 (d)2040

(13) Total time to complete the 200 instructions using a nonpipelined processor =……
(a) 4000 (b)1200 (c)8000 (d)2000

(14) The speedup ratio is equal to S=
(a) 8.69 (b) 1 (c) 3 (d)3.94

(15) If we assume that $t_n = 80$ ns, the speedup becomes
(a) 1 (b)2 (c)8 (d)4

(Q3) Consider an unpipelined Processor with a 2 ns clock cycle; 5 cycles for ALU, 4 cycles for branches; 6 cycles for memory operations; relative frequencies 45%, 10%, and 45%; where for pipelined processor there is a 0.2 ns pipeline overhead (e.g., due to stage imbalance, pipeline register setup, clock skew).

(16) *Average instruction time unpipelined* =
(a)4.4 (b)10.7 (c) 8 (d) none

(17) *Average instruction time pipelined* =
(a) 2.2 (b) 20 (c) 6 (d) none

(18) speedup by pipelining =
(a) 1.78 (b)4.86 (c) 0.5 (d) none

With My Best wishes DR. Ahmed Hesham Mostafa