Board 2: Switching noise with good and bad layout **Final Board Report**

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Plan of Record

The purpose of this board design is to demonstrate how good and bad layout practices affect the amount of switching noise in a PCB, as well as putting into practice the best measurement techniques for measuring switching noise.

Board 2 is designed to drive two hex inverters from a 60% duty cycle, 500 Hz 555 timer clock signal. Resistive loads will be connected across the hex inverter outputs, which will drive switching noise due to the switching currents due to the changing voltage across the resistors. The layout of the two hex inverters will be implemented differently: one will be with good design practices, with a decoupling capacitor placed close to the IC and a continuous ground plane, and one with bad design practices, with the decoupling capacitor far from the IC and individual ground traces routed through a common path.

Quiet high and quiet low outputs are provided on the hex inverters to measure switching noise. The quiet high output, which is connected to the internal Vcc rail on the hex inverter and should normally show a DC voltage at Vcc, will be used to measure the synchronous power rail noise. The quiet low output, which is connected to the Vss rail on the hex inverter and should normally show a DC voltage at Vss (0V), will be used to measure ground bounce and cross talk. The loads will consist of red LEDs in series with 50 ohm resistors. Red LEDs are selected to provide the lowest forward voltage drop of the selectable LED colors in order to drive the highest current through the resistors and thus result in larger switching noise. With a 5 V Vcc and 2 V forward voltage drop through the red LEDs, 60 mA of current is expected in each of the three resistors for each hex, so 180 mA total. Since the hex inverter will be supplying the current, a fast 555 timer with a lower current limit can be used – this will increase switching noise with faster rise and fall times.

The Vcc rail of the hex inverters and 555 timer will be selectable between a 5 V and a 3.3 V LDO regulated signal. Both voltages are within rated input voltages to drive the ICs and loads, but the difference in switching noise will be demonstrated between them. A 22 uF capacitor will be placed close to the LDO output to stabilize its feedback loop by slowing the output response. A switch will be included to demonstrate the effect of including or not including this capacitor.

The hex inverter inputs corresponding to the loaded outputs will be pulled up to Vcc when not connected to the 555, in order to keep the outputs low when not driven by the 555. Switches will be included to select one or both hex inverters to be driven by the 555. Finally, test points for the voltage on an unloaded output of the hex inverter, the voltage on a loaded output, and the current through one of the load resistors will be included to determine the Thevenin resistance of the hex inverter.

Finally, indicator LEDs will be included to demonstrate when each portion of the board is operating.

Block Diagram and Schematic

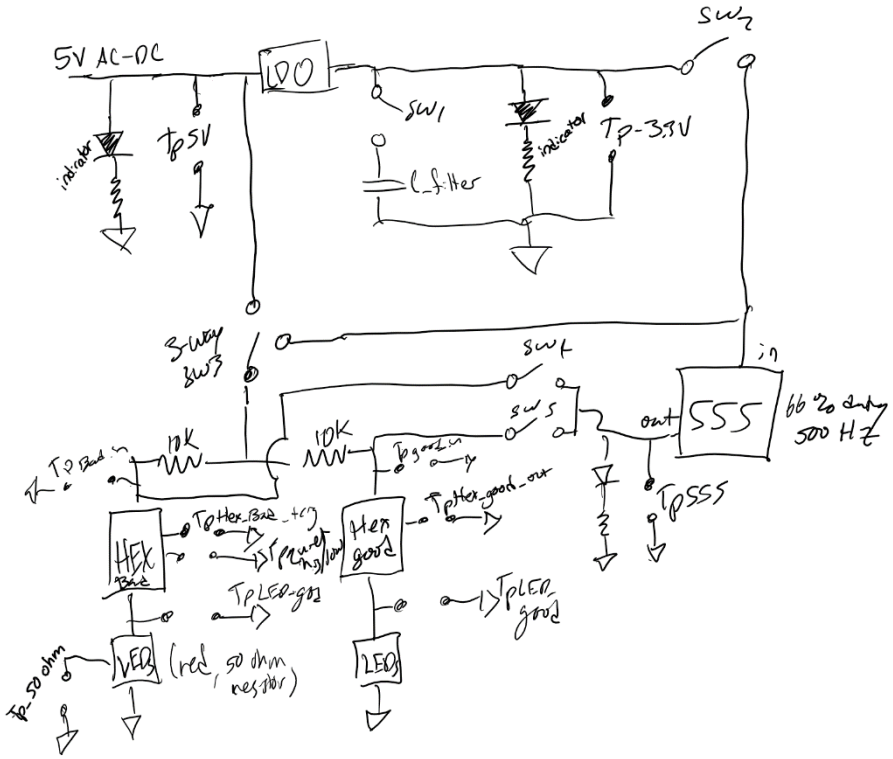

Figure 1: Board 2 Block Diagram

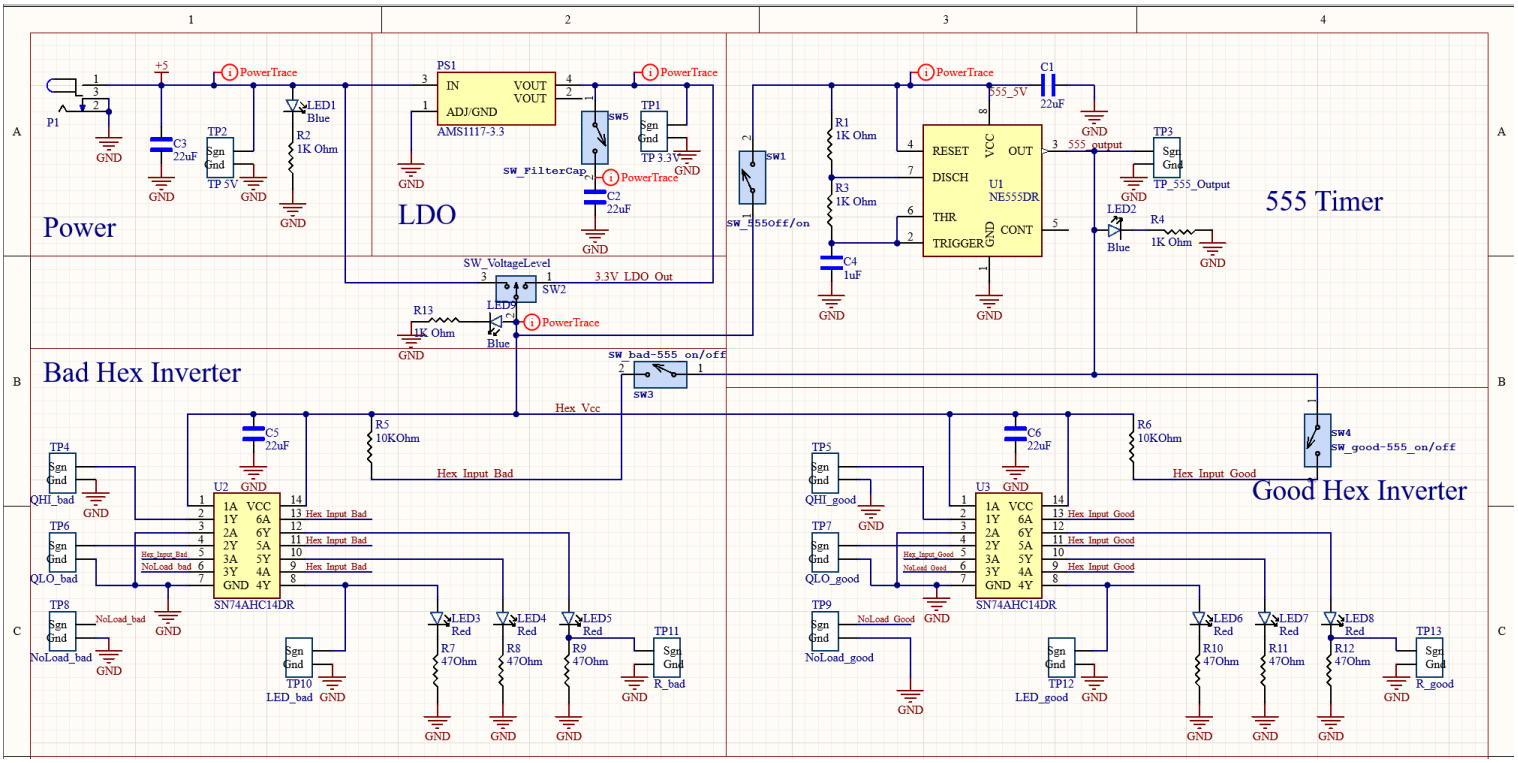

Figure 2: Board 2 Schematic

The schematic shows the design choice for astable operation of the 555 timer. Resistors R1 and R3 at 1k ohm will set the duty cycle to 66%, and the 1uF C4 will set the frequency to 480 Hz.

One mistake was made in this schematic that was discovered upon testing. The quiet high and quiet low

No special features are expected in this board, so the cost should be the minimum possible for a basic board provided by the fabrication shop.

Assembly and Bring-up Plan

The use of isolation switches will simplify debugging and soldering. The entire board can be soldered at once, and isolation switches incrementally switched on to verify correct operation of each section.

Test points will be used to verify correct operation of the board. At TP_5V, a 5V DC voltage should be seen. At TP_3.3V, a 3.3V DC voltage should be seen. With SW_FilterCap removed and the hex inverter loads being driven, more synchronous switching noise should be seen at TP_3.3V. At TP_555Output, a 480 Hz, 66% duty cycle pulsed voltage should be seen at the selected Vcc (5V DC or 3.3 V DC). On the good hex inverter layout, TP_QHI should show a DC Vcc signal with synchronous switching noise when triggered on one of the switching nodes, such as TP_NoLoad. TP_QLO should show a DC Vss (0V) voltage with synchronous switching noise. TP_NoLoad should show the inverted 555 output signal. TP_LED should show the inverted 555 output signal at a slightly lower amplitude due to the hex inverter Thevenin resistance. With the 555 input to the hex switched off, TP_NoLoad and TP_LED should be shorted to Vss and show a DC 0 V signal. At the corresponding test points on the bad layout hex inverter, more synchronous switching noise should be seen at TP_QHI and TP_QLO.

The switching noise on both the rising and falling edges will be measured at the quiet high and quiet low outputs on each of the hex inverters when each is individually driven by the 555 timer. The rail compression, which is the difference between the measured voltages on the Vcc and Vss rails (and the actual voltage between Vcc and gnd that the outputs see), will be measured by taking the difference between the synchronous switching noise on the quiet high and quiet low pins. The Thevenin resistance of the hex inverter will be calculated using the measured voltage drop at TP_LED versus TP_NoLoad and the current at TP_R.

Board Layout and Assembled Board

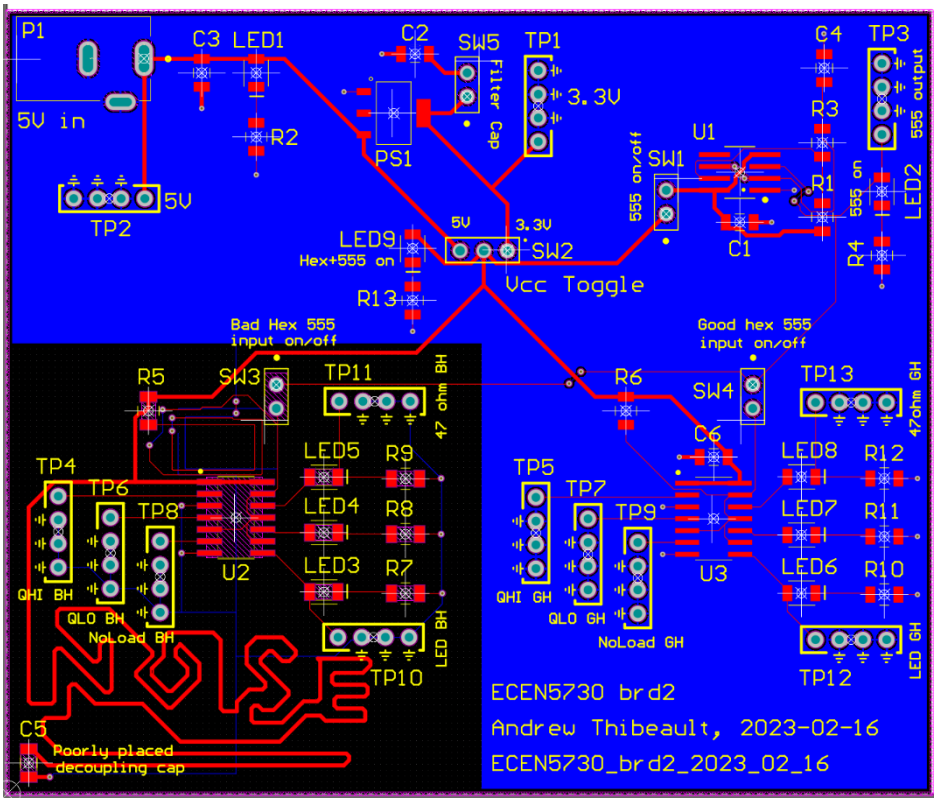

Figure 3: Board 2 Layout

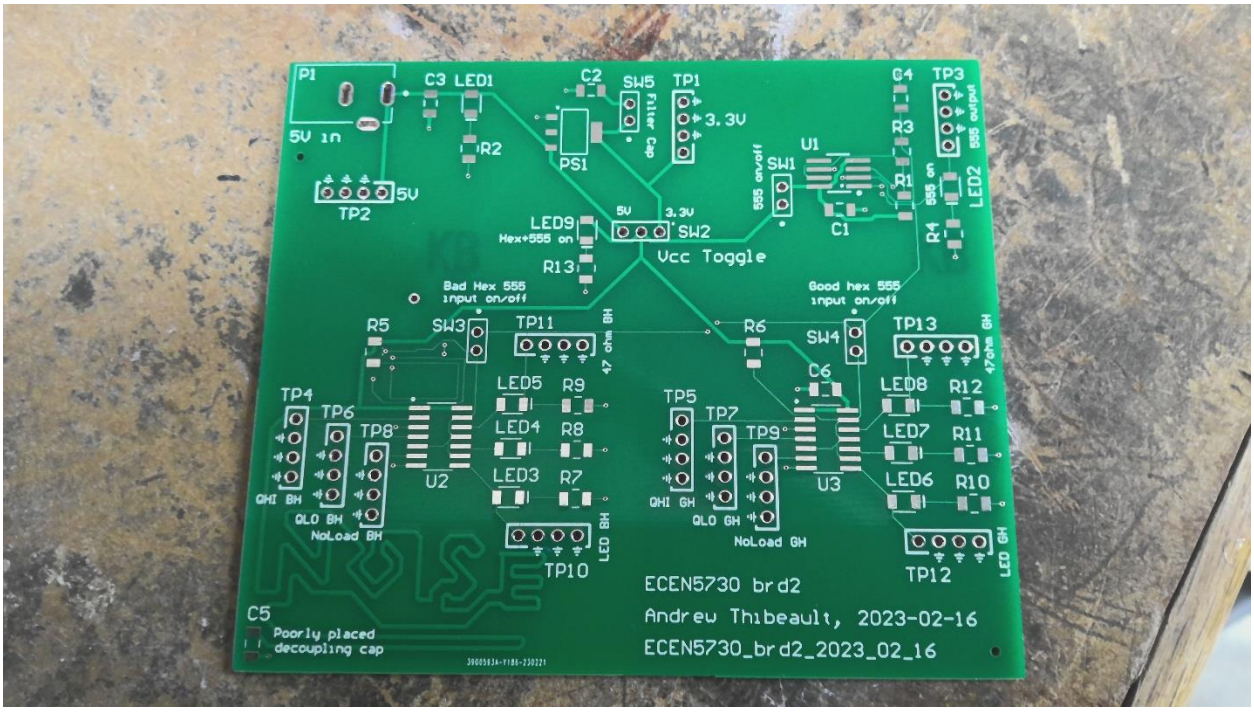

Figure 4: Bare Board 2

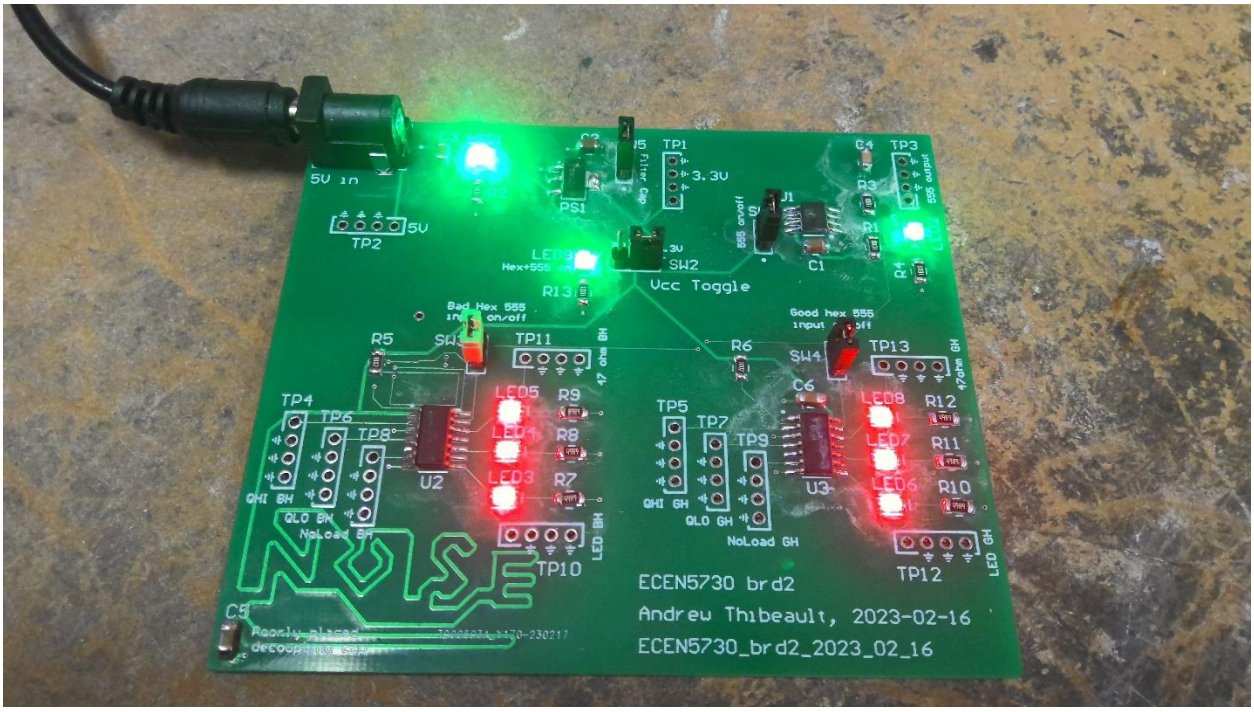

Figure 5: Fully Assembled Board 2

Test Results and Discussion

The board was assembled and tested for working conditions without issue.

The 5V AC-DC converter ended up providing a 5.53 V signal. The output of the LDO was tightly regulated at 3.3 V, so it would be a wise choice to use such an LDO if a tightly regulated input voltage was needed in a circuit, though that is not the case on this board. With both hex inverters being driven by the 555 timer and the LDO filter capacitor switch removed, 137 mV of synchronous switching noise was seen at the LDO output. With the switch applied, 65 mV of noise was seen. The filtering capacitor clearly is a good design choice to reduce noise on the power rail.

The results of the switching noise on the different hex inverter layouts while driven by the 555 timer individually with 5V Vcc is shown in the table below.

Hex layout	Rise time	Quiet high noise rising edge	Quiet low noise rising edge	Rail compression rising edge	Fall time	Quiet high noise falling edge	Quiet low noise falling edge	Rail compression falling edge
Good	2.0 ns	562 mV	271 mV	825 mV	1.7 ns	494 mV	300 mV	613 mV
Bad	5.7 ns	1.69 V	118 mV	1.74 V	1.8 ns	3.36 V	519 mV	3.68 V

Table 1: Switching Noise Results

Generally, switching noise was significantly decreased on the good hex layout as compared to the bad hex layout. The one instance where switching noise seems to increase on the good hex layout is on the quiet low rising edge measurement. This is likely due to the nearly three times faster rise time on the good hex layout as compared to the bad hex layout. A faster rise time results in a larger dI/dt with the same dI (total load current), which in turn results in more inductive switching noise. Were the switching times on each hex the same, we should expect to see greater switching noise on the bad hex inverter. In the falling edge case, in which the fall times are nearly identical for each hex, the quiet low rise time is greater on the bad hex. The greater switching noise on the quiet high output on the bad hex layout results from the long inductive loop between the Vcc pin and the decoupling capacitor. This results in more noise on the power rail as seen by the IC. The greater switching noise on the quiet low output on the bad hex inverter results from the lack of a continuous return plane, with ground connections from the hex instead routed individually, and all returning to the rest of the board ground through a shared return. This design results in more cross talk through more tightly linked mutual inductances of these return paths, and greater ground bounce. These both drive higher switching noise on the Vss pin.

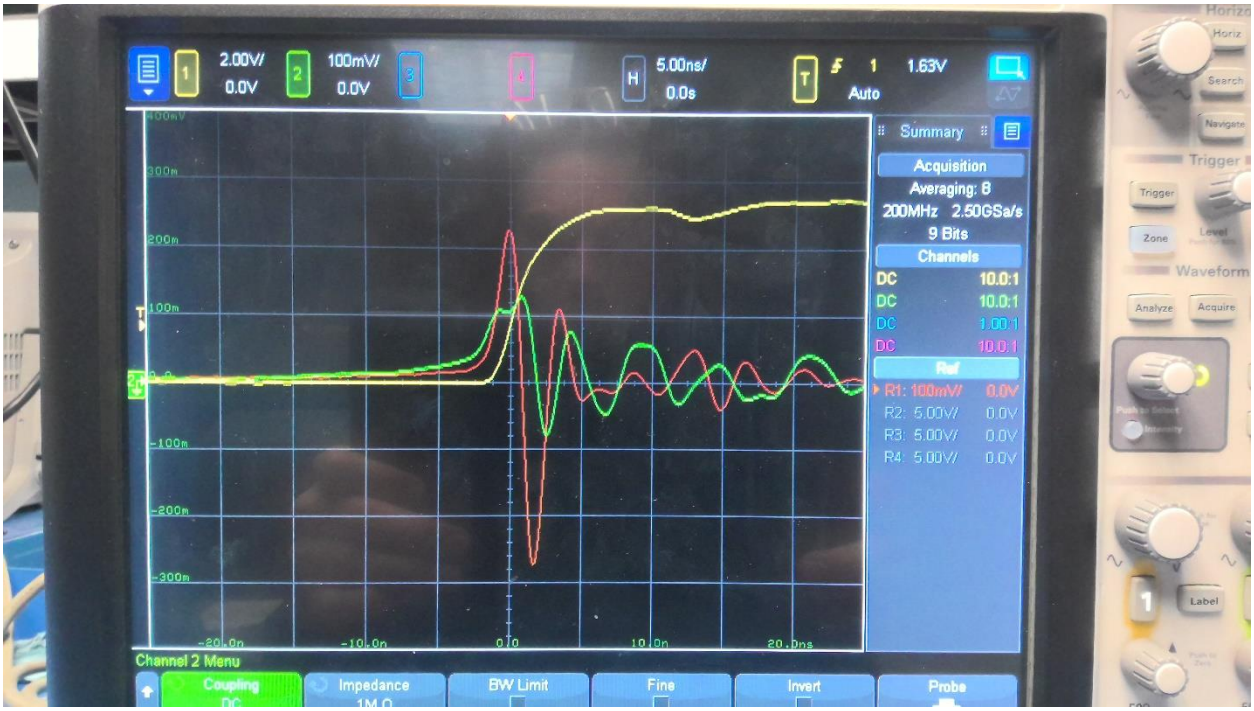

Figure 6: Quiet Low Rising Edge Noise. Good layout in red, bad in green.

Figure 7: Quiet low Falling Edge Noise. Good layout in red, bad in green.

The rail compression is dominated by the quiet high noise in each case.

Figure 8: Rising edge rail compression on good layout

The switching noise on the 5V rail was also measured. In each case, the noise on the 5V rail was significantly lower than that on the quiet high output on the hex inverter. For example,

on the rising edge using the good hex, the noise on the 5V rail at TP2 (5V) as seen on the assembled board was 15 mV, compared to 562 mV on the quiet high output of the hex inverter. Despite being electrically shorted to the same rail, the hex inverter Vcc is decoupled from the power rail via the 22 uF decoupling capacitor, so the 5V test point does not see the majority of the noise that the Vcc pin on the hex sees.

The operation of the board using the 5 V power rail was compared to that using the 3.3 V power rail. Generally, the 3.3 supply resulted in less switching noise, as should be expected due to a smaller dI value in the dI/dt that the load resistors drive. For example, the rising edge switching noise on the good hex layout for each Vcc value is shown below.

Power Rail	Rise Time	Quiet High Switching Noise	Quiet Low Switching Noise
5 V	2.0 ns	562 mV	271 mV
3.3 V	2.4 ns	240 mV	133 mV

Table 2: Rising edge switching noise on good hex layout with differing Vcc values

The rise time is slightly longer, and the switching noise significantly lower. If the circuit using the switched voltage signal did not depend on the amplitude of the signal, the 3.3 V rail could be used to decrease noise. Just to note, on the bad hex layout, the rise time decreased from 5.4 ns to 4.0 ns. This is likely due to ground bounce deceasing with smaller change in voltage, and thus ringing decreasing, which drives longer rise times.

The Thevenin resistance of the hex inverter was calculated using measured voltages and currents on the loaded and unloaded hex outputs.

Test Point (as seen on layout)	Voltage
TP9 (NoLoad GH)	5.30 V
TP 12 (LED GH)	4.00 V
TP13 (47ohm GH)	1.80 V (36 mA considering 50 ohm resistance actually used)

Table 3: Measurements for Thevenin Resistance

These values resulted in a calculated Thevenin resistance of 16.25 ohm.

Final Thoughts

Overall, this board design worked well and went without significant error. Several small errors were encountered. Firstly, the individual ground traces on the bad hex inverter layout were connected to the ground plane using a via, as I could not figure out how to connect a trace directly to the ground plane. In the future, I will ensure to change the properties of the ground plane to pour over all same net objects. This will allow direct connection to the ground plane. Another error I made was in improperly labeling the quiet high and quiet low test points. This resulted in a moment of confusion, but the source of the mix up was quickly determined by intuition and checking against my layout. In the future, I will spend more time checking over my schematic so that an error like this does not propagate down the pipeline. Finally, my assembled

board did not come with the red LEDs connected. This was reportedly due to supply issues, and is no fault of my own, though it is good to know that such things can happen. In the future, I will ensure to leave ample time to correct for such unavoidable errors.

The implementation of a continuous ground plane and closely-placed decoupling capacitor should be used on all future boards since these design choices do not increase cost or risk, but just give the benefit of reducing switching noise. I also now know to filter the output of an LDO to reduce noise on the power rail. I am also more informed as to how to choose a correct supply voltage: a higher supply voltage should only be used if necessary, as it will increase switching noise. Finally, I understand the concept of rail compression, and will be aware of the fact that rail compression can drive switching noise-related voltage swings even larger due to the 180° phase difference between Vcc and Vss synchronous switching noise.