# Experiment #4
# Step-Up DC-DC Converter

# Part 2:
# Frequency Responses and Feedback Controller

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## Step 1: Measurement of control-to-output transfer function

The frequency response of the control-to-output transfer function of the open-loop cascaded boost converter was measured using the Bode 100 Network Analyzer. The boost converter was loaded with a 470 ohm power resistor and powered by a 12 V power supply. The ac signal from the network analyzer was injected between the trimpot used to adjust duty cycle, and the control input of the 3525 PWM controller IC.

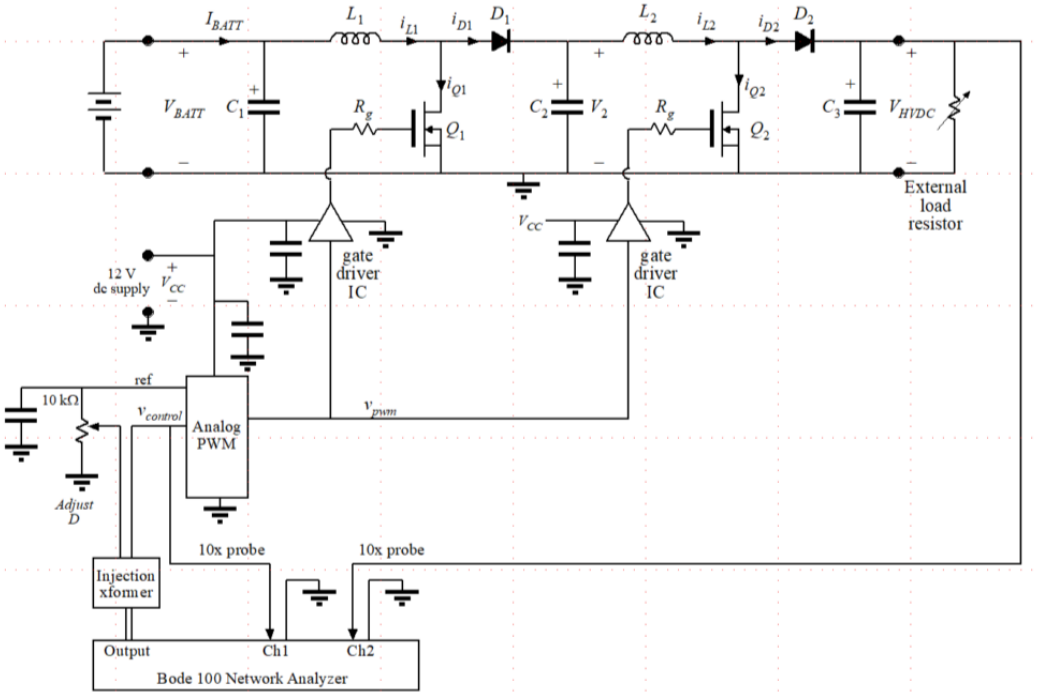


**Figure 1: Setup for measurement of $G_{VC}(s)$**

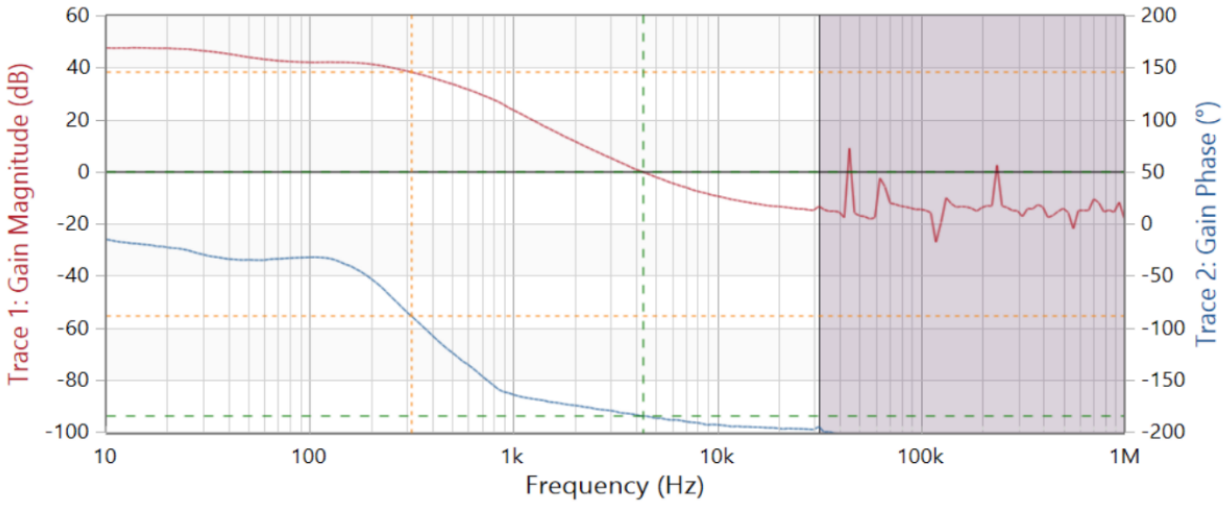


**Figure 2: Measured loop gain, open loop cascaded boost converter**

The transfer function appears dominantly as a complex-conjugate pole at 315 Hz and a right half plane zero around 7 kHz, with a DC gain of about 47 dB. The crossover frequency is 4.33 kHz, with a phase margin of -4.4°.

Using the measured inductance values from Experiment 4 Part 1, an LTspice simulation of our boost converter was performed.

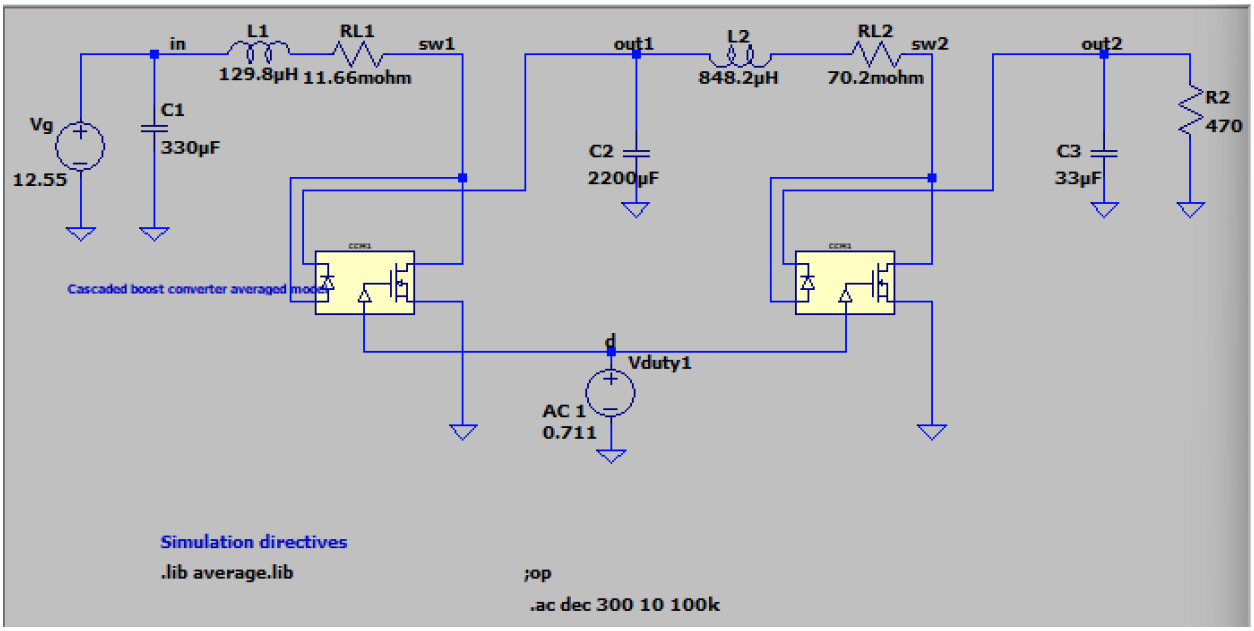


**Figure 3: LTspice schematic of open loop boost converter**

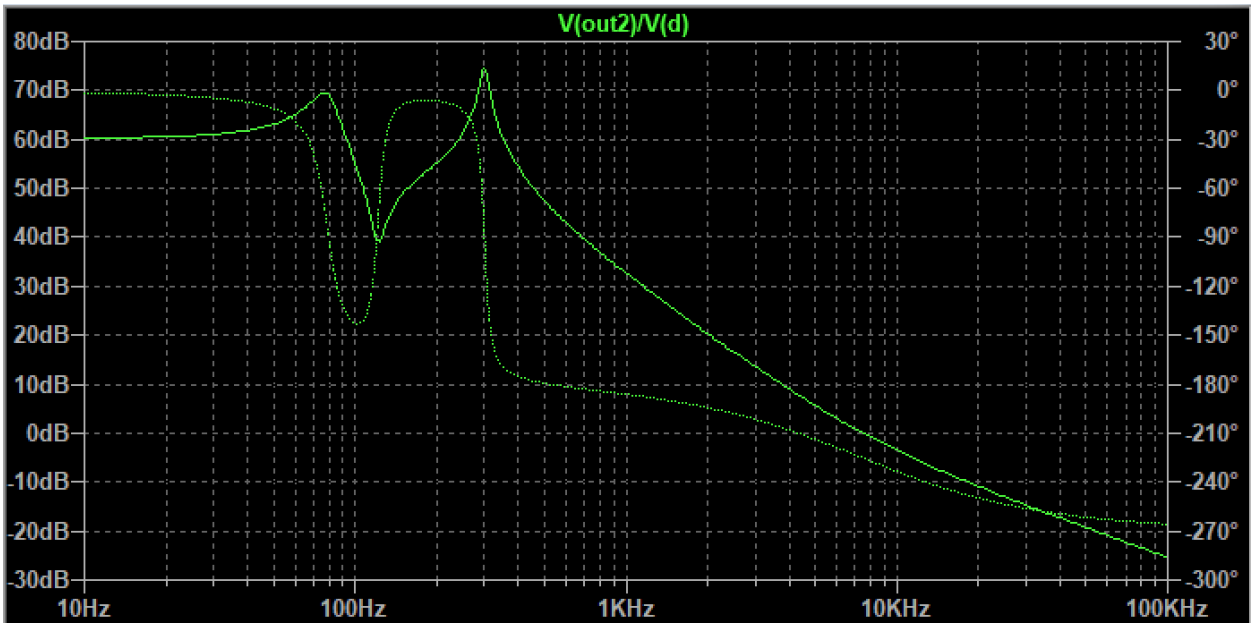


**Figure 4: Simulated open loop $G_{VC}(s)$ bode plot**

The simulated transfer function also shows a low frequency complex conjugate pole at 303 Hz and a right half plane zero at 10.7 kHz, comparable to that seen in the measured transfer function. The crossover frequency is also comparable, though slightly higher than measured, at 7.3 kHz.

The most significant departure from the measured transfer function is the appearance of a complex-conjugate pole at 78 Hz followed by a complex conjugate zero at 121 Hz. These features appear only very minorly in the measured transfer function, with a small phase dip around 55 Hz. It is likely that parasitic resistance in the real boost converter dampens these complex-conjugate features. This assumption is verified in simulation by increasing the series resistances of the inductors to model extra parasitic resistance throughout the circuit. For example, increasing the inductor series resistances by 10x results in the following transfer function frequency response, which demonstrates damping of these two complex-conjugate features:


**Figure 5: Increased inductor series resistance simulated open loop $G_{VC}(s)$**

## Step 2: Analysis of control-to-output transfer function

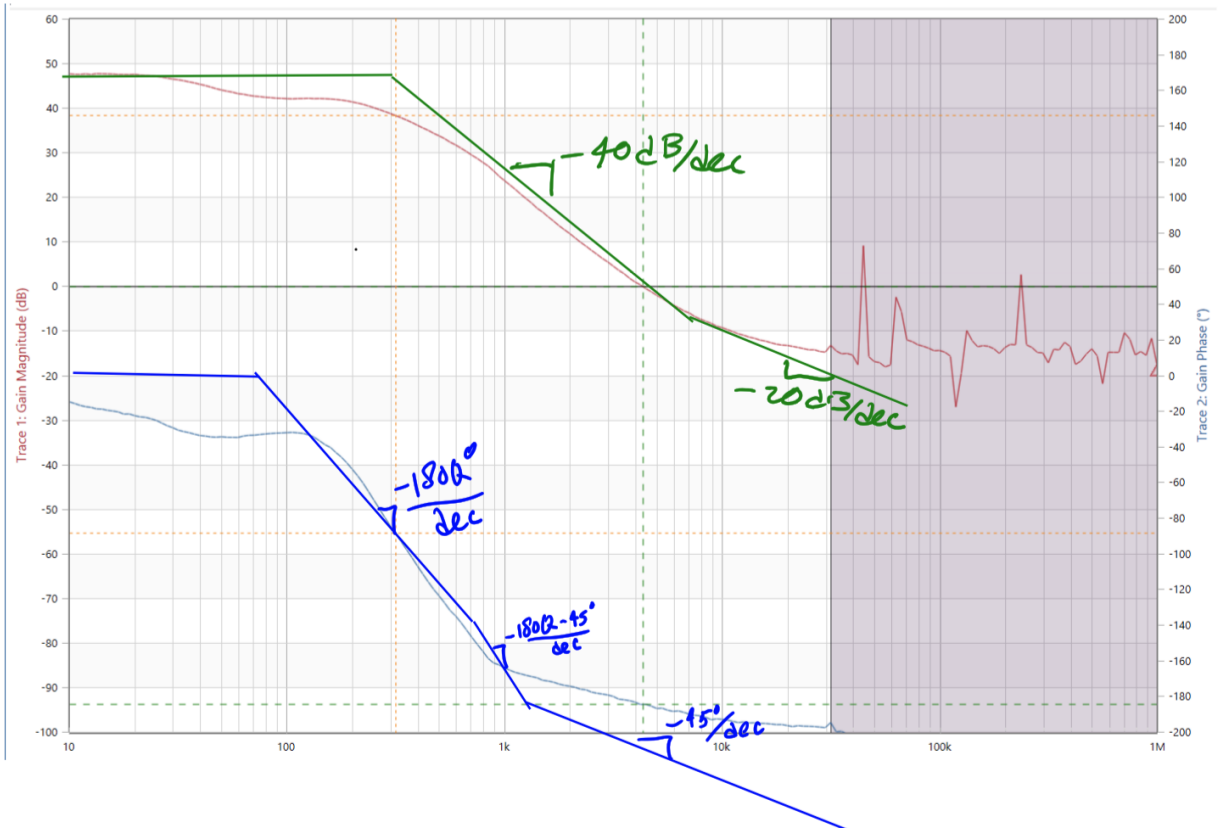


**Figure 6: Asymptotes fitted to measured $G_{VC}$ bode plot**

These asymptotes suggest a transfer function of the form:

$$G_{vc} = G_{d0}\frac{(1-\frac{s}{w_z})}{(1+\frac{s}{Qw_p}+(\frac{s^2}{w_p})}$$

The numerical values of the salient features of this transfer function are obtained from the plot:

DC gain: $G_{d0}$ = 47 dB

Complex conjugate pole: $f_P$ = 315 Hz, $Q_P$ = 0.77 (-2.28 dB)

RHP zero: $f_Z$ = 7 kHz

A small signal model for the cascaded boost converter is shown below:

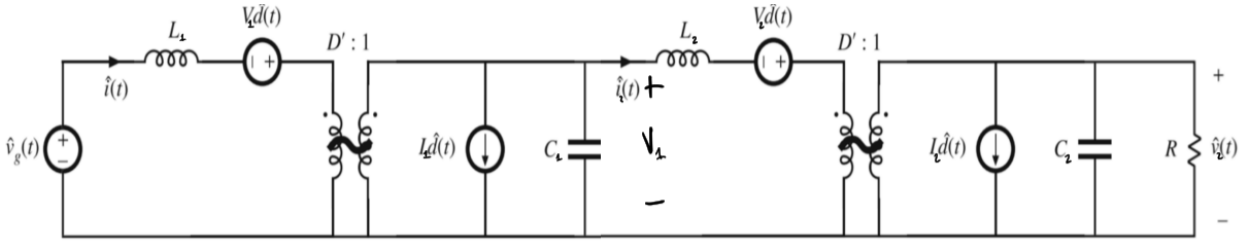


**Figure 7: Cascaded boost small signal model**

$G_{VC}(s)$ for a single boost converter is

$$G_{vc}(s) = \frac{V}{D'} \frac{(1 - \frac{Ls}{D'^2 R})}{(1 + \frac{Ls}{D'^2 R} + \frac{LCs^2}{D'^2})}$$

By approximating the first stage of the boost converter as a voltage source dependent on d(t), with $R=V_1/I_2$ as in figure 7,

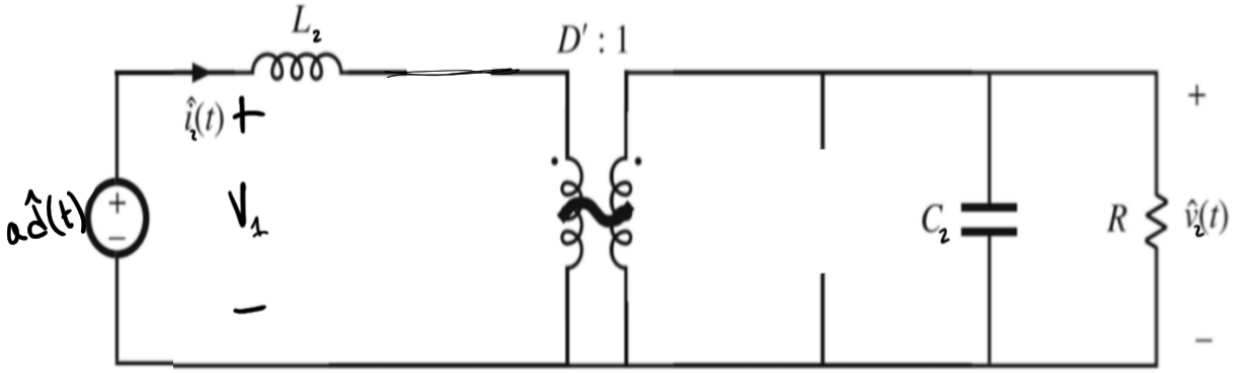


**Figure 8: Small signal model of cascaded boost, first stage approximated,**

**where** $$a = \frac{V_1}{D'} \frac{(1 - \frac{L_1 I_2}{D'^2 V_1} s)}{(1 + \frac{L_1 I_2}{D'^2 V_1} s + \frac{L_1 C_1}{D'^2} s^2)}$$

This model results in a $G_{VC}(s)$ for the cascaded boost as

$$G_{vc}(s) = \frac{V_1}{D'^2} \frac{(1 - \frac{L_1 I_2}{D'^2 V_1} s)}{(1 + \frac{L_2}{D'^2 R} s + \frac{L_2 C_2}{D'^2} s^2)(1 + \frac{L_1 I_2}{D'^2 V_1} s + \frac{L_1 C_1}{D'^2} s^2)} + \frac{V_2}{D'^2} \frac{(1 - \frac{L_2}{D'^2 R} s)}{(1 + \frac{L_2}{D'^2 R} s + \frac{L_2 C_2}{D'^2} s^2)}$$

This model is complex to simplify. In order to obtain numerical values for the salient features of this transfer function, the function was input to matlab. A transfer function mirroring that given by LTspice resulted.

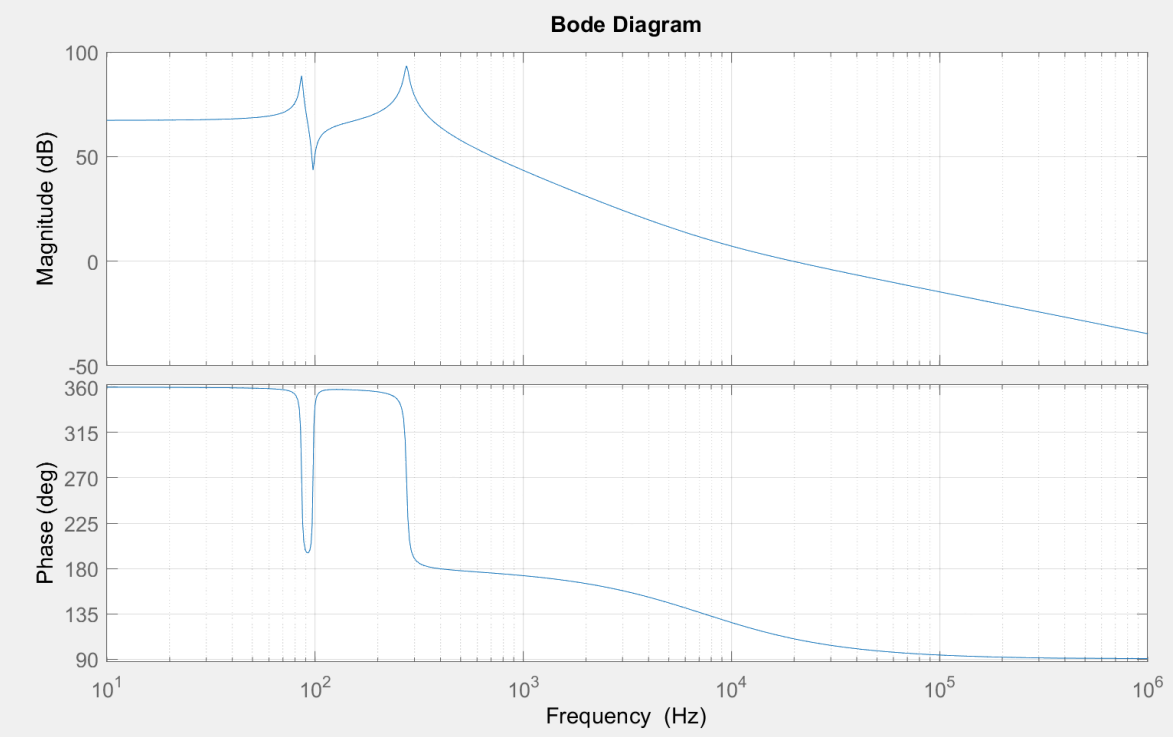


**Figure 9: Matlab generated bode plot of analytically derived $G_{vc}$**

This function contains the following features:

DC gain: 67 dB
Quadratic Pole: $f_{P1}$ = 86.1 Hz, $Q_{P1}$ = 21.6 dB (12.0)
Quadratic Zero: $f_{Z1}$ = 97.7 Hz, $Q_{Z1}$ = 23.5 dB (15.0)
Quadratic Pole: $f_{P2}$ = 275 Hz, $Q_{P2}$ = 26.4 dB (20.9)
RHP Zero: $f_{Z2}$ = 7.37 kHz

## Step 3: Compensator circuit design

Our measured Bode Plot was very similar to the Bode plot obtained in LTSpice using the 100 kHz values for our inductor resistances, which were higher than the 100 Hz inductor resistances. We concluded that while using the 100 kHz Inductor Resistances was less accurate in theory, in practice it effectively modeled parasitic resistances throughout the circuit, and as a result we would not need to change our compensator design from the Prelab, which is shown below.

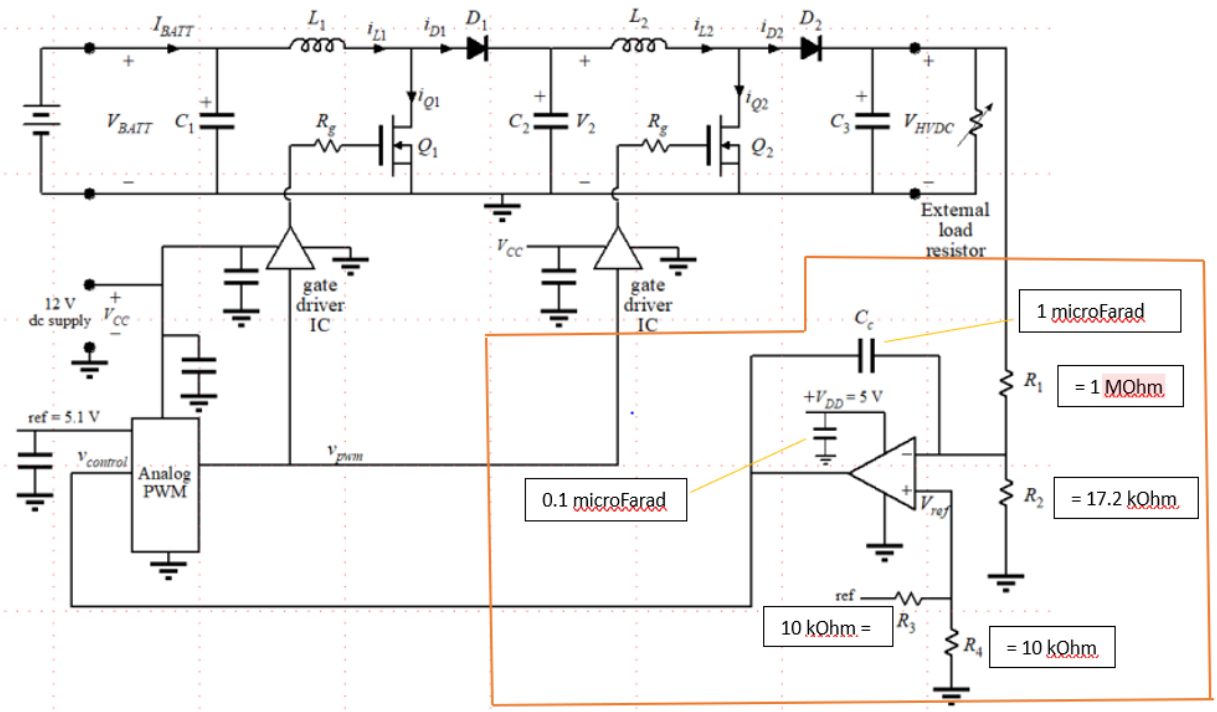


**Figure 10: Circuit diagram of our Integral Compensator combined with the rest of our Cascaded Boost Circuit. The Integral Compensator is highlighted in Orange.**

## Step 4: Start up of the closed-loop regulated converter

Once the integral compensator was connected to our cascaded boost converter, the control stage of the converter was powered up, and the frequency and duty cycle were recorded. As there was no power being provided to the power stage of the converter, the integral compensator always attempted to increase the voltage by maximizing the duty cycle. Therefore the recorded duty cycle is also the maximum duty cycle of the circuit.

The frequency was recorded as: 64.8 kHz,

And the maximum duty cycle was recorded as: 82.1%.

Due to an issue in the wiring of the non-inverting input of the op-amp, we added a large amount of capacitance to the soft-start mechanism to stop the input current from saturating. The final value of the capacitance used in the soft-start was 66 microFarads, and as a result the start-up time is much larger than the objective start-up time of 1 second. An oscilloscope capture of the output voltage during the converter start-up is shown below.

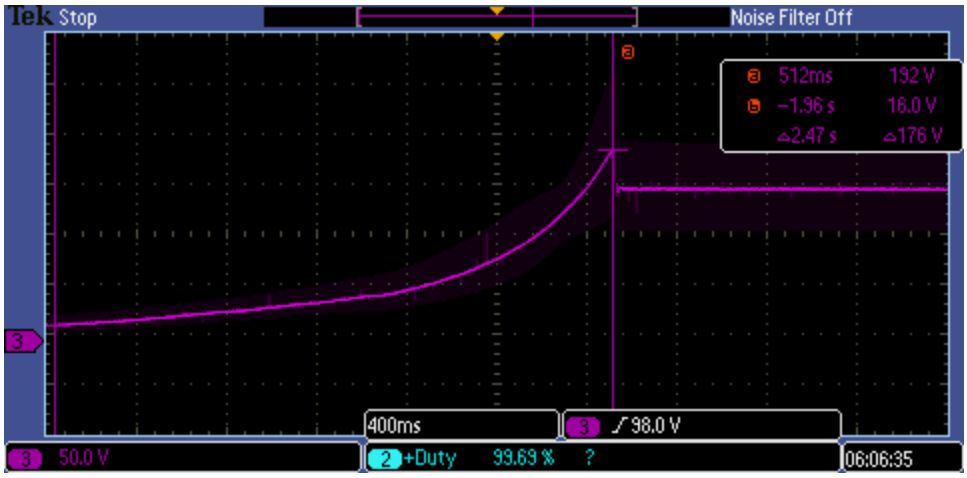


**Figure 11: Oscilloscope capture of the output voltage of the Converter during start-up. The start-up time is shown on the cursor measurements as 2.47 seconds**

## Step 5: Measurement of loop gain

The Bode 100 Network Analyzer was again used to measure the frequency response of the closed loop gain.

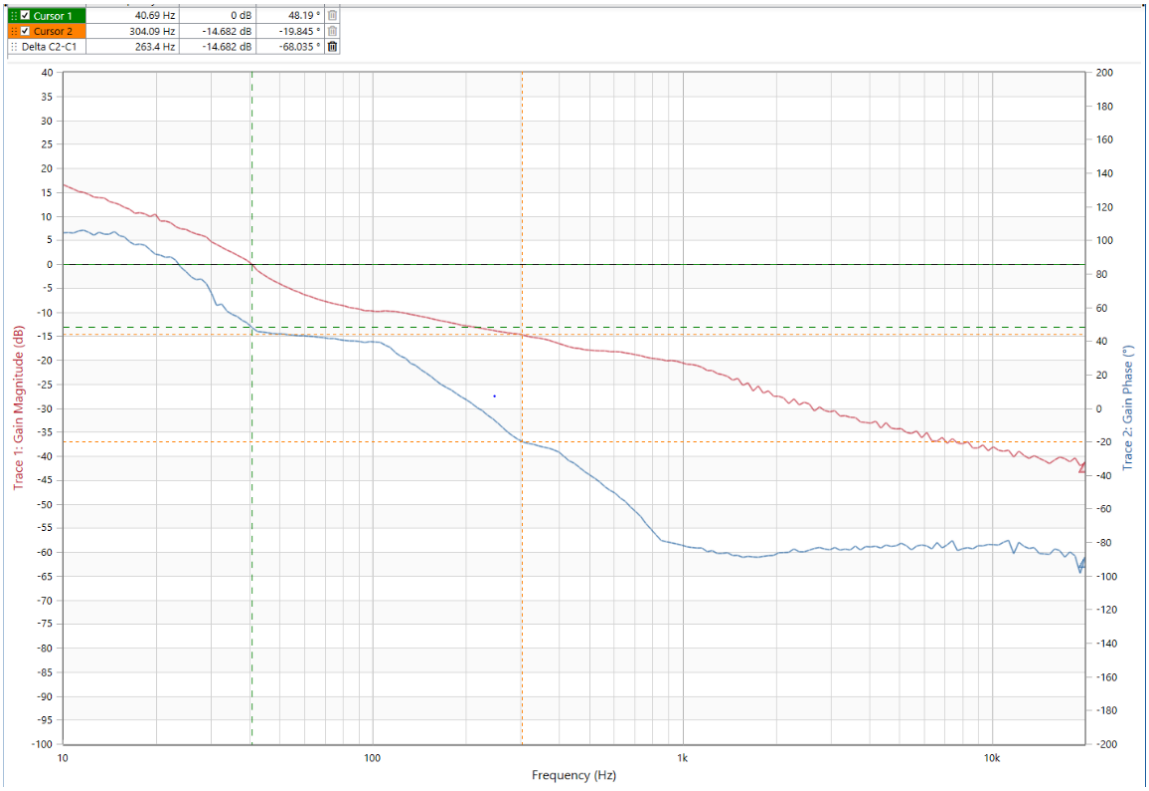


**Figure 12: Closed-loop loop gain measurement**

The crossover frequency of the closed-loop loop gain is 40.7 Hz, with a phase margin of 48.2° (the phase of the bode 100 network analyzer is shifted by 180°).

Simulation of this system using the higher inductor series resistances results in the following bode plot for the loop gain:


**Figure 13: LTspice simulated closed-loop loop gain**

While our simulated crossover frequency agreed with our experimental results, our simulated phase margin was much higher than our experimental. Our experimental phase margin was 40 degrees, far below our goal of 70 degrees. Our experimental phase is decreasing below the crossover frequency, so lowering the crossover frequency would increase the phase. Therefore, a possible solution is to add a resistor before the inverting input of the Op-Amp to lower the crossover frequency.

The transfer function of the control voltage over the output voltage can be expressed as shown below:

$$\frac{Vc}{Vout} = \frac{1}{sC_cR_1}$$

Adding a resistor before the inverting input of the Op-Amp makes it effectively a resistor in series with $R_1$, and the transfer function will become:

$$\frac{Vc}{Vout} = \frac{1}{sC_c(R_1 + R_{new})}$$

## Step 6: Regulation performance

The Voltage Regulation Performance of the Integral Compensator was tested with a 500 Ohm load and a nominal input voltage of 12.1 V. The output voltage with this nominal input voltage was recorded at 150.31 V. The input and output voltages and currents, as well as the efficiency and duty cycle, were measured at two extreme input voltages of 11 and 14 V. The For an input voltage of 11 V, the following results were obtained:
Input Voltage: 11.00 V
Input Current: 4.61 A
Output Voltage: 150.34 V
Output Current: 0.305 A
Duty Cycle: 74.5%
Efficiency: 90.5%

For an input voltage of 14 V, the following results were obtained:
Input Voltage: 14.02 V
Input Current: 3.5 A
Output Voltage: 150.27 V
Output Current: 0.302 A
Duty Cycle: 70.9%
Efficiency: 92.5%

The Closed-Loop Load Regulation for the Compensator can the Voltage Regulator can be calculated with the equation,

$$\frac{\Delta V}{V} = \frac{V_{HVDC,max} - V_{HVDC,min}}{V_{HVDC,nom}}$$

$$\frac{150.34V - 150.27V}{150.31V} * 100 = 0.047\%$$

With a Closed-Loop Load Regulation of 0.047%, our Voltage Regulator has excellent load-regulation performance.

## Step 7: Regulator improvements

The measured phase margin of the closed-loop loop gain is less than 70°. One simple way to adjust this is to decrease the DC gain to lower the crossover frequency, since the phase is decreasing in the vicinity of the current crossover frequency.
A 6.6 kohm resistor is added in series between the inverting input of the compensator op-amp and the output voltage of the converter.

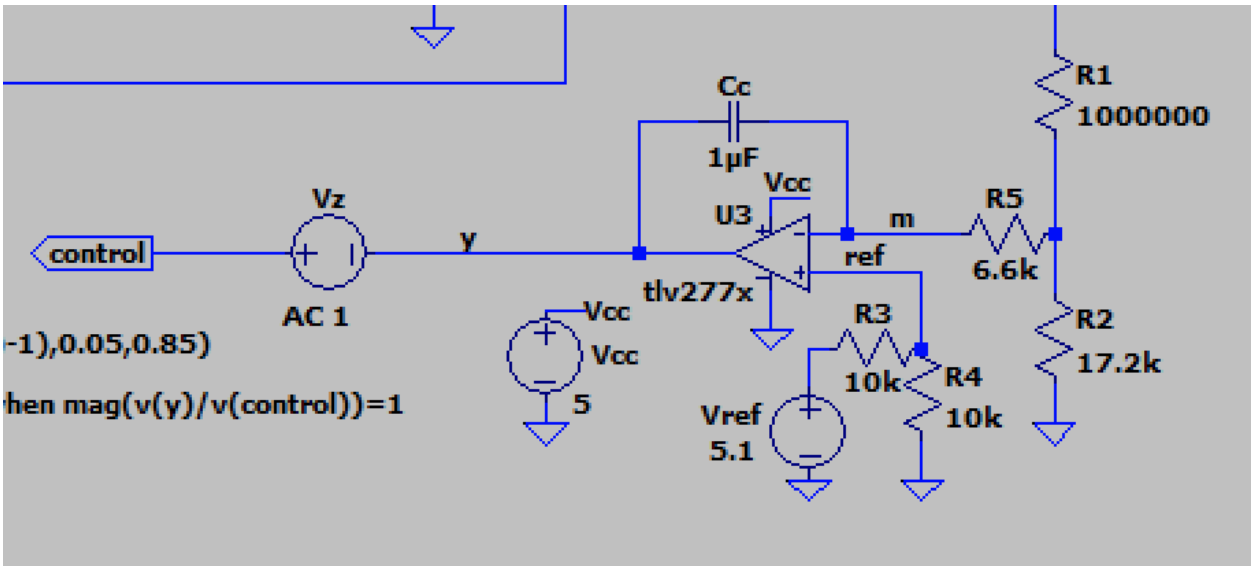


**Figure 14: Updated compensator design, with R5=6.6kohm added to decrease DC gain**

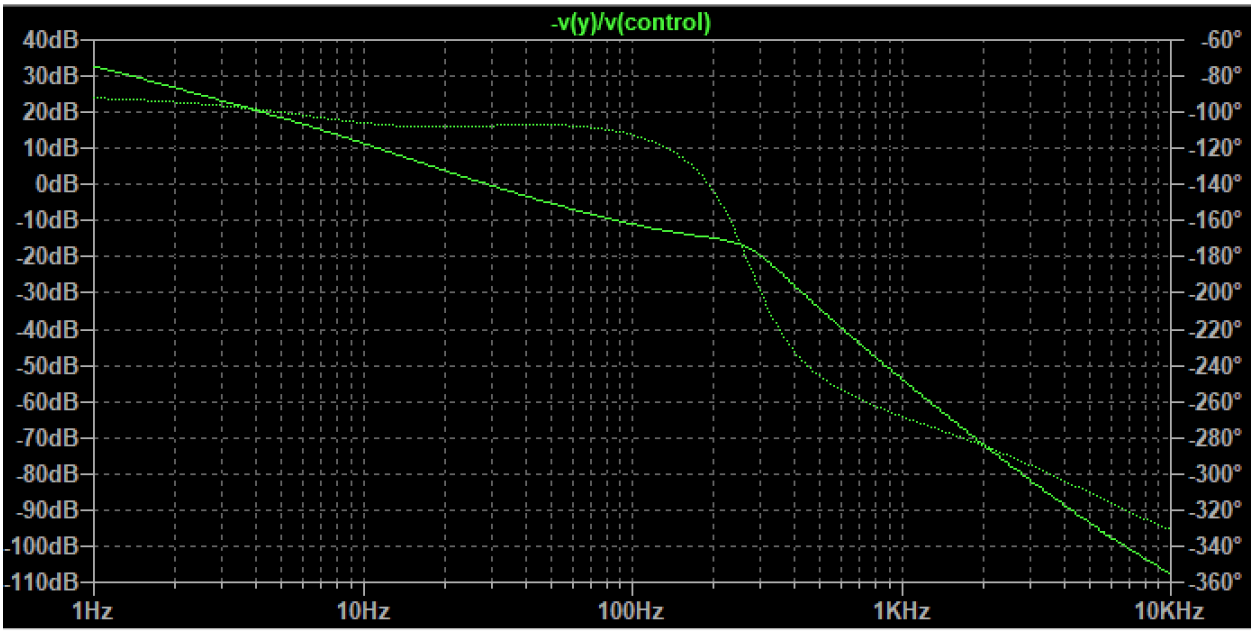


**Figure 15: Loop gain with update compensator design**

We can use simulation to verify our design. Using the higher parasitic series resistance values for the inductors as mentioned above, before updating the compensator, the simulated loop gain

matches well with the measured gain, with nearly identical crossover frequency (38.5 dB simulated vs 40.7 dB measured), except with a phase shift (73° phase margin simulated, vs 48.2° measured). Despite the phase shift, the magnitude response can still be used to determine the gain needed in the actual compensator. From the measured loop gain, it appears that lowering the DC gain to reduce the crossover frequency to about 30 Hz should result in a phase margin greater than 70°. In simulation, this is achieved with a resistor value of 6.6kohm.