Andrew Thibeault 2023-03-12

Plan of Record

The purpose of this lab is to design a "Golden Arduino" which meets the same connectivity specs as the commercial Redboard Arduino Uno, but has features for better noise control, assembly, test, and bring up.

The following features will be demonstrated on this board:

1) An Atmega 328 that will be bootloaded to turn it into an Arduino.
2) The Arduino IDE can be run on the board, along with any standard sketch.
3) The same header pin footprint as the commercial version will be used.
4) Noise should be 20 to 50% of the noise on the commercial board.
5) Near field emissions should be much less than 10% of that of the commercial board.

The stretch goals for this board are:

1) Test points will be added to the digital buses so that they can be viewed with a scope, in order to see the actual bus traffic on these digital lines.
2) A current sensing resistor will be added to the power rail so that in-rush and steady state currents can be measured. A differential pair of single ended probes will be needed to measure the voltage across this resistor.

Special design considerations to take note of for the components to be used follows:

- CH340g, the interface between the USB port and the UART to the 328
    - TXD on the CH340 connects to RXD on the 328, RXD on the CH340 connects to TXD on the 328.
    - Power Vcc at 5V; connect the 3.3 V pin to a decoupling capacitor only.
- Resonators
    - Will use ceramic resonators because of their smaller size, lower cost, and availability, despite their slightly lower stability than quartz crystals.
    - Need 22 pF shunt capacitors at each end of resonator to suppress higher order modes.
    - May need shunt resistor (1 Mohm) to kickstart oscillation, but noise should take care of this. I will include this on the 12 MHz crystal just in case.
    - Route traces from the crystal pins of the 328 to the crystal, and the capacitor traces, as short as possible due to noise sensitivity and trace capacitance; no vias, or routing over gaps in the return path.
- Debouncing circuits for the 328 reset pin: used to prevent bouncing on the switch to avoid multiple resets
    - A manual switch will be added to the normally-pulled-high reset pin to allow manual reset. A resistor and capacitor pair with time constant 10 msec (i.e., 1 uF and 10 kohm) will be used in the following configuration to prevent bouncing on the reset pin.

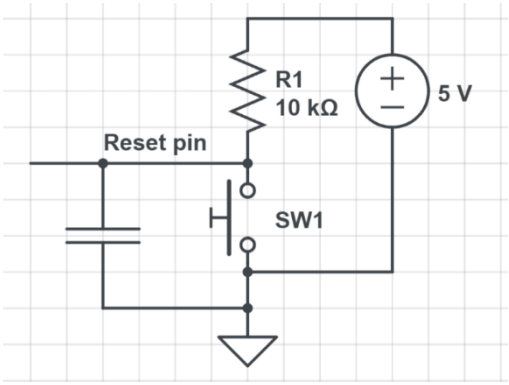

Figure 1: Deboucing Circuit

    - The CH340g DTR pin will also be used to trigger a reset. The DTR is pulled low for many seconds while communicating over the USB bus, so a high pass filter will be used to only allow the initial pulled low signal to trigger the reset. This will be implemented using a series capacitor between the DTR pin and the Reset pin, with the capacitance much larger than the capacitance in the debounce circuit (e.g. If the debounce capacitor is 1 uF, then the high pass capacitor should be at least 22 uF).
- The ATmega 328 microprocessor
    - Note that the RXD pin of the 328 is PD0 and the TXD is PD1.
    - Put indicator LEDs on the TX and RX pins using a 10k resistor and series LED. These are default logic level high (low when transmitting), so the LEDs should be connected between 5V and TX/RX instead of TX/RX to GND.
    - Use a separate connection to the AVCC and VCC pins, and each gets their own decoupling capacitor. Add an LC filter between the power rail and the AVCC pin to keep noise on the Vcc rail from propagating to the AVCC rail, using a ferrite bead (10 uH, with a 22 uF decoupling capacitor)
    - All pins should come out to header pins except for the RX and TX pins which connect to the 340 chip. The 16 MHz crystal connects to the XTAL pins.
- The TVS chip will be used to protect a connected computer from high voltage discharge to the USB hub chip on the computer.
    - Connect GND to pin 2, 5 V to pin 5, D+ to pin 1, and D- to pin 3, where D+ and D- are data lines.
- Power
    - Instead of using a linear regulator to drop power from 7-12V to 5V, will instead require 5V to be supplied to board.

Final Board Design Details

The final schematic and layout of Board 3 are shown on the following two pages.

As can be seen in the schematic, 22 uF decoupling capacitors are included on every power die on the ICs, as well as near each power header pin. These decoupling capacitors are placed close to their respective pins in the layout.

The board is well labeled, and testing and operation was easy due to this.

Generally, the layout is well organized, though it became slightly congested with all of the extra test points and by the use of 1206 parts. Soldering components in the vicinity of the resonators for the 328 and the CH340 was difficult due to the necessary close proximity of all of these parts. A plan had to be developed for soldering these parts after several soldering mistakes were made initially; solder the ICs first, with the smallest pins, followed by using solder paste on the ceramic resonators (the large pad area and conduction of the resonators made soldering difficult due to heat loss, and the conductive layer on top of the resonators necessitated minimal solder usage to avoid shorts), followed by the remaining capacitors and resistors which are located towards the outside of these areas.

One other area that could be improved is the orientation and routing of the ATMEGA328. This component was placed near last in my layout design, which constrained the routing, and a non-ideal orientation of the IC was chosen which necessitated longer trace lengths. This was not realized until late in the routing, so it was left in place. This will be improved on Board 4.

Cross-unders had to be used relatively extensively, especially in the vicinity of the ATMEGA328, as shown below. This is particularly a problem in this area, where the signal lines are concentrated and noise reduction is most important. This could be improved with better orientation of the ATMEGA, relocation of the ISP pins and reset circuitry, or use of a 4-layer board to avoid breaks in the ground plane.

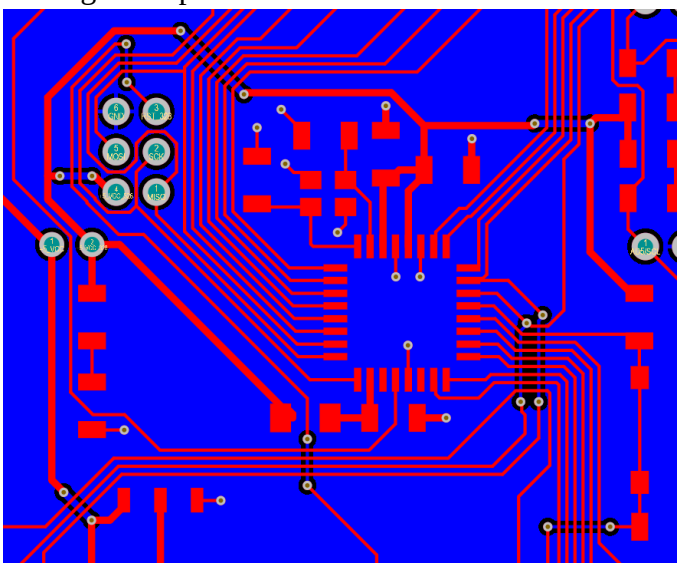

Figure 2: Layout in vicinity of ATMEGA328

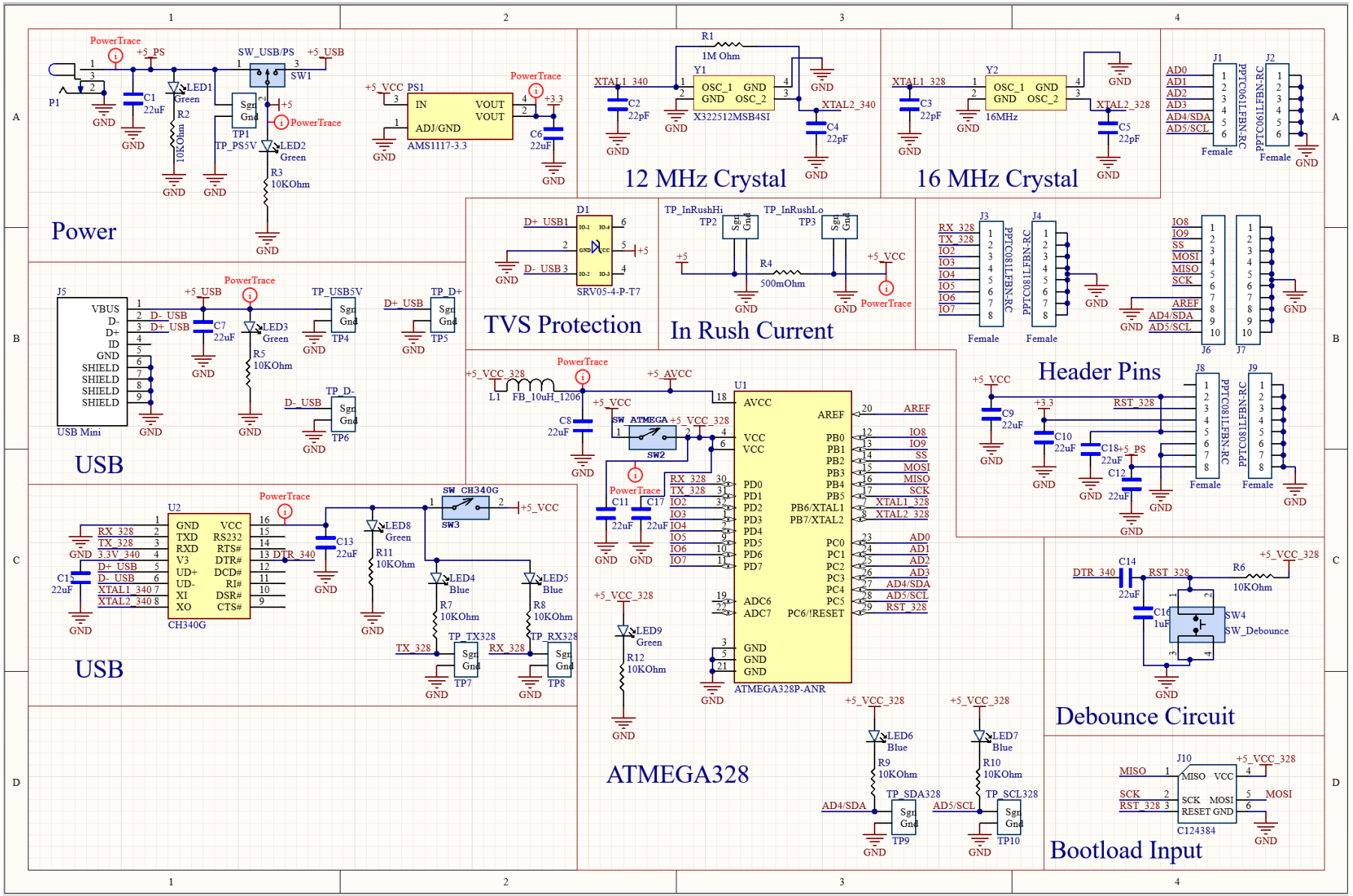

Figure 3: Board 3 Schematic

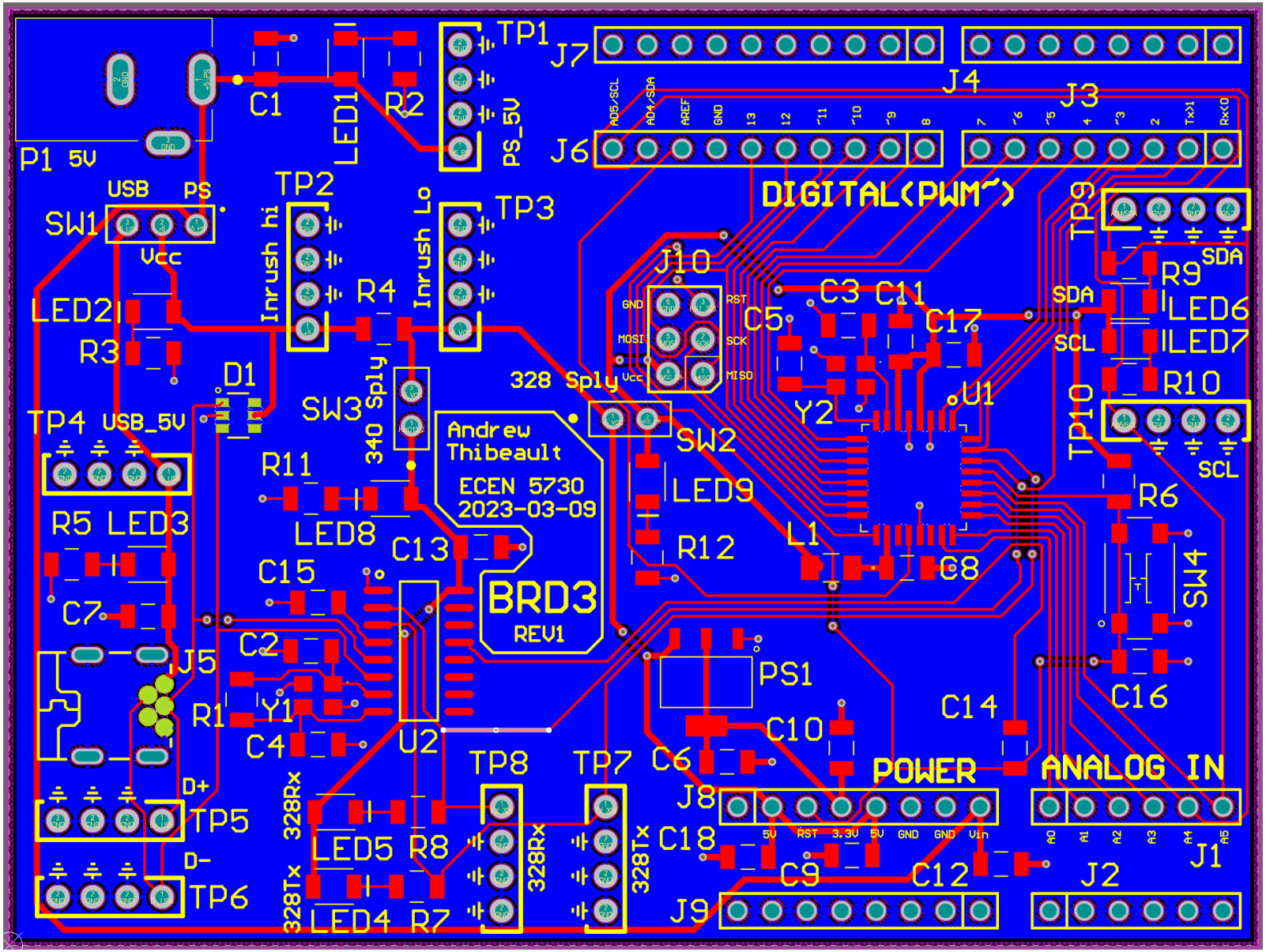

Figure 4: Board 3 Layout

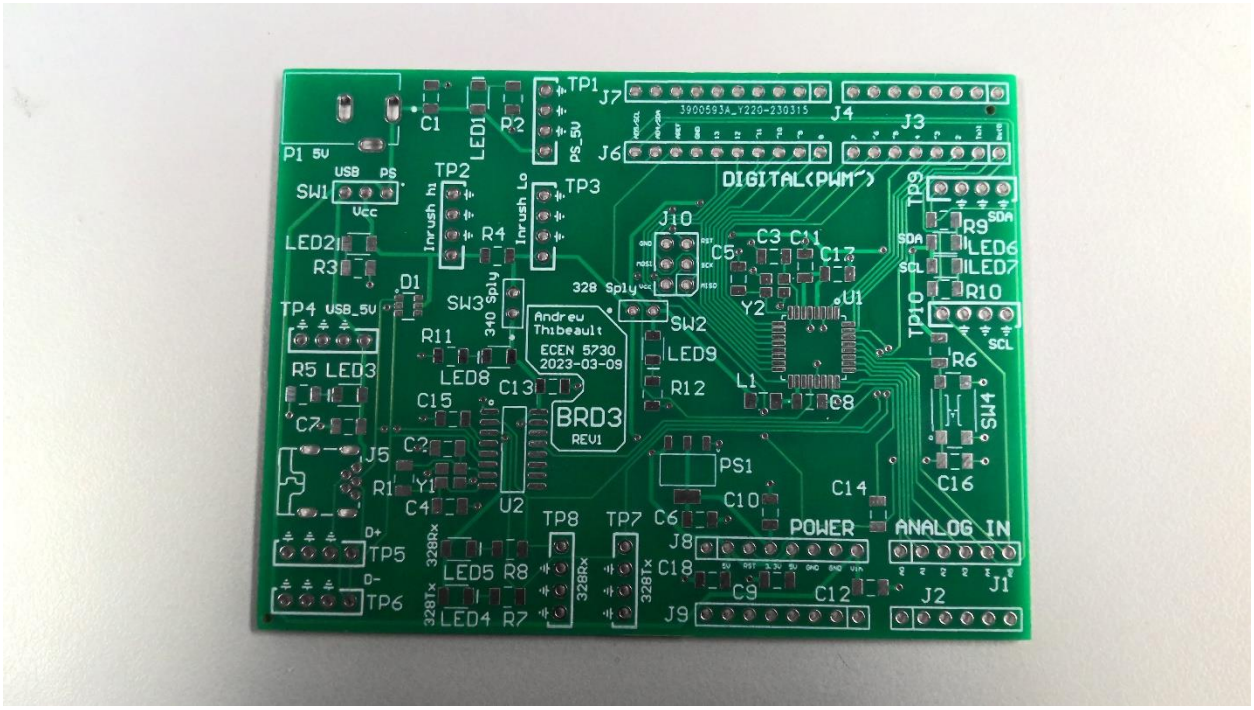

Figure 5: Bare Board 3

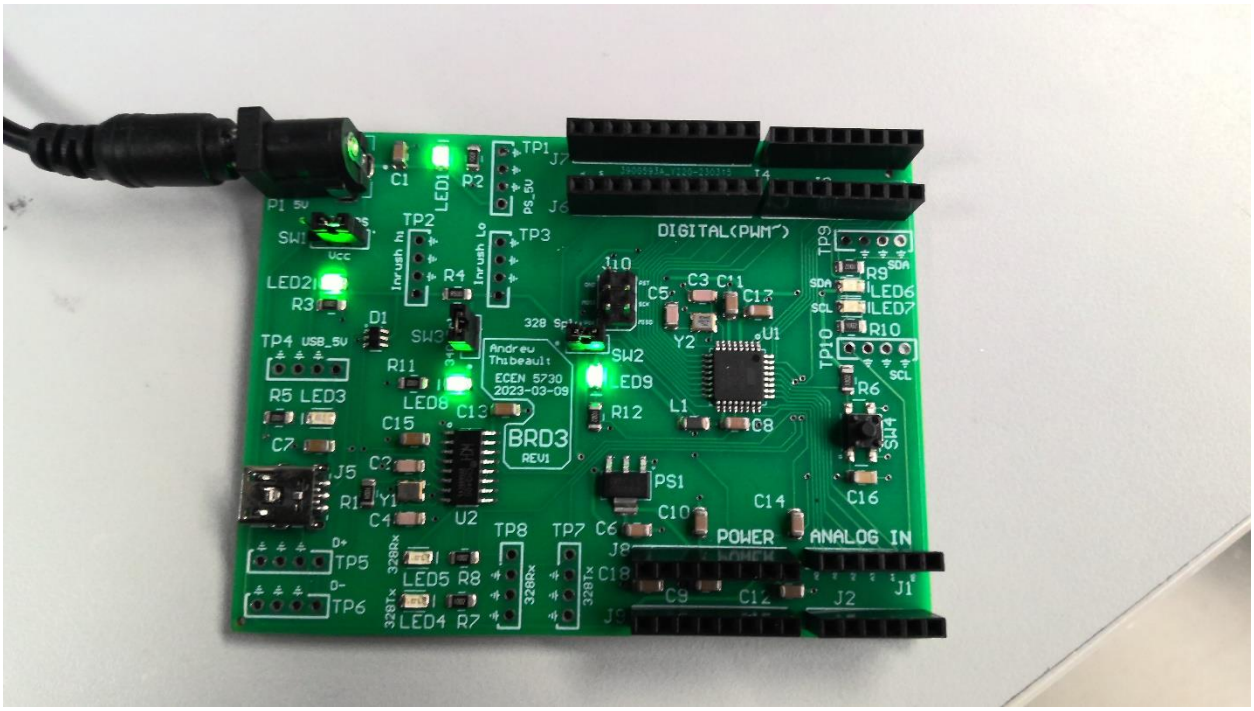

Figure 6: Fully Assembled and Powered Board 3

Functioning of Board 3

The board powered up successfully. One issue was noticed in initial testing, that the 328 received power when the 340 was powered, but SW2, which isolates the 328 from power, was open. My assumption is that the Rx and Tx connections between the 340 and 328 supplied power to the 328, as these pins are normally high. This bug did not present any issues in operation of the board, when SW2 was closed.

The boot loader code was successfully burned onto the Atmega 328 without issue.

The simple blink program was run on the Arduino, with the delay adjusted to pulse the signal at 5 Hz:

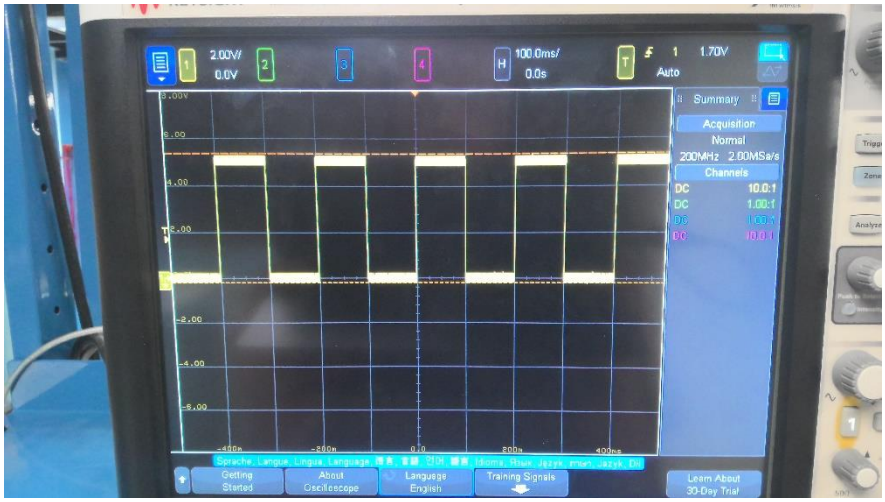

Figure 7: Pin 13 on Board 3 while running Blink with delay adjusted to pulse at 5 Hz

An LED was not included on pin 13 of Board 3, as is the default location of the “Builtin LED” on Arduino Unos. This will be included on Board 4, so that programs using indicator LEDs can be operated without the need to watch for the signal on pin 13.

Performance of Board 3

Switching noise was compared between a commercial Arduino and my Board 3 design. An Arduino program was run on the board that switches pins 10-12, loaded with about 50-60 mA total load current, and asynchronously switches pin 7 controlling a heavily loaded MOSFET (about 350 mA load current). With the Atmega as the aggressor signal (pins 10-12 switching), noise was measured at quiet-high (measuring noise on power rail) and quiet-low (measuring ground bounce and cross talk noise) test points on the Atmega die, as well as on the power rail further from the chip. With the board as the aggressor (pin 7, MOSFET switching), power rail noise was measured at the power rail test point and the quiet-high test point.

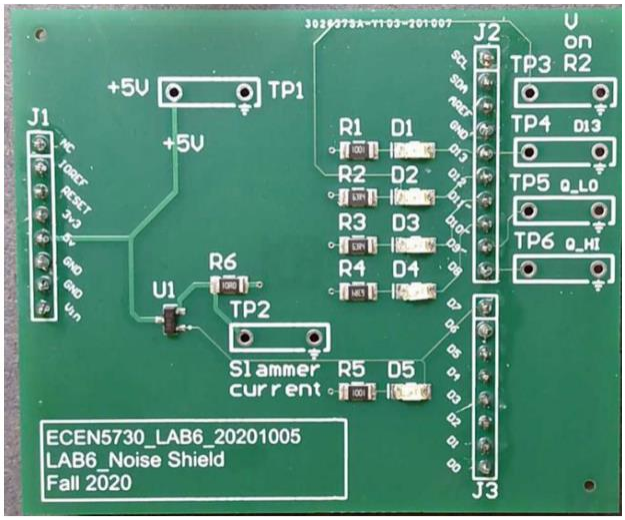

Figure 8: Shield used for testing noise

Results are tabulated below for both boards. In the measurements tables, the noise on Board 3 as scaled proportionally to the dI/dt of the commercial board rising and falling edges is included. This is not a rigorous comparison, but is included to demonstrate the noise reduction taking into account the faster switching on Board 3 (which itself is due to the reduction in loop inductance).

Board	V_on 63 ohm resistor (TP3)	Estimated Total Aggressor Current	Rise Time	Fall Time	Q_LO Noise (TP5), Rising Edge	Q_LO Noise (TP5), Falling Edge	Q_HI Noise (TP6), Rising Edge	Q_HI Noise (TP6), Falling Edge	Power Rail Noise (TP1), Rising Edge	Power Rail Noise (TP1), Rising Edge
Keyestudio Arduino Uno	1.59 V	77 mA	7.0 ns	6.7 ns	277 mV	683 mV	387 mV	393 mV	32 mV	53 mV
Board 3	1.92 V	93 mA	5.5 ns	6.1 ns	249 mV	572 mV	333 mV	316 mV	30 mV	45 mV
Board 3 (noise scaled to Keyestudio dI/dt)			(0.65 scale factor)	(0.75 scale factor)	161 mV	429 mV	216 mV	237 mV	20 mV	34 mV

Table 1: Noise Measurements with Atmega 328 as Aggressor Signal

Scenario	Noise as Percent of Commercial Board Noise					
Scenario	Q_LO Noise (TP5), Rising Edge	Q_LO Noise (TP5), Falling Edge	Q_HI Noise (TP6), Rising Edge	Q_HI Noise (TP6), Falling Edge	Power Rail Noise (TP1), Rising Edge	Power Rail Noise (TP1), Rising Edge
Board 3 Measured	89.9 %	83.7 %	86.0 %	80.4 %	93.8 %	84.9 %
Board 3 Scaled	58.1 %	62.8 %	55.8 %	60.3 %	62.5 %	64.2 %

Table 2: Board 3 Noise as Percent of Commercial Board Noise with Atmega 328 as Aggressor Signal

Board	V_on 10 ohm resistor (TP2)	Estimated Total Aggressor Current	Rise Time	Fall Time	Q_HI Noise (TP6), Rising Edge	Q_HI Noise (TP6), Falling Edge	Power Rail Noise (TP1), Rising Edge	Power Rail Noise (TP1), Rising Edge
Keyestudio Arduino Uno	3.5 V	350 mA	20.0 ns	8.0 ns	443	253	480	720
Board 3	3.65 V	365 mA	19.1 ns	7.6 ns	384	258	531	730
Board 3 (noise scaled to Keyestudio dI/dt)			(.916 scale factor)	(.91 scale factor)	349	235	483	664

Table 3: Noise Measurements with board as Aggressor Signal

Scenario	Noise as Percent of Commercial Board Noise			
Scenario	Q_HI Noise (TP6), Rising Edge	Q_HI Noise (TP6), Falling Edge	Power Rail Noise (TP1), Rising Edge	Power Rail Noise (TP1), Rising Edge
Board 3 Measured	86.7 %	102.0 %	110.6%	101.4%
Board 3 Scaled	78.8 %	92.9 %	100.6 %	92.2 %

Table 4: Board 3 Noise as Percent of Commercial Board Noise with Atmega 328 as Aggressor Signal

With the chip as the aggressor signal, power rail noise (Quiet-high), as well as ground bounce and crosstalk noise (Quiet-low) are reduced, and the output pins are able to switch faster. The goal of achieving 20-50% of the noise of the commercial board was not achieved, though the scaled measurements near the 50% mark. The reduction in noise is due to several factors. In comparison to the commercial Arduino, my Board 3 has more decoupling capacitance placed closer to each IC, as well as using a continuous ground plane rather than individual ground traces. Likely the bigger factor is the use of the continuous ground plane, as the Keyestudio Arduino appears to use 0402 capacitors placed not too far from the respective ICs. Using 0402 capacitors decreases the inductive loop length in comparison to the 1206 parts used on my Board 3. Example scope traces are shown below that visually demonstrate the reduction in noise.

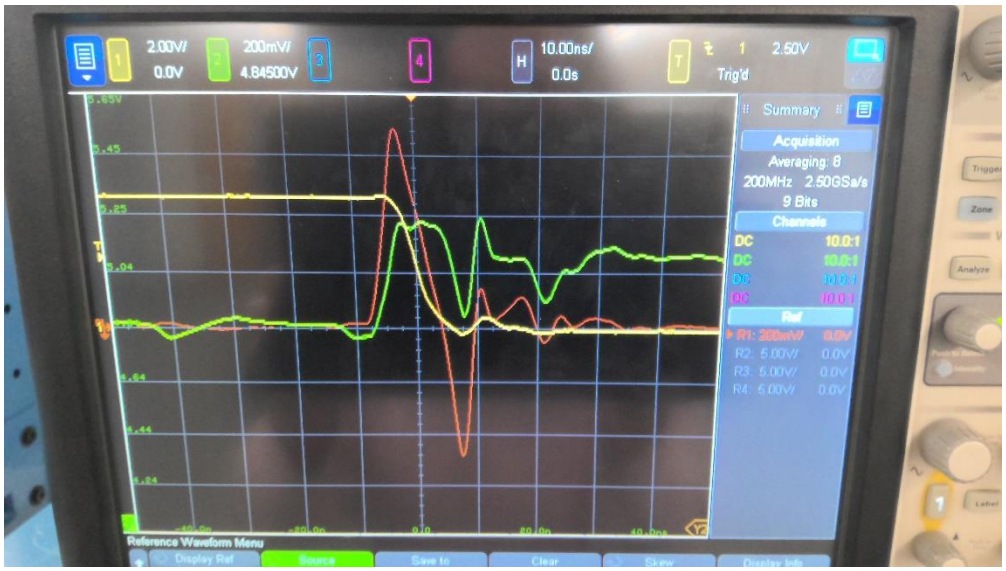

Figure 9: Noise on Commercial Arduino QHi (green) and QLo (red) test points with Atmega as Aggressor Signal (yellow)

Figure 10: Noise on Board 3 QHi (green) and QLo (red) test points with Atmega as Aggressor Signal (yellow)

With the board as the aggressor signal, there is a minimized reduction in noise on my Board 3 as compared to the commercial board. The power rail noise is essentially the same on both boards, though it makes sense that this would not be affected much, since there is not capacitance near to the power rail test point to decouple the test point from the signal effects. There is capacitance closer to the Qhi pin via decoupling capacitance on the Atmega 328 on my board 3, so some reduction in rail noise on the IC die makes sense.

Finally, the near field emissions synchronous with the MOSFET switching signal were measured with a 10x probe shorted to its own ground with a small loop, placed near to the board, as in the picture below.

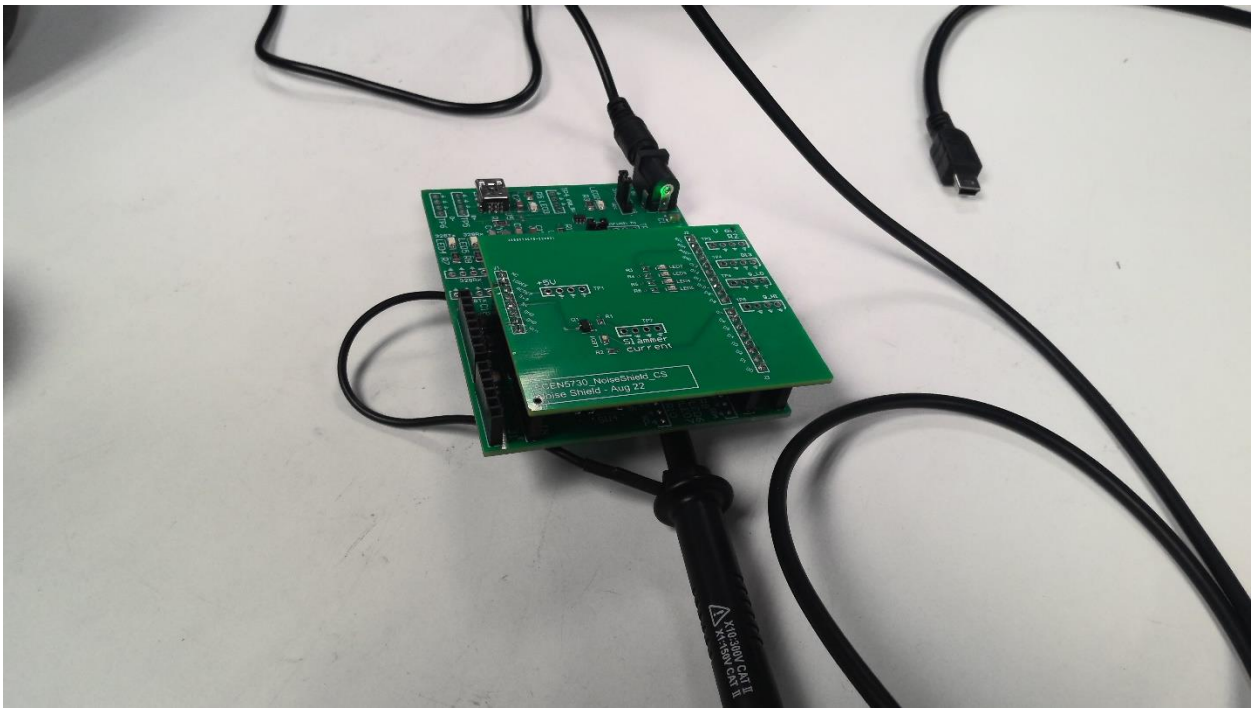

Figure 11: Near Field Emissions Measurement Setup

Board	Near field emissions, rising edge	Near field emissions, falling edge
Keyestudio Arduino	101 mV	164 mV
Board 3	44 mV	47 mV

Table 5: Near Field Emissions Measurements Synchronous with MOSFET switching

The near field emissions are reduced considerably in my Board 3, likely due to the shorter inductive loops from the use of close decoupling capacitors and a continuous ground plane (shorter return path with continuous ground plane).

Inrush Current Measurements

Inrush current onto Board 3 at power-on was measured using the differential test points across the 500 mohm sense resistor in series with the power rail. With the board initially powered off, a single trigger event was captured when power was connected. The scope trace below shows a math function of the voltage difference between the differential test points at power-on.

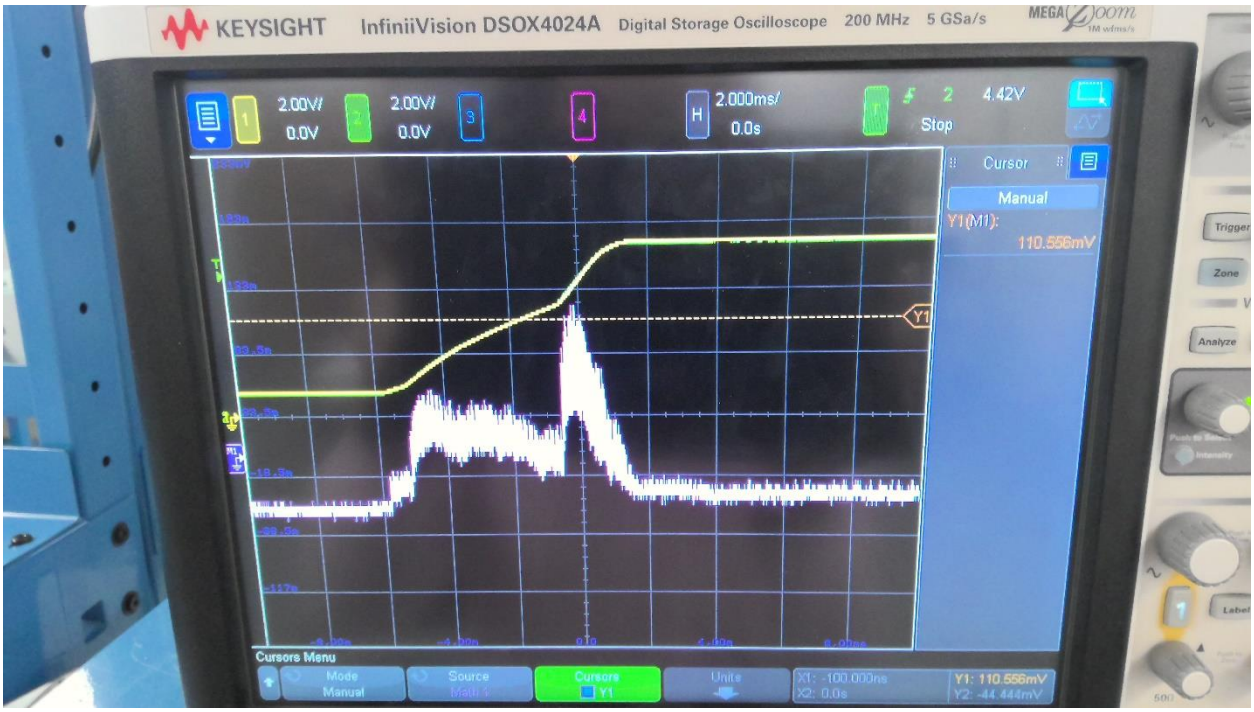

Figure 12: Inrush current at power-on of Board 3, differential voltage across sense resistor in purple

The differential voltage peaks at 110 mV, giving a peak inrush current of 220 mA. This current is well within the rating for the components used, despite the large amount of decoupling capacitance on the board that draws the inrush current.

Conclusion

This design for Board 3 successfully functioned as an Arduino, successfully burning the bootloader code onto the Atmega 328 and running simple sketches. The power rail noise and ground bounce and cross talk noise on my Golden Arduino was reduced to 50-70% of the noise on a commercial Arduino, due to the use of closely placed decoupling capacitors and the use of a continuous ground plane. Inrush current is within acceptable margins for the components used.

My board could be improved by better arrangement of components, particularly the orientation of the Atmega 328 in order to decrease the length of the signal traces. The use of a 4-layer board would help reduce the number of cross-unders used, which cause breaks in the return plane. These documented deficiencies demonstrate the benefit of prototyping a board before releasing to production.