

Experiment #3

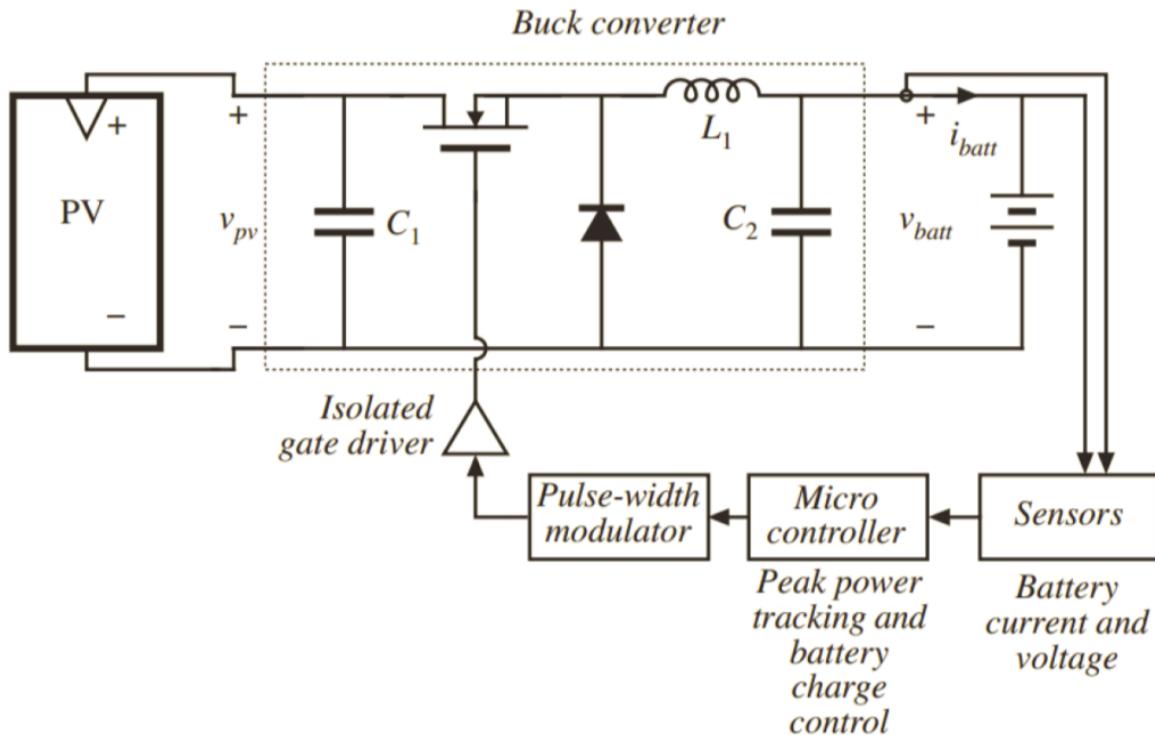
DC-DC Converter for Maximum Power Point Tracking (MPPT) and Charge Control

Part 1: Open-Loop Buck DC-DC Converter

Andrew Thibeault and Dane Thorn
ECEN 5517
2023-02-27

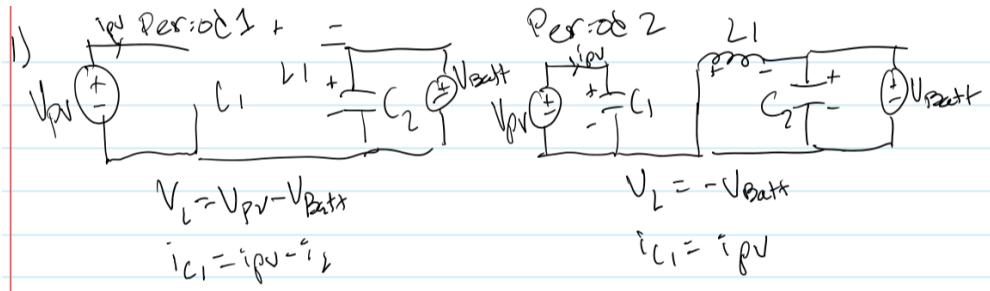
Introduction

The objective of this experiment is to design, construct, test, and demonstrate a buck DC-DC converter performing maximum power point tracking (MPPT) and battery charge control. Part 1 of this experiment is to focus on the converter operating in open loop, while the MPPT and charge control functions are addressed in Part 2. The circuit for the buck converter is shown below. An input filter is included through the use of C_1 . Battery current and voltage sensing circuitry will be included to perform peak power tracking and battery charge control (avoiding overcharging the battery). A transformer-isolated high-side gate driver is used to provide a large enough voltage at the gate to turn the MOSFET on while isolating the power circuitry voltages from the microcontroller.



Prelab 1

This prelab dealt with selecting components for the converter based on voltage and current stresses at expected operating points, as well as designing the inductor we would wind in class.



Charge balance: $i_{C1} = 0 = D(i_{PV} - I_L) + D' i_{PV}$

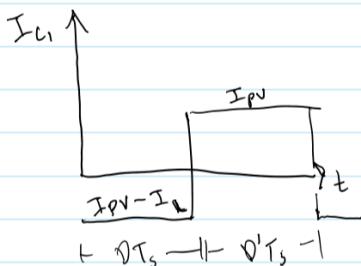
$$D = i_{PV} - DI_L$$

$$D = \frac{V_{Batt}}{V_{PV}} = \frac{13V}{12V} = .756 \Rightarrow I_L = \frac{i_{PV}}{D} = \frac{4.95A}{.756} = 6.55A, \text{ average inductor current}$$

$$2\Delta i_L = D'T_s \left(\frac{V_{Batt}}{2} \right), \text{ Selecting } f_s = 100 \text{ kHz}, \quad 2(.1 \cdot 6.55A) = (1 - .756) \left(\frac{1}{100 \text{ kHz}} \right) \cdot \left(\frac{13V}{2} \right)$$

$$L = 24.2 \mu H$$

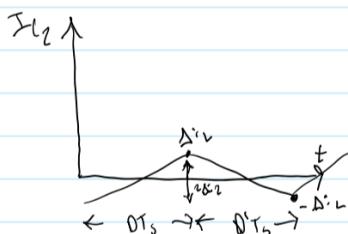
2) Current waveforms



$$\text{Max: } i_{PV} = 4.95 A$$

$$\text{Min: } i_{PV} - I_L = -1.6A$$

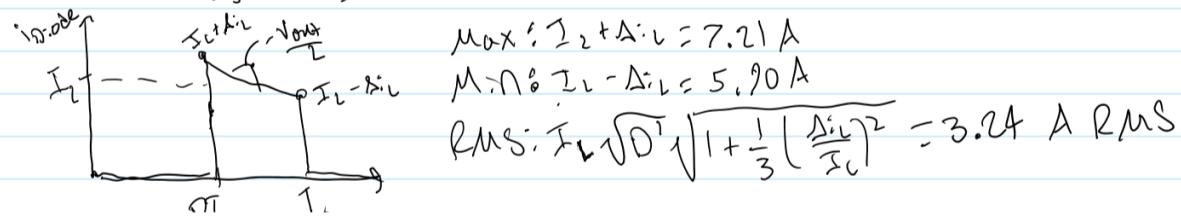
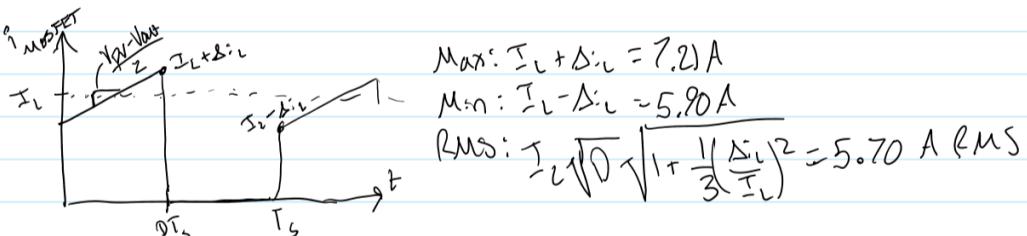
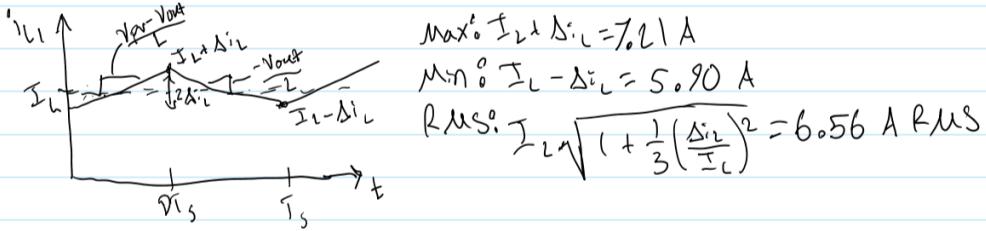
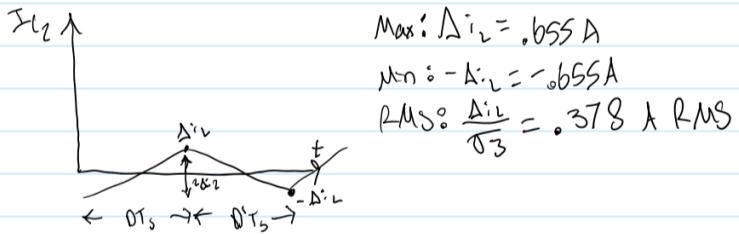
$$\text{RMS: } \sqrt{D(i_{PV} - I_L)^2 + D'(i_{PV})^2} = 2.81 A \text{ RMS}$$



$$\text{Max: } \Delta i_L = .655 A$$

$$\text{Min: } -\Delta i_L = -0.655 A$$

$$\text{RMS: } \frac{\Delta i_L}{\sqrt{3}} = .378 A \text{ RMS}$$



3) In this design, we can neglect core loss due to low ripple

core geometry
 choose $K_g: K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u}$ choose $B_{max} = 0.25$ as conservative limit
 $R \approx \text{Max power loss } 1W \rightarrow I^2 R = 1W \quad (I = I_{L,RMS} = 6.56A)$
 $R = 0.0232 \Omega$

$= 5.02 \cdot 10^{-3} \text{ cm}^5$
 \downarrow
 Kn : 5 as conservative estimate
 $I_{max} = I_{L,max} = 7.21A$
 $\rho = 1.724 \cdot 10^{-6} \Omega \cdot \text{cm}$
 Both core options are larger than this, so choose the smaller, $\boxed{PQ 26/25} \rightarrow A_c = 1.08 \text{ cm}^2, w_A = 0.503$

choose $n: n = \frac{L I_{max}}{B_{max} \cdot A_c} = 4.93 \rightarrow \text{round to } \boxed{5 \text{ turns}}$

wire
 choose $l_g: l_g = \frac{w_A \cdot A_c \cdot n^2}{l} = 0.153 \text{ mm} \rightarrow \boxed{0.00602 \text{ inches}} \text{ (unit shown in inches)}$

choose wire size $A_w: A_w \leq \frac{K_u w_A}{n} = 0.0503 \text{ cm}^2 \rightarrow \text{choose AWG 11}$

Due to AWG 11 not being a standard wire size, I would design for wire size before # of turns in the future.

4) $C_1: 3300 \mu\text{F}$ Rated voltage: 35V - This is well above maximum of V_{oc} of panel, 22.2V
 Rated ripple current (RMS): 40.80 A RMS - This is actually below what we expect to operate at: 6.56 A RMS. We may want a larger capacitor.

$C_2: 330 \mu\text{F}$ Rated voltage: 25V - Well above max of V_{back}
 Rated Ripple current (RMS): 865 mA - This is well within our expected ripple current, 378 mA RMS

MOSFET: Breakdown voltage: 55V
 Drain current maximum: 35 A } Both are well inside expected operating point maximum

Diode: Peak Reverse voltage: 45V
 Max forward current: 16A } Both are well within our expected max operating point.

Step 1: Initial Inductor Design

A further inductor design, considering laboratory available components, is shown below.

In order to reduce losses, we wanted to design our inductor with a current ripple of 20%.

Using initial parameters of :

$f_s = 100 \text{ kHz}$, $V_{out} = 13 \text{ V}$, $V_{mpp} = 17.2 \text{ V}$

and for an ideal Buck Converter

$$D = V_{out}/V_{mpp} = 0.76$$

We'll calculate our current ripple using I_{mpp} , as if our MPPT works ideally, the PV panel will operate at its MPP.

$$\text{Current ripple} = dI = 0.2 * I_{mpp} / D = 0.2 * (4.95A / 0.760) = 1.31 \text{ A}$$

$$L = (V_{mpp} - V) * (D/f_s) * (1/2dI)$$

$$L = 12.18 \text{ microHenries}$$

Which we'll round up to 13 microHenries to be safe.

To design our inductor we started by selecting our core size from the two sizes available. We selected the PQ 26/25 core, with a geometrical constant K_g of 0.125. Then we selected our wire gauge, number of turns, and air gap size to meet our goal of 13 microHenries.

We selected a wire of a small size in order to reduce the number of turns needed, reducing losses in the wire.

We then estimated an adequate number of turns. Using that, we calculated our gap length, and then checked that it did not exceed the restrictions of our geometric constant. The process and Results of our initial inductor plan are shown below.

Selecting PQ 26/25 core:

$$K_g = 0.125$$

$$A_c = 1.18 \text{ cm}^2$$

$$W_a = 0.503 \text{ cm}^2$$

$$MLT = 5.62 \text{ cm}$$

$$L_m = 5.55 \text{ cm}$$

Core weight = 36g

Rho = 1.725×10^{-6} Ohms*cm

μ_0 = permeability of free space = $4\pi * 10^{-7} N^2 * A^{-2}$

I_{sc} = Short circuit current = 5.45 A

K_g = $0.125 > (\rho L^2 * I_{max}^2 / (B_{max}^2 * R * K_u) * 10^8)$

nI_{max} = $B_{max} * lg / \mu_0$

B_{max} = 0.25 T

I_{max} = (I_{sc}/D)*1.1

(I_{max}/B_{max})² = (lg/(\mu₀*n))²

$\rho L^2 * lg^2 / (R * K_u * \mu_0^2 * n^2) = Aw * L^2 * lg^2 / (\rho * n * MLT * \mu_0^2 * n^2 * K_u)$

$0.125 > (13 \text{ microHenries})^2 * lg^2 * Aw / (\mu_0^2 * n^3 * \rho * MLT * K_u)$

Assume K_u = 0.5 to be safe

Pick wire size Aw AWG 44

13 microHenries = $(4\pi * 10^{-7} N/A^2) * 1.18 * 10^{-2} * 10^2 / lg$

Guess n = 10

lg = $\mu_0 * A_c * n^2 / L$

lg = 1.14 mm

plugging back into our KG equation,

K_g = $0.125 > 2.64 * 10^{-9}$

$0.5 > K_u * n * Aw / Wa = 2.68 * 10^{-4}$

B_{max} = $\mu_0 * n * I_{max} / lg = 7.17 * 10^{-4} T < 0.5 T$

So the specifications

Core: PQ 26/25

AWG 44

$$L_g = 1.14 \text{ mm}$$

$$n = 10$$

Satisfy the parameters such that our inductor is 13 microHenries and its core will not saturate.

Second Inductor Design:

As we did not have AWG 44 wire in the lab, we redesigned our inductor, using the same parameters as before but using a current ripple of 10%.

$$I_{\max} = (I_{\text{sc}}/D) * 1/2 = 7.89 \text{ A}$$

Once again selecting the PQ 26/25 core:

$$K_g = 1.25 > \rho * L^2 * I_{\max}^2 / (B_{\max}^2 * R * K_u)$$

$$n = (L * I_{\max}) / (B_{\max} * A_c) * 10^4 = 3.48$$

rounding up to err on the side of a larger inductance (and therefore a smaller current ripple)

$$n = 4$$

$$l_g = \mu_0 * A_c * n^2 / (L) * 10^{-4}$$

$$l_g = 0.18 \text{ mm} = 0.007 \text{ inches}$$

$$A_w < K_u * W_a / 10 = 0.063 \text{ cm}^2$$

Diameter of wire = 0.28 cm, AWG #11 is the largest wire possible to use, we used AWG #18 wire.

Plugging back into our K_g and B_{\max} equations, using $R = \rho * n * M_L * A_w$

$$K_g = 1.25 > A_w * L^2 * I_{\max}^2 / (B_{\max}^2 * n * M_L * K_u) = 1.23 \times 10^{-10}$$

$$B_{\max} = 0.25 \text{ T} > \mu_0 * n * I_{\max} / l_g = 0.22 \text{ T}$$

This should give an inductance of $L = 13.18$ microHenries without saturating our core.

Tertiary Inductor Design:

After constructing and testing our inductor the inductance was 8 microHenries at 100 kHz. As the inductance inversely proportional to the airgap, we reduced our airgap to 0.004 inches, giving us an expected inductance of

$$L = 8 \text{ microHenries} * (0.007 \text{ inches} / 0.004 \text{ inches})$$

$$L = 14 \text{ microHenries}$$

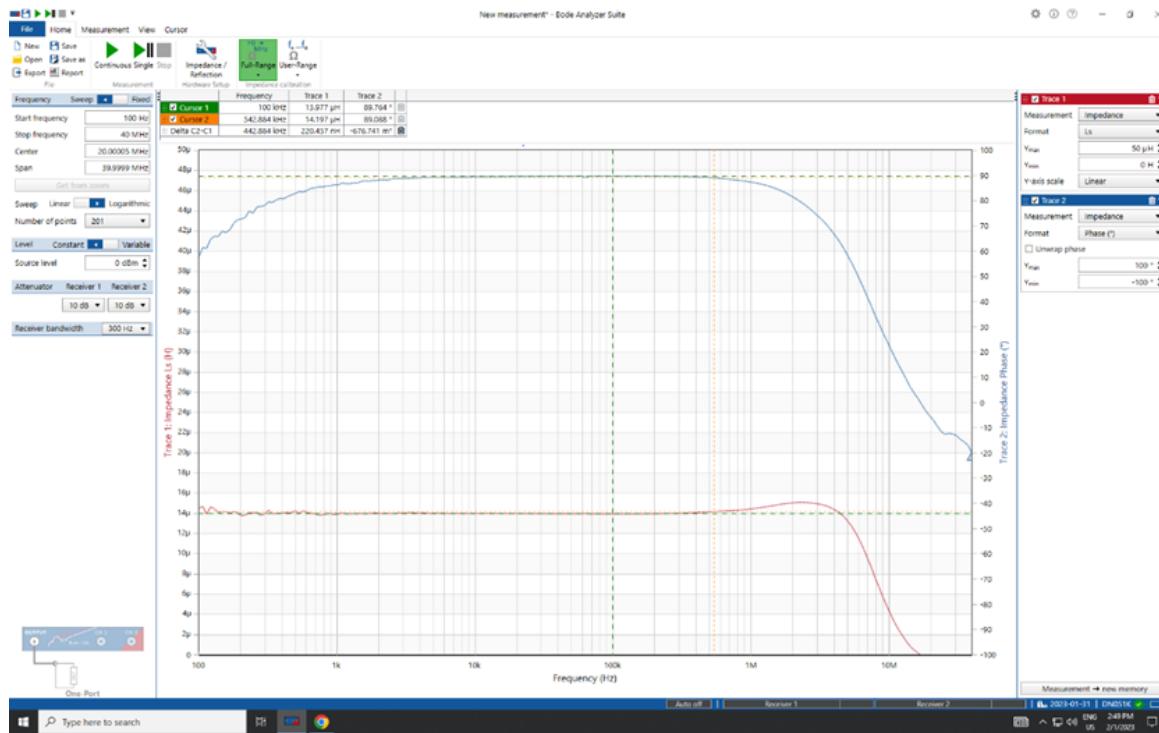


Figure 1: Bode plot of our inductance(shown in red), with the cursor one measurement above the Bode plot showing our inductance at 100 kHz as 13.977 microHenries.

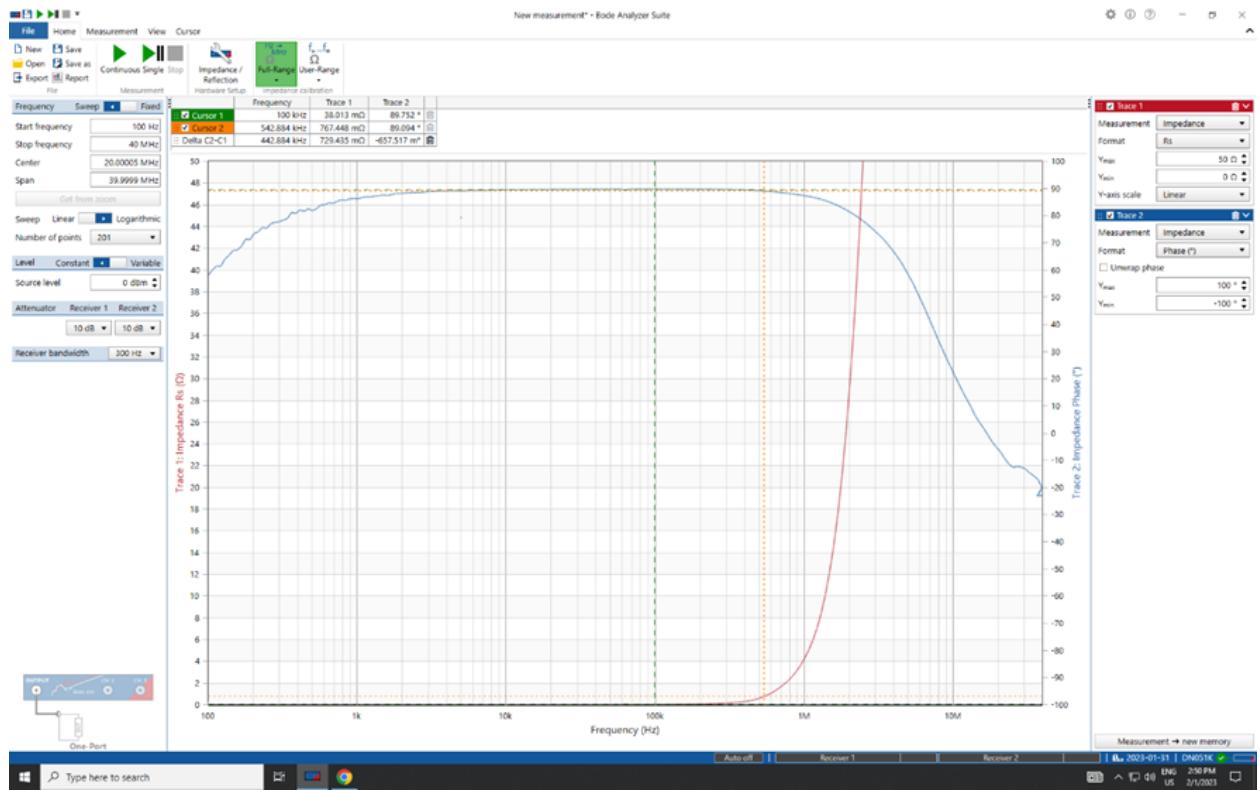


Figure 2: Bode plot of the resistance of our inductor(shown in red), with the cursor one measurement above the Bode plot showing our inductor resistance at 100 kHz as 38.013 mOhms

Step 2: Buck Power Stage Construction

The power MOSFET and Schottky diode were mounted on heat-sinks. #18 AWG wire was used to make interconnections in the power stage. Loops of wire long enough to insert a clip-on AC current probe were included for the MOSFET, inductor, input capacitor, and diode. Otherwise, wiring was kept short for connections with pulsating currents; the loop containing C₁, Q₁, and D₁ were kept as short as possible. A “star-grounding” strategy was employed for the power stage, with a single central point being the “ground” at the anode of the Schottky diode D₁. The controller ground was connected to the power-stage ground only at that single central point. Twisted pairs were used to make the signal and return connections between the LaunchPad and the gate driver circuit, and between the secondary side of the gate driver circuit and the gate-source terminals of the MOSFET Q₁.

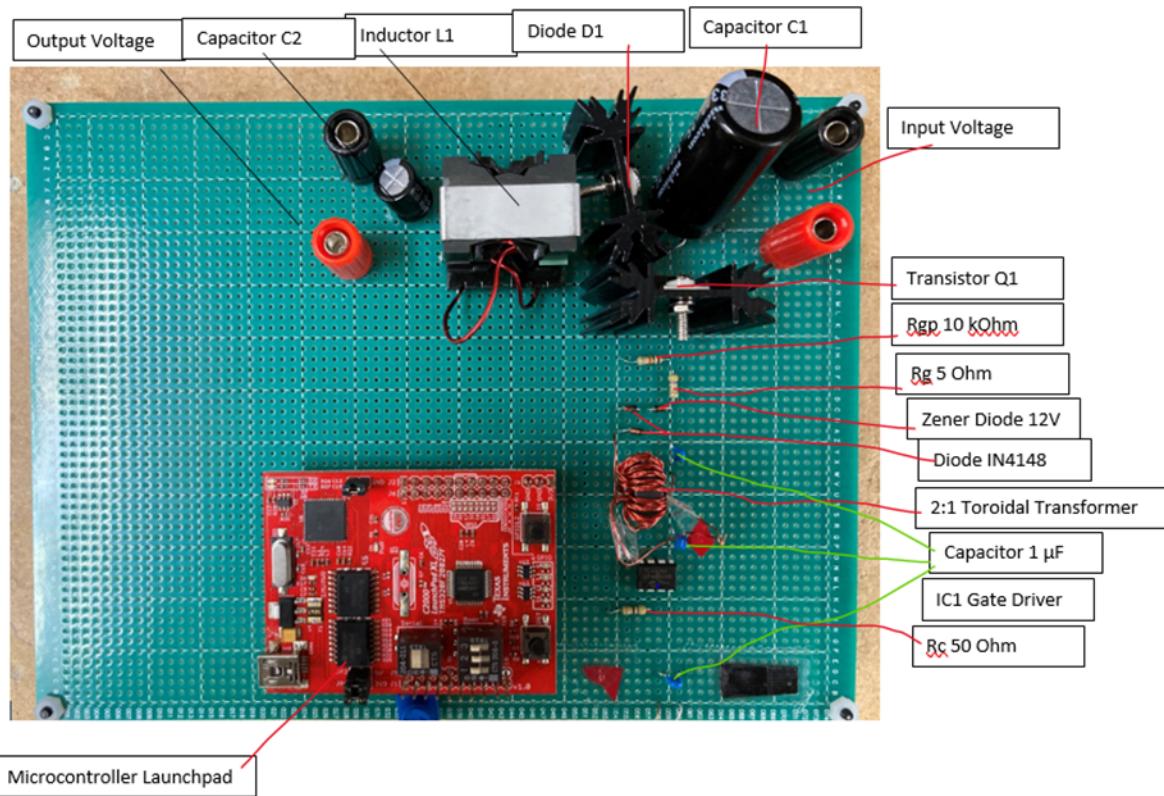


Figure 3: Completed circuit of the power and control stages as shown in the diagram in Figure 5

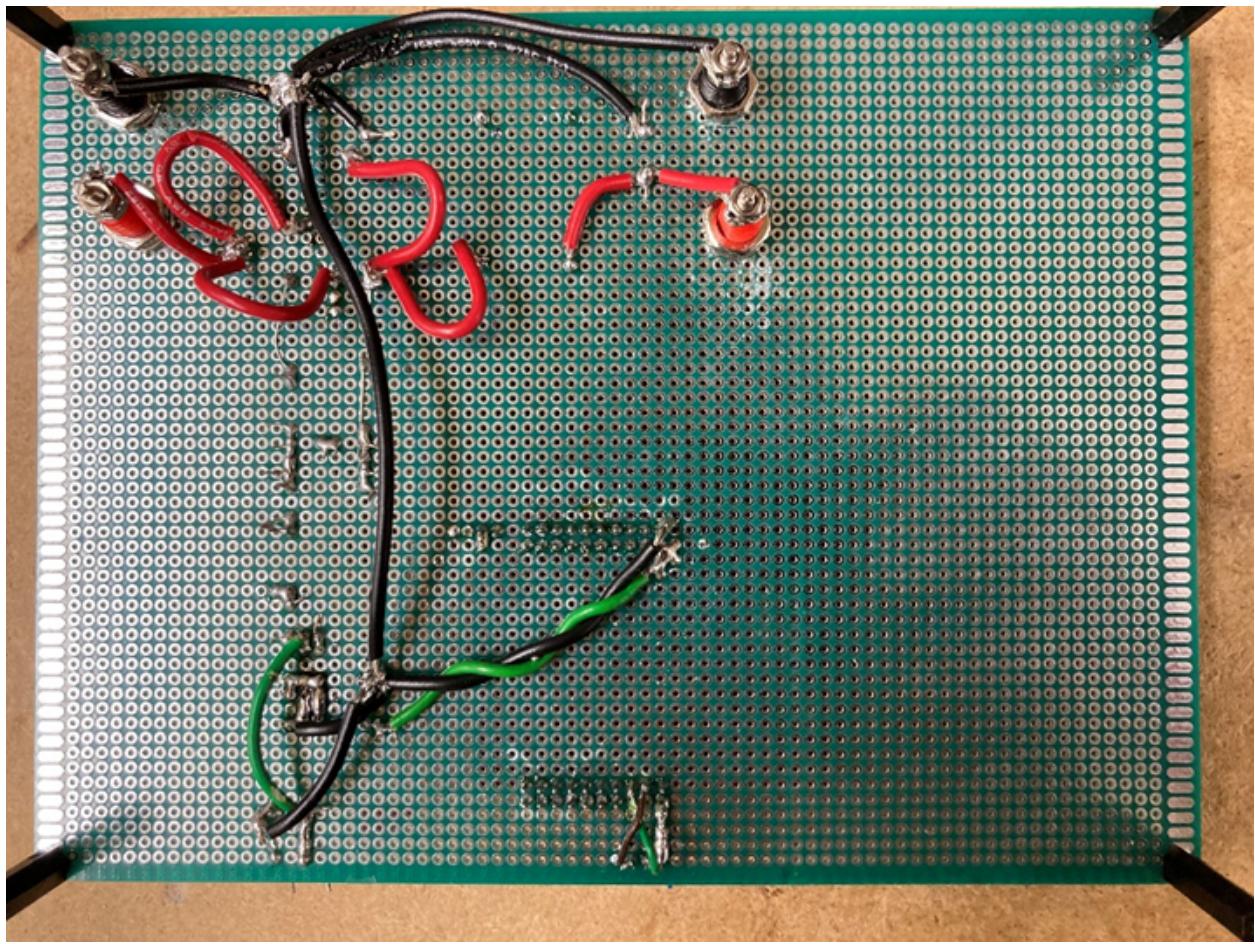


Figure 4: Wiring of the power and control stages shown in Figure 3

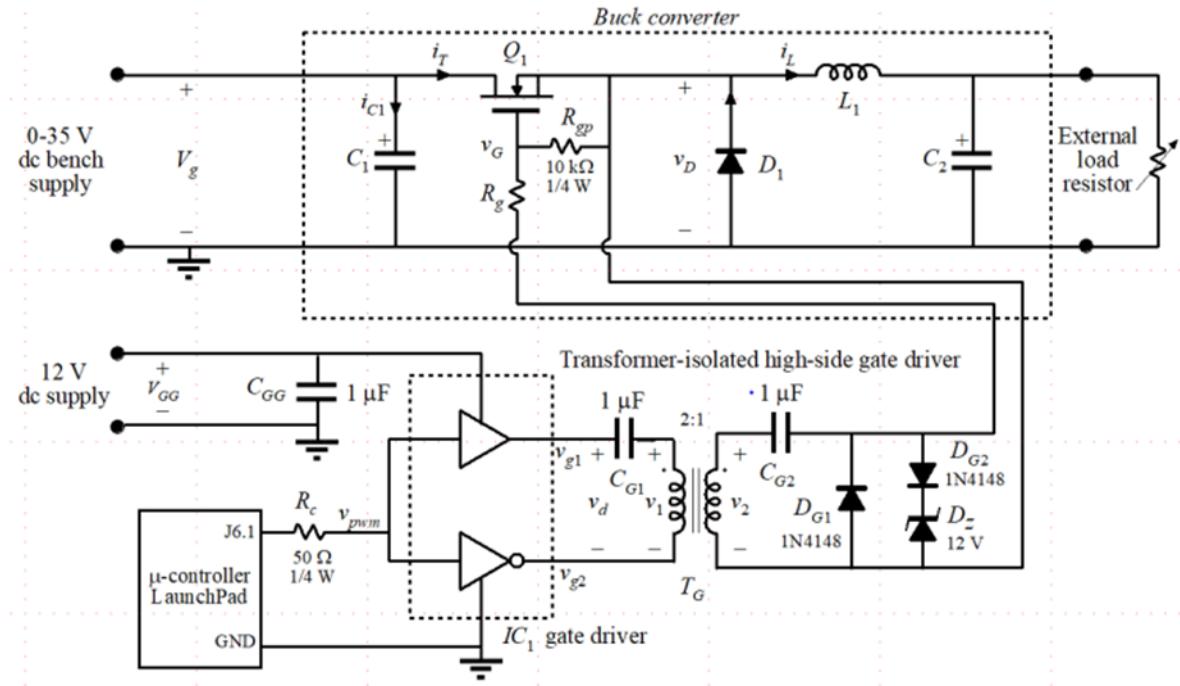


Figure 5: Schematic of the circuit shown in Figures 4 & 5

Step 3: Buck Power Stage Testing and Circuit Measurements

A rheostat was connected to the output of the converter, and the converter was powered with a bench power supply set to the rated full-power voltage of the PV panel (17.2 V). The duty cycle was adjusted to obtain an output of 13V, and the load resistance was decreased until the output power was around 85 W.

The Input and Output voltages and currents, as well as the input and output power and efficiency for the measurements shown in this step, are listed below.

Pulse_width = 520

D = 0.866

Input Voltage: 17.19 V

Input Current: 5.00 A

Output Voltage: 13.169 V

Output Current: 5.72 A

Efficiency = (Input Voltage*Input Current) / (Output Voltage*Output Current)

Efficiency = 0.88 = 88%

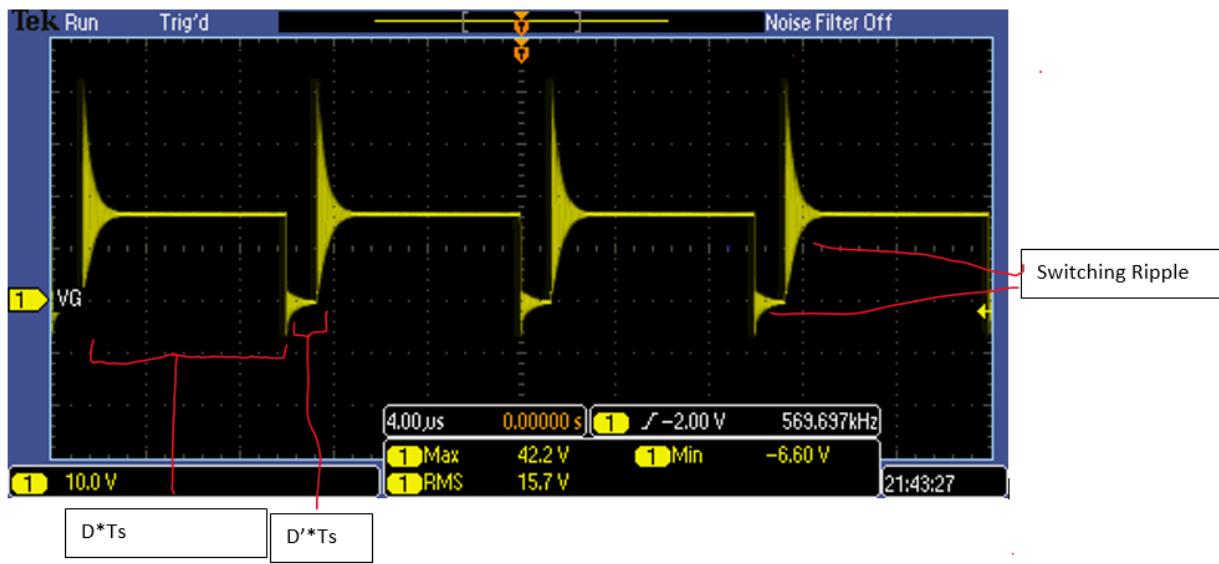


Figure 6: Oscilloscope measurement of Diode Voltage, with measured Minimum, Maximum, and RMS, a vertical scale of 10.0 V and a horizontal scale of 4.00 microseconds

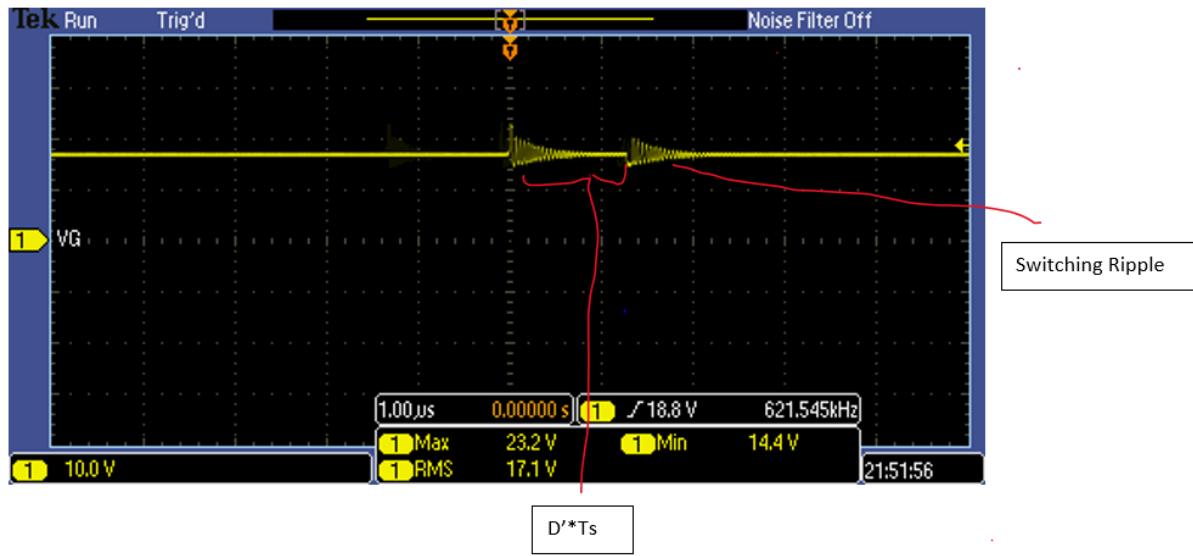


Figure 7: Oscilloscope measurement of the C1 Capacitor Voltage, with measured Minimum, Maximum, and RMS, a vertical scale of 10.0 V and a horizontal scale of 1.00 microseconds

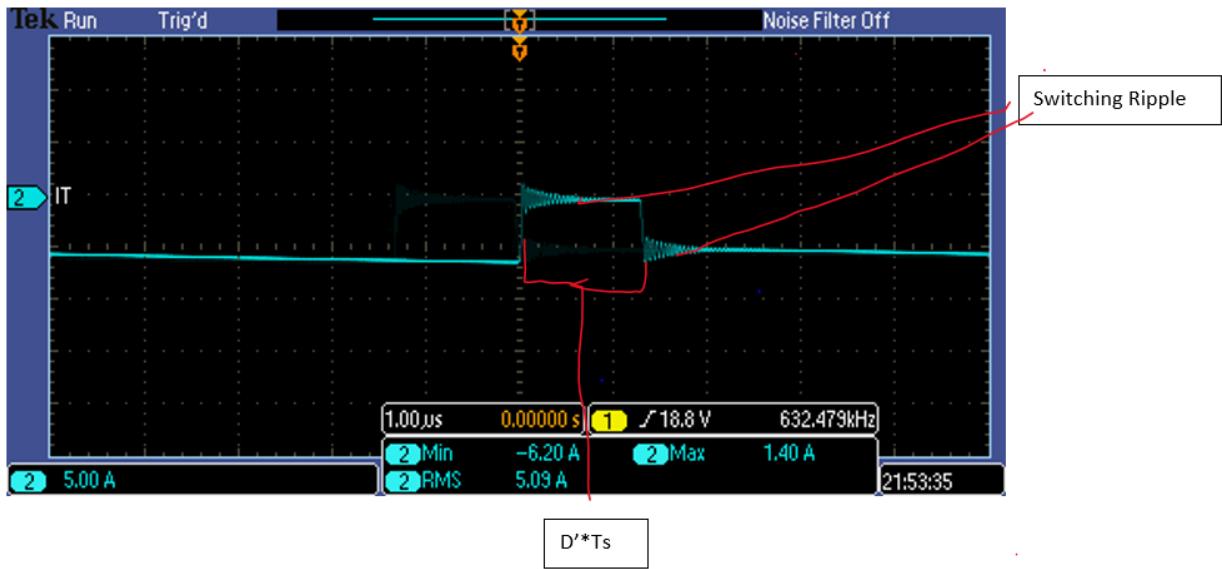


Figure 8: Oscilloscope measurement of Transistor Current, with measured Minimum, Maximum, and RMS, a vertical scale of 5 A and a horizontal scale of 1.00 microseconds

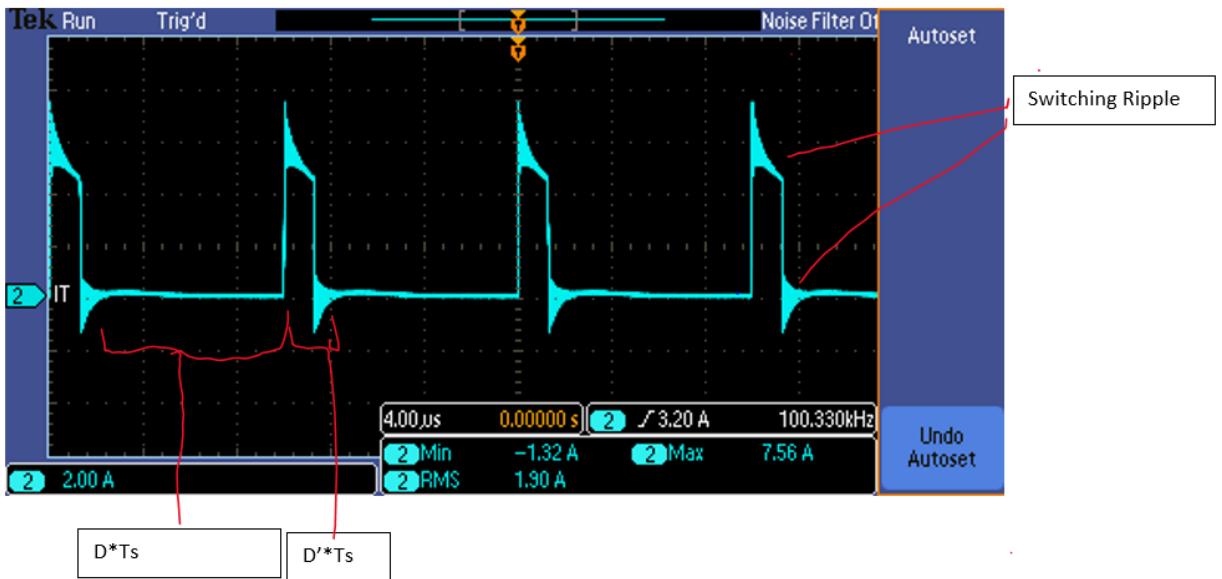


Figure 9: Oscilloscope measurement of Diode Current, with measured Minimum, Maximum, and RMS, a vertical scale of 2 A and a horizontal scale of 4.00 microseconds

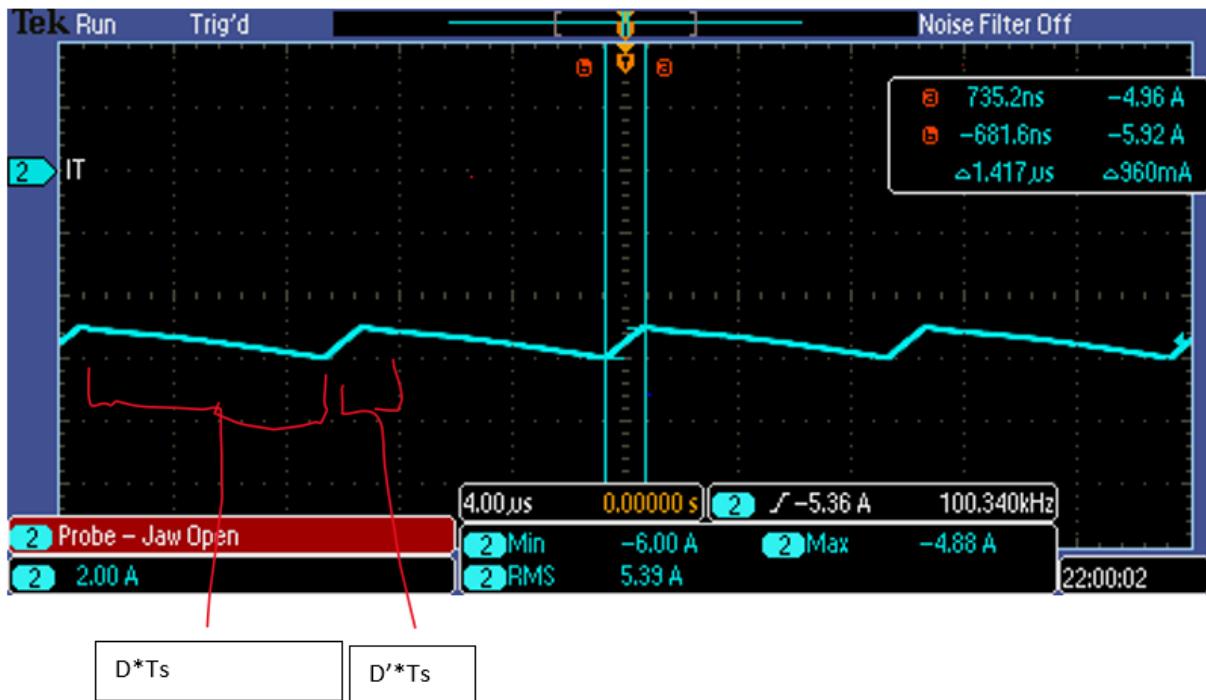


Figure 10: Oscilloscope measurement of Inductor Current(the probe jaw was inverted, resulting in an inverted inductor waveform), with measured Minimum, Maximum, and RMS, a vertical scale of 2 A and a horizontal scale of 4.00 microseconds, as well as cursor measurements of the maximum and minimum of a single waveform for calculation of the current ripple.

The measured current waveform gives an inductor current ripple of

$$\Delta I = (5.92 - 4.96)/2 \text{ A}$$

$$\Delta I = 480 \text{ mA}$$

dividing our current ripple by the RMS current, we find that

$$0.48 \text{ A}/5.39\text{A} = 0.089 = 8.9\%$$

This measured current ripple is much smaller than expected. A 20% current ripple was expected from our initial Inductor design.. Although we used a 10% current ripple for part of our tertiary Inductor design, we would still expect our final measured Inductance of 13.977 microHenries to

produce a ripple of roughly 20%, as a 13 microHenry Inductor was expected to produce a 20% current ripple .



Figure 11: Oscilloscope measurement of the C1 Capacitor Current, with measured Minimum, Maximum, and RMS, a vertical scale of 2 A and a horizontal scale of 4.00 microseconds

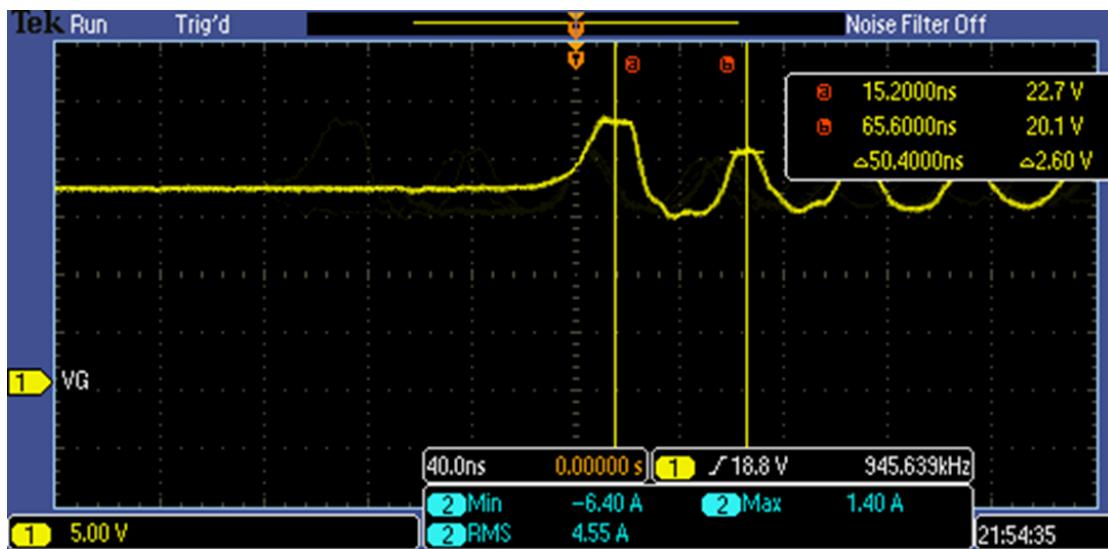


Figure 12: Highly magnified oscilloscope measurement of the C1 Capacitor Voltage ripple and cursor measurements, with a vertical scale of 5 V and a horizontal scale of 40 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

From the oscilloscope cursor measurements we can calculate the frequency of the Capacitor Voltage ripple as

$$f = 1/(50.40 * 10^{-9})$$

$$f = 19.84 \text{ MHz}$$

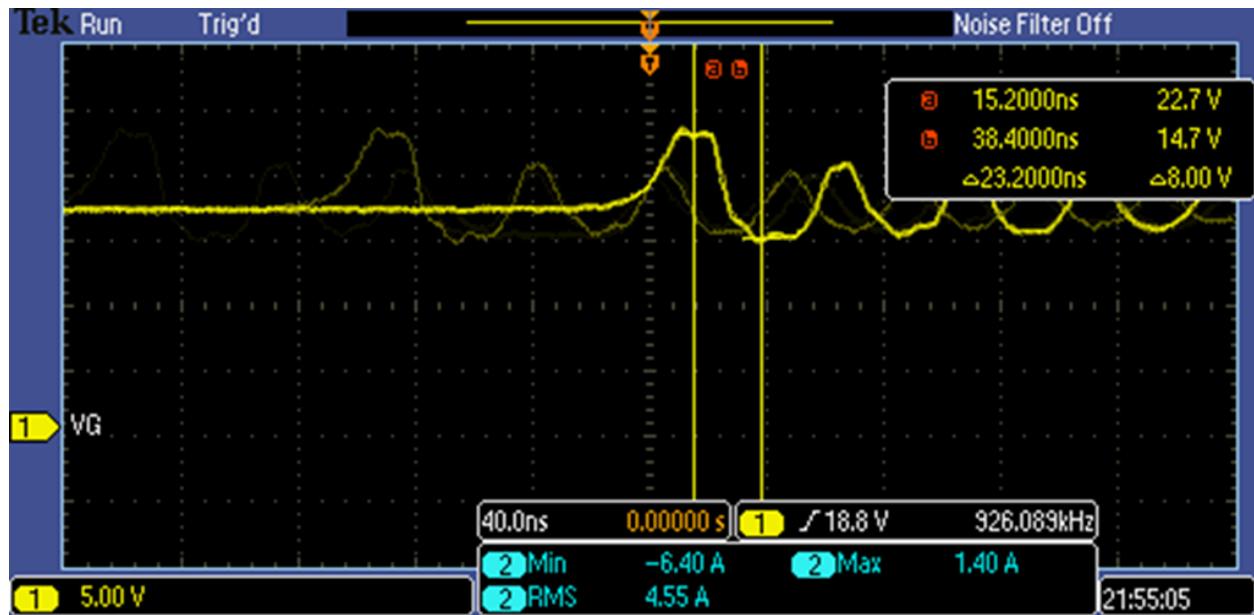


Figure 13: Highly magnified oscilloscope measurement of the C1 Capacitor Voltage ripple and cursor measurements, with a vertical scale of 5 V and a horizontal scale of 40 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

The waveform of the Capacitor Voltage is a DC Voltage, with a sinusoidal ripple occurring when the MOSFET switches on or off. The magnitude of the Capacitor Voltage ripple is 8.00 V.

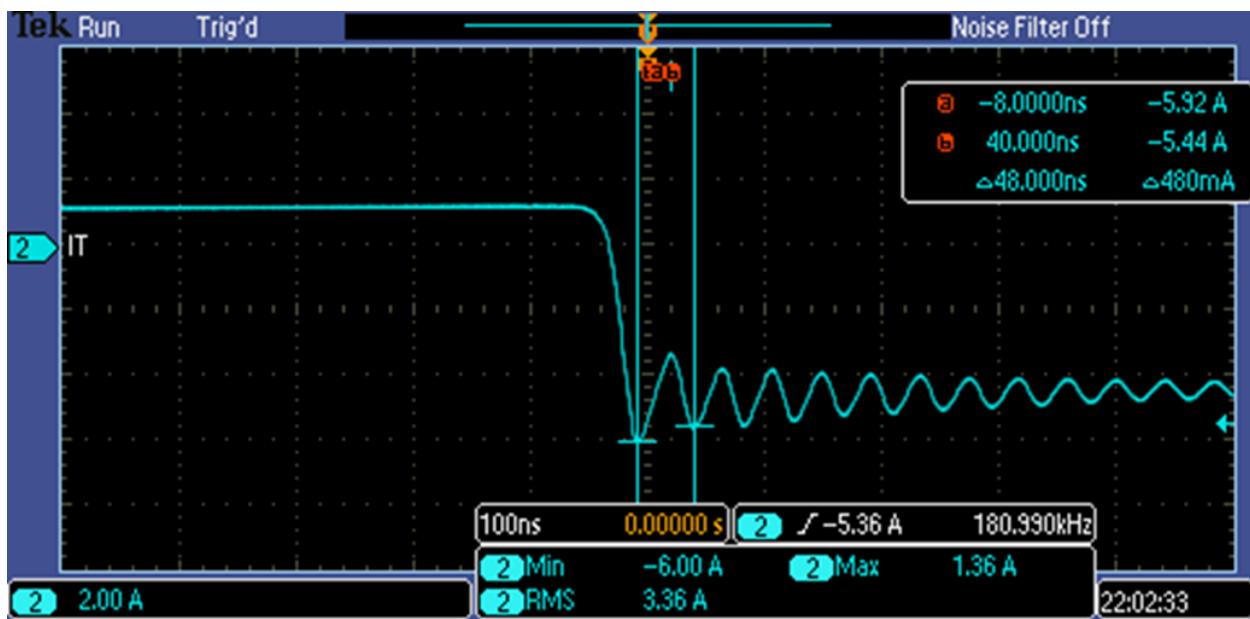


Figure 14: Highly magnified oscilloscope measurement of the Capacitor current ripple and cursor measurements, with a vertical scale of 2 A and a horizontal scale of 100 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

From the oscilloscope cursor measurements we can calculate the frequency of the Capacitor Current ripple as

$$f = 1/(48.0 * 10^{-9})$$

$$f = 20.83 \text{ MHz}$$

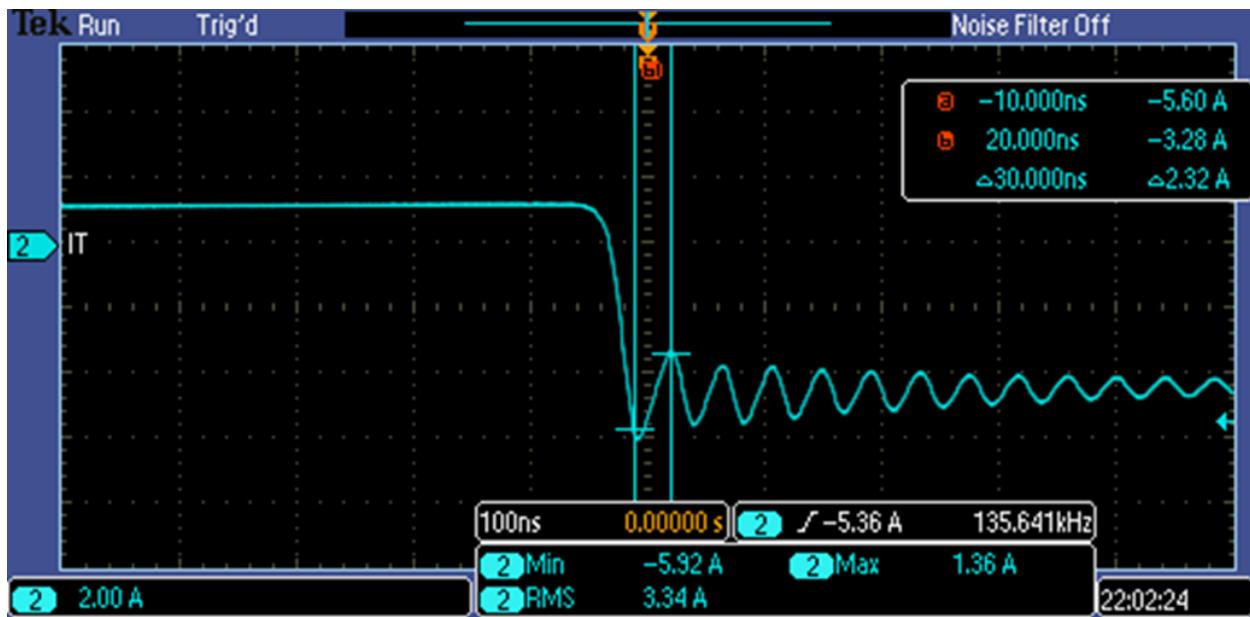


Figure 15: Highly magnified oscilloscope measurement of the Capacitor current ripple and cursor measurements, with a vertical scale of 2 A and a horizontal scale of 100 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

The magnitude of the Capacitor Current ripple is 2.32 A.

The capacitor impedance can be calculated as

$$Z = V_{\text{ripple}}/I_{\text{ripple}} = ((1/(2\pi f C))^2 + (R)^2)^{1/2} = 8.0V/2.32A = 3.45 \text{ Ohms}$$

Where R is the Equivalent Series Resistance(ESR).

We'll take our frequency f as the average of the Voltage and Current ripple frequencies,

$$f = (19.84 + 20.83)/2 \text{ MHz}$$

$$f = 20.34 \text{ MHz}$$

$$R = ((3.45 \text{ Ohms})^2 - (1/(2\pi f C))^2)^{1/2}$$

$$R = 3.45 \text{ Ohms}$$

The power loss caused by conduction through this Equivalent Series Resistance can be calculated as

$$P_c = (I_{rms})^2 * R = (3.34 \text{ A})^2 * 3.45 \text{ Ohms}$$

$$P_c = 38.49 \text{ W}$$

We clearly made a mistake in the measurements of the Voltage or Current ripples, as the power calculated to be consumed by the ESR is nearly half of the total power input into the Buck converter.

However, the RMS current of 3.34 Amps is slightly lower than the datasheets listed current ripple at 100 kHz of 4.08 Amps.

ESR Attempt #2:

Because this ESR did not make sense, we recalculated our ESR using the RMS of the voltage and current ripples instead of their amplitudes.

The Input and Output voltages and currents, as well as the input and output power and efficiency for this new attempt, are listed below.

Input Voltage: 17.20 V

Input Current: 5.28 A

Output Voltage: 12.828 V

Output Current: 6.13 A

Input Power: 90.816 W

Output Power: 83.64 W

Efficiency: 92.1%

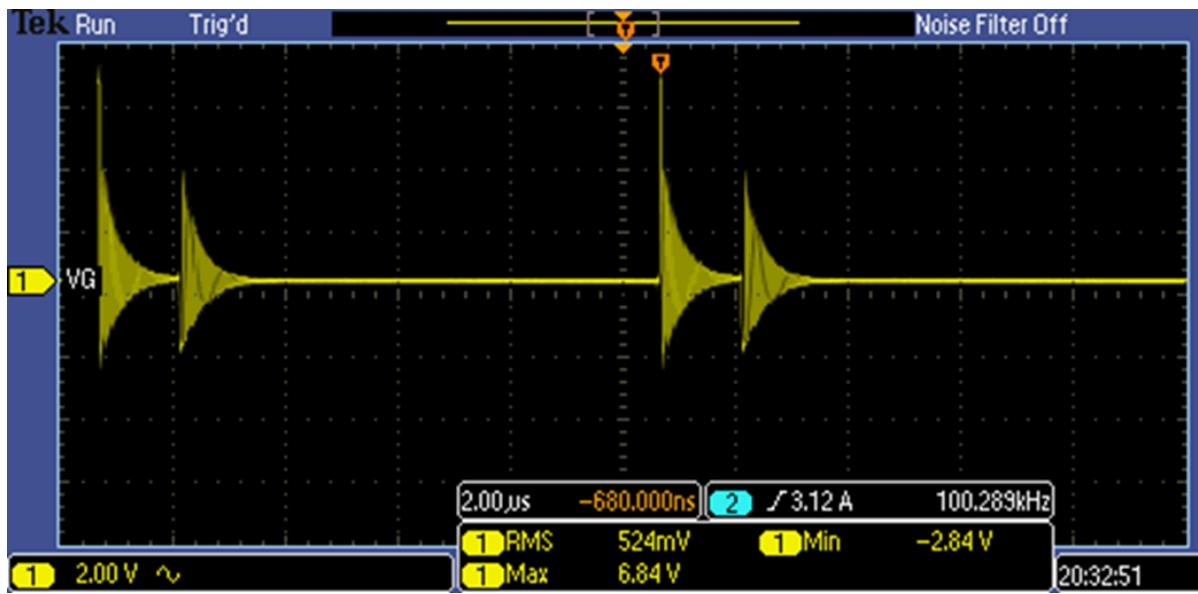


Figure 16: Oscilloscope measurement of Capacitor Voltage AC component, with measured Minimum, Maximum, and RMS, a vertical scale of 2.0 V and a horizontal scale of 2.00 microseconds.

The Vrms of the C1 Capacitor ripple is 524 mV = Vrms.

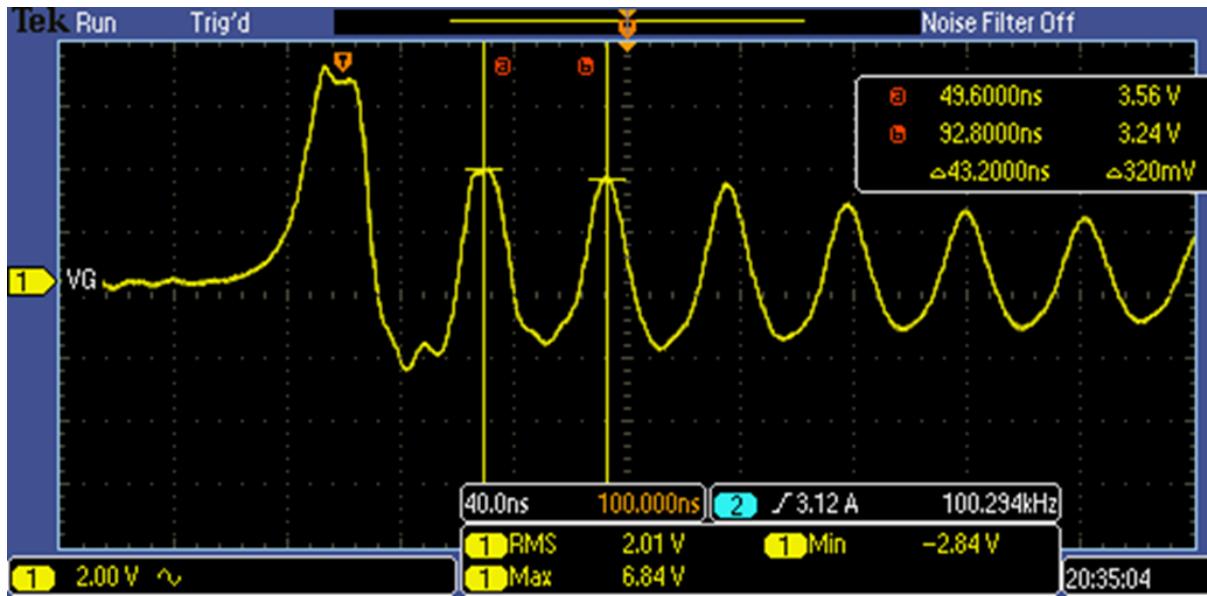


Figure 17: Highly magnified oscilloscope measurement of the Capacitor Voltage ripple and cursor measurements, with a vertical scale of 2 V and a horizontal scale of 40 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

From the oscilloscope cursor measurements we can calculate the frequency of the Capacitor Voltage ripple as

$$f = 1/(50.40 * 10^{-9})$$

$$f = 23.1 \text{ MHz}$$



Figure 18: Oscilloscope measurement of Capacitor Current AC component, with measured Minimum, Maximum, and RMS, a vertical scale of 2.0 A and a horizontal scale of 2.00 microseconds.

The RMS current of the C1 Capacitor ripple is 2.1 A = Irms.

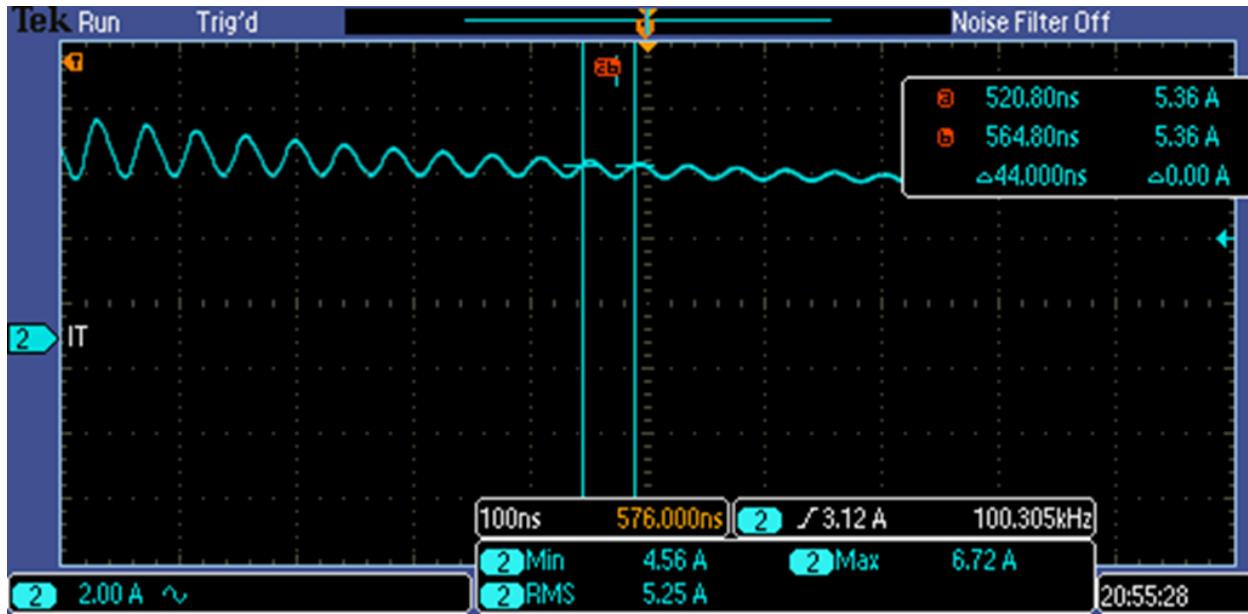


Figure 19: Highly magnified oscilloscope measurement of the Capacitor current ripple and cursor measurements, with a vertical scale of 2 A and a horizontal scale of 100 ns. The oscilloscope cursor measurements are shown in the top right of the photo.

From the oscilloscope cursor measurements we can calculate the frequency of the Capacitor Current ripple as

$$f = 1/(44.0 * 10^{-9})$$

$$f = 22.7 \text{ MHz}$$

The capacitor impedance can be calculated as

$$Z = V_{rms}/I_{rms} = ((1/(2\pi f C))^2 + (R)^2)^{1/2} = 0.524V/2.1A = 250 \text{ mOhms}$$

Where R is the Equivalent Series Resistance(ESR).

We'll take our frequency f as the average of the Voltage and Current ripple frequencies,

$$f = (22.7 + 23.1)/2 \text{ MHz}$$

$$f = 22.9 \text{ MHz}$$

$$R = ((250 \text{ mOhms})^2 - (1/(2*\pi*f*C))^2)^{1/2}$$

$$R = 250 \text{ mOhms}$$

The power loss caused by conduction through this Equivalent Series Resistance can be calculated as

$$P_c = (I_{rms})^2 * R = (3.34 \text{ A})^2 * 250 \text{ mOhms}$$

Where I_{rms} is the DC I_{rms} of the Capacitor C1.

$$P_c = 2.79 \text{ W}$$

This is a much more reasonable power loss than our previous calculation.

Step 4:

The load resistor was adjusted to obtain an output power of 15W.

To set our output power to roughly 15 W, we iterated our duty cycle and rheostat settings until we arrived at the duty cycle, and input and output voltages and currents of:

$$D = 0.866$$

Setting our output power to roughly 15 W:

Input Voltage, Current: 17.2 V, 0.87 A

Output Voltage, Current: 13.55 V, 1.071 A

$$P = 13.55 \text{ V} * 1.071 \text{ A}$$

$$P = 14.51 \text{ W}$$

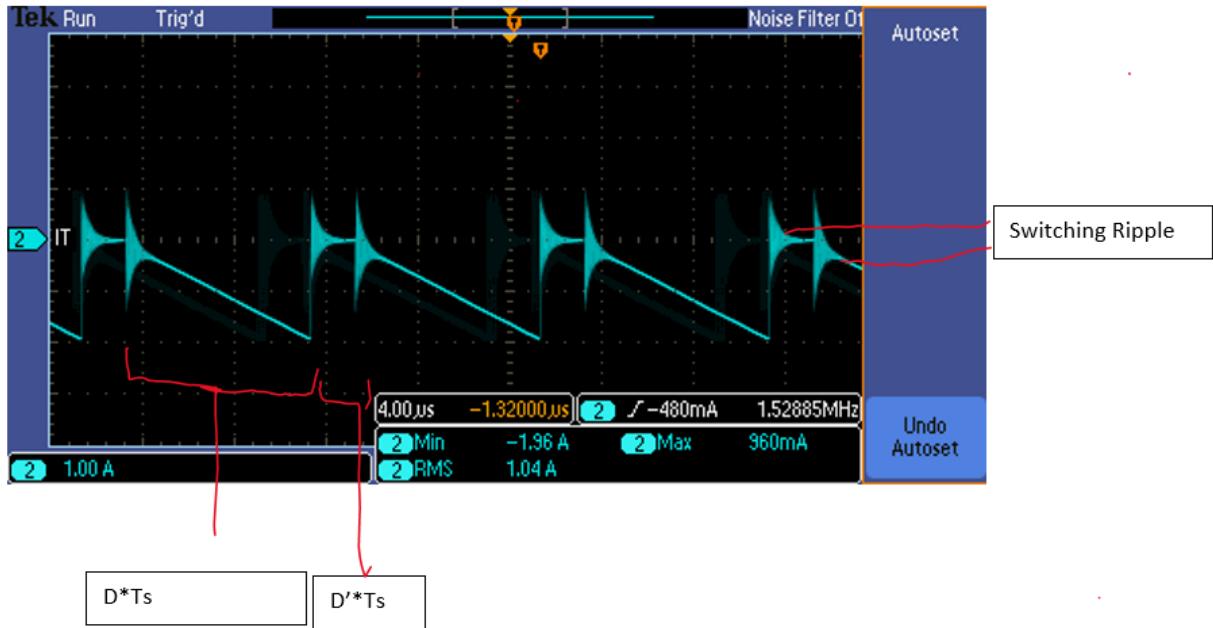


Figure 20: Oscilloscope measurement of Transistor Current at 15 W output, with measured Minimum, Maximum, and RMS measurements shown, a vertical scale of 1.0 A, and a horizontal scale of 4.00 microseconds

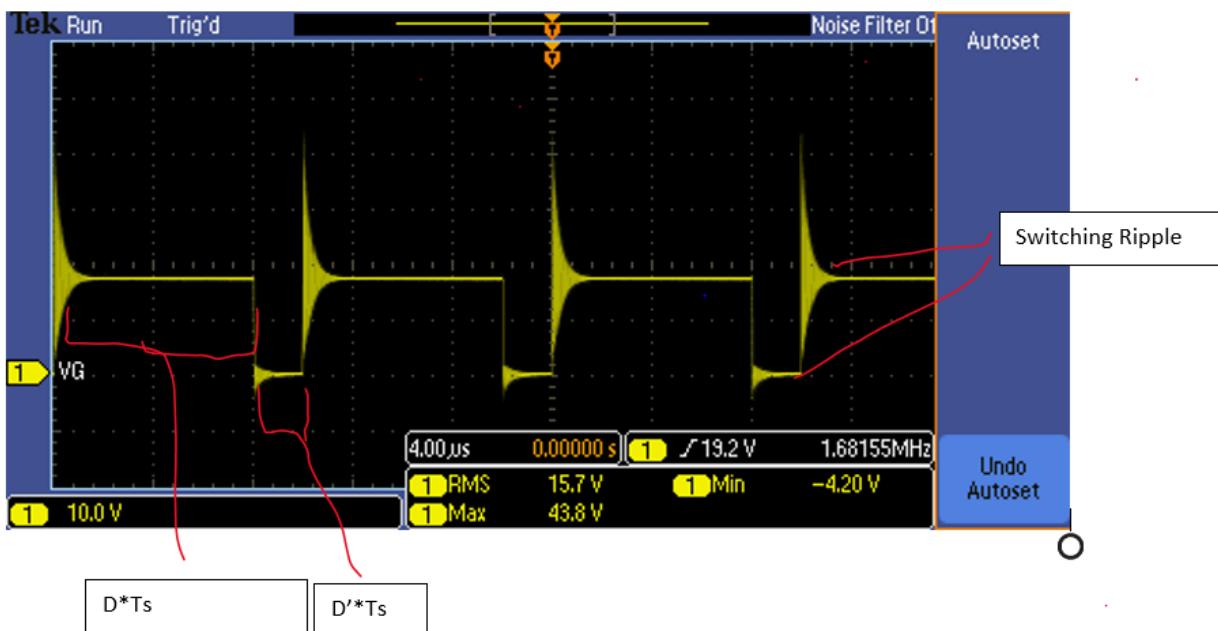


Figure 21: Oscilloscope measurement of Diode Voltage at 15 W output, with measured Minimum, Maximum, and RMS measurements shown, a vertical scale of 10.0 V, and a horizontal scale of 4.00 microseconds

We attempted to set the output power to 1 W by setting the rheostat at its highest possible resistance, but were only able to achieve an output power of 14.1 W with this method. The Input and Output Voltages and Currents for this maximum rheostat resistance setting are shown below.

Input Voltage, Current: 17.2V, 0.85A

Output Voltage, Current: 13.556V, 1.040 A

With the rheostat set to its maximum resistance the output power lowered to

$$P = 13.556 \text{ V} * 1.040 \text{ A}$$

$$P = 14.1 \text{ W}$$

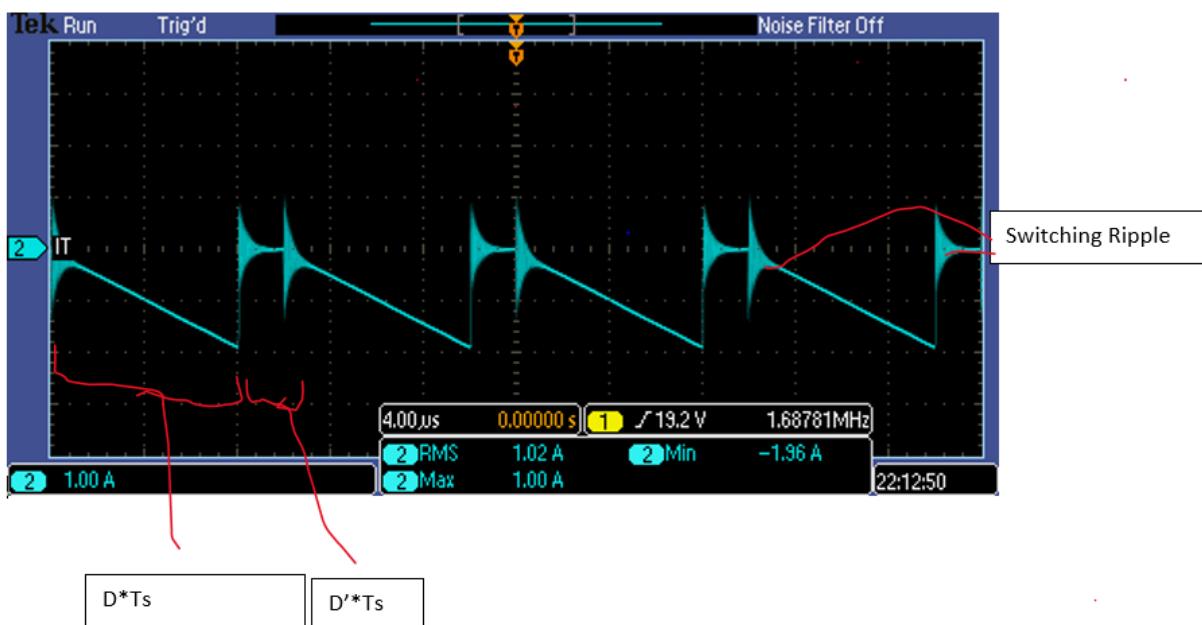


Figure 22: Oscilloscope measurement of Transistor Current at 14.1 W output, with measured Minimum, Maximum, and RMS measurements shown, a vertical scale of 1.0 A, and a horizontal scale of 4.00 microseconds

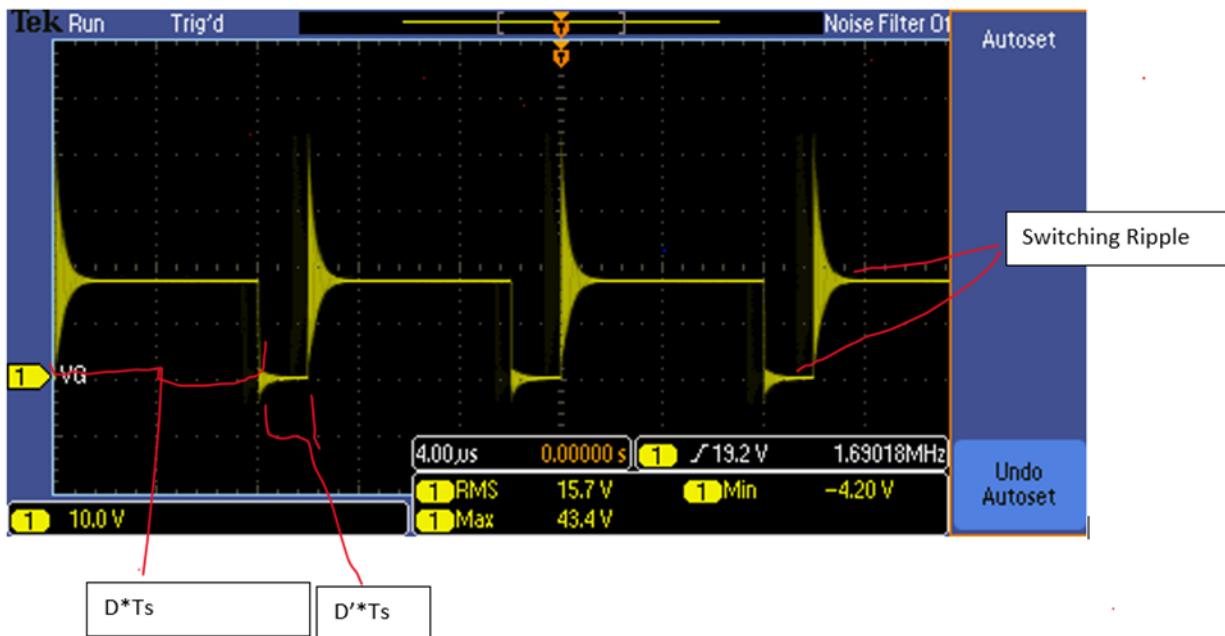


Figure 23: Oscilloscope measurement of Transistor Current at 4.1 W output, with measured Minimum, Maximum, and RMS measurements shown, a vertical scale of 10.0 V, and a horizontal scale of 4.00 microseconds

As our lowest achievable power was 14.1 W, our Transistor Current and Diode Voltage waveforms were nearly identical to the waveforms at the output power of 15 W (which was actually roughly achieved with an output of 14.51 W). Both sets of waveforms were CCM waveforms, however if we were able to achieve 1 W output power we would expect to see DCM waveforms.

Step 5: Open-loop behavior in PV system

The microcontroller program was modified to produce a signal that was proportional to a voltage applied to an A/D input of the microcontroller. A potentiometer was connected to provide a variable voltage signal to the microcontroller that corresponded to the duty cycle of the gate driver. The voltage signal varies between 0 and 3.3 V, and the programming of the microcontroller was modified as shown in figure 24.

```
84 // **** End of Setup ****
85
86 // Manually adjust duty cycle using trimpot connected to J5.3
87 // Read sensed_voltage on pin J5.3 (sensed_voltage=((trimpot_percent)/3.3V)*4095), and update
88 // duty cycle via updating pulse_width proportional to period
89 pulse_width=300;
90 update_duty(pulse_width);
91
92 while (1)
93 {
94     pulse_width = (int)(sensed_voltage/4095.0*period); // PWM duty cycle is D = pulse_width/period
95     update_duty(pulse_width); //Changes the duty cycle of the PWM output signal on pin J6.1
96 }
97
98 }
```

Figure 24: Modified ADC code to update duty cycle based on sensed voltage at potentiometer output

The PV panel was connected as an input to the buck converter, and the output connected to the battery. The PV panel was pointed at the sun on a mostly clear day, and the converter powered up. Using the potentiometer, the duty cycle was swept from 0 to 1, and voltage and current readings for the panel and the battery were recorded. These results are shown in table 1. Some outlying datapoints had to be discarded due to varying cloud conditions. These measurements were also taken near the end of the day, around 4:45 pm on Sunday 2/19, so solar insolation was changing rapidly with the near-setting sun. This may have resulted in differing solar insolation values across our measurements.

Sensed voltage (mV)	Duty Cycle	V_PV (V)	I_PV (A)	V_batt (V)	I_batt (A)
0	0	21.95	0	12.24	0
151	0.03687	21.74	0.005	12.25	0.008
285	0.0696	21.61	0.016	12.24	0.027
489	0.11941	21.24	0.047	12.25	0.077
711	0.17363	21.91	0.107	12.95	0.185
906	0.22125	21.74	0.168	12.25	0.289
1250	0.30525	21.49	0.286	12.26	0.485
1627	0.39731	21.33	0.48	12.28	0.8
1930	0.47131	21.12	0.678	12.3	1.11
2213	0.54042	20.96	0.825	12.31	1.33
2601	0.63516	20.32	1.3	12.35	1.98
3048	0.74432	18.33	3.37	12.49	4.47
3391	0.82808	16.66	3.94	12.51	4.73
3886	0.94896	14.42	4.06	12.48	4.25
4095	1	21.9	0	12.25	0
0	0	21.82	0	12.22	0
186	0.04542	21.74	0.007	12.21	0.012
446	0.10891	21.64	0.04	12.22	0.069

Table 1: PV and Battery Voltage and Current with Varying Duty Cycle

Step 6: Interpretation of data and simulations

This data is analyzed graphically below.

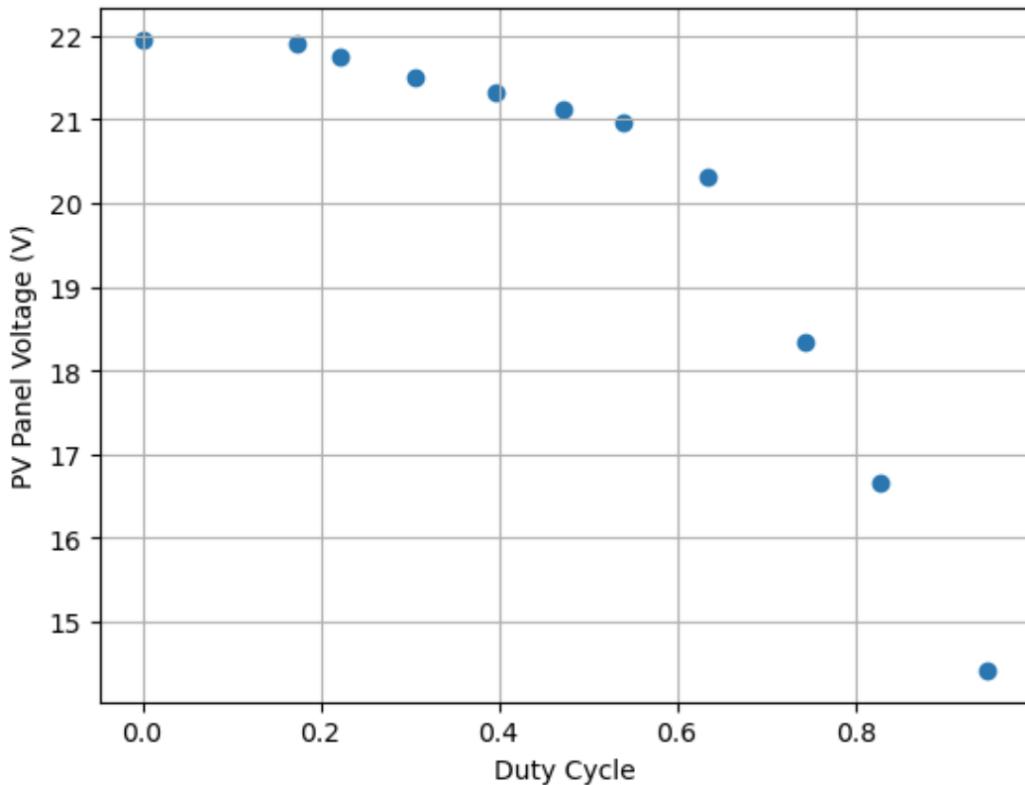


Figure 25: PV Voltage vs Duty Cycle

At duty cycle of 0, the MOSFET is never switched on, and thus the PV panel output appears as an open circuit, thus driving the PV panel towards its open circuit voltage, 22.2 V. As duty cycle increases, the conversion ratio $M(D)$ increases, and the PV voltage is driven down. However, initially, the PV voltage drops slowly with duty cycle, and after around $D = 0.6$, drops sharply with duty cycle. This is likely due to the battery voltage constraining the system below $D = 0.6$. The battery voltage cannot drop below about 12.2 V, and the PV voltage cannot rise above its open circuit voltage of 22.2 V, so the conversion ratio is forced higher in effect. Once $M(D)$ can be properly met by the limits of the battery above around $D = 0.6$, the PV voltage scales as would be expected given the conversion ratio.

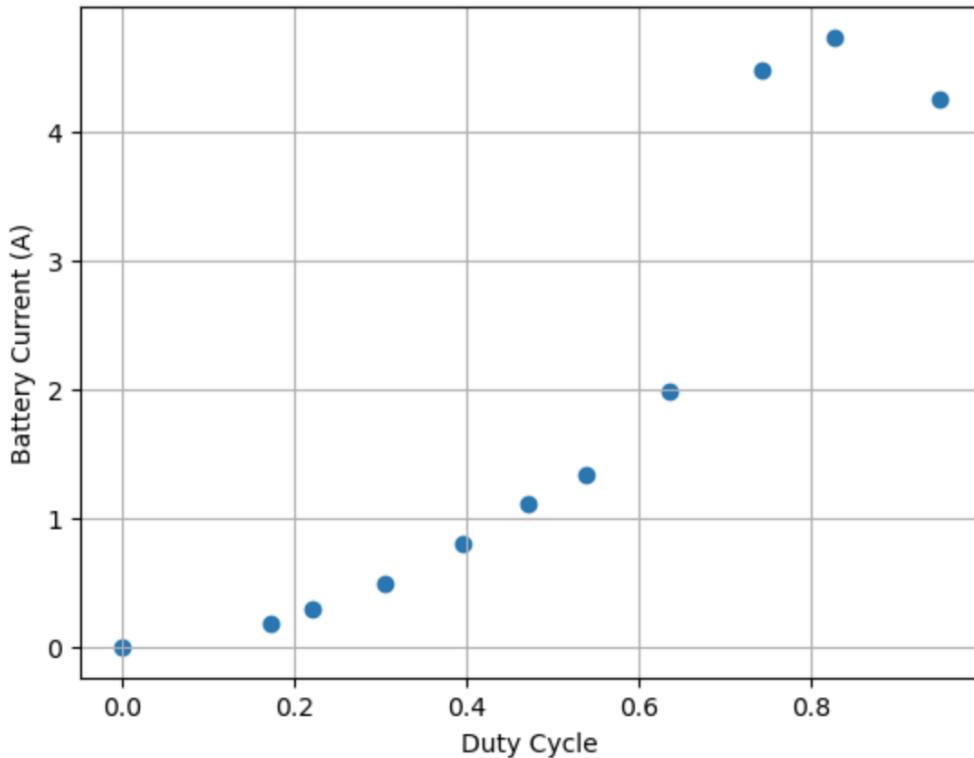


Figure 26: Battery Current vs Duty Cycle

The battery current is affected by the same phenomenon found in figure 25 examining PV Volgate. As the PV panel voltage drops slowly below $D = 0.6$, the PV current rises slowly dependent upon the PV I-V relationship. The battery current is constrained by the PV current and thus experiences the same slow increase until normal converter operation above $D = 0.6$.

The battery current peaks and then decreases at high duty cycle due to the relationship between PV current and battery current. In an ideal buck converter, this is $I_{\text{batt}} = I_{\text{pv}}/D$. At high duty cycle, the PV panel current changes little with a change in duty cycle, as seen in figure 27. The proportional change in duty cycle is greater than that in I_{pv} , and thus I_{batt} , inversely proportional to duty cycle, decreases.

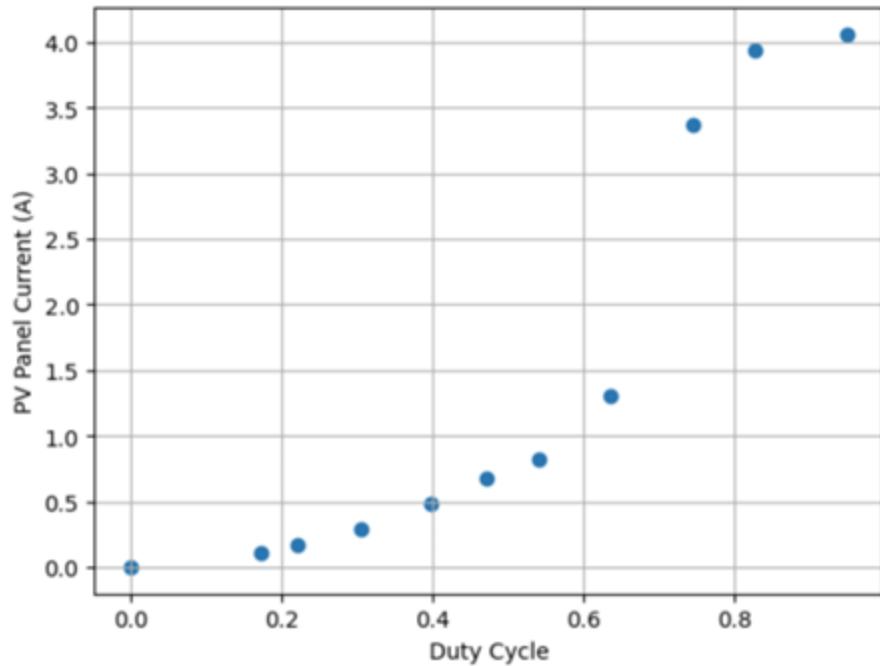


Figure 27: PV panel I-V curve with varying duty cycle

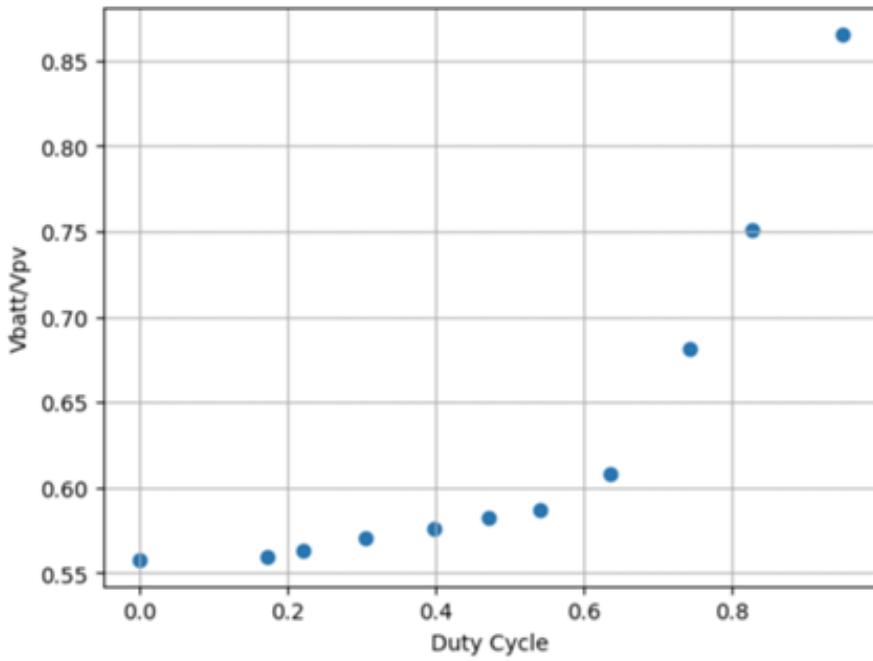


Figure 28: $V_{\text{batt}}/V_{\text{pv}}$ vs Duty Cycle

Finally, a graph of V_{batt}/V_{pv} ($M(D)$) vs duty cycle is presented in figure 28. Once again, this graph demonstrates the phenomenon due to the constrained nature of the voltages in the system. After about $D = 0.6$, $M(D)$ tracks linearly with D , nearly 1:1 as would be expected in an ideal buck converter.

Simulated Results

The PV-buck-battery system was simulated using LTspice, using parameter values found for our actual system. Parasitic elements were included, namely the equivalent series resistance of capacitor C1, and resistance of inductor L1. An attempt was made to include loop inductance in the diode-C1-MOSFET loop, but this caused transient simulations to take much too long to run, so this was omitted. Results for the same graphs analyzed for our real world system are shown below. One other limitation to our simulation was not having a battery model that varies like our real world battery. Instead, we maintained battery voltage at 12.55 V in simulation.

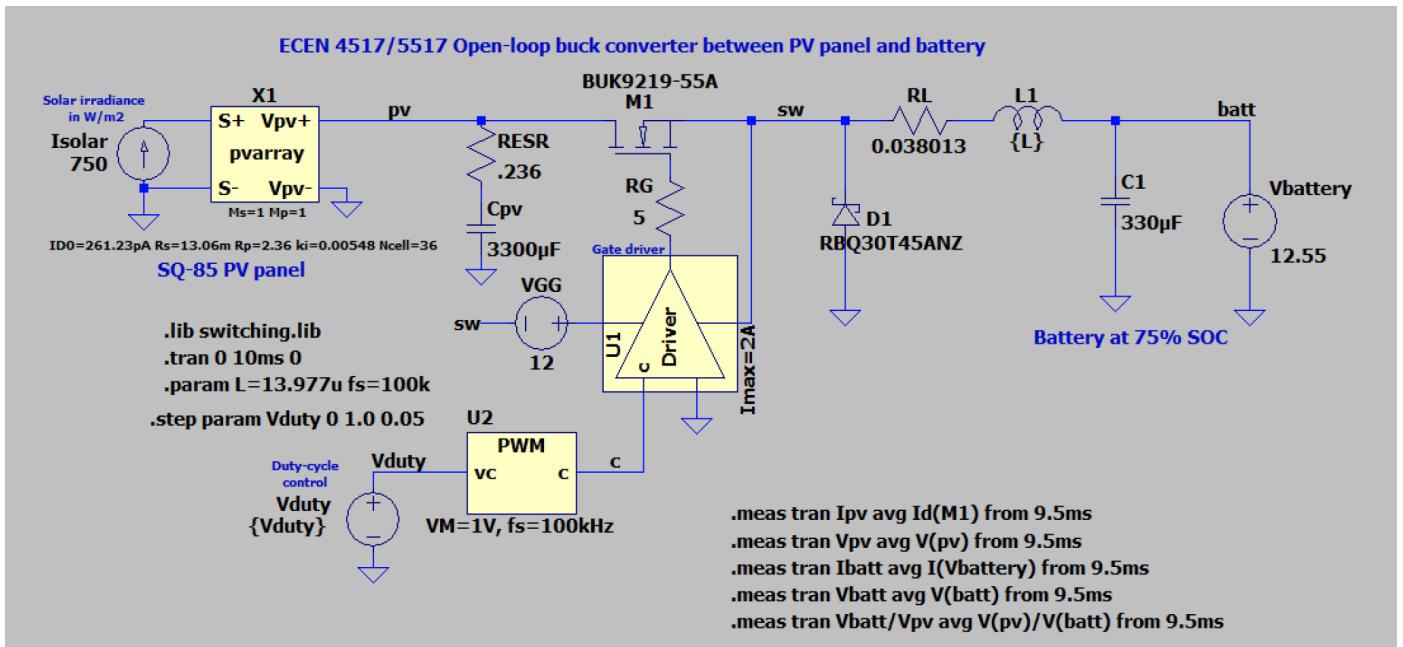


Figure 32: LTspice Circuit

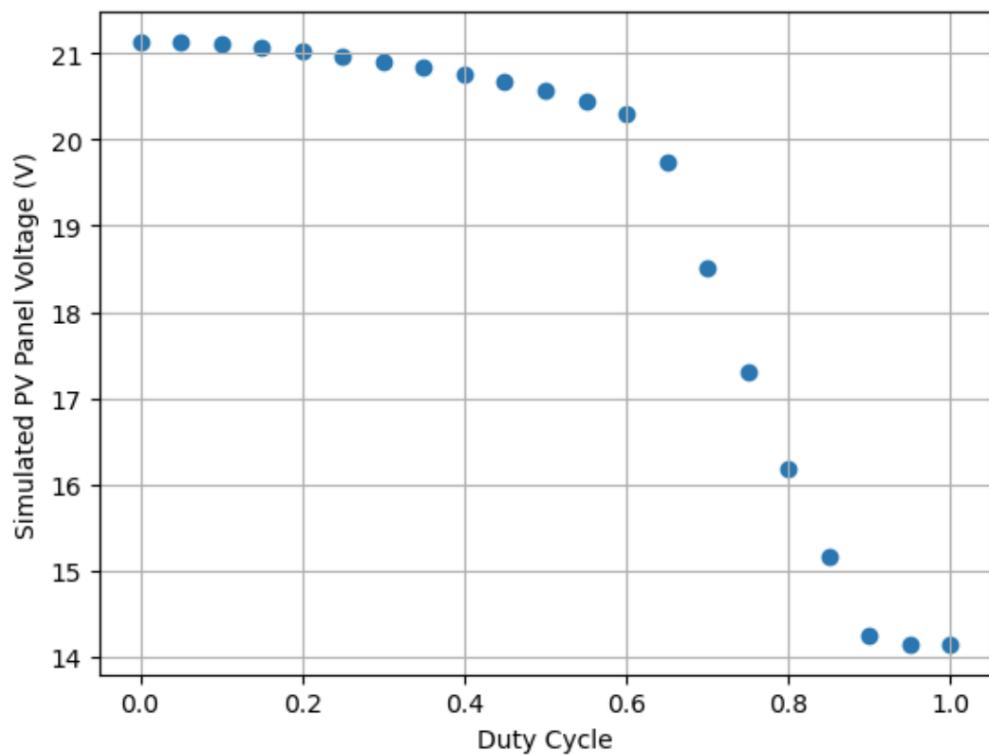


Figure 29: Simulated PV Voltage vs Duty Cycle

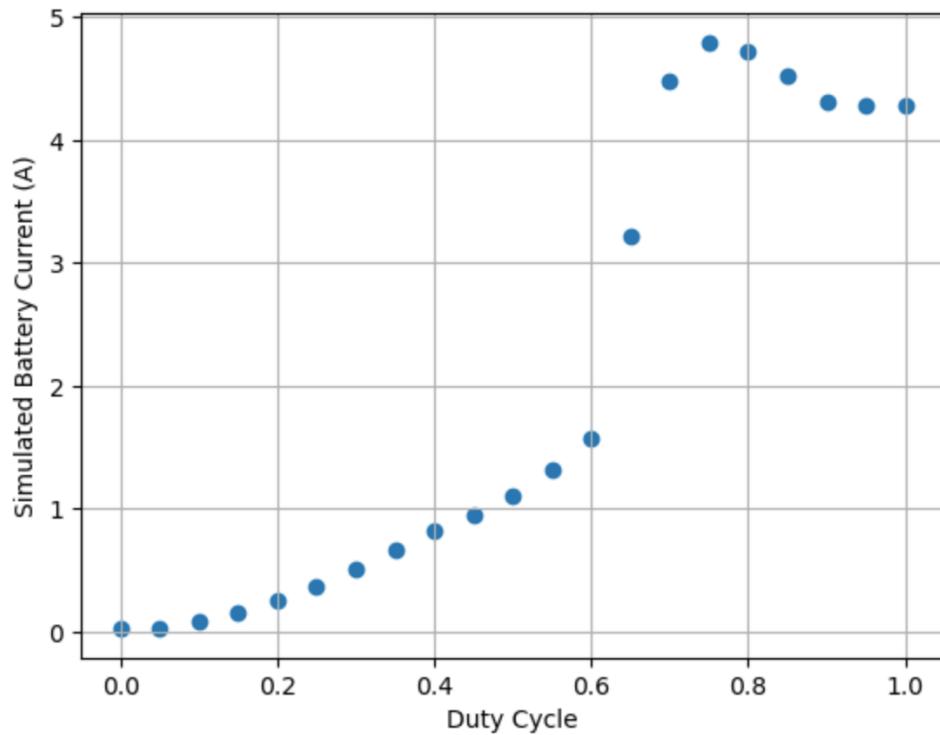


Figure 30: Simulated Battery Current vs Duty Cycle

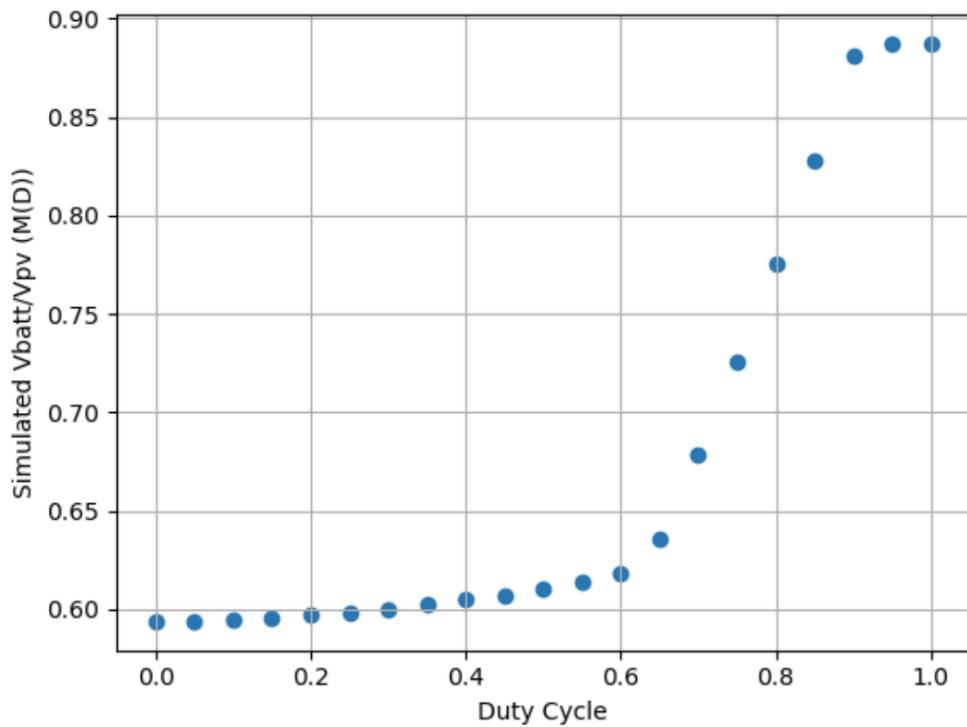


Figure 31: Simulated M(D) vs Duty Cycle

The simulated results match well with those from our buck converter system. They demonstrate the same constrained-system characteristics up to $D = 0.6$, and expected converter dynamics above this, until around $D = 0.9$. At this point, the buck converter ceases to operate in its typical fashion due to D nearing 1, with the MOSFET nearly always on and the diode nearly always off. The scaling of each of the graphs is slightly different - this may result from inaccurate solar insolation measurement, the use of constant battery voltage, or other un-modeled parasitic elements. Otherwise, simulated results are within about 10% of our measured values.

Optimal Operating Points and Comparison to Direct Energy Transfer

Based on measured data, the optimum duty cycle to operate at is around $D = 0.8$, in order to maximize battery current. More measurements in the region $D = 0.7$ to $D = 0.9$ would help determine this more precisely. The maximum power delivered to the battery at this duty cycle is about 60 W, though this is dependent on the solar insolation, which was measured to be 750 W/m^2 at time of data collection.

We can compare the battery charging power between MPPT and the direct energy transfer (DET) system. The power supplied to the battery in the DET system was 32 W at 550 W/m^2 solar irradiance. Scaling this to 750 W/m^2 using a linear scale would result in a power output of 44 W. The buck converter with variable duty cycle allowed for the PV panel to operate at its maximum power point while charging the battery, instead of being forced by the battery voltage to a non-ideal operating point as in the DET system. This resulted in a nearly 36% increase in power supplied to the battery given similar solar insolation conditions.