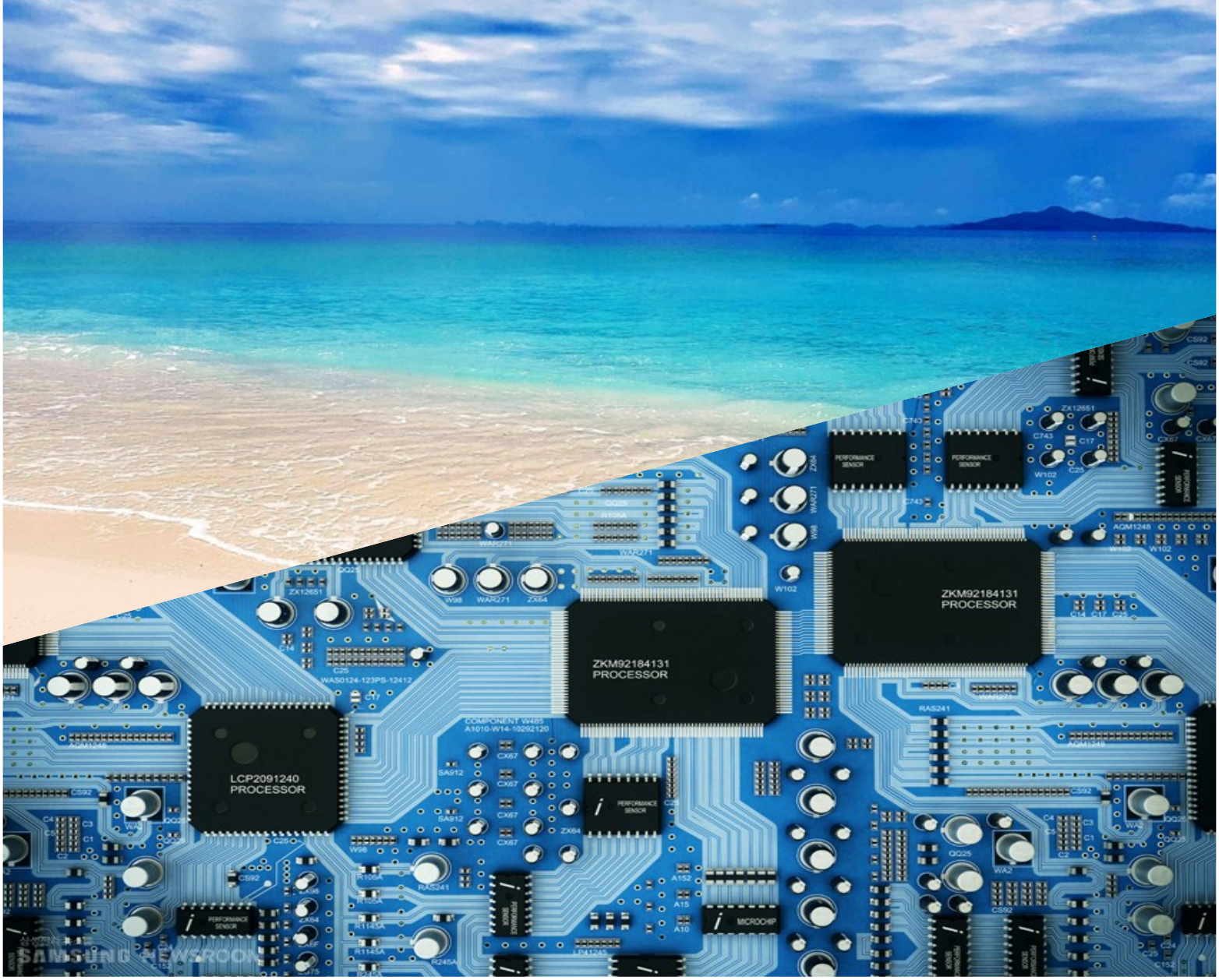

2022 AI-S^{2}oC

June Symposium

AI-Embedded S^{2}oftware on Chip Lab.

July 4, 2022

Kyungpook National University, Daegu

AI-S^{2}oC Lab

KNU

Contents

About

AI-S^{2}oC

Our research group focuses on the following architecture to realize the accelerated intelligence in systems-software-on-chip by dynamic partial replacement of on-chip hardware and embedded software.

Organizing committee

Daejin Park

Timetable

CT: Contributed Talk IT: Invited Talk

Monday, 4 of July (IT1-713)

09:40–10:00	**Opening**		
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10:30–11:00	CT	**Dongkyu Lee** Ph.D. Student, KNU	Clustering System: Platforms and Network Connections
11:00–11:30	CT	**Myeongjin Kang** Ph.D. Student, KNU	Introduction of Distributed Computing
11:30–12:00	CT	**Sunghoon Hong** Ph.D. Student, KNU	Cluster Board Analysis for Cluster Operations of Compute Modules
12:00–13:00	**Lunch**		
13:00–13:30	CT	**Jisu Kwon** Ph.D. Student, KNU	Study on the Tensorflow Lite and EdgeTPU Architecture
13:30–14:00	CT	**Heuijee Youn** Ph.D. Student, KNU	FPGA Programming with TerasIC DE1-SoC
14:00–14:30	CT	**Junseo Chang** B.S. Student, SNU	ML for Low Power Compiler Optimization
14:30–15:00	CT	**Dongkyu Jung** M.S. Student, KNU	Embedded board OS - Structure and Operation
15:00–15:30	CT	**Hyejoo Kim** B.S. Student, KNU	Implementation of Animated Walkthrough using Blender and Unity
15:30–16:00	**Break**		
16:00–16:30	CT	**Seunghyun Park** B.S. Student, KNU	Hardware Accelerator Design for CNN
16:30–17:00	CT	**Nayoung Kwon** B.S. Student, KNU	Introduction to Processor Optimization Development
18:00–18:30	IT	**Yonghun Lee** Ph.D. Student, AI Semiconductor Centor & KNU	Simulation of Maximum Power Point Tracking (MPPT) using Boost Converter in MATLAB-Simulink. Perturb & Observe Algorithm is used for the MPPT Implementation

List of Abstracts – Talks

Monday, 4 of July (IT1-713)

Singular Value Decomposition: Digital Twin and Image Processing

Seungmin Lee **CT**

Kyungpook National University 10:00–10:30

Digital twin is a technology that predicts results in advance by simulating real-world situations with a computer. Singular value decomposition is effective method in modeling the linear relationship between input data and output data as a transfer function. In particulate matter sensing experiment, the transfer function between the particle count of the test device and the particulate matter of the reference device was obtained using singular value decomposition. Then, by multiply the transfer matrix to particle count of the test device, we can predict the particulate matter of the test device which is similar to reference. In addition, we confirmed that the singular value decomposition is efficient for image processing such as compression and denoising.

Clustering System: Platforms and Network Connections

Dongkyu Lee **CT**

Kyungpook National University 10:30–11:00

Clustering is a technique to increase computational performance by operating multiple devices with low performance as a single device. To make a cluster-based acceleration board, we have studied the techniques of a cluster that will orchestrate each node. Also, the schematic of the Ethernet connection used for the connection between the cluster nodes was studied.

Introduction of Distributed Computing

Myeongjin Kang **CT**

Kyungpook National University 11:00–11:30

In this symposium, we would like to introduce distributed computing. The concept of distributed computing, the background to implement it, and the method of distributed computing will be introduced. In addition, based on the presentation at the conference HPDC 2022, I will introduce the current direction of distributed computing and the research being conducted to achieve distributed computing, and I will talk about how I can tie it to my research.

Cluster Board Analysis for Cluster Operations of Compute Modules

Sunghoon Hong **CT**

Kyungpook National University 11:30–12:00

A computer cluster is a set of computers in which several computers are connected and operate as one system. Cluster computers are generally connected through a high-speed local area network (LAN), and the operating system runs on each node used as a server. Because it is configured through a combination of an inexpensive microprocessor, a high-speed network, and software for distributed computing, it provides greater performance and safety than a single computer, and is cost-effective. In order to design a computer cluster system, let's learn about the cluster board.

Study on the Tensorflow Lite and EdgeTPU Architecture

Jisu Kwon **CT**

Kyungpook National University 13:00–13:30

The Coral Dev Board, designed by Google to enable AI on edge, is a combination of AP and hardware accelerator. This study analyze the difference between an AI application that conducts on a high-spec PC or server and an AI application that runs on edge device. The AI hardware accelerator EdgeTPU designed by Google is a lighter version of the existing TPU to a suitable for the edge. This study analyze what process we need to go through to transform Tensorflow model in order to use the EdgeTPU accelerator. Also, compare the execution time difference when using the CPU alone when executing the classification application on the Coral Dev Board and when receiving the acceleration of the Edge TPU. Using EdgeTPU to accelerate AI applications requires several constraints and preprocessing on the model. This study analyze the design direction of domain-specific hardware accelerators from the overhead that exists in the Edge TPU.

FPGA Programming with TerasIC DE1-SoC

Heuijee Youn **CT**

Kyungpook National University 13:30–14:00

Recently, as the demand for lightweight embedded boards has increased, the use of embedded boards has increased. Accordingly, I would like to explain the steps to apply the image processing studied previously to the lightweight embedded board. Intel's DE1-SoC Board was used, and Intel's tools such as Quartus and monitor programs were used. First, I studied the structure of the board and how to program it according to each structure. Using this method, I made a program to control the board such as GPIO, Gsensor, I2C, and control panel of the board. In addition, I learned the basic structure of image processing by outputting the canny edge detection algorithm to VGA using the CPU and FPGA on the board. In the future, I plan to conduct various studies such as lane recognition using opencl of the board, cnn classifier, and graphic animation implementation.

ML for Low Power Compiler Optimization

Junseo Chang **CT**

Seoul National University 14:00–14:30

The performance of the written code greatly depends on the compiler optimizations. While the -O3 options in LLVM and GCC compiler are well known for generating highly optimized codes, recent studies shows that compiler optimization using ML approaches generates faster and more efficient intermediate codes. These approaches utilizes exisiting compiler passes and find the optimal compiler optimizations by searching for optimal combinations and orders of passes which maximize performance. In this talk, we will introduce motivations in ML compiler optimizations, especially focusing on studies using RL approaches. We then demonstrate our ongoing research, which aim to develop compiler optimization ML model for generating optimal low power intermediate codes.

Embedded board OS - Structure and Operation

Dongkyu Jung **CT**

Kyungpook National University 14:30–15:00

Increased performance of embedded boards and various Linux lightweight tools have made operating systems available on various boards. Through many developments, tools to build a full package that can be executed with only a few settings of the user have also recently been distributed. In this symposium, we looked at the components needed to use the operating system on the embedded board and how the boot process goes from the board's power on to the user shell output.

Implementation of Animated Walkthrough using Blender and Unity

Hyejoo Kim **CT**

Kyungpook National University 15:00–15:30

We will learn about modeling and rendering used in VR and implement an animated walk-through that can be experienced directly. The end goal is to create a simple art gallery. Design a floor plan for a gallery and create a 3D architectural structure using Blender. Then, import the created model into Unity. Exhibit and view the photos you want through this gallery. Additionally, learn more about how to optimize your project for performance and VR convenience.

Hardware Accelerator Design for CNN

Seunghyun Park **CT**

Kyungpook National University 16:00–16:30

CNN models the brain structure of animals. It is the basic model for deep learning. The basic unit of the neural network is an operator called a 'neuron'. For a neural network to learn on its own, the weight and threshold of the neural network must be determined by itself from the given data. Each image of training data is read into the neural network, and the output value of the neural network is calculated. Then, the squared error with the correct answer attached to one image is calculated, and the weight and threshold are determined by computer so that the sum E of the squared error is minimized. The mathematical procedure is an optimization, and the sum of errors E is called the objective function for optimization. Thus, neural networks can learn on their own. In this project, We will propose a design for CNN and its algorithm ideas.

Introduction to Processor Optimization Development

Nayoung Kwon **CT**

Kyungpook National University 16:30–17:00

ASIC Chip design is made in more complicated processes. One of the process called CTS(Clock Tree Synthesis) is important role for Place and Route and Chip's timing problem. It assesses that RTL synthesizable verilog source puts to Open-Source Parser-Verilog added Shallow CTS Algorithm and the CTS output source is verified CTS synthesizable and speed of the progress through Digital Synthesis Flow. Shallow CTS Algorithm is used DFS(Depth First Search) and it proceeds buffer insertion from delay size. This research is provided whether the large size RTL source can check CTS synthesizable and can deduce CTS result.

Simulation of Maximum Power Point Tracking (MPPT) using Boost Converter in MATLAB-Simulink. Perturb & Observe Algorithm is used for the MPPT Implementation

Yonghun Lee **IT**

AI Semiconductor Center & Kyungpook National University 18:00–18:30

TBD

List of Participants

Professor	
Daejin Park	Kyungpook National Univ.

Post-Doc.	
Seungmin Lee	Kyungpook National Univ.

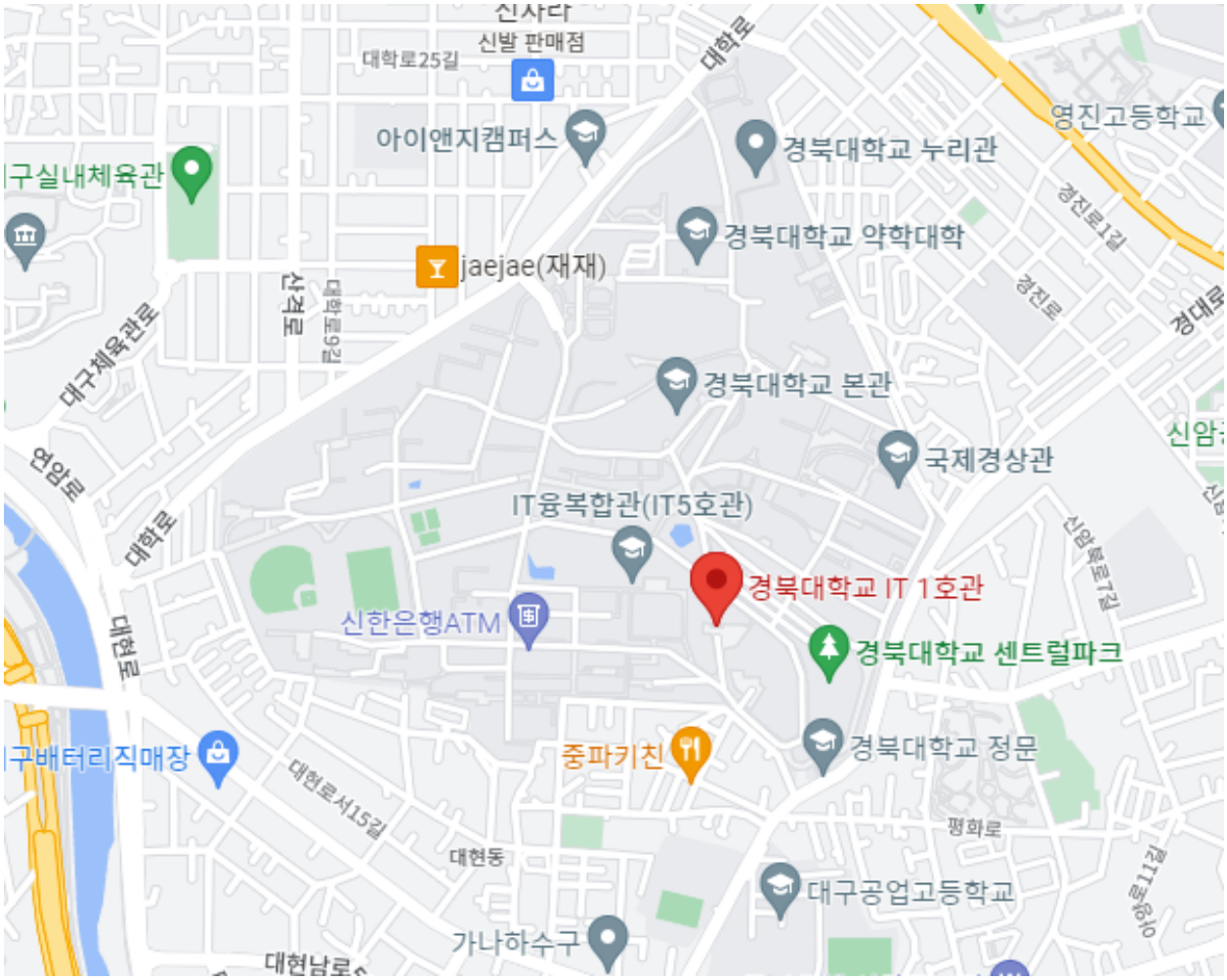
Ph.D. Student	
Sunghoon Hong	Kyungpook National Univ.
Dongkyu Lee	Kyungpook National Univ.
Jisu Kwon	Kyungpook National Univ.
Myeongjin Kang	Kyungpook National Univ.
Heuijee Youn	Kyungpook National Univ.
Seongho Cho	LG Display & KNU
Joonghyun An	SK Hynix & KNU
Yonghun Lee	AI Semiconductor Center & KNU

M.S. Student	
Dongkyu Jung	Kyungpook National Univ.

B.S. Student	
Junseo Chang	Seoul National Univ.
Nayoung Kwon	Kyungpook National Univ.
Seunghyun Park	Kyungpook National Univ.
Hyejoo Kim	Kyungpook National Univ.

Useful Information

AI-S^{2}oC Symposium will be held in **IT1, Room 613 (10:00–12:00)** and **IT1, Room 713 (13:00–19:00)**.



Partner Institutions and Sponsors

Our research group has been sponsored from the national research fund (NRF), research institutes and various industrial companies. Welcome to contact us about the technology transfer, technical consulting, and discussion for future collaboration.

Sponsors