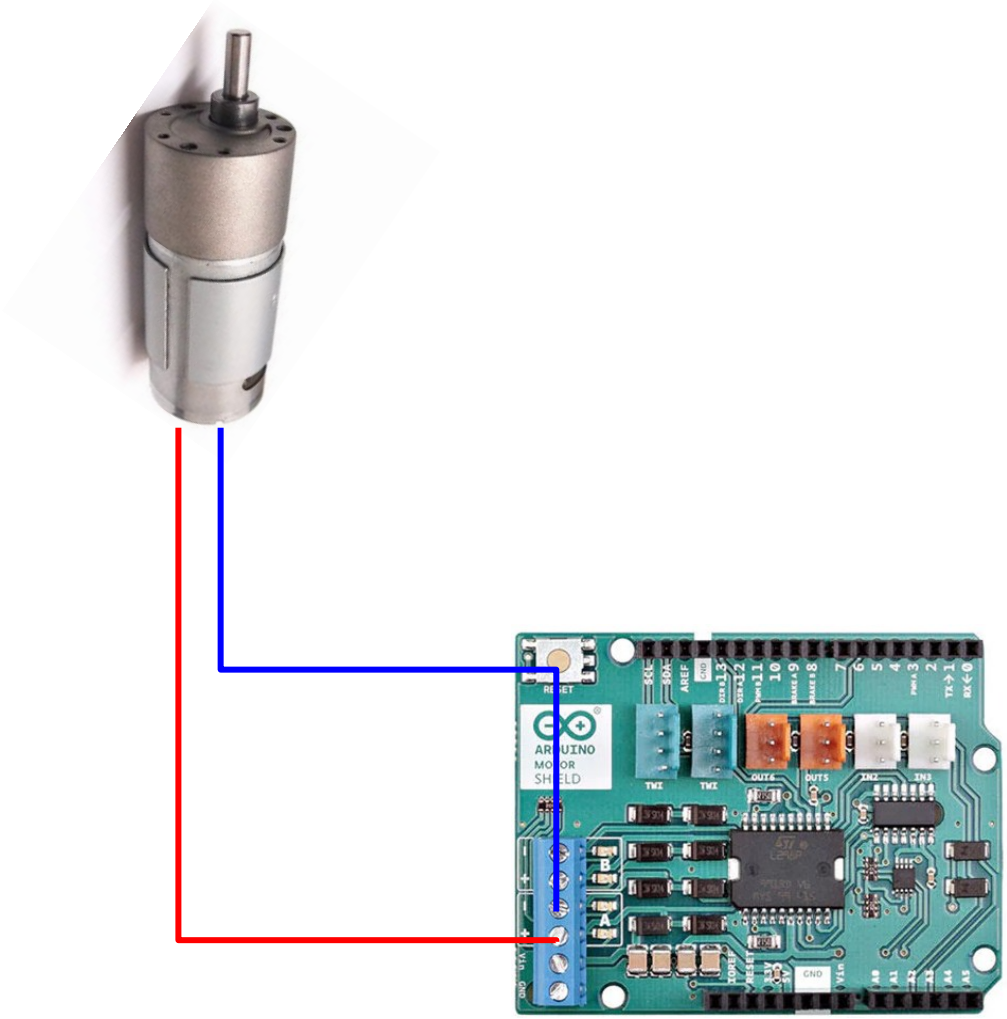
임베디드 기반 SW 개발 프로젝트

AURIX TC275 보드 PWM 사용

- Pulse Width Modulation 기반 모터 구동 -

현대자동차 입문교육
박대진 교수

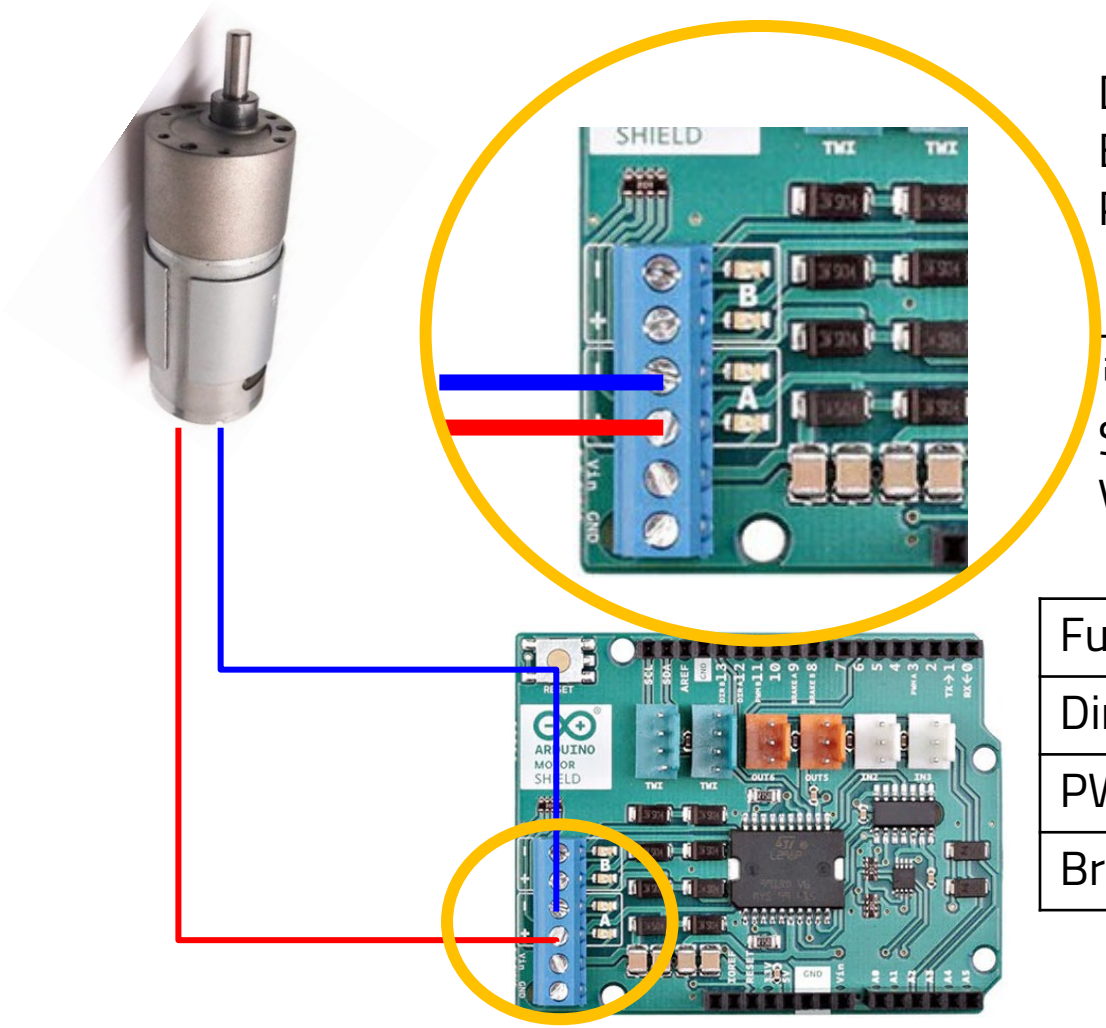
Lab: Motor Dimming



DC 모터의 출력은 입력되는 전압 값에 따라 결정된다.
모터쉴드는 디지털신호와 PWD 신호를 입력받아 모터를 제어하는 아날로그 신호를 생성한다.

Function	Motor shield	Shield buddy
Direction	D12	P10.1
PWM	D3	P2.1
Brake	D9	P2.7

Lab: Motor Dimming



Direction pin의 입력은 모터의 동작방향
Brake pin의 입력은 모터의 동작 여부
PWM pin의 입력은 모터의 동작 RPM을 결정

모터쉴드를 shield buddy에 장착하고, 모터 출력단에 모터의 +,- 케이블을 연결한다.
Shield buddy의 직류연결 단자나 모터쉴드의 Vin단자에 직류전원을 인가한다.

Function	Motor shield	Shield buddy
Direction	D12	P10.1
PWM	D3	P2.1
Brake	D9	P2.7

Lab: Motor Dimming

```
void initMotor(void)
{
    P10_IOCR0.U &= ~(0x1F << PC1_BIT_LSB_IDX);
    P02_IOCR0.U &= ~(0x1F << PC1_BIT_LSB_IDX);
    P02_IOCR4.U &= ~(0x1F << PC7_BIT_LSB_IDX);

    P10_IOCR0.U |= 0x10 << PC1_BIT_LSB_IDX;
    P02_IOCR0.U |= 0x11 << PC1_BIT_LSB_IDX;
    P02_IOCR4.U |= 0x10 << PC7_BIT_LSB_IDX;
}
```

Table 13-16 Port 10 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P10.1	I	General-purpose input	P10_IN.P1	P10_IOCR0. PC1	$0XXXX_B$
		GTM input	TIN103		
		QSPI1 input	MRST1A		
		GPT120 input	T5EUDB		
	O	General-purpose output	P10_OUT.P1		$1X000_B$
		GTM output	TOUT103		$1X001_B$
		QSPI1 output	MTSR1		$1X010_B$
		QSPI1 output	MRST1		$1X011_B$
		MSC0	EN01		$1X100_B$
		VADC output	VADCG6BFL1		$1X101_B$
		MSC0 output	END03		$1X110_B$
		Reserved	–		$1X111_B$

P10.1, P2.7 pin은 digital output을 위해 0x10을 setting
P2.1 pin은 PWM output을 위해 0x11을 setting

Function	Motor shield	Shield buddy
Direction	D12	P10.1
PWM	D3	P2.1
Brake	D9	P2.7

Lab: Motor Dimming

```
GTM_CMU_FXCLK_CTRL.U &= ~(0xF << FXCLK_SEL_BIT_LSB_IDX);
GTM_CMU_CLK_EN.U |= 0x2 << EN_FXCLK_BIT_LSB_IDX;

GTM_TOM0_TGC1_GLB_CTRL.B.UPEN_CTRL1 |= 0x2;
GTM_TOM0_TGC1_ENDIS_CTRL.B.ENDIS_CTRL1 |= 0x2;
GTM_TOM0_TGC1_OUTEN_CTRL.B.OUTEN_CTRL1 |= 0x2;

GTM_TOM0_CH9_CTRL.B.SL |= 0x1;
GTM_TOM0_CH9_CTRL.B.CLK_SRC_SR |= 0x1;

GTM_TOM0_CH9_SR0.U = 12500 - 1;
//GTM_TOM0_CH9_SR1.U = 1250 - 1;

GTM_TOUTSEL0.U &= ~(0x3 << SEL1_BIT_LSB_IDX);
}
```

TOUTSEL0 ⟶ TOUT00 ~~ TOUT15
TOUTSEL1 ⟶ TOUT16 ~~ TOUT31
TOUTSEL2 ⟶ TOUT32 ~~ TOUT47
TOUTSEL3 ⟶ TOUT48 ~~ TOUT63
TOUTSEL4 ⟶ TOUT64 ~~ TOUT79
TOUTSEL5 ⟶ TOUT80 ~~ TOUT95
TOUTSEL6 ⟶ TOUT96 ~~ TOUT103

P00.12	TIN21	TOUT21	TIM0_3	TIM1_3	TOM0_3	TOM1_3	ATOM 2_3	ATOM 3_3
P02.0	TIN0	TOUT0	TIM0_0	TIM1_0	TOM0_8	TOM1_8	ATOM 0_0	ATOM 1_0
P02.1	TIN1	TOUT1	TIM0_1	TIM1_1	TOM0_9	TOM1_9	ATOM 0_1	ATOM 1_1

TOUTSELn (n = 0-14)
Timer Output Select Register **($9FD30_H+n*4_H$)** **Reset Value: 0000 0000_H**

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
SEL15	SEL14	SEL13	SEL12	SEL11	SEL10	SEL9	SEL8
rw	rw	rw	rw	rw	rw	rw	rw

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
rw	rw	rw	rw	rw	rw	rw	rw

GTM 활성화 및 클락 설정을 동일하게 진행하고 P2.1 핀의 TOM출력에 맞게 레지스터 선정 및 비트 위치 설정
P2.1핀은 TOM_9 채널의 TOUT01과 연결되어 있고 이는 TOUTSEL0 레지스터에 위치하고 있다.
TOUT01은 2번째 핀이다.

Lab: Motor Dimming

```
GTM_CMU_FXCLK_CTRL.U &= ~(0xF << FXCLK_SEL_BIT_LSB_IDX);
GTM_CMU_CLK_EN.U |= 0x2 << EN_FXCLK_BIT_LSB_IDX;

GTM_TOM0_TGC1_GLB_CTRL.B.UPEN_CTRL1 |= 0x2;
GTM_TOM0_TGC1_ENDIS_CTRL.B.ENDIS_CTRL1 |= 0x2;
GTM_TOM0_TGC1_OUTEN_CTRL.B.OUTEN_CTRL1 |= 0x2;

GTM_TOM0_CH9_CTRL.B.SL |= 0x1;
GTM_TOM0_CH9_CTRL.B.CLK_SRC_SR |= 0x1;

GTM_TOM0_CH9_SR0.U = 12500 - 1;
//GTM_TOM0_CH9_SR1.U = 1250 - 1;

GTM_TOUTSEL0.U &= ~(0x3 << SEL1_BIT_LSB_IDX);
}
```

GTM_TOMi_TGC0_GLB_CTRL (i=0-2)
TOMi TGC0 Global Control Register(08030_H+i*800_H) Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPEN_CTRL7		UPEN_CTRL6		UPEN_CTRL5		UPEN_CTRL4		UPEN_CTRL3		UPEN_CTRL2		UPEN_CTRL1		UPEN_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST_CH7	RST_CH6	RST_CH5	RST_CH4	RST_CH3	RST_CH2	RST_CH1	RST_CH0	Reserved							HOST_TRIG
w	w	w	w	w	w	w	w	r							w

GTM_TOMi_TGC0_ENDIS_CTRL (i=0-2)
TOMi TGC0 Enable/Disable Control Register (08070_H+i*800_H) Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIS_CTRL7		ENDIS_CTRL6		ENDIS_CTRL5		ENDIS_CTRL4		ENDIS_CTRL3		ENDIS_CTRL2		ENDIS_CTRL1		ENDIS_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

25.11.2 TOM Global Channel Control (TGC0, TGC1)

25.11.2.1 Overview

There exist two global channel control units (TGC0 and TGC1) to drive a number of individual TOM channels synchronously by external or internal events.

Each TGC[y] can drive up to eight TOM channels where TGC0 controls TOM channels 0 to 7 and TGC1 controls TOM channels 8 to 15.

The TOM submodule supports four different kinds of signalling mechanisms:

GTM_TOMi_TGC0_GLB_CTRL (i=0-2)
TOMi TGC0 Global Control Register(08030_H+i*800_H) Reset Value: 00000000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPEN_CTRL7		UPEN_CTRL6		UPEN_CTRL5		UPEN_CTRL4		UPEN_CTRL3		UPEN_CTRL2		UPEN_CTRL1		UPEN_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST_CH7	RST_CH6	RST_CH5	RST_CH4	RST_CH3	RST_CH2	RST_CH1	RST_CH0	Reserved							HOST_TRIG
w	w	w	w	w	w	w	w	r							w

TOM_9 채널은 TGC1에서 drive한다
GTM_TOM0_TGC1에서 채널 9는 2번째 채널 이므로 CTRL1의 UPEN, ENDIS, OUTEN을 설정 한다.

Lab: Motor Dimming

```
GTM_CMU_FXCLK_CTRL.U &= ~(0xF << FXCLK_SEL_BIT_LSB_IDX);
GTM_CMU_CLK_EN.U |= 0x2 << EN_FXCLK_BIT_LSB_IDX;

GTM_TOM0_TGC1_GLB_CTRL.B.UPEN_CTRL1 |= 0x2;
GTM_TOM0_TGC1_ENDIS_CTRL.B.ENDIS_CTRL1 |= 0x2;
GTM_TOM0_TGC1_OUTEN_CTRL.B.OUTEN_CTRL1 |= 0x2;

GTM_TOM0_CH9_CTRL.B.SL |= 0x1;
GTM_TOM0_CH9_CTRL.B.CLK_SRC_SR |= 0x1;

GTM_TOM0_CH9_SR0.U = 12500 - 1;
//GTM_TOM0_CH9_SR1.U = 1250 - 1;

GTM_TOUTSEL0.U &= ~(0x3 << SEL1_BIT_LSB_IDX);
}
```

GTM_TOM0_CHx_CTRL (x=0-14)
TOM0 Channel x Control Register'
$(08000_H+x*0040_H)$ Reset Value: 00000800_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		GCM	SPE M	Rese rved	OSM	Rese rved	TRIG OUT	Reserved			RST _CC U0	Reserved			
r		rw	rw	r	rw	r	rw	r			rw	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rese rved	CLK_SRC_SR			SL	Reserved										
r	rw			rw	r										

Field	Bits	Type	Description
SL	11	rw	Signal level for duty cycle 0_B Low signal level 1_B High signal level If the output is disabled, the output TOM_OUT[x] is set to inverse value of SL.

GTM_TOM0_CHx_CTRL (x=0-14)
TOM0 Channel x Control Register'
$(08000_H+x*0040_H)$ Reset Value: 00000800_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		GCM	SPE M	Rese rved	OSM	Rese rved	TRIG OUT	Reserved			RST _CC U0	Reserved			
r		rw	rw	r	rw	r	rw	r			rw	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rese rved	CLK_SRC_SR			SL	Reserved										
r	rw			rw	r										

CLK_SRC _SR	[14:12]	rw	**Clock source select for channel** The register CLK_SRC is updated with the value of CLK_SRC_SR together with the update of register CM0 and CM1. The input of the FX clock divider depends on the value of FXCLK_SEL (see CMU). 000_B CMU_FXCLK(0) selected: clock selected by FXCLKSEL 001_B CMU_FXCLK(1) selected: clock selected by FXCLKSEL/ 2^4 010_B CMU_FXCLK(2) selected: clock selected by

TOM_9 채널 CTRL의 SL, CLK_SRC_SR에서 신호값의 종류, clock cycle을 설정한다.
Shadow register에 CM0 값을 설정한다.

Lab: Motor Dimming

```
    //initERU();
    initMotor();
    initGTM();
    initVADC();
    //initButton();

    GTM_TOM0_TGC1_GLB_CTRL.U |= 0x1 << HOST_TRIG_BIT_LSB_IDX;

    unsigned short duty = 0;

    while(1)
    {
        VADC_startConversion();
        unsigned int adcResult = VADC_readResult();

        duty = 12500 * adcResult / 4096;

        P10_OUT.U |= 0x1 << P1_BIT_LSB_IDX;
        P02_OUT.U |= 0x1 << P1_BIT_LSB_IDX;
        P02_OUT.U &= ~(0x1 << P7_BIT_LSB_IDX);

        GTM_TOM0_CH9_SR1.U = duty;
    }
    return (1);
}
```

Init 함수 설정 및 TOM의 trigger event를 발생시킨다.

가변저항의 아날로그 출력을 받아 ADC로 변환 후 생성한 duty값을 모터쉴드로 전송한다.

결과, 가변저항의 저항 값에 따라 DC 모터의 RPM이 변경된다.

감사합니다. 휴식~~