

IE1204 Lecture 16

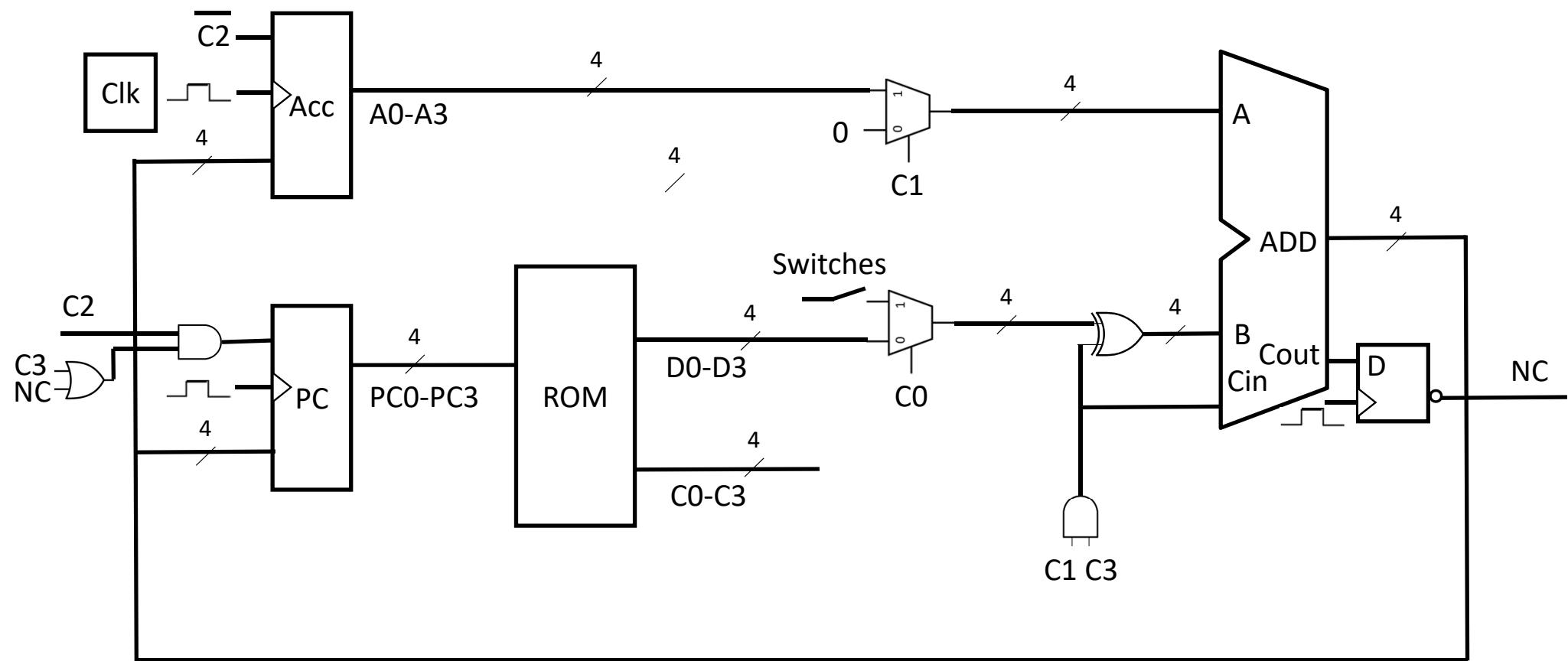
Single Cycle Computer and its parts

(See also Chapter 7)

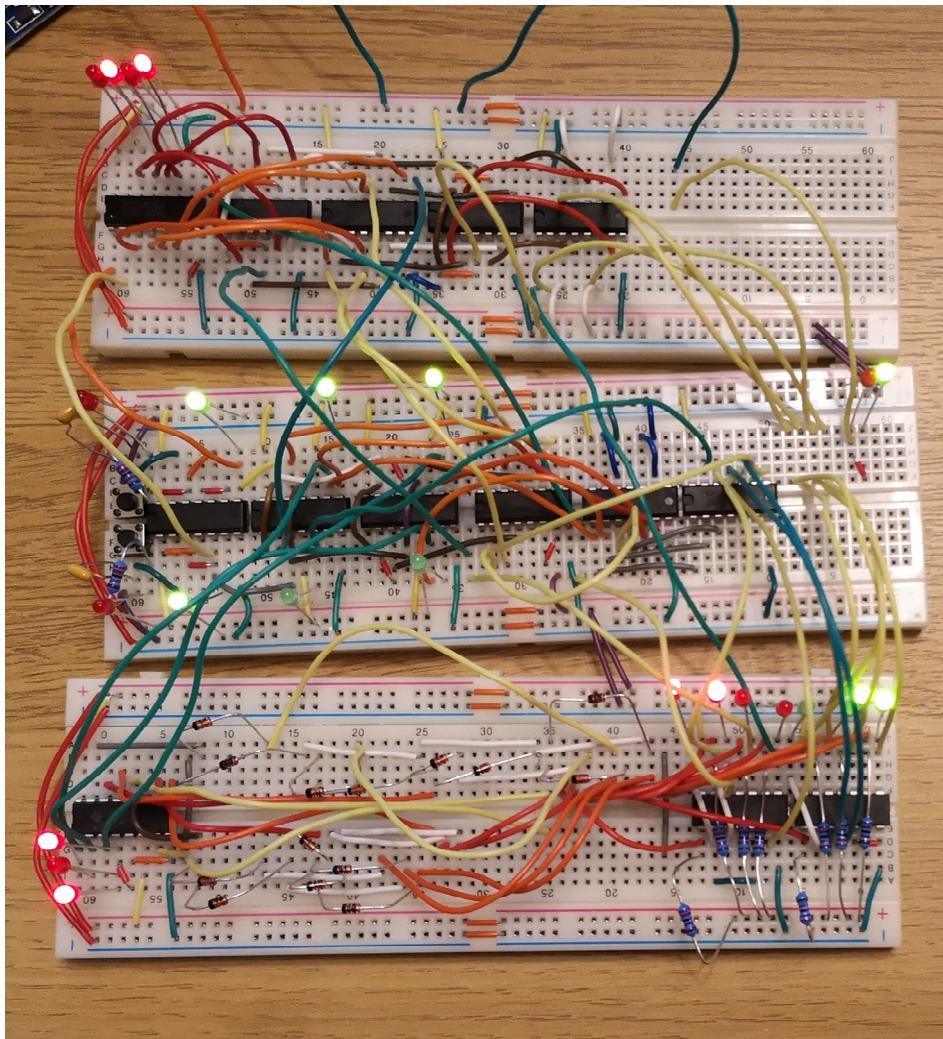
Carl-Mikael Zetterling

2019-10-11

Overview Single Cycle Computer

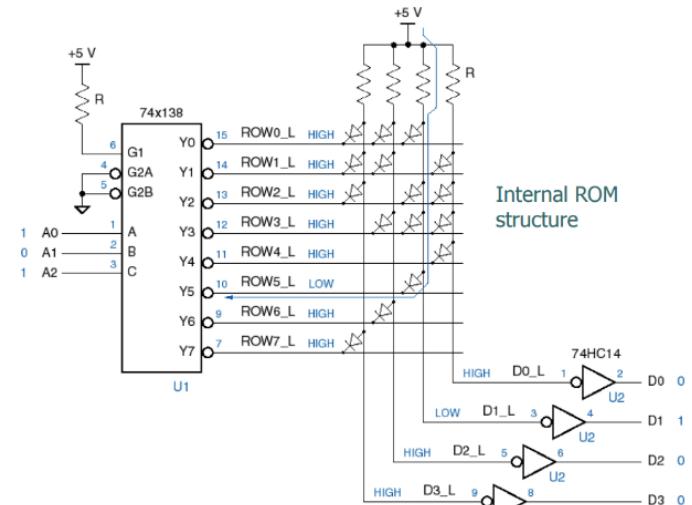
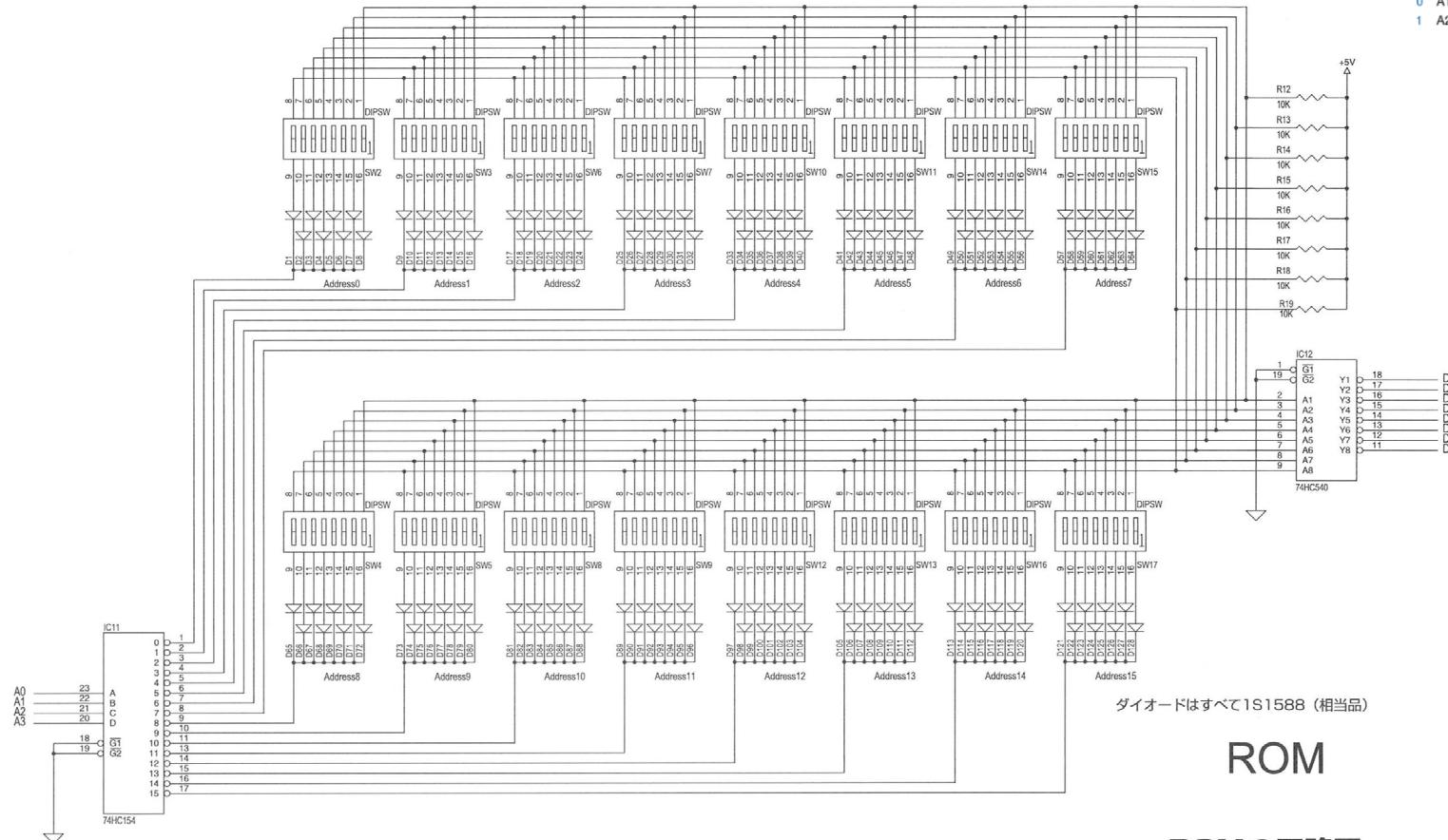


Single Cycle Computer* on Breadboard



* Requires 2 Lab Kits and
one extra Breadboard

Diode ROM



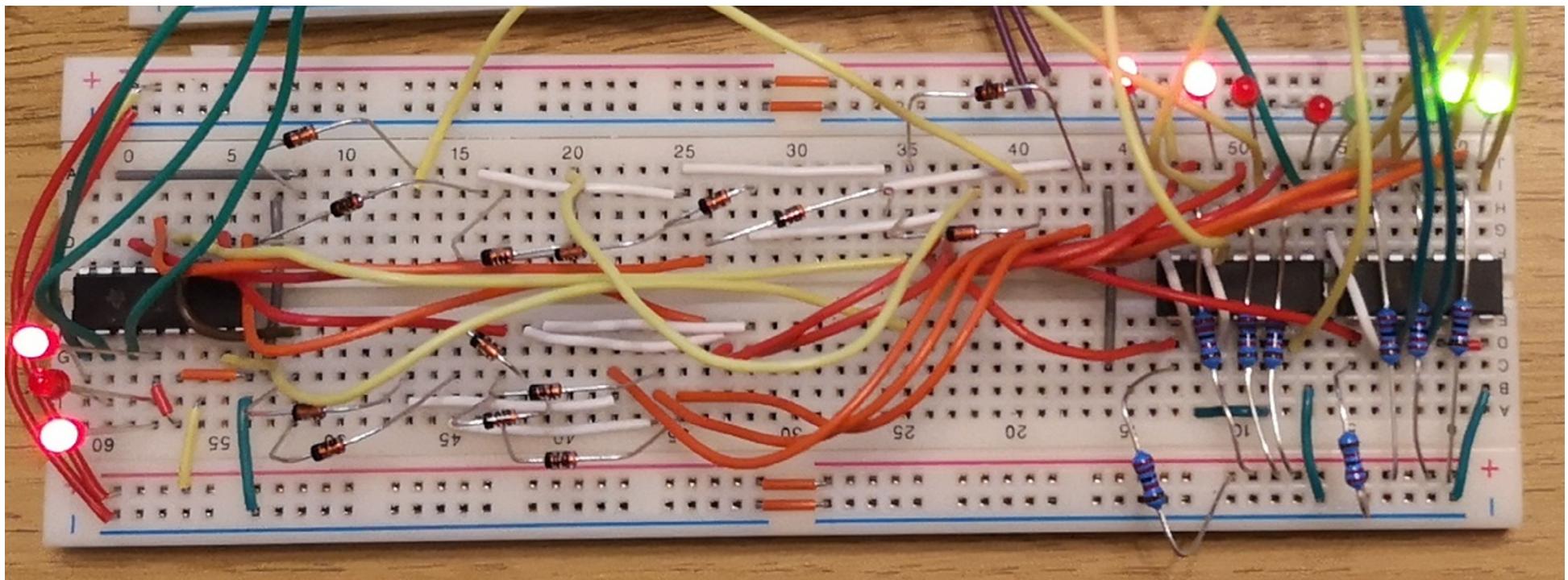
Internal ROM structure

ダイオードはすべて1S1588（相当品）

ROM

ROMの回路図

Diode ROM



74HC161

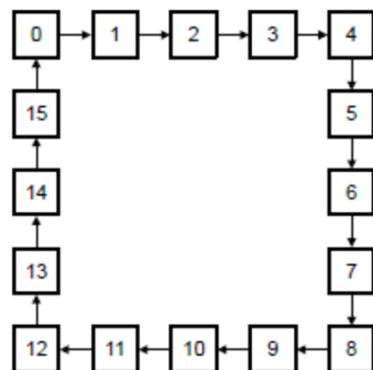


Fig. 7. State diagram

Table 2. Pin description

Symbol	Pin	Description
MR	1	asynchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V _{cc}	16	supply voltage

Table 3. Function table[1]

Operating modes	Input						Output	
	MR	CP	CEP	CET	PE	D _n	Q _n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	I	I	L	L
	H	↑	X	X	I	h	H	[2]
Count	H	↑	h	h	h	X	count	[2]
Hold (do nothing)	H	X	I	X	h	X	q _n	[2]
	H	X	X	I	h	X	q _n	L

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q_n = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition

X = don't care

↑ = LOW-to-HIGH clock transition

[2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)

Accumulator and Program Counter

Nexperia

74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset

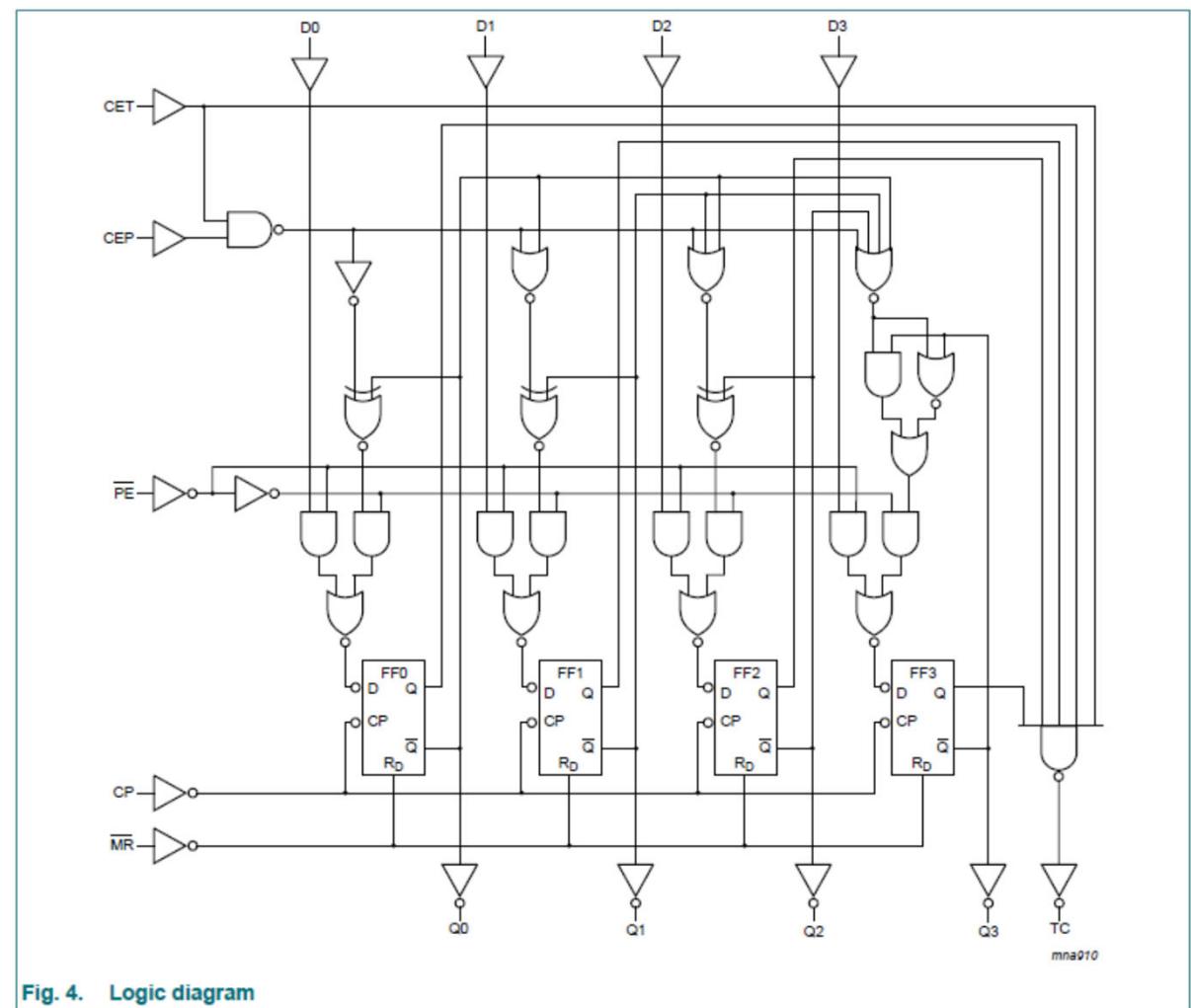


Fig. 4. Logic diagram

Accumulator and Program Counter

RESET

Nexperia

74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset

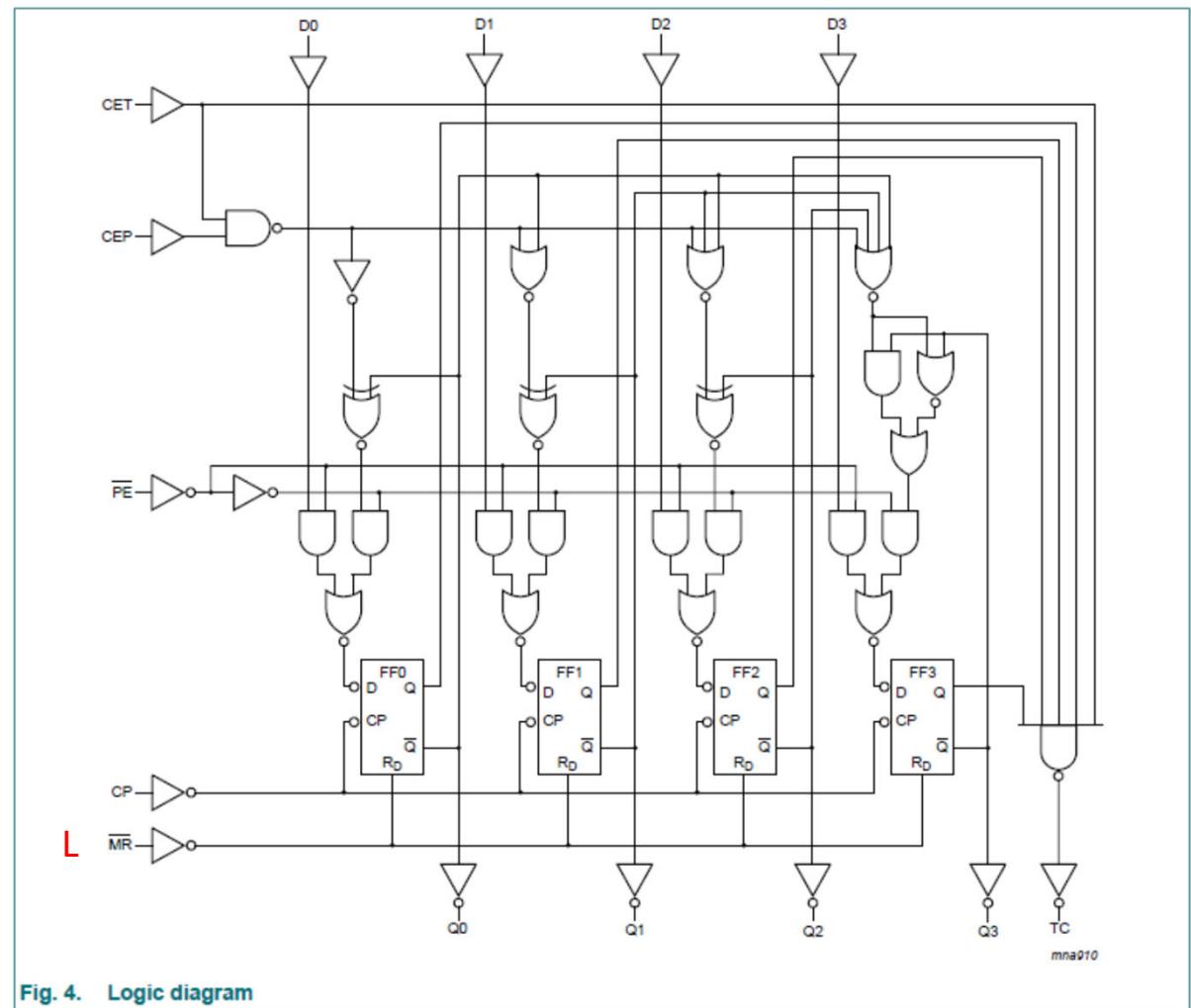
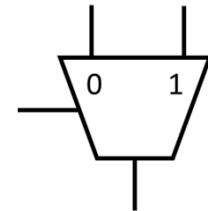


Fig. 4. Logic diagram

Accumulator and Program Counter

LOAD



x 4

Nexperia

74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset

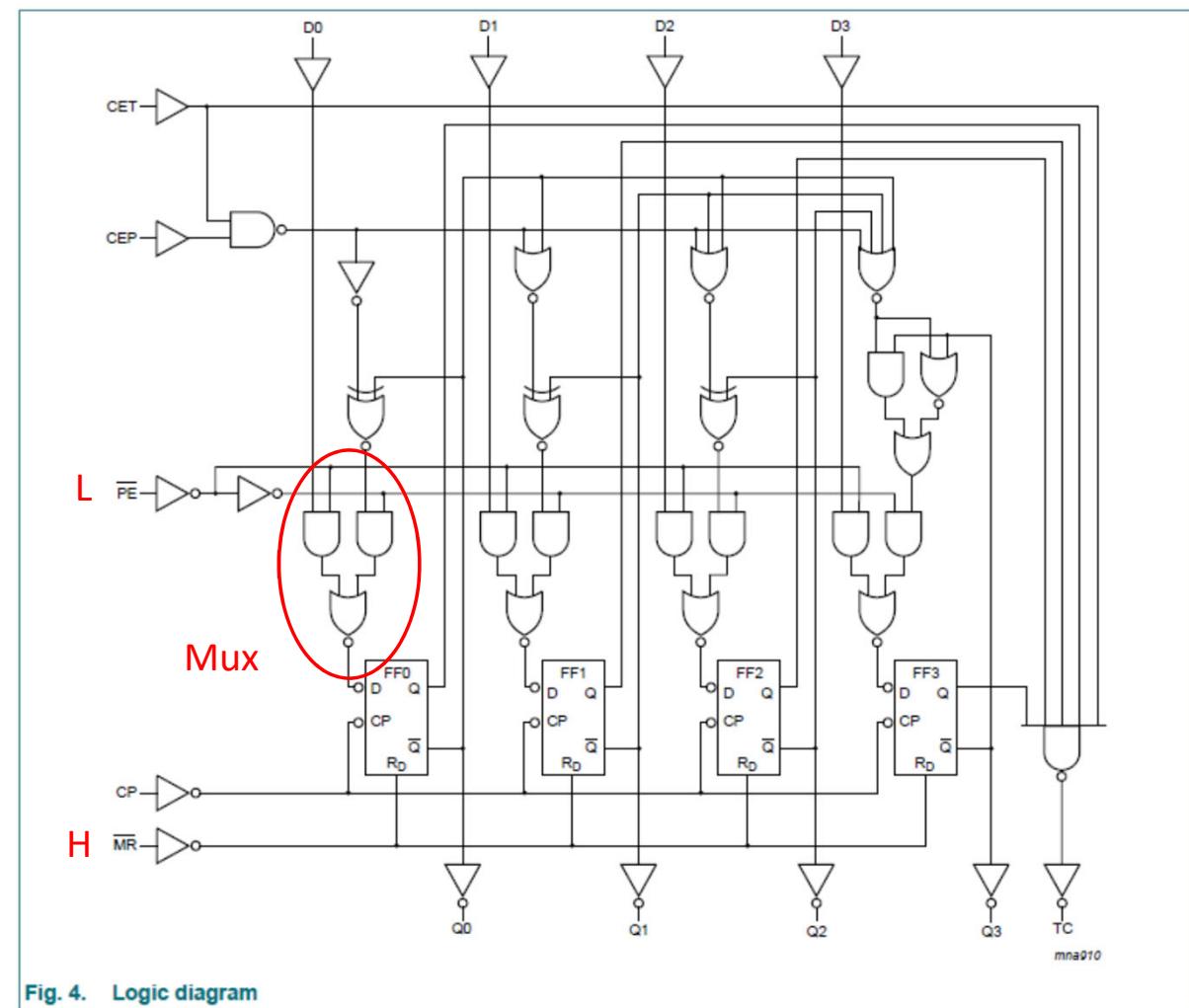
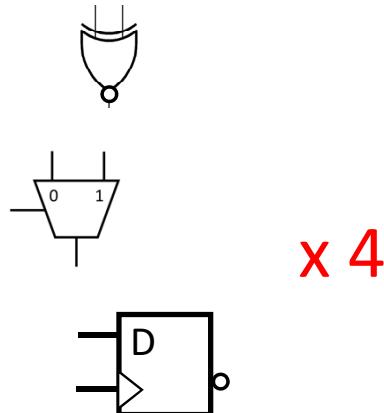


Fig. 4. Logic diagram

Accumulator and Program Counter

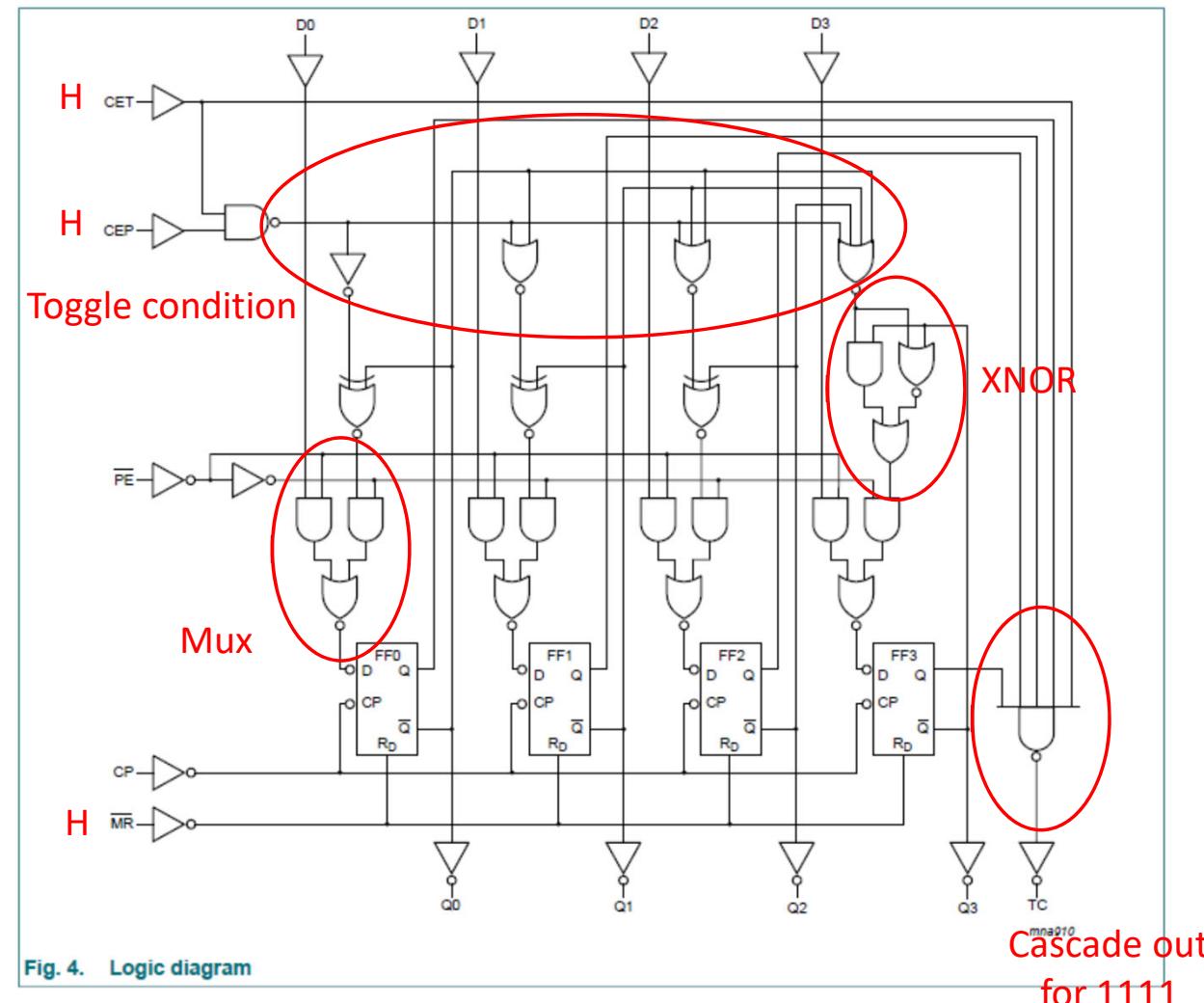
COUNT



Nexperia

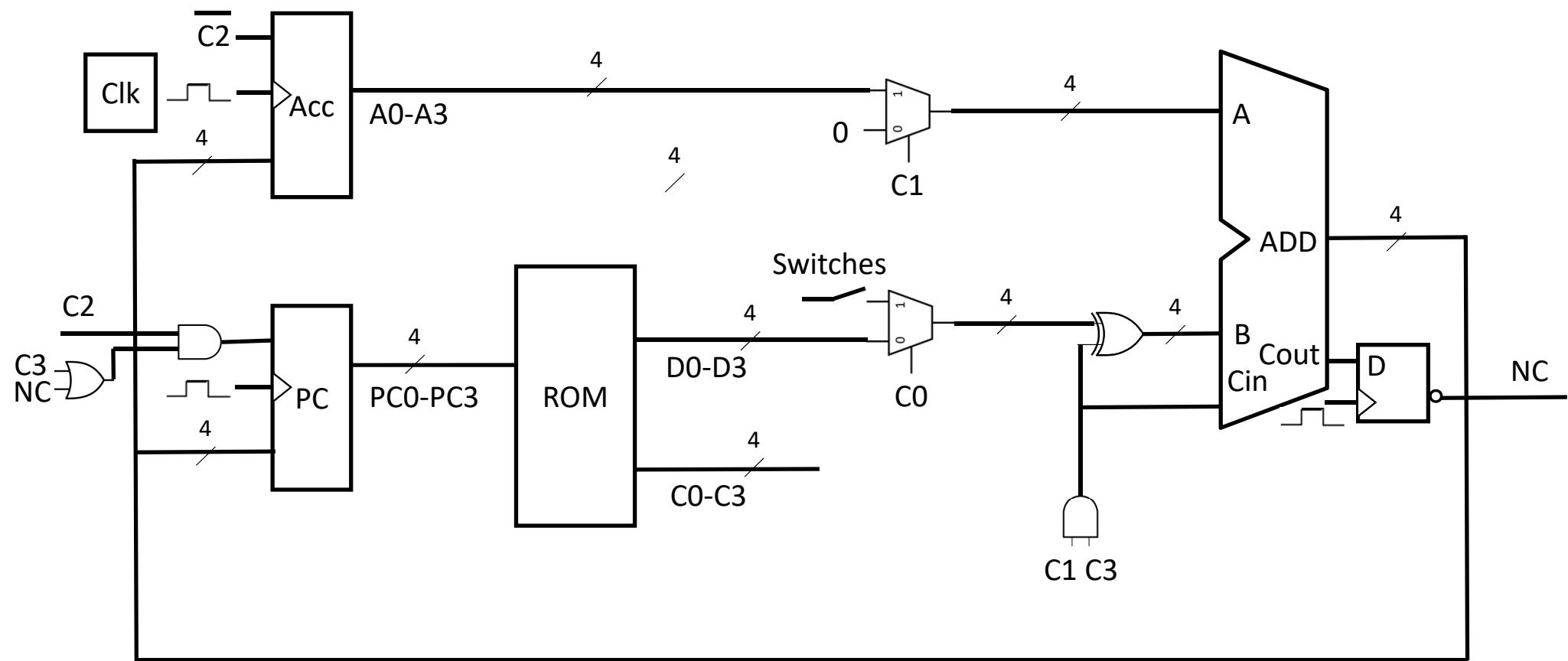
74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset



Operations (OP-codes)

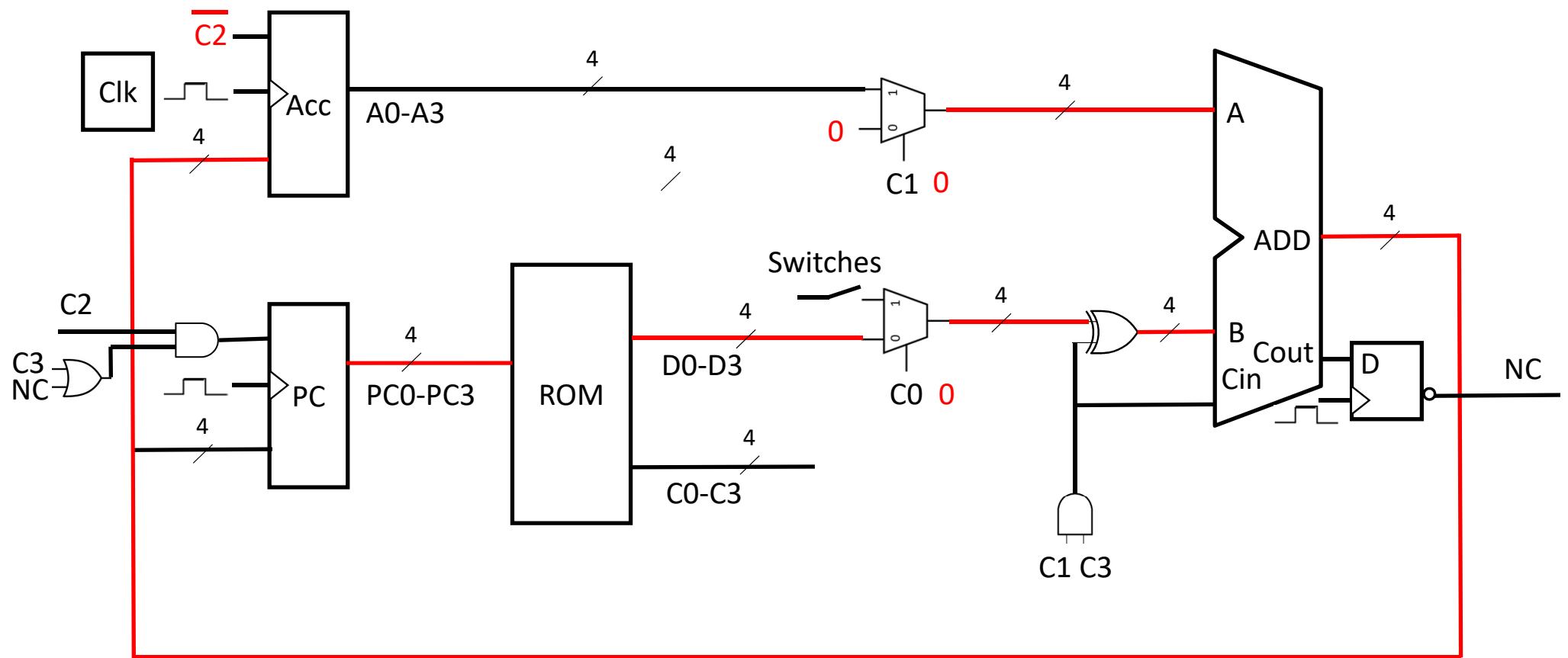
Overview Single Cycle Computer



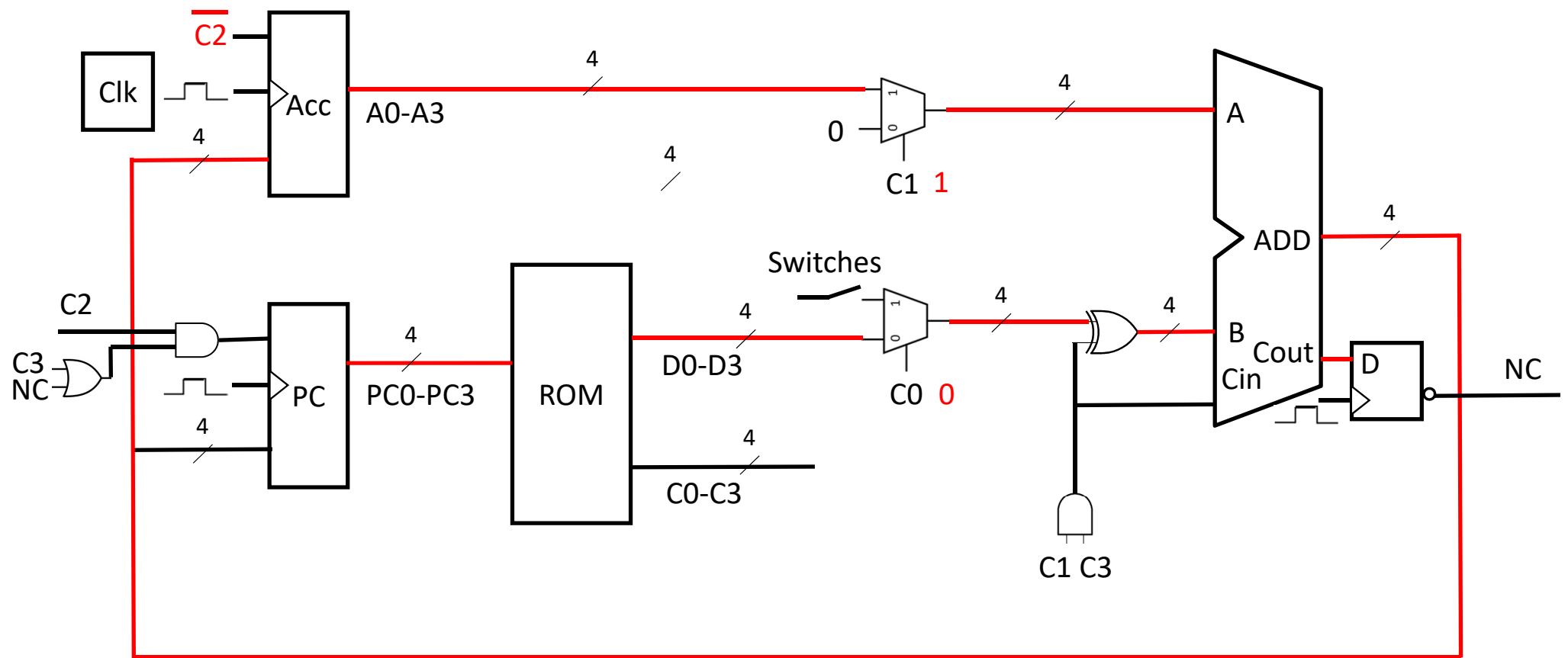
Sample Program

Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
000	00	0	0	0	0	0	0	0	0	Move A, 0	Reset Accumulator
001	21	0	0	1	0	0	0	0	1	ADD A, 1	Add 1 to accumulator
010	41	0	1	0	0	0	0	0	1	JNC 001	If no carry go back to Address 001
011	05	0	0	0	0	0	1	0	1	Move A, 5	Load 0101 to Accumulator
100	0A	0	0	0	0	1	0	1	0	Move A, A	Load 1010 to Accumulator
101	C3	1	1	0	0	0	0	1	1	JMP 011	Jump to Address 011

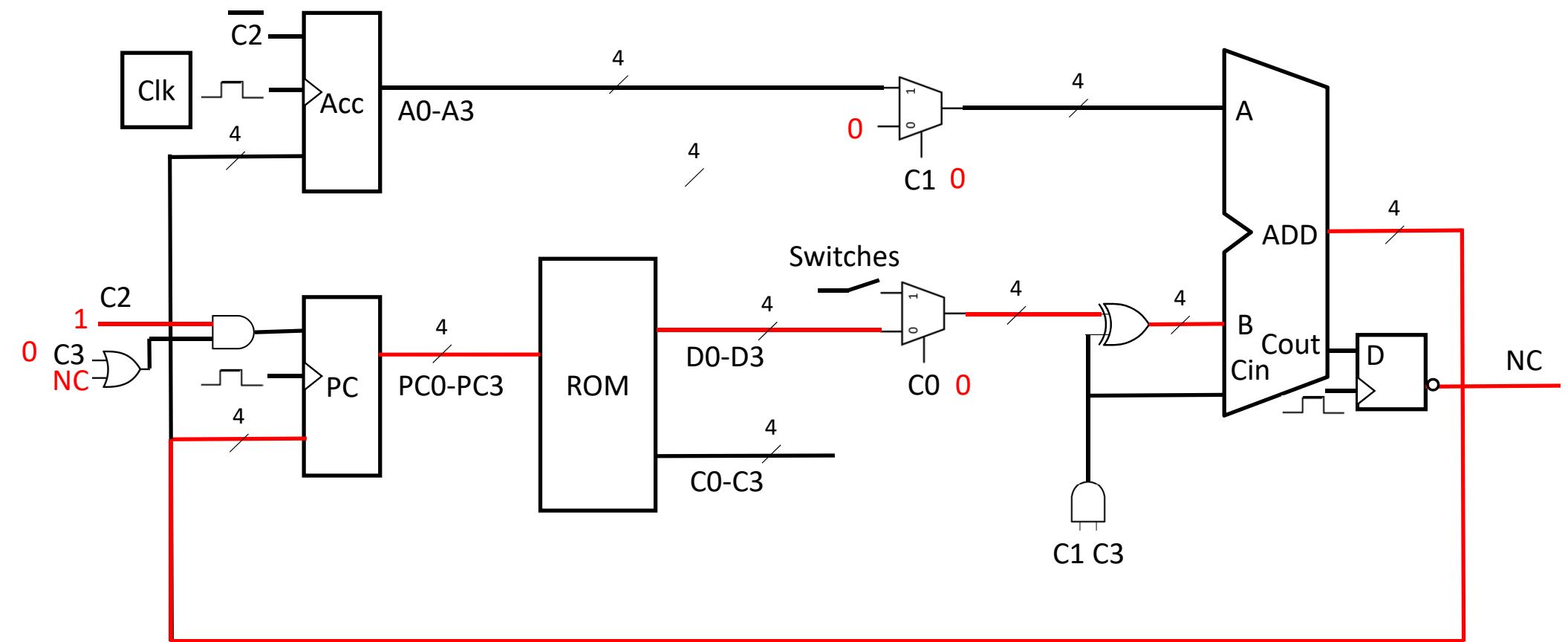
Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
000	00	0	0	0	0	0	0	0	0	Move A, 0	Reset Accumulator



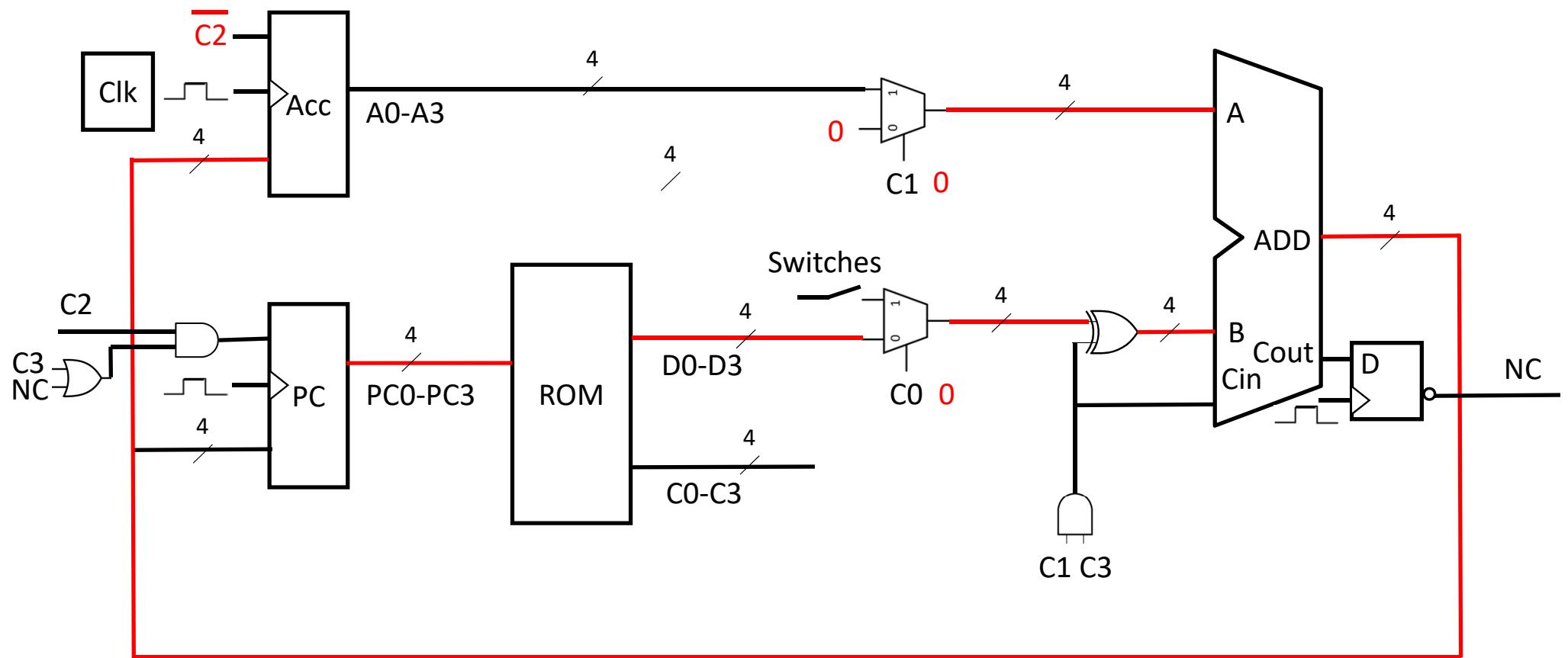
Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
001	21	0	0	1	0	0	0	0	1	ADD A, 1	Add 1 to accumulator



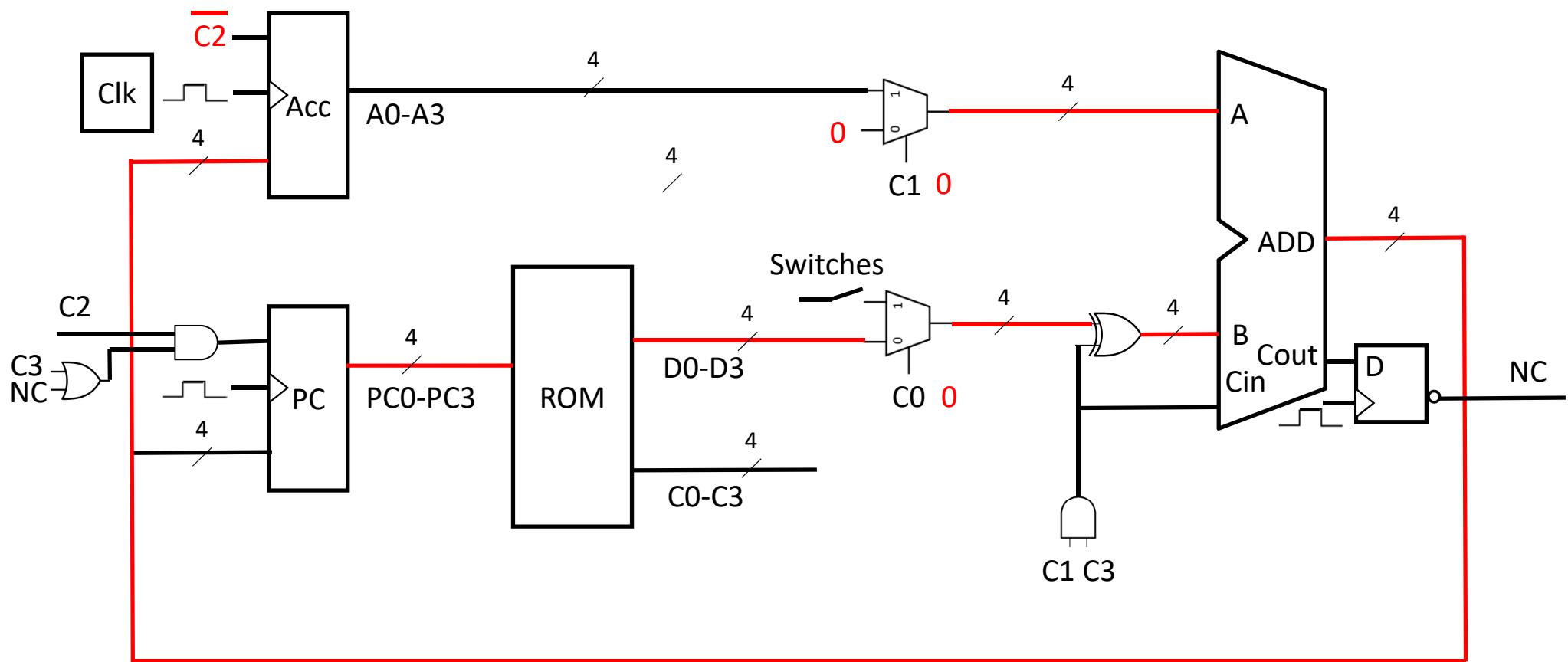
Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
010	41	0	1	0	0	0	0	0	1	JNC 001	If no carry go back to Address 001



Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
011	05	0	0	0	0	0	1	0	1	Move A, 5	Load 0101 to Accumulator



Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
100	0A	0	0	0	0	1	0	1	0	Move A, A	Load 1010 to Accumulator



Address	HEX	C3	C2	C1	C0	D3	D2	D1	D0	Operation	Comment
101	C3	1	1	0	0	0	0	1	1	JMP 011	Jump to Address 011

