



Intel® FPGA Download Cable User Guide



Online Version



Send Feedback

UG-USB81204

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1. Introduction to Intel® FPGA Download Cable

The Intel® FPGA Download Cable interfaces a USB port on a host computer to an FPGA mounted on a printed circuit board. The cable sends configuration data from the host computer to a standard 10-pin header connected to the FPGA. You can use the Intel FPGA Download Cable to iteratively download configuration data to a system during prototyping or to program data into the system during production.

1.1. Intel FPGA Download Cable Revision

Table 1. Intel FPGA Download Cable Revision

| Revision | Indicator | Description | RoHS Compliant |
|----------|--|--|----------------|
| Rev. A | Ribbon cable. No revision marking on the casing. | 10-pin female connector that is connected to the Intel FPGA Download Cable through a ribbon cable. | No |
| Rev. B | "Rev. B" on the casing. | 10-pin female connector that is connected to the Intel FPGA Download Cable through a flexible PCB cable. | No |
| Rev. C | "Rev. C" on the casing. | 10-pin female connector that is connected to the Intel FPGA Download Cable through a flexible PCB cable. | Yes |

1.2. Supported Devices and Host Systems

You can use the Intel FPGA Download Cable with supported Intel FPGAs, serial configuration devices, and host systems.

Table 2. Supported Devices and Host Systems

| FPGA | Serial Configuration Device | Host System |
|--|--|------------------|
| Intel Agilex® series Intel Stratix® series Intel Arria® series Intel Cyclone® series Intel MAX® series | EPCS devices EPCQ devices EPCQ-L devices | Windows Linux |

2. Specifications for Intel FPGA Download Cable

The Intel FPGA Download Cable has a universal USB connector that plugs into the PC USB port, and a female connector that plugs into a male header on the device board. This section shows the hardware components, their dimensions, and lists the pins, operating conditions and power requirements.

2.1. Block Diagram and Dimension

Figure 1. Block Diagram of the Intel FPGA Download Cable

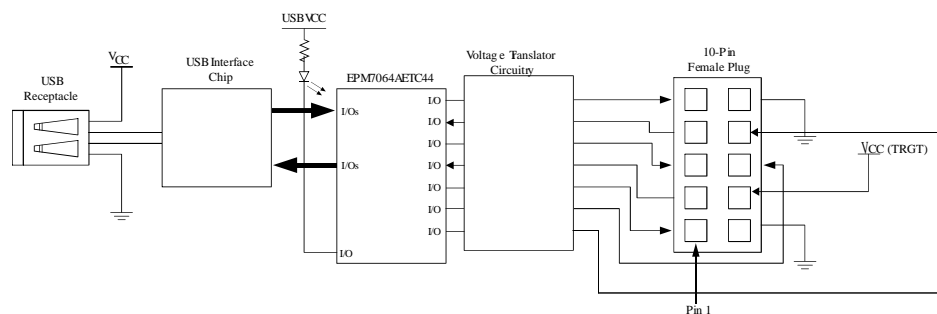
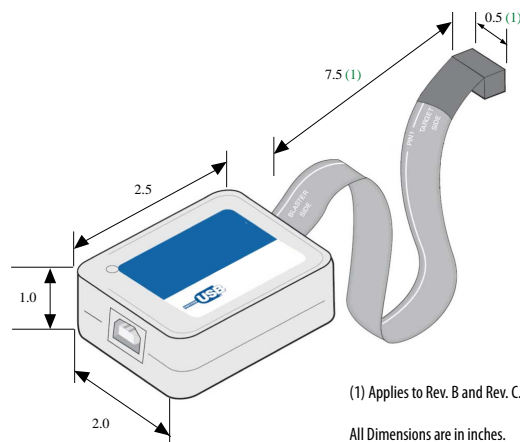


Figure 2. Dimension of the Intel FPGA Download Cable

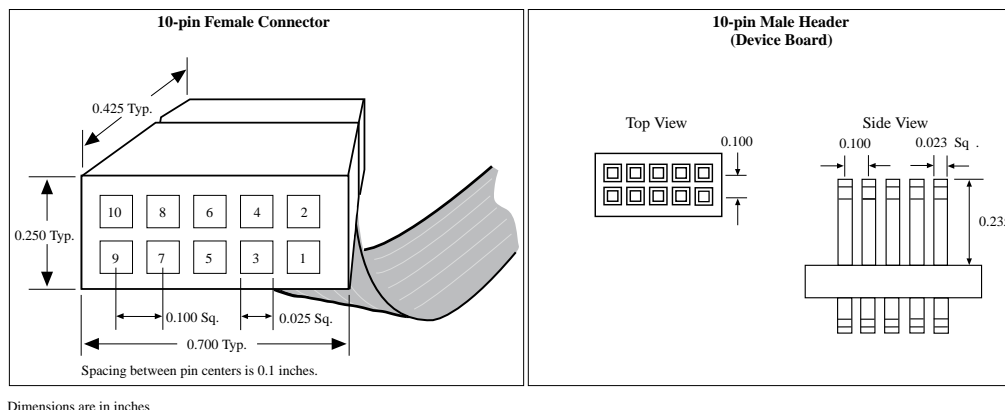


2.2. Cable-to-Board Connection

The Intel FPGA Download Cable has a 10-pin female connector, which plugs into a 10-pin male header on the device board. The male header consists of two rows of five pins, which are connected to the programming or configuration pins of the device.

A 10-pin surface mount header can be used for the JTAG, AS, or PS download cable. However, Intel recommends using a through-hole connector because of the repeated insertion and removal force needed.

Figure 3. Connectors and Dimensions



2.3. Pin Description

The following table lists the pins of the Intel FPGA Download Cable female plug and describes their functions in the JTAG, active serial and passive serial modes.

Table 3. Signal Names of the Intel FPGA Download Cable Female Plug

| Pin | AS Mode | | PS Mode | | JTAG Mode | |
|-----|------------------------|--|------------------------|--|------------------------|--|
| | Signal Name | Description | Signal Name | Description | Signal Name | Description |
| 1 | DCLK | Clock signal. | DCLK | Clock signal. | TCK | Clock signal. |
| 2 | GND | Signal ground. | GND | Signal ground. | GND | Signal ground. |
| 3 | CONF_DONE | Configuration done. | CONF_DONE | Configuration done. | TDO | Data from device. |
| 4 | V _{CC} (TRGT) | Target power supplied by the device board. | V _{CC} (TRGT) | Target power supplied by the device board. | V _{CC} (TRGT) | Target power supplied by the device board. |
| 5 | nCONFIG | Configuration control. | nCONFIG | Configuration control. | TMS | JTAG state machine control. |
| 6 | nCE | Cyclone chip enable. | — | — | — | — |
| 7 | DATAOUT | Active serial data out. | nSTATUS | Configuration status. | — | — |
| 8 | nCS | Serial configuration device chip select. | — | — | — | — |
| 9 | ASDI | Active serial data in. | DATA0 | Data to device. | TDI | Data to device. |
| 10 | GND | Signal ground. | GND | Signal ground. | GND | Signal ground. |

2.4. Operating Conditions

Use the provided maximum ratings, recommended operating conditions and DC operating conditions to ensure the correct usage of the Intel FPGA Download Cable.

Table 4. Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---|-------------------------|-------|------|------|
| $V_{CC(TRGT)}$ | Target supply voltage | With respect to ground | -0.3 | 5.5 | V |
| $V_{CC(USB)}$ | USB supply voltage | With respect to ground | -0.5 | 6.0 | V |
| I_I | Input current | TDO or dataout | -10.0 | 10.0 | mA |
| I_O | Output current for Rev. A or Rev. B cable | TCK, TMS, TDI, nCS, nCE | -20.0 | 20.0 | mA |
| | Output current for Rev. C cable | | -50.0 | 50.0 | mA |

Table 5. Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|--|------------|-------|-------|------|
| $V_{CC(TRGT)}$ | Target supply voltage, 5.0-V operation | — | 4.75 | 5.25 | V |
| | Target supply voltage, 3.3-V operation | — | 3.0 | 3.6 | V |
| | Target supply voltage, 2.5-V operation | — | 2.375 | 2.625 | V |
| | Target supply voltage, 1.8-V operation | — | 1.71 | 1.89 | V |
| | Target supply voltage, 1.5-V operation | — | 1.43 | 1.57 | V |

Table 6. DC Operating Conditions for Intel FPGA Download Cable Rev. A and B

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|---------------------------------|---|----------------------|-------|------|
| V_{IH} | High-level input voltage | — | $V_{CC(TRGT)} - 0.2$ | — | V |
| V_{IL} | Low-level input voltage | — | — | 0.15 | V |
| V_{OH} | 5.0-V high-level output voltage | $V_{CC(TRGT)} = 4.5\text{ V}, I_{OH} = 1\text{ mA}$ | 4.4 | — | V |
| | 3.3-V high-level output voltage | $V_{CC(TRGT)} = 3.0\text{ V}, I_{OH} = 1\text{ mA}$ | 2.9 | — | V |
| | 2.5-V high-level output voltage | $V_{CC(TRGT)} = 2.375\text{ V}, I_{OH} = 1\text{ mA}$ | 2.275 | — | V |
| | 1.8-V high-level output voltage | $V_{CC(TRGT)} = 1.71\text{ V}, I_{OH} = 1\text{ mA}$ | 1.61 | — | V |
| | 1.5-V high-level output voltage | $V_{CC(TRGT)} = 1.43\text{ V}, I_{OH} = 1\text{ mA}$ | 1.33 | — | V |
| V_{OL} | 5.0-V low-level output voltage | $V_{CC(TRGT)} = 5.5\text{ V}, I_{OL} = 1\text{ mA}$ | — | 0.125 | V |

continued...

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|--------------------------------|---|-----|-------|---------------|
| | 3.3-V low-level output voltage | $V_{CC(TRGT)} = 3.6 \text{ V}, I_{OL} = 1 \text{ mA}$ | — | 0.125 | V |
| | 2.5-V low-level output voltage | $V_{CC(TRGT)} = 2.625 \text{ V}, I_{OL} = 1 \text{ mA}$ | — | 0.125 | V |
| | 1.8-V low-level output voltage | $V_{CC(TRGT)} = 1.89 \text{ V}, I_{OL} = 1 \text{ mA}$ | — | 0.125 | V |
| | 1.5-V low-level output voltage | $V_{CC(TRGT)} = 1.57 \text{ V}, I_{OL} = 1 \text{ mA}$ | — | 0.125 | V |
| $I_{CC(TRGT)}$ | Operating current (No Load) | Typical $I_{CC(TRGT)} = 16 \text{ uA}$ | — | 100 | μA |

Table 7. DC Operating Conditions for Intel FPGA Download Cable Rev. C

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---------------------------------|--|----------------|-----|---------------|
| V_{IH} | High-level input voltage | $V_{CC(TRGT)} \geq 2.0 \text{ V}$ | 2.0 | — | V |
| | | $V_{CC(TRGT)} < 2.0 \text{ V}$ | $V_{CC(TRGT)}$ | — | V |
| V_{IL} | Low-level input voltage | $V_{CC(TRGT)} \geq 2.0 \text{ V}$ | — | 0.8 | V |
| | | $V_{CC(TRGT)} < 2.0 \text{ V}$ | — | 0 | V |
| V_{OH} | 5.0-V high-level output voltage | $V_{CC(TRGT)} = 4.5 \text{ V}, I_{OH} = -10 \text{ mA}$ | 3.8 | — | V |
| | 3.3-V high-level output voltage | $V_{CC(TRGT)} = 3.0 \text{ V}, I_{OH} = -8 \text{ mA}$ | 2.3 | — | V |
| | 2.5-V high-level output voltage | $V_{CC(TRGT)} = 2.375 \text{ V}, I_{OH} = -6 \text{ mA}$ | 1.8 | — | V |
| | 1.8-V high-level output voltage | $V_{CC(TRGT)} = 1.71 \text{ V}, I_{OH} = -4 \text{ mA}$ | 1.2 | — | V |
| V_{OL} | 5.0-V high-level output voltage | $V_{CC(TRGT)} = 5.5 \text{ V}, I_{OL} = 10 \text{ mA}$ | — | 0.8 | V |
| | 3.3-V high-level output voltage | $V_{CC(TRGT)} = 3.6 \text{ V}, I_{OL} = 8 \text{ mA}$ | — | 0.7 | V |
| | 2.5-V high-level output voltage | $V_{CC(TRGT)} = 2.625 \text{ V}, I_{OL} = 6 \text{ mA}$ | — | 0.6 | V |
| | 1.8-V high-level output voltage | $V_{CC(TRGT)} = 1.89 \text{ V}, I_{OL} = 4 \text{ mA}$ | — | 0.5 | V |
| $I_{CC(TRGT)}$ | Operating current (No Load) | Typical $I_{CC(TRGT)} = 16 \text{ uA}$ | — | 100 | μA |

2.5. Power Requirements

The Intel FPGA Download Cable $V_{CC(TRGT)}$ pin must be connected to a specific voltage for the device being programmed. Connect pull-up resistors to the same power supply as the Intel FPGA Download Cable $V_{CC(TRGT)}$.

Table 8. $V_{CC(TRGT)}$ Power Requirements

| Device Family | Voltage Required |
|---|---|
| FPGAs | |
| Arria GX | As specified by V_{CCSEL} |
| Arria II GX | As specified by V_{CCPD} or V_{CCIO} of Bank 8C |
| Arria V | As specified by V_{CCPD} |
| Intel Arria 10 | As specified by V_{CCPGM} or V_{CCIO} |
| Cyclone III | As specified by V_{CCA} or V_{CCIO} |
| Cyclone IV | As specified by V_{CCA} or V_{CCIO} |
| Cyclone V | As specified by V_{CCPGM} or V_{CCPD} |
| Intel Cyclone 10 GX | As specified by V_{CCPGM} or V_{CCIO} |
| Intel Cyclone 10 LP | As specified by V_{CCA} or V_{CCIO} |
| Intel MAX 10 | As specified by V_{CCIO} |
| Stratix II, Stratix II GX, and Stratix GX | As specified by V_{CCSEL} |
| Stratix V, Stratix IV, and Stratix III | As specified by V_{CCPGM} or V_{CCPD} |
| Intel Stratix 10 | As specified by V_{CCIO_SDM} |
| Intel Agilex 7 | As specified by V_{CCIO_SDM} |
| Configuration Devices | |
| EPCS | 3.3 V |
| EPCQ | 3.3 V |
| EPCQ-L | 1.8 V |

2.6. RoHS Compliance

Table 9. Hazardous Substances and Concentration

A value of 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold as specified by the SJ/T11363-2006 standard.

| Part Name | Lead (Pb) | Cadmium (Cd) | Hexavalent Chromium (Cr6+) | Mercury (Hg) | Polybrominated Biphenyls (PBB) | Polybrominated Diphenyl Ethers (PBB) |
|-------------------------|-----------|--------------|----------------------------|--------------|--------------------------------|--------------------------------------|
| Electronic components | 0 | 0 | 0 | 0 | 0 | 0 |
| Populated circuit board | 0 | 0 | 0 | 0 | 0 | 0 |
| Manufacturing process | 0 | 0 | 0 | 0 | 0 | 0 |
| Packing | 0 | 0 | 0 | 0 | 0 | 0 |



3. Using the Intel FPGA Download Cable

To start using the Intel FPGA Download Cable, you must install the drivers on your system and set up the hardware in the Intel Quartus® Prime software. Intel recommends that you use the latest version of the Intel Quartus Prime software.

To program or configure the device, connect the host system to the device board using the Intel FPGA Download Cable and initiate the programming or configuration using the Intel Quartus Prime Programmer. You can also use the cable with the Intel Quartus Prime Signal Tap Logic Analyzer for logic analysis.

3.1. Installing the Intel FPGA Download Cable Driver on Windows

1. Locate the Intel FPGA Download Cable driver in `\<Quartus Prime system directory>\drivers\usb-blaster`.
If the driver is not in your directory, download the driver from www.altera.com/support/software/drivers.
2. Connect the Intel FPGA Download Cable to your PC.
3. Open **Device Manager**. In the **Other devices** tab, select and right click **USB-Blaster**. Then, click **Update Driver Software**.
4. Click **Browse**. Browse to `\<Quartus Prime system directory>\drivers\usb-blaster` and click **Next**.
The Windows security warning is displayed.
5. Click **Install** to begin installing the driver.
6. Click **Finish** when the driver is installed.
7. Restart your system.

Related Information

[Cable and Adapter Drivers Information](#)

3.2. Installing the Intel FPGA Download Cable Driver on Linux

The Intel Quartus Prime software uses the USB drivers (usbfs) provided by Red Hat Linux to access the Intel FPGA Download Cable. You need system administration (root) privileges to configure the drivers. You must also change the permission on the ports before using the Intel FPGA Download Cable to program devices.

Related Information

[Cable and Adapter Drivers Information](#)

3.2.1. Installing on Red Hat Enterprise 4 or Earlier Versions

1. Add the following lines to the `/etc/hotplug/usb.usermap` file:

```
#
#Intel FPGA Download Cable
#
usbblaster 0x03 0x09fb 0x6001 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0
usbblaster 0x03 0x09fb 0x6002 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0
usbblaster 0x03 0x09fb 0x6003 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0 0x0
```

2. Create a file named `/etc/hotplug/usb/usbblaster` and write:

```
#!/bin/sh
#Intel FPGA Download Cable hotplug script
# Allow any user to access the cable
chmod 666 $DEVICE
```

3. Make the file executable.

Now you can set up the programming hardware in the Intel Quartus Prime software.

3.2.2. Installing on Red Hat Enterprise Linux 6

1. Create a file named `/etc/udev/rules.d/51-usbblaster.rules`
2. In the file, add the following lines, depending on the type of download cable.

Ensure that all the code is in one line.

— Intel FPGA Download Cable:

```
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6001",
MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6002",
MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6003",
MODE="0666"
```

— Intel FPGA Download Cable II:

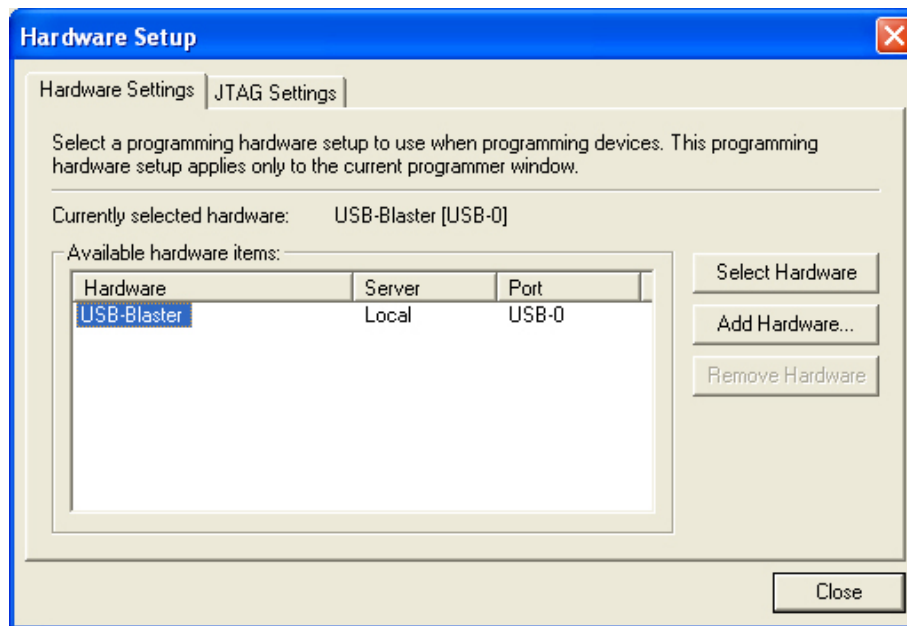
```
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6010",
MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6810",
MODE="0666"
```

Now you can set up the programming hardware in the Intel Quartus Prime software.

3.3. Setting up the Intel FPGA Download Cable Hardware in the Intel Quartus Prime Software

1. Launch the Intel Quartus Prime software.
2. Click **Tools > Programmer**.
3. Click **Hardware Setup**.

Figure 4. Hardware Setup Dialog Box



The **Hardware Settings** tab of the **Hardware Setup** dialog box is displayed.

4. From the **Currently selected hardware** drop-down list, select **USB-Blaster [USB-0]**.
5. Click **Close** to close the **Hardware Setup** dialog box.
6. In the **Programmer** window, select the desired programming mode from the **Mode** drop-down list.

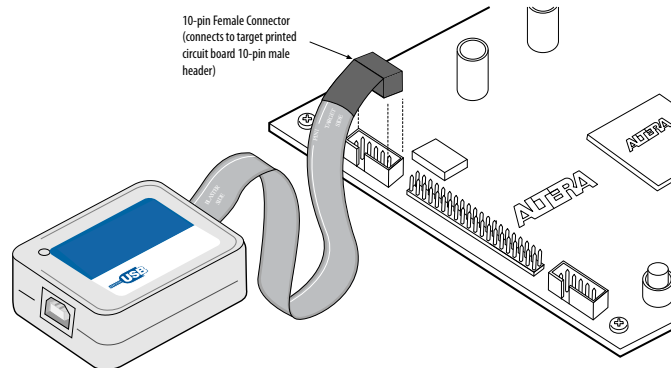
Table 10. Programming Modes

| Mode | Description |
|--------------------------------|---|
| Joint Test Action Group (JTAG) | Programs or configures all supported Intel devices except EPCS, EPCQ, and EPCQ-L devices. |
| In-Socket Programming | USB-Blaster does not support this programming mode. |
| Passive Serial | Configures all supported Intel devices except EPCS, EPCQ, and EPCQ-L devices. |
| Active Serial Programming | Programs a single EPCS, EPCQ, or EPCQ-L device. |

3.4. Connecting the Intel FPGA Download Cable to the Board

1. Disconnect the power cable from the device board.
2. Connect the Intel FPGA Download Cable to your PC.
3. Plug the Intel FPGA Download Cable into the 10-pin header on the device board.

Figure 5. Connection to the Device Board



4. Connect the power cable to the device board.
The **Found New Hardware** wizard may open and prompt you to install a new hardware driver. Close the wizard and follow the steps provided in subsequent sections to install the hardware driver.
5. To disconnect the Intel FPGA Download Cable from the device board, follow these steps to ensure that the cable is not damaged.
 - a. Remove power from the device board.
 - b. Unplug the Intel FPGA Download Cable from the board.
 - c. Unplug the Intel FPGA Download Cable from your PC.



A. Additional Information

A.1. Windows Troubleshooting Procedure for Intel FPGA Download Cable

In the Windows version of the Intel Quartus Prime software, you may encounter that the Intel FPGA Download Cable may occasionally not work well; although you may not observe any problems in the physical connections. In many cases, it is due to:

- Incorrect Windows settings or some unknown problem with the Intel FPGA Download Cable driver
- The version of JTAG related software like **Jtagconfig** or **Jtagserver** not matching the version of Intel Quartus Prime software
- The version of the Intel FPGA Download Cable driver is old, not proper, or corrupted

The troubleshooting steps are listed in the following sections.

A.1.1. Jtagconfig version setting (Intel Quartus Prime software root directory setting)

1. Open a command prompt of Windows OS
2. Execute the following command: `Jtagconfig -v`

Example message:

```
Version 18.1.1 Build 646 04/11/2019 SJ Standard Edition
```

3. If the version in the message does not match the Intel Quartus Prime version that you use, you must modify the user system variables for your Windows account or the system variables.

A.1.1.1. Automatic Setting

1. Go to <Quartus Prime software install folder>\quartus\bin64 for Intel Quartus Prime. Go to <Quartus Prime Programmer install folder>\qprogrammer\bin64 or <Quartus Prime Programmer install directory>\qprogrammer\quartus\bin64 for Intel Quartus Prime Programmer tool.

2. Execute the following command:

```
qreg.exe --force -jtag -setqdir
```

3. Intel recommends you verify the environment variables using the manual setting procedure explained in the section below.

A.1.1.2. Manual Setting

1. Open Environment Variables window of Windows OS
Windows Settings > Type "Environment" into the search area > Choose Edit the system environment variables
2. Check if Path variable has %QUARTUS_ROOTDIR%\bin64 in System variables or User variables for your account. If not present, add %QUARTUS_ROOTDIR%\bin64
3. Check if QUARTUS_ROOTDIR variable is in a right path that **bin64** folder locates
Directory for Intel Quartus Prime: <Quartus Prime software install folder>\quartus
Directory for Intel Quartus Prime Programmer tool: < Quartus Prime Programmer install folder>\qprogrammer or < Quartus Prime Programmer install directory>\qprogrammer\quartus
4. If you notice these variables in both System variables or User variables for your account, Intel recommends that one of them should be deleted.
5. Restart your computer and check the version of **jtagconfig** using step 1 and 2

A.1.2. Jtagserver Setting

1. Open Windows OS command prompt
2. Execute the following command: `jtagconfig --serverinfo`

Example message is

```
Installed JTAG server is '<Quartus Prime install folder>\quartus
\bin64\jtagserver.exe'
Service manager reports server is running
Server reports path: <Quartus Prime install folder>\quartus
\bin64\jtagserver.exe
Server reports version: Version 18.1.1 Build 646 04/11/2019 SJ Standard
Edition
Remote clients are disabled (no password)
```

If the installed JTAG server doesn't match the version of Intel Quartus Prime software you use, install the same version of JTAG server as the Intel Quartus Prime software.

3. Set the environment variables correctly following the steps described in the **jtagconfig** version setting in the sections above.
4. Execute the following command

```
Jtagserver -uninstall
Jtagserver -install
```

5. Restart your computer

A.1.3. Install/Reinstall the Intel FPGA Download Cable driver

1. Connect your Intel FPGA Download Cable or Intel FPGA Download Cable II
2. Open **Device Manager** window of Windows OS

Windows Settings > Type "Device Manager" into the search area
> Choose Device Manager

3. Find Intel FPGA Download Cable II under JTAG cables or Intel FPGA Download Cable under Universal Serial Bus controllers
4. Choose Intel FPGA Download Cable or Intel FPGA Download Cable II
5. Right click and choose **Uninstall device** from context menu
6. Enable **Delete the driver software for this device** and click **Uninstall**
7. If you see another Intel FPGA Download Cable or Intel FPGA Download Cable II, uninstall it too
8. Reinstall the drivers following the steps in section [Installing the Intel FPGA Download Cable Driver on Windows](#) on page 9

A.2. Troubleshooting Procedure for Error when scanning hardware - No Devices

You might see this error when connecting multiple download cables to your computer and executing `jtagconfig` command.

```
Error when scanning hardware - No devices
```

It takes a certain finite amount of time for your computer to finish the USB device enumeration after connecting USB devices. The more USB devices are connected, the more time is required for the USB device enumeration.

The above error occurs when `jtagconfig` command is executed before your computer finishes the USB device enumeration to recognize all download cables connected. The error seems to occur only when `jtagconfig` command is executed right after multiple download cables are connected

Troubleshooting Procedure

You need to wait for a while until your computer finishes the USB device enumeration after your Intel FPGA Download Cable is connected. You can use Device Manager on Windows or `lsusb` command on Linux to check if your Intel FPGA Download Cable is recognized on your computer.

For Windows: Open **Device Manager** and check if Intel FPGA Download Cable II (JTAG interface) under JTAG cables or Intel FPGA Download Cable under Universal Serial Bus controller is listed.

For Linux: Open a command shell, type `lsusb`, and check if the device with ID of `09fb:6001`, `09fb:6002`, `09fb:6003`, `09fb:6010`, or `09fb:6810` is listed.

B. Document Revision History for the Intel FPGA Download Cable User Guide

| Document Version | Changes |
|------------------|--|
| 2024.01.16 | <ul style="list-style-type: none"> Updated Table: <i>Supported Devices and Host Systems</i> to include Intel Agilex series FPGAs support. Updated Table: $V_{CC(TrGT)}$ <i>Power Requirements</i> to include $V_{CC(TrGT)}$ power requirements for Intel Cyclone 10 GX, Intel Cyclone 10 LP, Intel Stratix 10, and Intel Agilex 7 device families. |
| 2020.03.11 | Updated Intel FPGA Download Cable Block Diagram in Block Diagram and Dimension on page 4 |
| 2019.10.23 | Added the following sections: <ul style="list-style-type: none"> Windows Troubleshooting Procedure for Intel FPGA Download Cable on page 13 Troubleshooting Procedure for Error when scanning hardware - No Devices on page 15 |
| 2019.06.11 | Updated <i>Block Diagram of the Intel FPGA Download Cable</i> to show correct position of Pin 1 in the section Block Diagram and Dimension on page 4 |
| 2019.04.12 | <ul style="list-style-type: none"> Corrected the unit in the <i>Recommended Operating Conditions</i> and <i>DC Operating Conditions for Intel FPGA Download Cable Rev. C</i> tables. Added how to install USB drivers for Red Hat Enterprise systems. |

| Date | Version | Changes |
|--------------|------------|---|
| October 2016 | 2016.10.31 | <ul style="list-style-type: none"> Changed instances of Quartus II to Quartus Prime. Changed instances of USB-Blaster Download cable II to Intel FPGA Download Cable. Updated document template. |
| August 2015 | 2015.08.20 | <ul style="list-style-type: none"> Removed <code>PROC_RST</code> signal which is not supported in USB-Blaster. |
| May 2015 | 2015.05.04 | <ul style="list-style-type: none"> Updated the document organization. Added new devices in the following sections: <i>Supported Devices and Host Systems</i> and <i>Power Requirements</i>. Updated the procedure on driver installation for Windows. Revised the pin width of the female plug. |
| April 2009 | 2.5 | <ul style="list-style-type: none"> Updated "Supported Devices" section. Updated "Software Requirements". Deleted handnote in "Installing the USB-Blaster Driver on Windows Vista Systems". Updated Table 2-1. Added a handnote in "Circuit Board Header Connection". Updated Table 2-5. |
| April 2008 | 2.4 | <ul style="list-style-type: none"> Added "Statement of China-RoHS Compliance". Added Table 2-8. Added "Installing the USB-Blaster Driver on Windows Vista Systems". |
| continued... | | |

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| Date | Version | Changes |
|---------------|---------|--|
| May 2007 | 2.3 | <ul style="list-style-type: none"> Updated "Introduction". Added warning note about USB-Blaster cable in "Hardware Setup" section. Added information on Linux setup in "Installing the USB-Blaster Driver on Linux" section. Added footnote note on driver information just before the "Setting Up the USB-Blaster Hardware in the Quartus II Software" section. Updated USB-Blaster installation procedure for QII 6.1 (32-bit or 64-bit) in "Installing the USB-Blaster Driver on Windows 2000 and Windows XP Systems" section. |
| March 2007 | 2.2 | <ul style="list-style-type: none"> Update to "Installing the USB-Blaster Driver on Windows 2000 and Windows XP Systems" section. |
| July 2006 | 2.1 | Minor update to Chapter 2, USB-Blaster Specifications. |
| June 2006 | 2.0 | <ul style="list-style-type: none"> Updated Figure 2-1, Table 2-1, and Table 2-7. Added Table 2-6. |
| December 2004 | 1.2 | Update to conditions in Table 2-2. |
| November 2004 | 1.1 | Minor update. |
| July 2004 | 1.0 | Initial release. |