Cyclone® 10 LP Device Schematic Review Worksheet

This document is intended to help you review your schematic and compare the pin usage against the *Intel Cyclone 10 LP Device Family Pin Connection Guidelines (PDF)* version 2017.06.02 and other referenced literature for this device family. The technical content is divided into focus areas such as FPGA power supplies, configuration, and FPGA I/O.

Within each focus area, there is a table that contains the voltage or pin name for all of the dedicated and dual purpose pins for the device family. In some cases, the device density and package combination may not include some of the pins shown in this worksheet, you should cross reference with the pin-out file for your specific device. Links to the device pin-out files are provided at the top of each section.

Before you begin using this worksheet to review your schematic and commit to board layout, Intel highly recommends:

1) Review the latest version of the Cyclone 10 LP Device Errata Sheet (no errata exists at the time this document was published) and the Knowledge Database for Cyclone 10 LP Device known issues(no such file at the time this document was published).

2) Compile your design in the Quartus® Prime software to completion.

For example, there are many I/O related placement restrictions and VCCIO requirements for the I/O standards used in the device. If you do not have a complete project, then at a minimum a top level project should be used with all I/O pins defined, placed, and apply all of the configurable options that you plan to use. All I/O related megafunctions should also be included in the minimal project, including, but not limited to, external memory interfaces, PLLs, altlvds, altgx, and altddio. The I/O Analysis tool in the Pin Planner can then be used on the minimal project to validate the pinout in the Quartus Prime software to assure there are no conflicts with the device rules and guidelines.

When using the I/O Analysis tool you must ensure there are no errors with your pinout. Additionally, you should check all warning and critical warning messages to evaluate their impact on your design. You can right click your mouse over any warning or critical warning message and select "Help". This will bring open a new Help window with further information on the cause of the warning, and the action that is required.

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For example, the following warning is generated when a PLL is driven by a global network where the source is a valid dedicated clock input pin, but the pin is not one dedicated to the particular PLL:

Warning: PLL "<PLL Instance Name>" input clock inclk[0] is not fully compensated and may have reduced jitter performance because it is fed by a non-dedicated input
        Info: Input port INCLK[0] of node "<PLL Instance Name>" is driven by clock~clkctrl which is OUTCLK output port of Clock Control Block type node clock~clkctrl

The help file provides the following:

CAUSE: The specified PLL's input clock is not driven by a dedicated input pin. As a result, the input clock delay will not be fully compensated by the PLL. Additionally, jitter performance depends on the switching rate of other design elements. This can also occur if a global signal assignment is applied to the clock input pin, which forces the clock to use the non-dedicated global clock network.

ACTION: If you want compensation of the specified input clock or better jitter performance, connect the input clock only to an input pin, or assign the input pin only to a dedicated input clock location for the PLL. If you do not want compensation of the specified input clock, then set the PLL to No Compensation mode.

When assigning the input pin to the proper dedicated clock pin location, refer to Clock Networks and PLLs in Cyclone 10 LP Devices (PDF) for the proper port mapping of dedicated clock input pins to PLLs.

There are many reports available for use after a successful compilation or I/O analysis. For example, you can use the "All Package Pins" and "I/O Bank Usage" reports within the Compilation – Fitter – Resource Section to see all of the I/O standards and I/O configurable options that are assigned to all of the pins in your design, as well as view the required VCCIO for each I/O bank. These reports must match your schematic pin connections.

The review table has the following heading:

Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues

The first column (Plane/Signal) lists the FPGA voltage or signal pin name. You should only edit this column to remove dedicated or dual purpose pin names that are not available for your device density and package option.

The second column (Schematic Name) is for you to enter your schematic name(s) for the signal(s) or plane connected to the FPGA pin(s).

The third column (Connection Guidelines) should be considered "read only" as this contains Intel's recommended connection guidelines for the voltage plane or signal.

The fourth column (Comments/Issues) is an area provided as a "notepad" for you to comment on any deviations from the connection guidelines, and to verify guidelines are met. In many cases there are notes that provide further information and detail that compliment the connection guidelines.

Here is an example of how the worksheet can be used:

Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
<Plane / Signal name provided by Intel> VCCINT	*<user entered text>* +1.2V	*<Device Specific Guidelines provided by Intel>*	*<user entered text>* Connected to +1.2V plane, no isolation is necessary. Missing low and medium range decoupling, check PDN. See Notes (1-1) (1-2) (1-3) (1-6) (1-7).

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Section I: Power

Cyclone 10 LP Recommended Reference Literature/Tool List

Cyclone 10 LP Device Pin-Out Files

Cyclone 10 LP Device Family Pin Connection Guidelines (PDF)

Cyclone 10 LP Early Power Estimator

Power Delivery Network (PDN) Tools/Guidelines

PowerPlay Power Analyzer Support Resources

AN 800: Cyclone 10 LP Device Design Guidelines (PDF)

AN 583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs (PDF)

AN 597: Getting Started Flow for Board Designs (PDF)

Intel Board Design Resource Center (General board design guidelines, PDN design, isolation, tools, and more)

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / **Issues**
VCCINT		These are internal logic array voltage supply pins. In Cyclone 10 LP devices, all VCCINT pins must be connected to the same supply voltage and physical plane either 1.0V or 1.2V. Cyclone 10 LP devices with VCCINT 1.0V, and Cyclone 10 LP devices with VCCINT 1.2V have different ordering codes (note (1-3)). VCCINT can be shared with VCCD_PLL with proper isolation filters. Verify your solution using the Power Distribution Network (PDN) tool. Decoupling depends on the design decoupling requirements of the specific board.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-6) (1-7).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / <u>Issues</u>
VCCD_PLL[1..4]		Digital power for PLLs [1..4]. These pins must be connected to power even if the PLLs are not used. You are required to connect these pins to either 1.0V(if VCCINT 1.0V) or 1.2V(if VCCINT 1.2V), even if the PLL is not used. Cyclone 10 LP devices with VCCINT 1.0V, and Cyclone 10 LP devices with VCCINT 1.2V have different ordering codes (note (1-3)). With a proper isolation filter VCCD_PLL can be sourced from the same regulator as VCCINT. Verify your solution using the Power Distribution Network (PDN) tool. Use an isolated switching power supply with a +/- 3% maximum voltage ripple. Decoupling depends on the design decoupling requirements of the specific board.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-5) (1-6) (1-7).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / <u>**Issues**</u>
VCCA[1..4]		Analog power for PLLs [1..4]. All VCCA pins must be powered and must be powered up and powered down at the same time, even if not all the PLLs are used. Connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear or switching power supply with +/- 3% maximum voltage ripple. It is advised to keep this pin isolated from other VCC pins for better jitter performance. Decoupling depends on the design decoupling requirements of the specific board.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-4) (1-5) (1-6) (1-7).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / **Issues**
VCCIO[1..8]		These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. Connect these pins to 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V supplies, depending on the I/O standard assigned to the I/O bank. Decoupling depends on the design decoupling requirements of the specific board.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-6) (1-7).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / <u>Issues</u>
VREFB[1..8]N[0..2]		Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins. The pin capacitance is higher on VREF pins than regular I/O pins, thus you should avoid placing fast edge rate signals such as clocks on these pins, and avoid using these pins in buses since the I/O timing will not be consistent with the rest of the bus. If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Ensure the reserve unused pin option used in Quartus Prime software for these pins do not conflict with the board connection. Decoupling depends on the design decoupling requirements of the specific board.	Verify Guidelines have been met or list required actions for compliance. See Note (1-1).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / **Issues**
GND		Device ground pins. All GND pins must be connected to the board GND plane.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-6).
GNDA[1..4]		Ground pins for PLL[1..4] and other analog circuits in the device. The designer can consider connecting the GNDA pins to the GND plane without isolating the analog ground plane on the board provided the digital GND plane(s) are stable, quiet, and with no ground bounce effect.	Verify Guidelines have been met or list required actions for compliance. See Notes (1-1) (1-2) (1-6).

Notes:

1-1. Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the operating frequency of the circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage ripple requirements of the plane. The power plane should then be decoupled using the appropriate number of capacitors to achieve this impedance.

On-board capacitors do not decouple higher than approximately 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis, Intel's Power Distribution Network (PDN) Tool serves as an excellent decoupling analysis tool.

1-2. This worksheet does not include power estimation for the different power supplies provided. Ensure each power supply is adequate for the device current requirements. Refer to Intel's Early Power Estimation Tools and PowerPlay Power Analyzer Support Resources for further guidance.

Use Intel's Early Power Estimation Tools to ensure the junction temperature of the device is within operating specifications based on your design activity.

1-3. There are two variants of Cyclone 10 LP devices; one powered with a core voltage VCCINT of 1.0V, and the other powered with a core voltage VCCINT of 1.2V. Each variant has different ordering codes.

1-4. These supplies may share power planes across multiple Cyclone 10 LP devices.

1-5. Use separate power islands for the VCCA pins and the VCCD_PLL pins. The PLL power supplies may originate from other planes on the board, but must be isolated using ferrite beads or other equivalent methods. If using ferrite beads, choose 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply is connected to (VCCA or VCCD_PLL), and high impedance at 100MHz. Refer to AN583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs (PDF) for further guidance.

1-6. Intel highly recommends using an independent PCB via for each independent power or ground ball on the package. Sharing power or ground pin vias on the PCB could lead to noise coupling into the device and result in reduced jitter performance. Please refer to Intel's Power Distribution Network (PDN) Tool to analyze the effects of circuit board geometries on the effectiveness of the power distribution network.

1-7. Refer to the Intel Cyclone 10 LP Device Family Pin Connection Guidelines for examples on power supply sharing guidelines.

1-8. Figure 1 in the Intel Cyclone 10 LP Device Family Pin Connection Guidelines illustrates power supply sharing guidelines for the Cyclone 10 LP devices.
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Additional Comments:

Section II: Configuration

Cyclone 10 LP Recommended Reference Literature/Tool List

Cyclone 10 LP Device Pin-Out Files

Cyclone 10 LP Device Family Pin Connection Guidelines (PDF)

Configuration, and Remote System Upgrades in Cyclone 10 LP Devices (PDF)

Intel FPGA USB Download Cable User Guide (PDF)

Intel FPGA Download Cable II User Guide (PDF)

ByteBlaster II Download Cable User Guide (PDF)

AN 597: Getting Started Flow for Board Designs (PDF)

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Configuration Scheme	Configuration Voltage	

Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
MSEL[0:3]		Configuration input pins that set the configuration scheme. Some of the smaller Cyclone 10 LP devices or package options do not support AS configuration with fast delay (3.0V/2.5V) and do not have the MSEL[3] pin. These pins are internally connected through a 9-KΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND either directly or through 0-Ω resistors. Refer to the "configuration and Remote System Upgrades in Cyclone 10 LP Devices" chapter in the Cyclone 10 LP Handbook. If only JTAG configuration is used, connect these pins to GND.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
nCE		Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.	Verify Guidelines have been met or list required actions for compliance.
nCONFIG		Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If you are using PS configuration scheme with a download cable, connect this pin through a 10-KΩ resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-KΩ resistor to VCCIO.	Verify Guidelines have been met or list required actions for compliance.
CONF_DONE		This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-KΩ pull-up resistor. When using a Passive configuration scheme this pin should also be monitored by the configuration device or controller.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
nCEO		When not using this pin, you can leave it unconnected. During multi-device configuration, this pin feeds the nCE pin of a subsequent device. In this case, tie the 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. During single device configuration, this pin can be used as a regular I/O. This pin is not available for regular I/O usage in multi-device configuration mode, see rd04132011_29.	Verify Guidelines have been met or list required actions for compliance.
nSTATUS		This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-KΩ pull-up resistor. When using a Passive configuration scheme this pin should also be monitored by the configuration device or controller.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
TCK		Connect this pin to a 1-KΩ pull-down resistor to GND. Treat this signal like a clock and follow typical clock routing guidelines. To disable the JTAG circuity connect TCK to GND.	Verify Guidelines have been met or list required actions for compliance.
TMS		Connect this pin to a 1-KΩ to 10-KΩ pull-up resistor to VCCA. To disable the JTAG circuitry, connect TMS to VCCA.	Verify Guidelines have been met or list required actions for compliance. See Notes (2-2) (2-3).
TDI		Connect this pin to a 1-KΩ to 10-KΩ pull-up resistor to VCCA. To disable the JTAG circuitry, connect TDI to VCCA.	Verify Guidelines have been met or list required actions for compliance. See Notes (2-2) (2-3).
TDO		If the TDO pin is not used, leave this pin unconnected.	Verify Guidelines have been met or list required actions for compliance.

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Optional Dual Purpose Pins			
Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
nCSO		This pin functions as nCSO in AS. When not programming the device in AS mode, nCSO is not used. If the pin is not used as an I/O, you should leave the pin unconnected.	Verify Guidelines have been met or list required actions for compliance.
ASDO, DATA1		This pin functions as ASDO in AS mode, and as DATA1 in PS and FPP modes. When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O, then you should leave the pin unconnected.	Verify Guidelines have been met or list required actions for compliance.
DATA[2:7]		When not programming the device in FPP mode, these pins are available as a user I/O pins. If these pins are not used as I/Os, you should leave them unconnected.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / **Issues**
DCLK		Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS modes, DCLK is an output from the FPGA that provides timing for the configuration interface.

Do not leave this pin floating. Drive this pin either high or low.

You can configure DCLK as a user I/O only after active serial configuration. | Verify Guidelines have been met or list required actions for compliance. |
| CRC_ERROR | | Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits.

When using this pin, connect it to an external 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device.

When not using CRC error detection, this pin can be used as regular I/O.

When not using this pin, it can be left floating. | Verify Guidelines have been met or list required actions for compliance.

See Notes (2-4) (2-5). |

Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
DEV_CLRn		When the dedicated input DEV_CLRn is not used for its dedicated function, and if this pin is not used as an I/O, tie this pin to GND.	Verify Guidelines have been met or list required actions for compliance.
DEV_OE		When the dedicated input DEV_OE is not used for its dedicated function, and if this pin is not used as an I/O, tie this pin to GND.	Verify Guidelines have been met or list required actions for compliance.
DATA0		If you are using a serial configuration device in AS configuration mode, you must connect a 25-Ω series resistor at the near end of the serial configuration device for the DATA0 pin. When the dedicated input for DATA0 is not used and this pin is not used as an I/O pin, then you should to leave this pin unconnected.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
INIT_DONE		When using this pin, connect it to an external 10-KΩ pull-up resistor to an acceptable voltage for all devices in the chain that satisfies the input voltage of the receiving device. When not using this pin, it can be left floating or tied to GND. This pin can be used as an I/O pin when not enabled as INIT_DONE in the Quartus Prime software. It cannot be used as a user I/O after configuration if INIT_DONE is enabled in the Quartus Prime software.	Verify Guidelines have been met or list required actions for compliance.
CLKUSR		If CLKUSR is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, then you should connect this pin to GND.	Verify Guidelines have been met or list required actions for compliance.

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
JTAG Header		Power the ByteBlaster II or USB-Blaster or USB-Blaster II cable's VCC (pin 4 of the header) with VCCA. For multi-device JTAG chains with different VCCIO voltages, voltage translators may be required to meet the I/O voltages for the devices in the chain and JTAG header. The ByteBlaster II, USB-Blaster and USB-Blaster II cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the ByteBlaster II Download Cable User Guide and the USB-Blaster/USB-Blaster II Download Cable User Guide.	Verify Guidelines have been met or list required actions for compliance.

Notes:
2-1. FPP configuration is supported in most devices, except for the E144 package.

2-2.You must follow specific requirements when interfacing Cyclone 10 LP devices with 2.5V, 3.0V, and 3.3V configuration voltage standards. All I/O pin input signals must maintain a maximum AC voltage of 4.1V. Refer to Configuration and JTAG Pin I/O Requirements in the chapter Configuration and Remote System Upgrades of Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook

2-3. Connect the pull-up resistor to the same supply voltage as the USB Blaster/USB Blaster II, MasterBlaster (VIO pin), ByteBlaster II, ByteBlasterMV, or EthernetBlaster cable. The voltage supply can be connected to the VCCA of the device.

2-4. CRC error detection is only supported in Cyclone 10 LP devices with VCCINT 1.2 V, and not in Cyclone 10 LP devices with VCCINT 1.0 V.

2-5. There are two variants of Cyclone 10 LP devices; one powered with a core voltage VCCINT of 1.0V, and the other powered with a core voltage VCCINT of 1.2V. Each variant has different ordering codes.

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Additional Comments:

Section III: I/O

Cyclone 10 LP Recommended Reference Literature/Tool List

Cyclone 10 LP Device Pin-Out Files

Cyclone 10 LP Device Family Pin Connection Guidelines (PDF)

Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook

AN 800: Cyclone 10 LP Device Design Guidelines (PDF)

AN 597: Getting Started Flow for Board Designs (PDF)

Intel Board Design Resource Center (General board design guidelines, PDN design, isolation, tools, and more)

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Part A: Clock Pins

Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p		Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins. Connect unused CLK or DIFFCLK pins to GND. Use dedicated clock pins to drive clocks into the device. These pins can connect to the device PLLs. Refer to chapter "Clock Networks and PLLs in Cyclone 10 LP Devices" of Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook for further details.	Verify Guidelines have been met or list required actions for compliance. See Notes (3-1) (3-3) (3-4).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n		Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins. Connect unused CLK or DIFFCLK pins to GND. Use dedicated clock pins to drive clocks into the device. These pins can connect to the device PLLs. Refer to chapter "Clock Networks and PLLs in Cyclone 10 LP Devices" of Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook for further details.	Verify Guidelines have been met or list required actions for compliance. See Notes (3-1) (3-3) (3-4).

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
PLL[1..4]_CLKOUTp		Optional positive terminal for external clock outputs from PLL [1..4]. Each pin can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output. When not using this pin as a clock output, this pin may be used as a user I/O pin. Unused pins can be tied to GND or left unconnected. If unconnected, use the Quartus Prime software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.	Verify Guidelines have been met or list required actions for compliance. See Notes (3-1) (3-2) (3-5).
PLL[1..4]_CLKOUTn		Optional negative terminal for external clock outputs from PLL [1..4]. Each pin can be assigned to single-ended or differential I/O standards if it is being driven by a PLL output. When not using this pin as a clock output, this pin may be used as a user I/O pin. Unused pins can be tied to GND or left unconnected. If unconnected, use the Quartus Prime software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.	Verify Guidelines have been met or list required actions for compliance. See Notes (3-1) (3-2) (3-5).

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Part B: Dedicated and Dual Purpose Pins			
Plane/Signal	**Schematic Name**	**Connection Guidelines**	**Comments / Issues**
RUP[1..4]		Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7 in device. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If RUP and RDN are not used, these pins can function as a regular I/O pins.	Verify Guidelines have been met or list required actions for compliance. See Note (3-1).
RDN[1..4]		When using OCT, tie RUP pins to the required bank VCCIO through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. When using OCT, tie RDN pins to GND through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that unused RUP pins be connected to VCCIO of the bank in which the RUP pin resides or GND and unused RDN pins be connected to GND. Ensure the reserve unused pin option used in Quartus Prime software for these pins do not conflict with the board connection.	

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Plane/Signal	Schematic Name	Connection Guidelines	Comments / Issues
NC		Do not drive signals into these pins. When designing for device migration, these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating. For further information see Knowledge Database solution rd03132006_933.	Verify Guidelines have been met or list required actions for compliance. See Note (3-1).

Additional Comments:

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Part C: Dual Purpose Differential I/O pins			
Plane/Signal	**Schematic Name**	**Connection Guidelines**	**Comments / Issues**
DIFFIO_[L,R,T,B] [0..61][p,n] (Not all pins are available in each device / package combination)		Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/ receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as single ended user I/O pins. Unused pins can be left unconnected or tied to GND. Connect unused pins as defined in the Quartus Prime software.	Verify Guidelines have been met or list required actions for compliance. See Note (3-1).

<Project Name> <Date>

Notes:

3-1. Refer to Knowledge Database solution rd12102002_3281 for further information regarding the concerns when I/O pins are left floating with no internal or external bias. Ensure there are no conflicts between the Quartus Prime software device wide default configuration for unused I/Os and the board level connection. Intel recommends setting unused I/O pins on a project wide basis to behave as inputs tri-state with weak pull up resistor enabled. Individual unused pins can be reserved with specific behavior such as output driving ground or as output driving VCC to comply with the PCB level connection.

3-2. The Quartus Prime *.pin file created after compiling the design project in the Quartus Prime software lists unused clock input pins as GND+(unused input clocks PLLs). Verify that any pins listed as such in the Quartus Prime *.pin file are connected to the board as indicated in these recommendations.

3-3. The number of dedicated global clocks for each device density is different. Refer to chapter "Clock Networks and PLLs in Cyclone 10 LP Devices" of Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook for device specific resource availability.

3-4. The differential TX/RX channels for each device density and package is different. Refer to chapter "I/O and High Speed I/O in Cyclone 10 LP Devices" of Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook for device specific resource availability.

3-5. The number of PLLs consisting of GPLLs and MPLLs for each device density is different:

10CL006 and 10CL010 support 2 PLLs.
10CL016 and other larger Cyclone 0 LP densities support 4 PLLs.

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Additional Comments:

Section IV: Document Revision History

Revision	Description of Changes	Date
V1.0	Initial release, based on Cyclone 10 LP Device Family Pin Connection Guidelines version 2017.06.02.	July 2017
V1.1	Checked and updated based on Cyclone 10 LP Device Family Pin Connection Guidelines version 2017.11.06	Nov 2017

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